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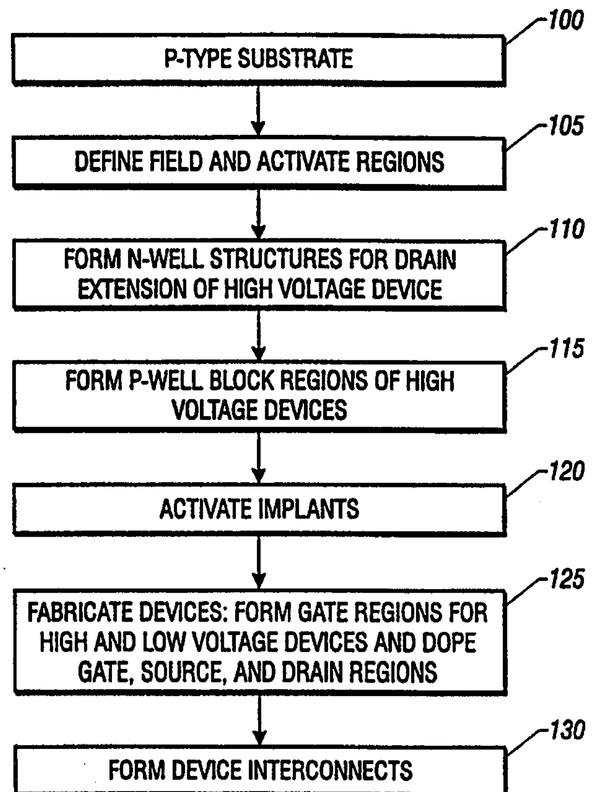
(54) Title: A HIGH VOLTAGE TRANSISTOR HAVING A FIELD OXIDE GATE REGION

(57) Abstract

A high voltage transistor, formed in a bulk semiconductor material (200), has a gate region (230) defined by a relatively thick field oxide (205) and a source (220) and drain (225) on opposite sides of the field oxide (205).



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A HIGH VOLTAGE TRANSISTOR HAVING A FIELD OXIDE GATE REGION

1. Background of the Invention

5 The present invention relates generally to integrated metal oxide semiconductor (MOS) devices and, in particular, to combining high voltage and low voltage devices on a single semiconductor substrate.

Refinements in the design and fabrication of integrated circuits (ICs) have provided circuits having more than one million transistors. With continued 10 research and development, the microelectronics industry continues to push transistor densities even higher. One consequence of increasing transistor densities is that device operating voltages are generally getting lower. Whereas, older transistor-transistor logic (TTL) circuits were designed to operate at 5 volts (v), newer circuits such as memory devices and central processing units (CPU) 15 are being designed to operate at 3.3v, 2.5v, and 1.8v.

2. Summary of the Invention

The invention generally provides methods and apparatus to fabricate high voltage transistors (operating at approximately 12 volts and above) on a 20 substrate of higher density, low voltage (operating at approximately 5 volts and below) devices. In one embodiment, a high voltage transistor is fabricated on a substrate of low voltage devices without any additional photolithographic or process steps. In other embodiments, photolithographic and process steps are added to allow operational refinements of the high voltage transistor.

25 Including high voltage and low voltage devices on a common substrate allows the fabrication of integrated circuits having increased functionality at a reduced cost over (functionally) equivalent combinations of circuits, some incorporating high voltage devices and some incorporating low voltage devices. Examples of high voltage circuits that can be implemented on a substrate of 30 predominately low voltage devices in accordance with the invention include, but are not limited to: (1) on-chip programming devices for use in programmable read-only memory devices; (2) high voltage sense circuits; (3) liquid crystal display drivers; (4) servo control circuits; and (5) disk drive read channel

circuitry. Other features and advantages of the invention will become apparent from the following detailed description.

3. Brief Description of the Drawing

5 Figure 1 shows a high voltage device fabrication process flow.

Figures 2A through 2D illustrate semiconductor substrate cross-sections corresponding to the process flow of FIG. 1.

Figures 3A and 3B show test data for one illustrative high voltage device.

Figure 4 shows another high voltage device fabrication process flow.

10 Figures 5A and 5B illustrate semiconductor substrate cross-sections corresponding to the process flow of FIG. 4.

Figure 6 shows another high voltage device fabrication process flow.

Figure 7 illustrates a semiconductor substrate cross-section corresponding to the process flow of FIG. 6.

15 Figure 8 shows another high voltage device fabrication process flow.

Figures 9A and 9B illustrate semiconductor substrate cross-sections corresponding the process flow of FIG. 8.

Figure 10 shows yet another high voltage device fabrication process flow.

20 4. Detailed Description

New low voltage devices are more susceptible to high voltage signals that prior devices. For example, a circuit implemented in 1.8v technology can be damaged when exposed to a high voltage signal, i.e., a signal of approximately 12v and above. It would be beneficial to integrate both low voltage and high
25 voltage/drive capability into a single circuit on a single substrate. The combined integration of low and high voltage devices would make possible the design and manufacture of complete functional circuits; circuits having both logic and direct input-output (I/O) control capability.

Recent complimentary metal oxide semiconductor (CMOS) technology
30 advances have focused on using energy implant technology to form retrograde twin-well structures within which devices are constructed. Retrograde twin-well

technology is characterized by reduced well thermal drives, well defined well edges, thinner field oxide requirements, reduced well-to-well spacing design rules, and greater accuracy and flexibility in defining the n-well/p-well doping profiles. Retrograde twin-well processing technology may be exploited to fabricate high voltage transistors (designed to operate at approximately 12v and above) on a substrate predominantly populated with devices designed to operate at approximately 5v and below.

While detailed embodiments of the present invention are described, it should be understood that the disclosed embodiments are merely exemplary of the invention. The details disclosed herein are not to be interpreted as limiting, but merely as the basis of the claims and as a basis for teaching one skilled in the art how to make and/or use the claimed invention.

Figures 1 and 2 illustrate formation of a high voltage NMOS device in a p-type substrate having low voltage devices. Figure 1 shows an illustrative process flow and FIG. 2 substrate cross-sections corresponding to some of the process flow steps of FIG. 1. High voltage device fabrication begins with a p-type substrate (step 100, element 200) having an ionic concentration of approximately $5e^{14}$ to $5e^{15}$ Boron (B) atoms/cm^3. Field and active regions of both the high voltage and low voltage devices are defined using an isolation technology (step 105). Suitable isolation technologies include local oxidation of silicon (LOCOS) and its variants such as semirecessed, sidewall-masked isolation (SWAMI), self-aligned planar-oxidation technology (SPOT), sealed-interface local oxidation (SILO), and fully recessed oxide (FUROX) as well as non-LOCOS techniques such as trench technology. Figure 2 illustrates a general LOCOS technique using a field oxide 205 of silicon dioxide (SiO_2), typically 2000Å to 5000Å thick. P-well regions 210 may be used to form low voltage devices.

Following isolation, n-well structures 215 are formed in the substrate (step 110) to provide high voltage device drain extensions and regions in which low voltage p-type devices can be formed. N-well regions 215 may be formed using one or more energy implants. For example, a first implant of arsenic (As) or phosphorous (P) at 50 KeV to 200 KeV (preferably 100 KeV), followed by a

second implant of As and/or P at 250 KeV to 700 KeV (preferably 400 KeV), followed by a third implant of As and/or P at 500 KeV to 2 MeV, preferably 800 KeV, may be designed to create a retrograde n-well having approximately $2e^{11}$ to $2e^{13}$ ions/cm^2. An additional layer of photoresist (not shown in FIG. 2) may be
5 used to shield areas of the substrate where no implantation is desired.

For additional isolation between the low and high voltage devices a p-well block can be constructed (step 115). The p-well block does not require an additional process step (e.g., implantation), but rather a change in existing low voltage device p-well masking to ensure a physical separation between low
10 voltage device p-wells and adjacent high voltage device n-wells. Thus, p-well blocks are formed during low voltage device p-well formation at no additional process cost. The p-well block ensures there are three distinct regions at the surface of the substrate: p-well; n-well; and bulk. The electrically decoupled bulk regions (i.e., the bulk regions are not used to set any electrical characteristic
15 of the low voltage devices) enable formation of useful and stable high voltage devices.

P-well block formation (step 115) is followed by a relatively short and low temperature anneal phase designed to activate the implantation regions (step 120). A typical activation anneal uses an 850C to 1000C bake for 15 to 60
20 minutes. The anneal's relatively low temperature and short time period limits the lateral diffusion of the implanted ions, resulting in relatively sharp well edges and well ionic concentration of approximately $1e^{16}$ to $5e^{17}$ ions/cm^3.

High voltage gate regions 230 are formed and source 220, drain 225, and gate 230 regions are doped in the normal course and at the same time as the
25 source, drain, and gate structures of the substrate's low voltage devices (step 125). Source 220 and drain 225 regions can be n+ regions by implantation of As and/or P ions at a dose of approximately $1e^{15}$ to $6e^{15}$ ions/cm^2 to yield a concentration of approximately $1e^{20}$ ions/cm^3. Gate structure 230 can be made of polysilicon and is typically 1700Å to 4000Å thick. During low voltage device
30 fabrication, field oxide 205 is preferably made as thick as practical yet thin enough to support the desired low voltage device spacing (e.g., design rules).

Generally, as gate oxide thickness decreases a high voltage devices drive capacity increases while stray capacitance associated with the low voltage devices' increases. The increased capacitance can limit the operational speed of the low voltage devices. The high voltage device's threshold voltage (V_{th}) may be
5 adjusted by the silicon band-gap voltage (approximately 1.2 volts) by using either n+ or p+ material for the gate structure instead of polysilicon.

Finally, conductive paths are formed to allow use of both the high voltage and low voltage devices (step 130). Materials suitable for forming device interconnections include, but are not limited to, aluminum (Al), molybdenum
10 (Mo), tungsten (W), titanium nitride (TiN), and titanium-tungsten combinations (Ti:W).

Figures 3A and 3B show test data for a high voltage device having an approximately 50 μm channel width and an approximately 5 μm channel length. The substrate's low voltage device characteristics were as follows: gate
15 breakdown voltage of approximately 7.5 volts; drain breakdown voltage of approximately 6.0 volts; device operating voltage of approximately 3.3 volts; device-to-device spacing of approximately 0.6 μm; and a gate oxide thickness of approximately 70Å. As shown, no aberrant behavior (breakdown, snap-back, or punch-through) was detected even at high voltage device gate voltages of 20 volts
20 and well voltages (bulk voltage to source voltage) of 4 volts.

A high voltage device in accordance with FIGs. 1, 2, and 3 may be used to, for example, implement a circuit for sensing high voltage signals and/or for generating drive currents in excess of 6 mA per device without negatively impacting the operational characteristics of the low voltage devices or incurring
25 any additional processing steps. Several high voltage devices may be combined to implement circuits having output drive capability in excess of 50 mA without requiring large amounts of substrate area. The low voltage devices could be used to implement any desired conventional functional circuit such as a microprocessor or a disk drive control unit.

30 Referring to FIGs. 4 and 5, an alternative embodiment is shown which uses an additional mask to expose the high voltage device gate oxide region (step

400) and a timed etch (step 405) to selectively reduce the gate oxide's thickness 500. With the addition of this one operation (one mask to open a photoresist window over the high voltage device's gate oxide and one etch), the drive capacity of the high voltage device may be increased approximately five times
5 without affecting low voltage device characteristics. The etch (step 405) may be performed, for example, by a timed buffered oxide etch (BOE) or buffered hydrofluoric acid (HF) etch. The precise time of the etch depends at least upon the gate oxide's initial thickness and concentration of the etchant (e.g., HF). The gate oxide 500 may be taken as thin as desired (within control limits of the timed
10 etch), typically 400Å to 1000Å. The effect of this operation is to increase high voltage device transconductance which, also has the effect of reducing the high voltage device's gate breakdown voltage. For a gate oxide thickness of 400Å, the high voltage device gate breakdown voltage is in excess of 40 volts. This embodiment retains all of the advantages, and can be modified in the same
15 manner, as the prior embodiment while incurring only a minimal added fabrication cost.

Referring to FIGs. 6 and 7, the prior embodiment is modified to provide a high voltage device gate implantation step (600) after the gate oxide has been exposed (step 400) but before it has been etched (step 405). Implant energies
20 may be between approximately $1e^{11}$ to $1e^{12}$ ions/cm^2, generally using B or boron-fluoride (BF_2) ions. Shallow implantation energies of approximately 100 KeV to 200 KeV, and deep implantation energies of approximately 100 KeV to 1 MeV may be used. Gate region implantation may also be performed before the gate etch (step 405) and, if so, implantation energies as low as 25 KeV for a
25 shallow implant, and 300 KeV for a deep implant may be used. If the modified p-type gate material 710 is annealed at the same time the source and drain regions are annealed (step 120), no additional processing is necessary. Gate region implantation (step 600 and region 705) can allow the high voltage device source and drain regions to be more closely spaced which, in turn, tends to
30 reduce the effect of the device's channel length and increases the high voltage device's current drive capability. Implantation (step 600) also allows an

increased flexibility in setting the high voltage device's electrical characteristics, such as its threshold voltage.

In yet another embodiment, the timed etch-back operation of FIGs. 4 through 7 is replaced with an oxide growth process, see FIGs. 8 and 9. Following step 110, a layer of silicon nitride 900 is deposited on the surface of the semiconductor (step 800). After the high voltage gate regions are exposed (step 400), the silicon nitride is etched and a layer of oxide is grown (step 805), and is typically 300Å to 1000Å using any convenient dry or wet oxide growth process. Following gate oxide formation, the silicon nitride is stripped (step 810) using any convenient stripping agent (e.g., phosphoric acid) and processing continues as described above (e.g., at step 115; see FIGs. 1, 4, and 6). One benefit of this approach is that the gate oxide thickness 905 can be better controlled than in an etch process. This added control, in turn, allows the design of a high voltage device with more tightly controlled electrical characteristics such as threshold voltage, current drive capability, and input capacitance. This embodiment retains all of the advantages, and can be modified in the same manner as the prior embodiments.

In yet another embodiment, see FIG. 10, a gate region implantation (step 600) is performed after the gate oxide has been grown, but before the silicon nitride has been stripped (step 810). Following the nitride strip, fabrication continues in accordance with step 115 through 130 as discussed above (step 1000).

In those embodiments using a gate region implantation (see, e.g., element 710 in FIG. 7), a typical silicon nitride layer of 800Å to 2500Å is sufficiently thick to stop implantation energies of up to approximately 100 KeV. If higher implantation energies are desired, the photoresist used to pattern the silicon nitride, which may be up to approximately 3 μm thick, may be left in place during implantation. (The gate region must be kept essentially clear of both the silicon nitride and photoresist.) The protection afforded the substrate by the photoresist in combination with the silicon nitride can shield the substrate from ion energies of up to approximately 2 MeV. Following implantation, the

photoresist and silicon nitride may be stripped (using any convenient technique) and processing continued.

One of ordinary skill will recognize that many variations of the described processes may be made while still achieving fabrication of a high voltage device. For example: isolation (step 105) and well formation (step 110) steps may be done in reverse order -- step 110 followed by step 105; a standard p-buried layer for epi replacement may be formed in the substrate 200 before any other steps (i.e., before step 105); channel stop implants can be formed in the high voltage device gate region (i.e., under the high voltage device gate filed oxide 205) to allow finer control over device threshold voltage or, alternatively, the substrate's bulk dopant level may be adjusted prior to fabrication to fulfill the same goal; gate region ion implantation may be performed either before or after a gate oxide is formed. In addition, a PMOS high voltage device may be formed by stating with an n-type substrate material, forming p-wells, and p+ source and drain regions. The embodiments described herein constitute exemplars only, other embodiments are within the scope of the following claims.

What is claimed is:

1. A semiconductor device comprising:
a source formed in bulk silicon;
5 a drain formed in the bulk silicon; and
a field oxide formed on the bulk silicon between the source and drain, the field oxide forming a gate.

2. A semiconductor transistor formed in a bulk material, comprising:
10 an insulator formed in the bulk material; and
a transistor having a source and drain on opposite sides of the insulator.

3. The semiconductor transistor of claim 2 wherein the insulator is silicon dioxide.

15

4. The semiconductor transistor of claim 2 wherein the bulk material is silicon having a p-type conductivity and the source and drain have a n-type conductivity.

20 5. The semiconductor transistor of claim 2 wherein the bulk material is silicon having a n-type conductivity and the source and drain have a p-type conductivity.

6. A semiconductor device formed in bulk silicon having a bulk conductivity
25 type, comprising:
a source formed in the bulk silicon and having a first conductivity type opposite that of the bulk conductivity type;
a drain formed in the bulk silicon having the first conductivity type;
a field oxide formed on the bulk silicon and between the source and the
30 drain; and
a gate formed on the field oxide.

7. The semiconductor device of claim 6 wherein the bulk conductivity type is p-type.

8. The semiconductor device of claim 6 wherein the first conductivity type is
5 p-type.

9. The semiconductor device of claim 6 wherein the field oxide is between approximately 1000 angstroms and approximately 5000 angstroms thick.

10 10. The semiconductor device of claim 6 wherein the field oxide is greater than approximately 50 angstrom.

11. The semiconductor device of claim 7 further comprising:
a n+ region formed within the source; and
15 a n+ region formed within the drain.

12. The semiconductor device of claim 8 further comprising:
a p+ region formed in the source; and
a p+ region formed in the drain.

20

13. A semiconductor transistor formed in bulk silicon having p-type conductivity, comprising:
a source formed in the bulk silicon having a first n-type conductivity region and a first n+ conductivity type region;
25 a drain formed in the bulk silicon having a second n-type conductivity region and a second n+ conductivity type;
a field oxide of silicon dioxide formed on the bulk silicon and between the source and the drain; and
a gate formed on the field oxide.

30

14. The semiconductor device of claim 13 wherein the field oxide is greater than approximately 50 angstrom thick.

15. A high-energy retrograde twin-well CMOS process comprising:
providing a substrate having a surface;
defining field regions and active regions on the surface of the substrate;
forming source and drains in the substrate; and
forming a high voltage device having a drain corresponding on to a first active region, a source corresponding to a second active region, and a gate corresponding to a field region, wherein the field region is between the source and drain.

16. The process of claim 15 wherein the substrate is silicon.

17. The process of claim 16 wherein the substrate has p-type conductivity.

18. The process of claim 16 wherein the substrate has n-type conductivity.

19. The process of claim 17 wherein the source and drains are n-well structures.

20. The process of claim 19 wherein the source and drain well structures further comprise a region having n+ conductivity.

21. The process of claim 18 wherein the substrate has n-type conductivity.

22. The process of claim 21 wherein the source and drains are p-well structures.

23. The process of claim 22 wherein the source and drain well structures further comprise a region having p+ conductivity.

24. The process of claim 15 wherein the well structures are formed by high-energy ion implantation.

25. The process of claim 24 wherein the high-energy ion implantation
5 comprises a plurality of implant operations, each implant at a different energy.

26. The process of claim 15 wherein the field regions are defined by an oxide layer between approximately 1000 angstroms and approximately 6000 angstroms thick.

10

27. The process of claim 15 further comprising the step of annealing.

28. A high-energy retrograde twin-well CMOS process comprising:

providing a substrate having a surface;

15 forming a patterned layer of field oxide on at least a portion of the substrate surface to define field regions and active regions;

etching the field oxide over a selected field region;

forming source and drains in the substrate in selected active regions;

forming a high voltage device having a drain, a source, and a gate
20 corresponding to the selected field region.

29. The process of claim 28 wherein the substrate is silicon.

30. The process of claim 28 wherein the field oxide is silicon dioxide.

25

31. The process of claim 29 wherein the substrate has p-type conductivity.

32. The process of claim 29 wherein the substrate has n-type conductivity.

30 33 The process of claim 31 wherein the source and drains are n-well structures.

34. The process of claim 33 wherein the source and drain well structures further comprise a region having n+ conductivity.

35. The process of claim 32 wherein the substrate has n-type conductivity.

5

36. The process of claim 35 wherein the source and drains are p-well structures.

37. The process of claim 36 wherein the source and drain well structures

10 further comprise a region having p+ conductivity.

38. The process of claim 28 wherein the well structures are formed by high-energy ion implantation.

15 39. The process of claim 38 wherein the high-energy ion implantation comprises a plurality of implant operations, each implant at a different energy.

40. The process of claim 28 wherein the field regions are defined by an oxide layer between approximately 1000 angstroms and approximately 6000 angstroms

20 thick.

41. The process of claim 28 further comprising the step of annealing.

42. The process of claim 28 further comprising implanting a selected ion into

25 the etched field region.

43. The process of claim 42 wherein the step of implanting a selected ion into the etched field region is a high-energy ion implantation operation.

30 44. The process of claim 42 wherein the high-energy ion implantation comprises a plurality of implant operations, each implant at a different energy.

45. A high-energy retrograde twin-well CMOS process comprising:
providing a substrate having a surface;
forming a patterned layer of field oxide on at least a portion of the substrate surface to define field regions and active regions;
5 forming source and drains in the substrate in selected active regions;
etching the field oxide over a selected field region to substantially eliminate the field oxide of the selected field region;
growing an silicon oxide layer of a specified thickness over the etched field region; and
10 forming a high voltage device having a drain, a source, and a gate, the gate corresponding to the selected field region.

46. The process of claim 45 wherein the substrate is silicon.

15 47. The process of claim 45 wherein the field oxide is silicon dioxide.

48. The process of claim 46 wherein the substrate has p-type conductivity.

49. The process of claim 46 wherein the substrate has n-type conductivity.

20

50. The process of claim 48 wherein the source and drains are n-well structures.

51. The process of claim 50 wherein the source and drain well structures
25 further comprise a region having n+ conductivity.

52. The process of claim 49 wherein the substrate has n-type conductivity.

53. The process of claim 52 wherein the source and drains are p-well
30 structures.

54. The process of claim 53 wherein the source and drain well structures further comprise a region having p+ conductivity.

55. The process of claim 45 wherein the source and drains are formed by
5 high-energy ion implantation.

56. The process of claim 55 wherein the high-energy ion implantation comprises a plurality of implant operations, each implant at a different energy.

10 57. The process of claim 45 wherein the grown silicon oxide layer is between approximately 50 angstroms and 800 angstroms thick.

58. The process of claim 45 further comprising implanting a selected ion into the selected field region.

15

59. The process of claim 58 wherein the step of implanting a selected ion into the selected field region is a high-energy ion implantation operation.

60. The process of claim 59 wherein the high-energy ion implantation
20 comprises a plurality of implant operations, each implant at a different energy.

61. The process of claim 45 further comprising the step of annealing.

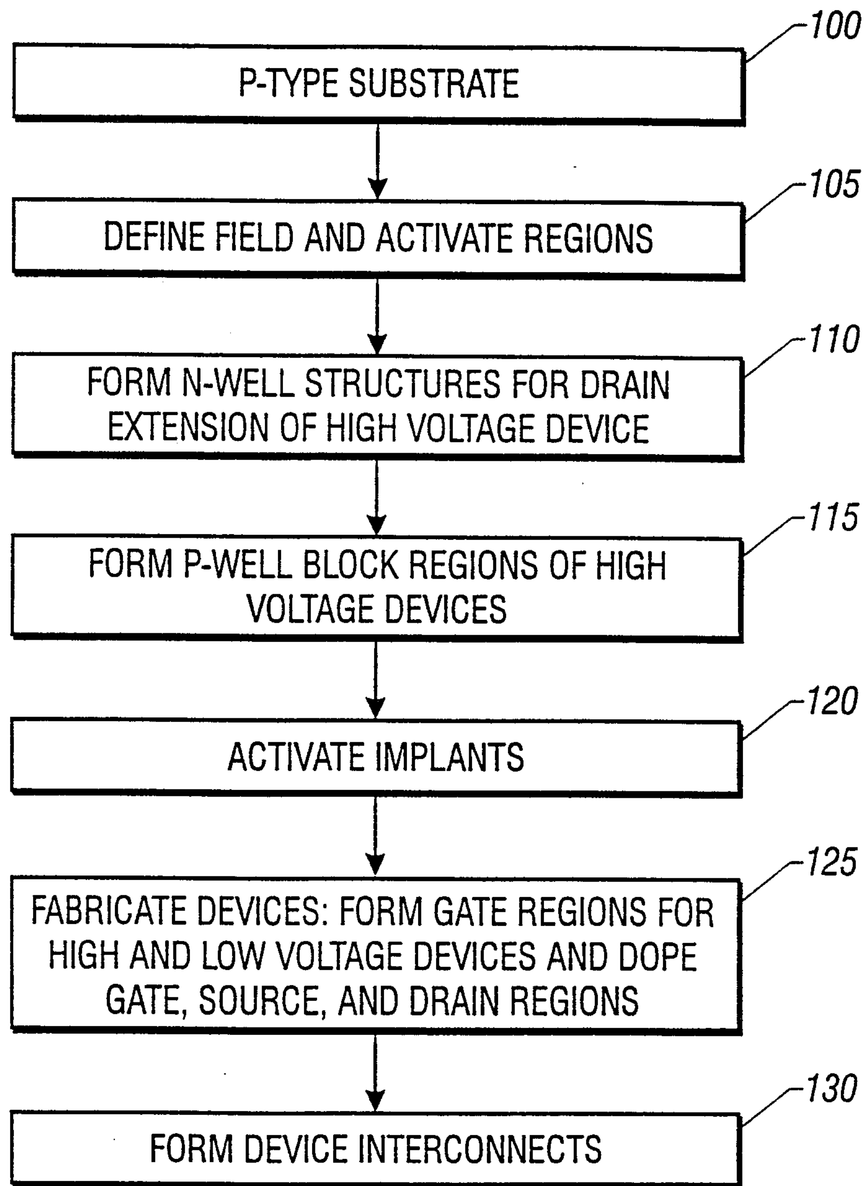

FIG. 1

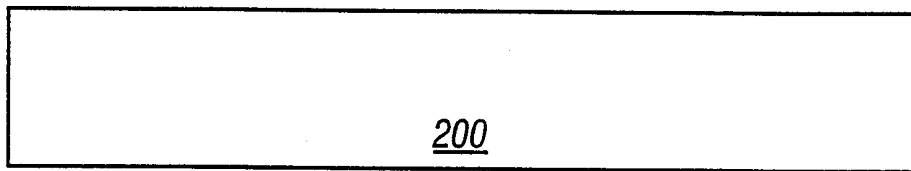

FIG. 2A

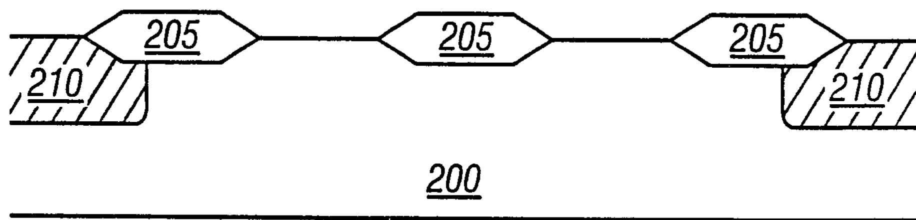

FIG. 2B

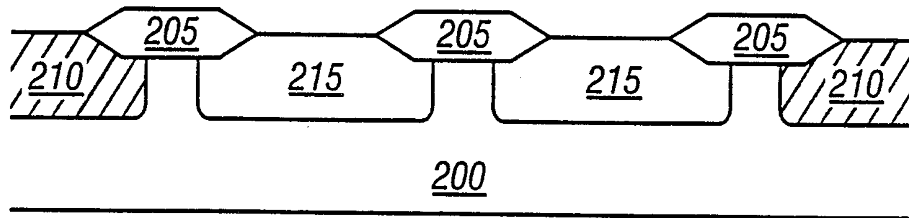

FIG. 2C

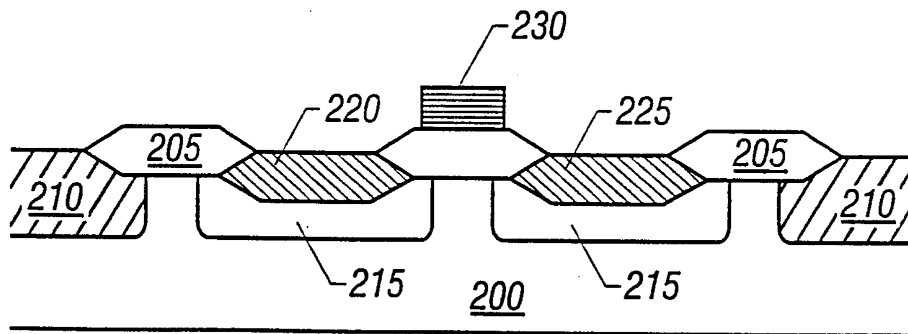

FIG. 2D

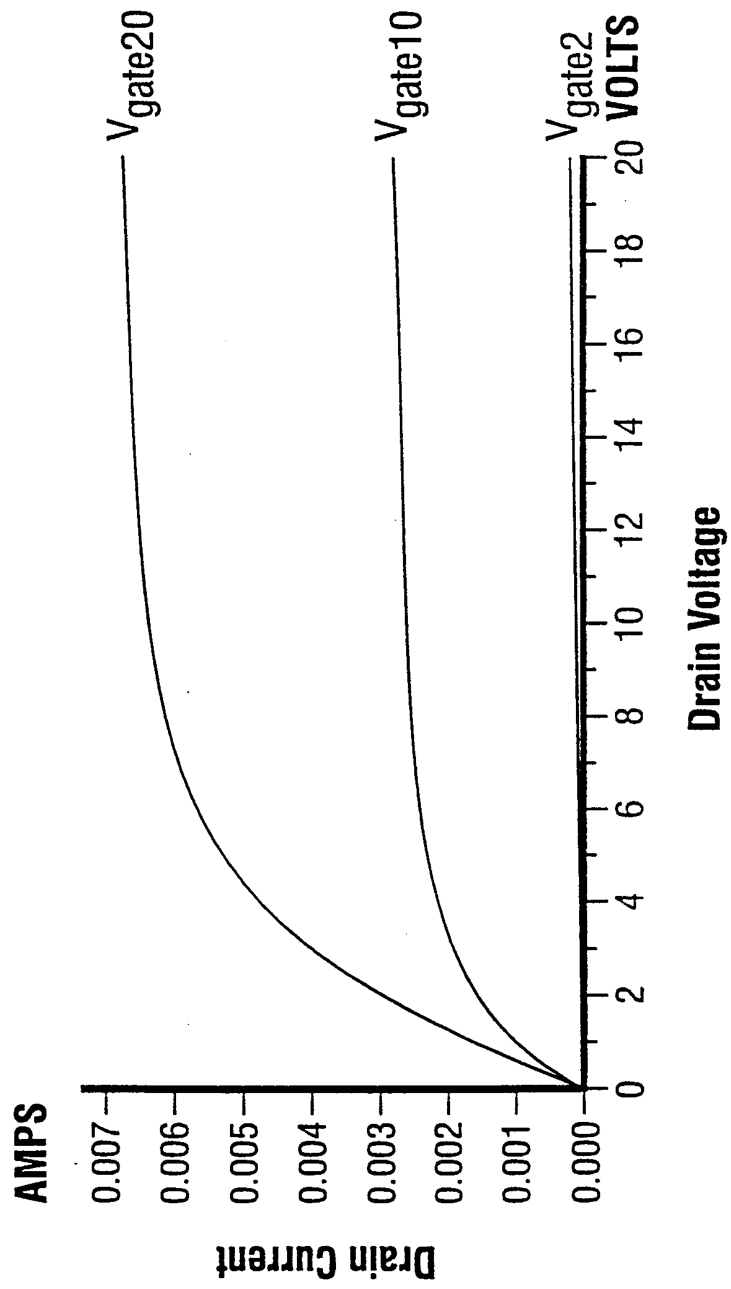

FIG. 3A

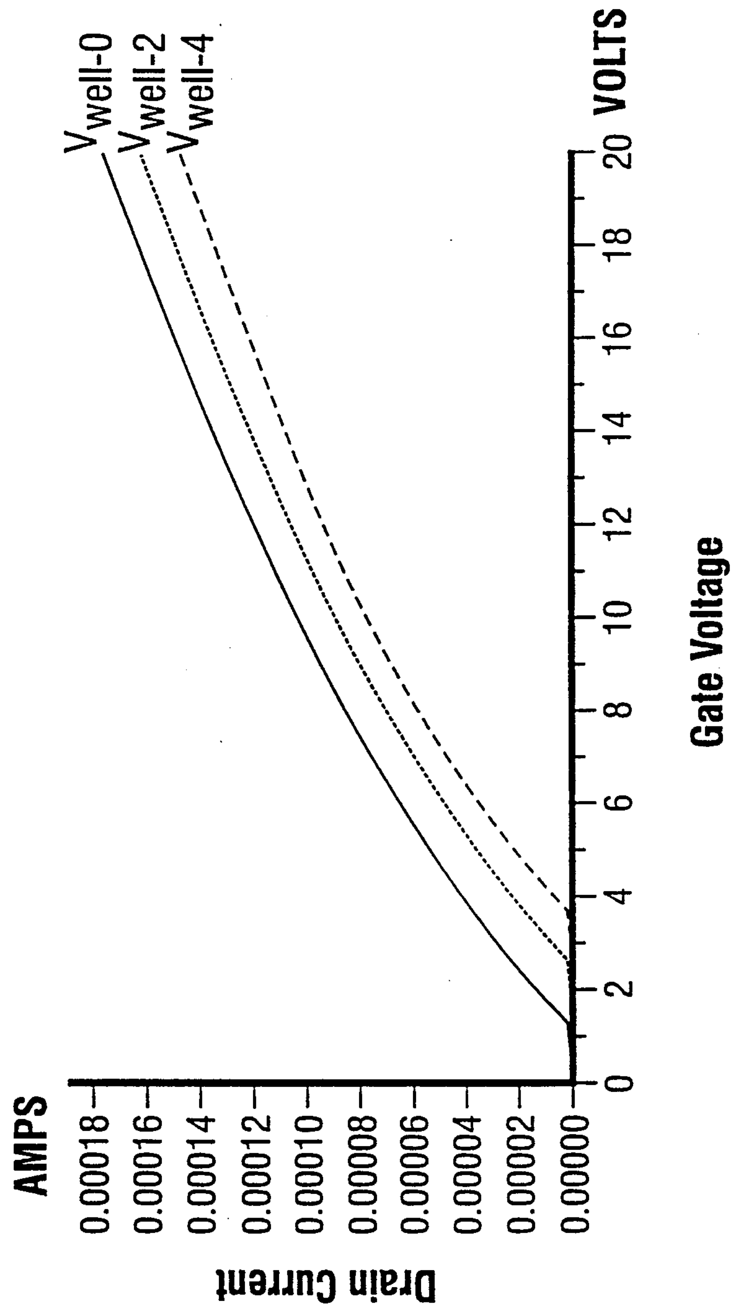

FIG. 3B

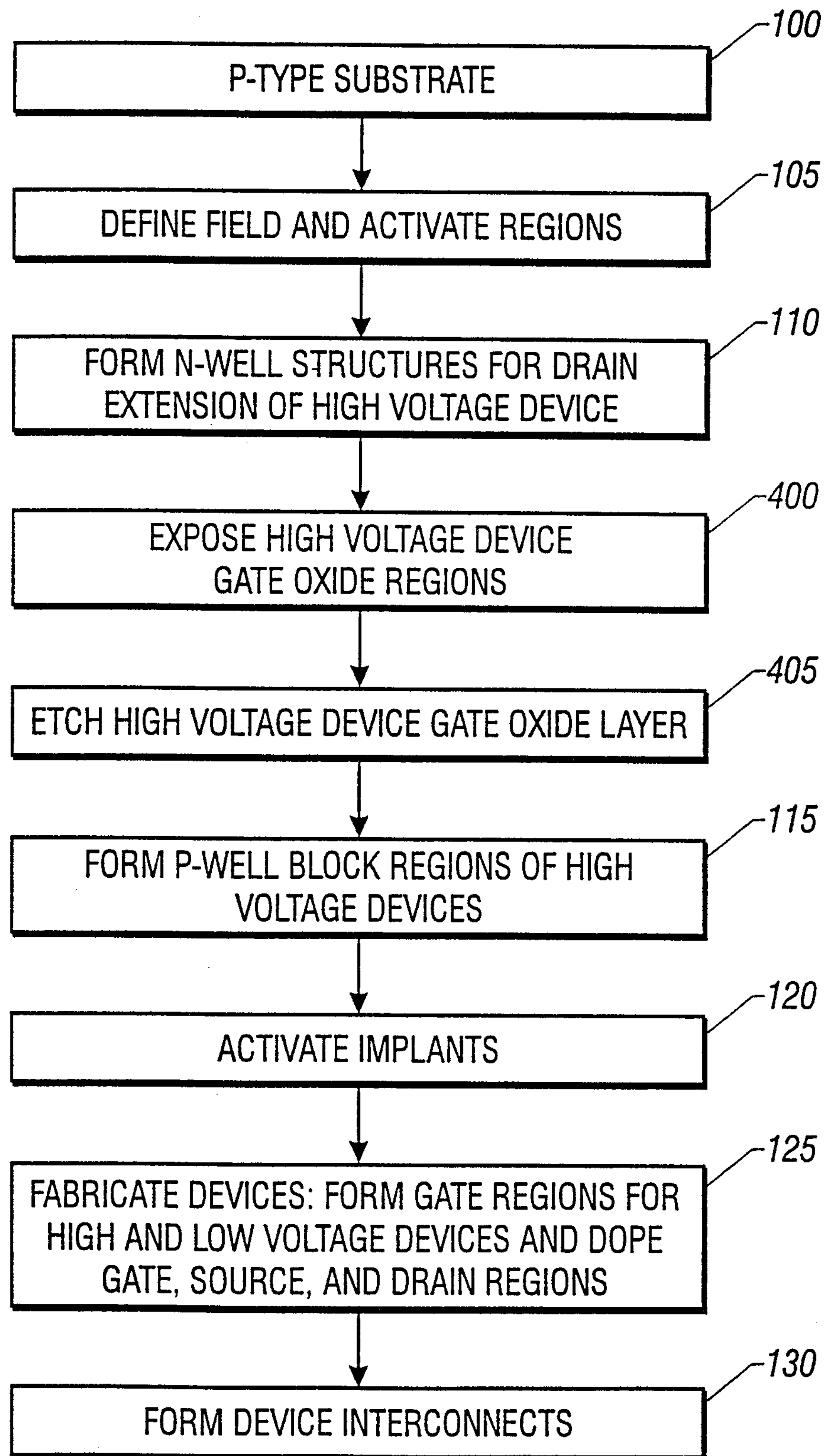

FIG. 4

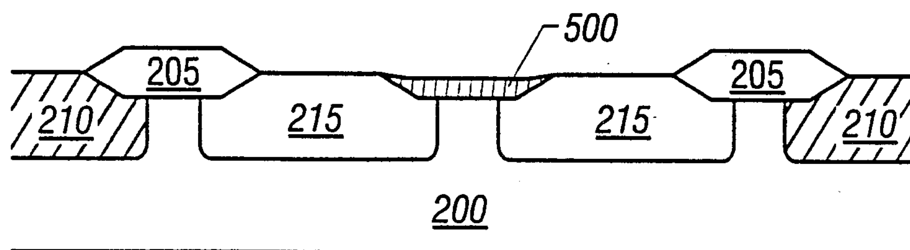

FIG. 5A

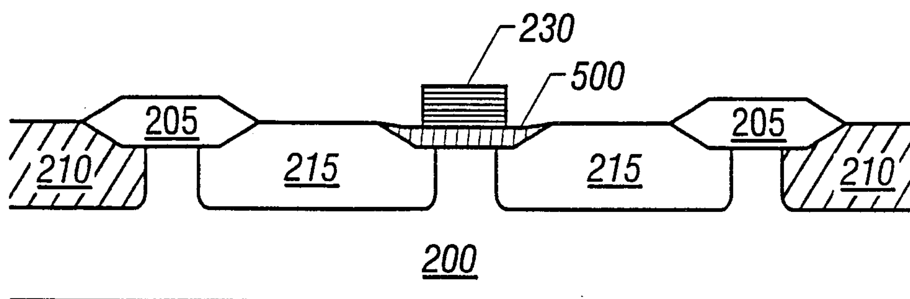

FIG. 5B

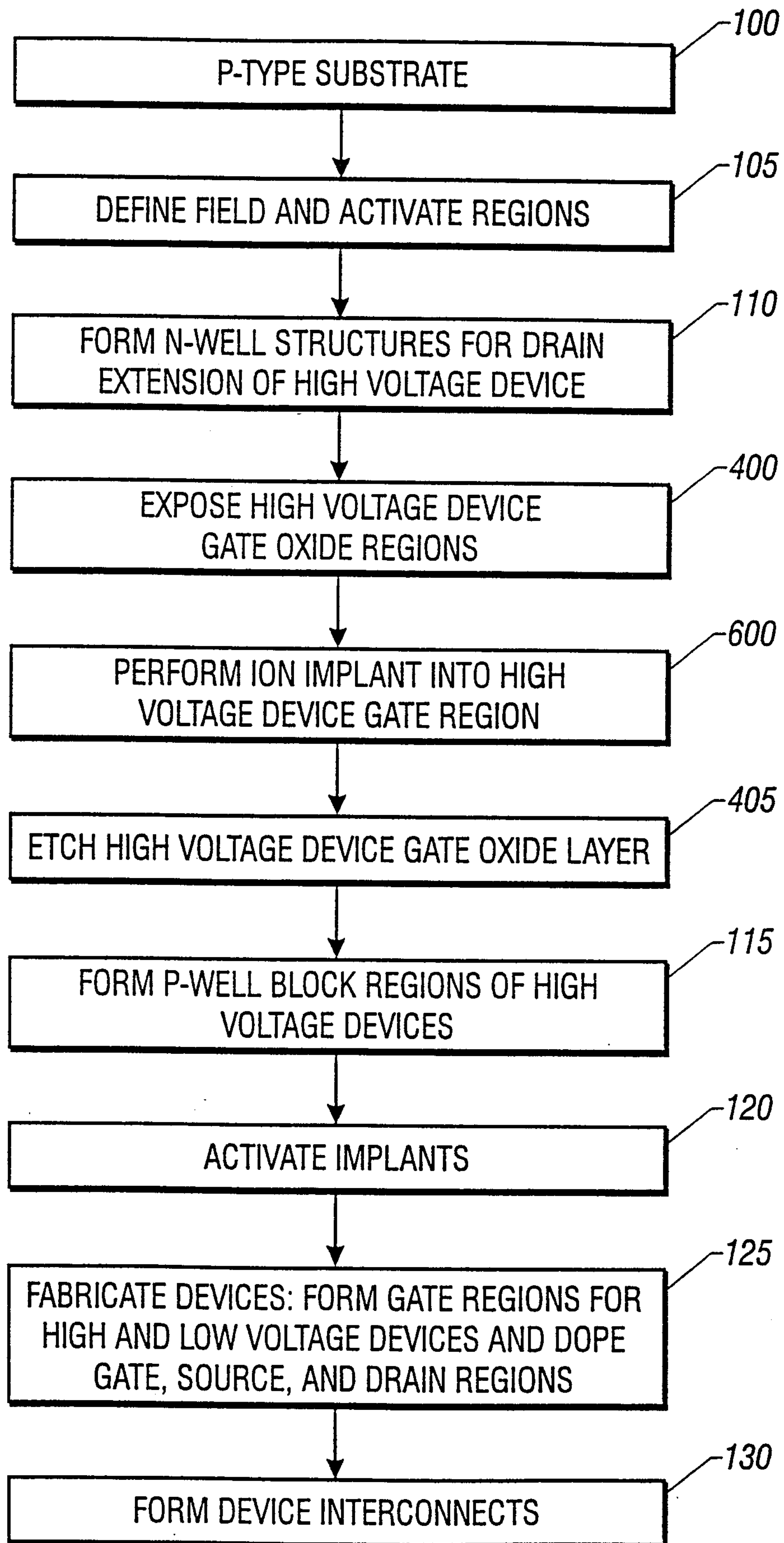

FIG. 6

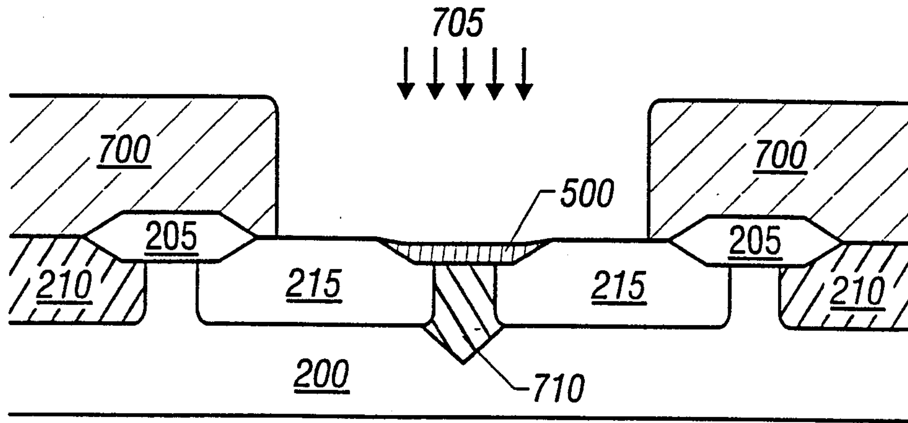

FIG. 7

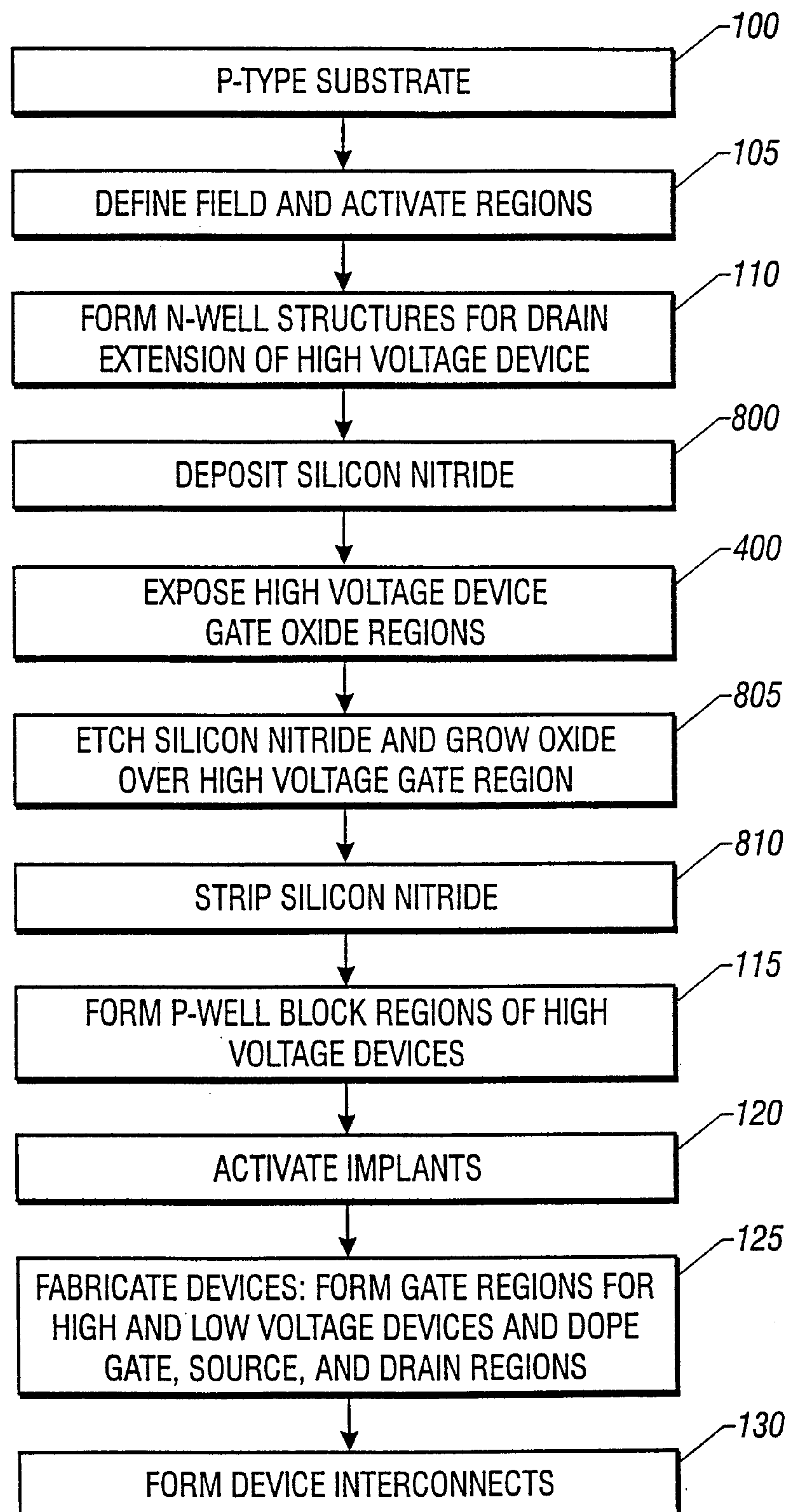

FIG. 8

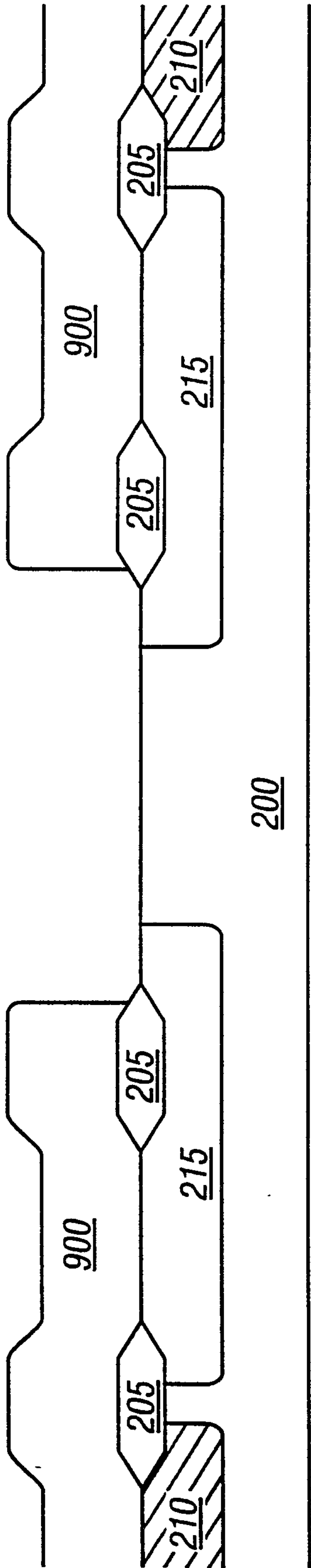

FIG. 9A

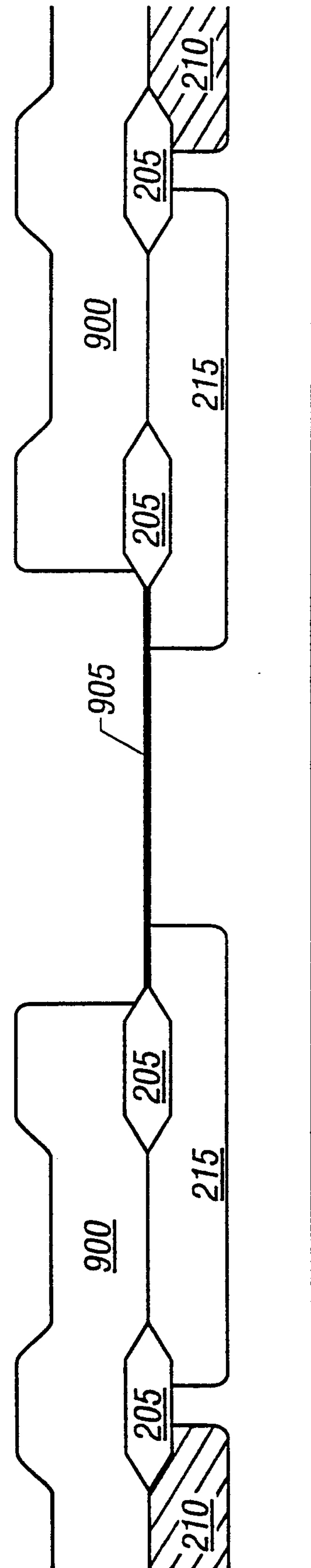

FIG. 9B

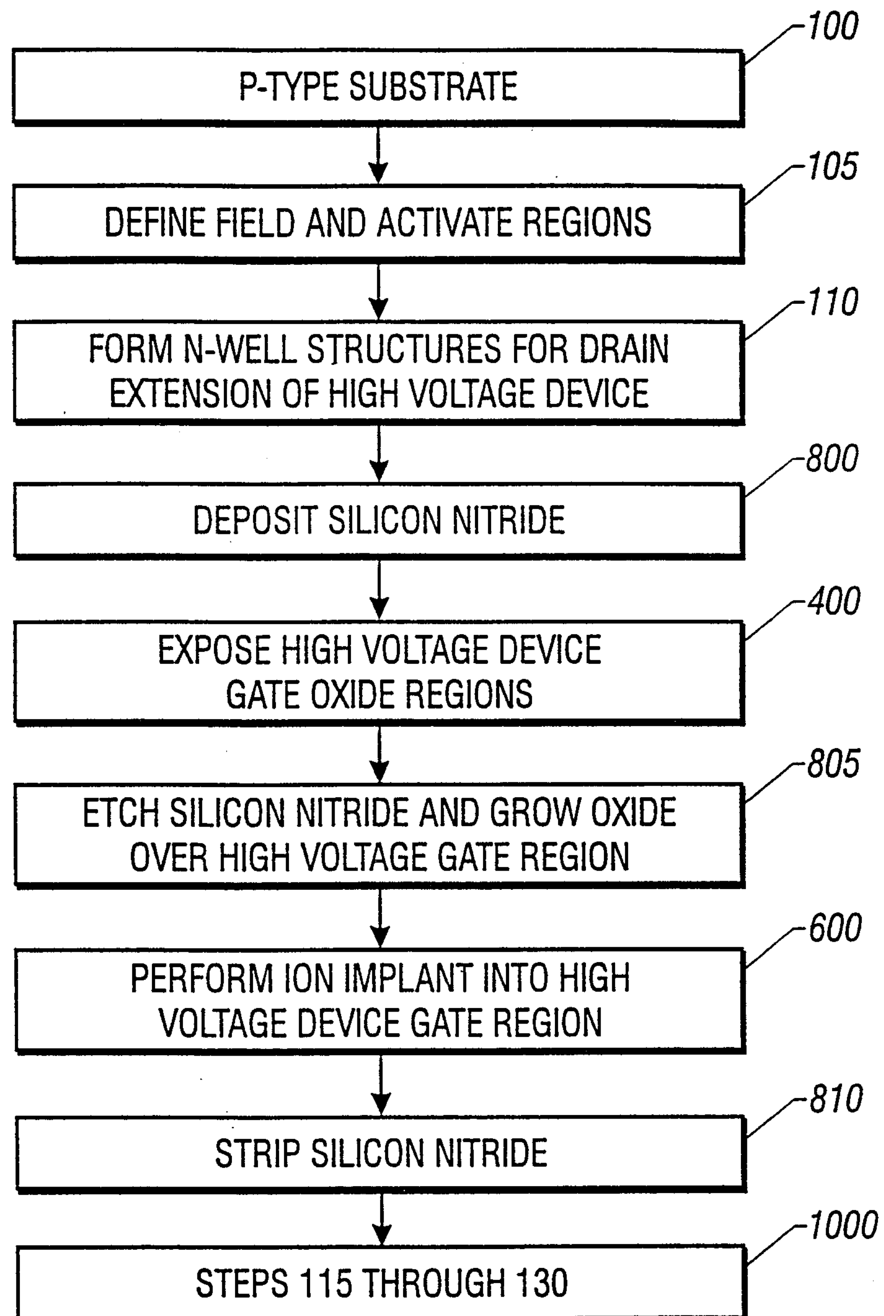

FIG. 10

INTERNATIONAL SEARCH REPORT

Inter ›nal Application No
PCT/US 99/00591

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L29/78 H01L27/088 H01L21/336 H01L29/423 H01L21/8234

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	EP 0 462 040 A (HELLO SA) 18 December 1991 see the whole document	1-14 15-26
X A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 453 (E-1417), 19 August 1993 -& JP 05 102478 A (NEC CORP), 23 April 1993 see abstract	1-14 21-24, 33-38, 50-55
X	EP 0 217 525 A (ADVANCED MICRO DEVICES INC) 8 April 1987 see the whole document	1-23,26

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 May 1999	28/05/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Mimoun, B

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/00591

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5 495 122 A (TADA GEN) 27 February 1996 see column 5, line 60 - column 6, line 21	27,41,61
Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 225 (E-0927), 14 May 1990 -& JP 02 056963 A (FUJI ELECTRIC CO LTD), 26 February 1990 see abstract	28-32
Y	PATENT ABSTRACTS OF JAPAN vol. 097, no. 006, 30 June 1997 -& JP 09 036243 A (RICOH CO LTD), 7 February 1997 see abstract	28-32
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 542 (E-1290), 12 November 1992 -& JP 04 206770 A (MITSUBISHI ELECTRIC CORP), 28 July 1992 see abstract	28
X	US 5 108 937 A (TSAI YU-HSEIN ET AL) 28 April 1992 see the whole document	45-55
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/00591

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 484 (E-1426), 2 September 1993 -& JP 05 121436 A (CASIO COMPUT CO LTD), 18 May 1993 see abstract -----	24,25, 39,56

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter onal Application No
PCT/US 99/00591

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