(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 December 2004 (02.12.2004)

PCT

(10) International Publication Number
WO 2004/104820 A2

(51) International Patent Classification[7]: G06F 7/46

(21) International Application Number:
PCT/GB2004/000059

(22) International Filing Date: 12 January 2004 (12.01.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/473,204 23 May 2003 (23.05.2003) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK,

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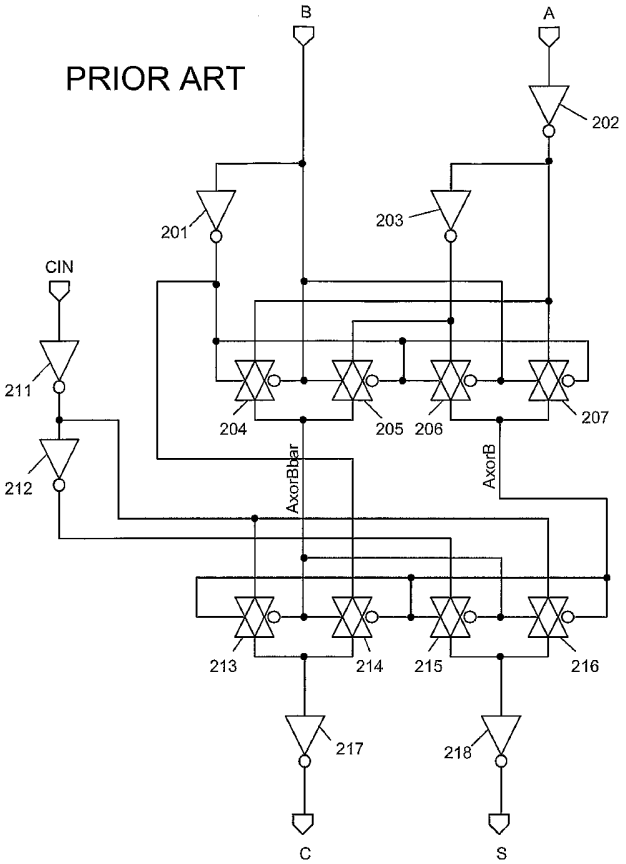
(54) Title: A SUM BIT GENERATION CIRCUIT



(57) Abstract: A circuit for generating a sum bit representing the sum of three binary input signals; the circuit comprising: first logic arranged to generate a first intermediate signal as the logical XOR of the first and second binary input signals and a second intermediate signal as the inverse of the logical XOR of the first and second binary input signals; and second logic arranged to receive said first and second intermediate signals generated by said first logic, and to generate an output signal as the logical XOR of the first intermediate signal and the third binary input signal, said second logic comprising at least two pass gates, wherein: a first gate terminal of a first of said pass gates is arranged to receive the third binary input signal, a second gate terminal of said first pass gate is arranged to receive the inverse of the third binary input signal, a first gate terminal of a second of said pass gates is arranged to receive the inverse of the third binary input signal, and a second gate terminal of said second pass gate is arranged to receive the third binary input signal; input terminals of the first and second pass gates are connected to receive the first intermediate signal and the second intermediate signal respectively; and output terminals of said pass gates are used to generate said output signal.

WO 2004/104820 A2

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

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A Sum Bit Generation Circuit

The present invention relates to digital electronic devices, and in particular, to a digital electronic device performing binary logic.

In many applications in binary arithmetic, one requires a device, called a full adder (FA), which receives three digital signals and then computes the binary representation of the number of high signals among the three signals. Further, it is often advantageous to design the device so that the delay in the computation is much smaller for one of the three signals than for the other two. This is typically achieved by performing the computation in two stages, the first involving only two of the signals, the second involving the third signal and the result of the first stage. We refer to the third signal as the *carry-in*.

In one implementation of the device pass-gates are used, as these are typically faster than standard CMOS gates. When designing the circuit to conform to a standard-cell methodology, however, pass-gates pose one disadvantage: A FA standard cell must be *characterisable*, which is to say that it must have a well defined input capacitance and output impedance. On their own, pass-gates are not characterisable; two of the input/output pins, corresponding to the source and drain terminals of the pass-gate, do not have a well defined input capacitance. As a result, these pins are not normally permitted to be connected directly to the input/output pins of the standard cell. This constraint often results in a design which is not as fast as it might be.

The following notation is used for logical operations on Boolean variables (such that take one of two values, high and low):

- a b denotes the AND of a and b, which is high if a and b are high.
- a + b denotes the OR of a and b, which is high if a is high or b is high.
- a $\oplus$ b denotes the exclusive OR of a and b, which is high if a and b have different values.
- a-bar is the complement of a, which is high if a is low.

- $\sum_{i=a\ i=b} S(i)$ denotes the OR of a plurality of Boolean expressions, i.e. S(a) + S(a+1) + ... + S(b).

A prior-art FA circuit, at the level of Boolean logic, is shown in figure 1. This is an efficient way to build a FA with a fast carry-in (CIN). The circuit has three inputs, A, B and CIN, and two outputs S and C.

Output S represents a sum bit in the addition of A, B and CIN, and S is the logical XOR of inputs A, B and CIN, i.e. $S = A \oplus B \oplus CIN$. S is high if an odd number of A, B and CIN are high and is low if an even number are high.

Output C represents an output carry bit from the addition of A, B and CIN. C is high if at least two of A, B and CIN are high, otherwise C is low.

The circuit comprises an XOR gate 100 with inputs A and B and an output $A \oplus B$. A second XOR gate 110 has inputs $A \oplus B$ (from the first XOR gate 100) and CIN, and an output S. A multiplexer (mux) 120 has $A \oplus B$ as a select input, B (or equivalently A) as a "0" input, and CIN as a "1" input and gives C as an output. C is equal to A if $A \oplus B$ is low; C is equal to CIN if $A \oplus B$ is high.

A prior-art implementation of the circuit of figure 1, using pass-gates, is shown in figure 2. Again, the circuit has inputs A and B, a carry input CIN, a carry output C and a sum output S.

The first XOR gate 100 is implemented using pass gates 204, 205, 206 and 207. These pass gates actually work in pairs to form two XOR gates, one of which generates $A \oplus B$ using pass gates 206 and 207, and the other of which generates the complement of $A \oplus B$ using pass gates 204 and 205. The second XOR gate 110 is implemented using pass gates 215 and 216. The multiplexer 120 is implemented using pass gates 213 and 214.

Input A is connected to the input of an inverter 202. The output of this inverter 202 is connected to the source terminal of pass gates 204 and 207. The output of inverter 202

is also connected to the input of a further inverter 203. The output of inverter 203 is connected to the source terminal of pass gates 205 and 206.

Input B is connected directly to the gate terminals of pass gates 205 and 207, and to the inverse gate terminals of pass gates 204 and 206. Input B is also connected to the input of inverter 201. The output of inverter 201 is connected to the gate terminals of pass gates 204 and 206, and to the inverse gate terminals of pass gates 205 and 207. The output of inverter 201 is also connected to the source terminal of pass gate 214.

Pass gates 206 and 207 and inverters 201, 202 and 203 function as an XOR gate, to generate the function A ⊕ B. The drain outputs of pass gates 206 and 207 are connected together to give a A ⊕ B output.

Only one of pass gates 206 and 207 is switched on at the same time, because pass gate 206 receives the opposite control signal on its gate terminals to that received by pass gate 207, due to the order of connection of the B input and the inverted B input to the gate terminals. Pass gate 206 is switched on only if B is low, but pass gate 207 is switched on only if B is high. Thus, if B is low, the signal passed by pass gate 206 is from the A input, but if B is high, the signal passed by pass gate 207 is from the inverted A input. By this means, the XOR function is performed.

Pass gates 204 and 205 and inverters 201, 202 and 203 also function as an XOR gate, but they generate the complement of the function A ⊕ B. The drain outputs of pass gates 204 and 205 are connected together to give a (A ⊕ B)-bar output, represented on the figure as AxorBbar.

Only one of pass gates 204 and 205 is switched on at the same time, because pass gate 204 receives the opposite control signal on its gate terminals to that received by pass gate 205, due to the order of connection of the B input and the inverted B input to the gate terminals. Pass gate 204 is switched on only if B is low, but pass gate 205 is switched on only if B is high. Thus, if B is low, the signal passed by pass gate 204 is

from the inverted A input, but if B is high, the signal passed by pass gate 205 is from the A input.

The drain outputs of pass gates 206 and 207 are connected to the gate terminals of pass gates 213 and 215 and the inverse gate terminals of pass gates 214 and 216, providing the A ⊕ B signal at these terminals. The drain outputs of pass gates 204 and 205 are connected to the gate terminals of pass gates 214 and 216 and the inverse gate terminals of pass gates 213 and 215, providing the (A ⊕ B)-bar signal at these terminals.

The carry input CIN is connected to the input terminal of inverter 211. The output of inverter 211 is connected to the source inputs of pass gates 213 and 216. The output of inverter 211 is also connected to the input of inverter 212. The output of inverter 212 is connected to the source input of pass gate 215. The source input of pass gate 214 is connected to the output of inverter 201, to receive a signal of not-B.

The pass gates 215 and 216 act together as an XOR gate to generate an output sum bit S. The drain outputs of pass gates 215 and 216 are connected together, and are connected to the input of inverter 218.

The pass gates 215 and 216 are switched by the A ⊕ B and (A ⊕ B)-bar outputs of the pass gates 204-207 in the first part of the circuit. When A ⊕ B is high, pass gate 215 is switched on, and the CIN signal is passed through to inverter 218, where it is inverted to generate not-CIN. When A ⊕ B is low, pass gate 216 is switched on, and the not-CIN signal is passed through to inverter 218, where it is inverted to generate not-CIN. In other words, the sum bit S is only high if only one of A, B and CIN, or all three of A, B and CIN is high.

The pass gates 213 and 214 act together as a multiplexer to generate a carry output bit C. The drain outputs of pass gates 213 and 214 are connected together, and are connected to the input of inverter 217.

The pass gates 213 and 214 are switched by the A ⊕ B and (A ⊕ B)-bar outputs of the pass gates 204-207 in the first part of the circuit. When A ⊕ B is high, pass gate 213 is switched on, and the not-CIN signal is passed through to inverter 217, where it is inverted to generate CIN. When A ⊕ B is low, pass gate 214 is switched on, and the not-B signal is passed through to inverter 217, where it is inverted to generate B. In other words, the carry output bit C is only high if at least two of A, B and CIN are high.

Since the implementation conforms to the standard-cell methodology, no pass-gate source or drain connection is connected to either an input pin or an output pin. As a result, the *critical path* from CIN to the outputs, along which signals take the longest time to propagate, passes through a total of three inverters 211, 212 and 218 and a pass-gate 215.

The present invention provides a circuit for generating a sum bit representing the least significant bit in the sum of three binary input signals. The three inputs may consist of a first and second binary input and a carry in input. The circuit may also generate a carry out bit, representing the most significant bit in the sum of the three binary input signals.

The circuit generates a first and a second intermediate signal using a first set of logic elements. These intermediate signals correspond to the logical XOR of the first and second inputs, and to the inverse of the logical XOR of the first and second inputs respectively.

The circuit then generates the sum bit using a second set of logic elements, which includes two pass gates. The first and second intermediate signals are used as inputs to each of the two pass gates respectively. The third input signal and its inverse are used as pass gate control inputs, where the order of connection of the third input signal and its inverse to the first pass gate control inputs is the opposite to that for the second pass gate control inputs, such that only one of the two pass gates can be open at any one time. The pass gates are connected in a configuration which generates a logical XOR of the third input signal and the first or second intermediate signal. The outputs of the two pass gates are connected together, and may be connected to an output inverter, to

generate the sum output bit. The advantage of connecting the output via an output inverter is that it ensures a low output impedence, which is important if the circuit is used in a standard cell.

The first set of logic elements may include a pair of high input impedence buffer components, with one buffer component being arranged to output the first intermediate signal, and the other buffer component being arranged to output the second intermediate signal. The buffer components may be any components which transfer the signal, but also provide a low output impedence. The buffer components may be inverters, transferring the inverted signal and providing a low output impedence. If inverters are used as buffer components, it is possible to simply interchange the connections providing the first and second intermediate signals respectively, to compensate for each signal being inverted.

The first set of logic elements may include pass gates for generating the logical XOR of the first and second inputs as the first intermediate signal. Alternatively, or additionally, a set of pass gates may be provided for generating the logical XNOR of the first and second inputs as the second intermediate signal. If only one set of pass gates is provided, the other intermediate signal may be generated using an inverter and the output of the set of pass gates.

The circuit may include a third set of logic elements to generate an output carry bit. The third set of logic elements may be a set of pass gates which is configured to function as a multiplexer. The first and/or second intermediate signals may be used to switch the multiplexer. The multiplexer inputs may be the third input signal or its inverse, and the first or second input signal or its inverse. The multiplexer inputs may be isolated from the source terminals of all other pass gates to prevent unwanted capacitance effects from slowing down the circuit.

Preferred embodiments of the invention provide an alternative implementation of a fast adder to that known in the prior art. Preferred embodiments of the invention conform to the standard-cell methodology, where no pass-gate source connection is connected to an input pin. Furthermore, preferred embodiments conforming to the standard-cell

methodology may also have no pass gate drain connection connected to an output pin. However, the present invention is not limited to such a technology or design.

Further aspects of the present invention include a circuit board comprising the circuit described in the claims, a standard cell comprising the circuit described in the claims, and an adder for adding together two multi-bit binary numbers, using a circuit as described in the claims.

Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a circuit diagram showing a gate-level implementation of a full adder with fast carry-in, as known in the prior art;

Figure 2 is a circuit diagram showing a prior-art implementation of a fast adder using inverters and pass-gates;

Figure 3 is a circuit diagram showing a first embodiment of the invention; and

Figure 4 is a circuit diagram showing a second embodiment of the invention.

Figure 3 is a circuit diagram corresponding to a first embodiment of the present invention, which provides modifications to the prior art circuit of figure 2. Again, the circuit has inputs A and B, a carry input CIN, a carry output C and a sum output S.

The circuit of figure 3 has modifications to reduce the delay from the carry-in to the outputs, but retain a characterisable circuit, with well defined input capacitance and output impedence. The circuit comprises a first subcircuit 1001, a second subcircuit 1002 and a third subcircuit 1003.

The first modification is that the XOR gate that produces the signal S is implemented so that the CIN signal is connected to the pass-gate mux's select inputs. This means that two inverters are no longer required just after the CIN input.

The second modification is that two inverters are added to buffer the signals A ⊕ B and (A ⊕ B)-bar. The inverters' outputs are connect only to the multiplexer producing the S output. These speed up any transitions on S caused by CIN.

The critical path from CIN to the output of the embodiment of the present invention passes through a total of two inverters and one pass-gate. This represents a saving of one inverter compared with the implementation in Fig. 2.

The first subcircuit comprises inverters 301, 302, 303, 321 and 322 and pass gates 304, 305, 306 and 307. A first binary input A is connected to the input of the inverter 302. The output of this inverter 302 is connected to the source terminal of pass gates 304 and 307. The output of inverter 302 is also connected to the input of inverter 303. The output of inverter 303 is connected to the source terminal of pass gates 305 and 306.

A second binary input B is connected directly to the gate terminals of pass gates 305 and 307, and to the inverse gate terminals of pass gates 304 and 306. Input B is also connected to the input of inverter 301. The output of inverter 301 is connected to the gate terminals of pass gates 304 and 306, and to the inverse gate terminals of pass gates 305 and 307. The output of inverter 301 is also connected to the source terminal of pass gate 314.

Pass gates 306 and 307 and inverters 301, 302 and 303 function as an XOR gate, to generate the function A ⊕ B. The drain outputs of pass gates 306 and 307 are connected together to give a A ⊕ B output.

Only one of pass gates 306 and 307 is switched on at the same time, because pass gate 306 receives the opposite control signal on its gate terminals to that received by pass gate 307, due to the order of connection of B and not-B to the gate terminals. Pass gate 306 is switched on only if B is low, but pass gate 307 is switched on only if B is high. Thus, if B is low, the signal passed by pass gate 306 is A, but if B is high, the signal passed by pass gate 307 is not-A. By this means, the XOR function is performed.

Pass gates 304 and 305 and inverters 301, 302 and 303 also function as an XOR gate, but they generate the complement of the function A ⊕ B. The drain outputs of pass gates 304 and 305 are connected together to give a (A ⊕ B)-bar output, represented on the figure as AxorBbar.

Only one of pass gates 304 and 305 is switched on at the same time, because pass gate 304 receives the opposite control signal on its gate terminals to that received by pass gate 305, due to the order of connection of B and not-B to the gate terminals. Pass gate 304 is switched on only if B is low, but pass gate 305 is switched on only if B is high. Thus, if B is low, the signal passed by pass gate 304 is not-A, but if B is high, the signal passed by pass gate 305 is A.

The outputs of the pass gates 306 and 307 are input to an inverter 322 acting as a high impedence buffer to generate an (A ⊕ B)-bar output. Similarly, the outputs of the pass gates 304 and 305 are input to an inverter 321 to generate an A ⊕ B output. The outputs of the inverters 321 and 322 comprise the outputs of the first subcircuit 1001.

The carry input CIN is connected to the input terminal of an inverter 311. The output of the inverter 311 is connected to the source input of a pass gate 313 in the third subcircuit 1003, to the inverse gate input of a pass gate 315 and to the gate input of a pass gate 316 in the second subcircuit 1002. The carry input CIN is directly connected to the gate input of pass gate 315 and to the inverse gate input of pass gate 316 of the second subcircuit 1002. The source input of pass gate 314 in the third subcircuit 1003 is connected to the output of inverter 301, which gives a signal of not-B.

The pass gates 315 and 316 of the second subcircuit 1002 act together as an XOR gate to generate an output sum bit S. The drain outputs of pass gates 315 and 316 are connected together, and are connected to the input of inverter 318.

The pass gates 315 and 316 are switched by the CIN input, and its complement CIN-bar. When CIN is high, pass gate 315 is switched on, and the A ⊕ B signal is passed

through to inverter 318, where it is inverted to generate (A ⊕ B)-bar. When CIN is low, pass gate 316 is switched on, and the (A ⊕ B)-bar signal is passed through to inverter 318, where it is inverted to generate A ⊕ B. In other words, the sum bit S is only high if only one of A, B and CIN, or all three of A, B and CIN is high.

The pass gates 313 and 314 of the third subcircuit 1003 act together to generate the carry output bit C. The drain outputs of pass gates 313 and 314 are connected together, and are connected to the input of inverter 317.

The pass gates 313 and 314 are switched by the A ⊕ B and (A ⊕ B)-bar outputs of the pass gates 304-307 in the first part of the circuit. When A ⊕ B is high, pass gate 313 is switched on, and the CIN-bar signal is passed through to inverter 317, where it is inverted to generate CIN. When A ⊕ B is low, pass gate 314 is switched on, and the B-bar signal is passed through to inverter 317, where it is inverted to generate B. The circuit would work equally well if the A-bar signal was used in place of the B-bar signal. In other words, the carry output bit C is only high if at least two of A, B and CIN are high.

Figure 4 is a circuit diagram corresponding to a second embodiment of the invention. In this second embodiment, the second and third subcircuits 2002 and 2003 are the same as those of the first embodiment shown in figure 3. However, in the second embodiment, the first subcircuit 2001 has only one pair of pass gates 406, 407. These pass gates are used to generate A ⊕ B. In order to generate (A ⊕ B)-bar, the outputs from the pass gates 406, 407 are connected to the input of an inverter 422, and the inverter 422 outputs the (A ⊕ B)-bar signal.

The output of inverter 422 is fed to the source terminal of pass gate 416 to allow the sum output bit to be generated. The output of inverter 422 is also fed to the inverse gate terminal of pass gate 413 and to the gate terminal of pass gate 414 to allow the carry output bit to be generated.

The A ⊕ B signal generated as the output of the pass gates 406 and 407 is suitable for directly controlling the gate terminal of a further pass gate. However, for controlling the source terminal of a further pass gate, it may be advantageous to use at least one intermediate inverter, to present a lower output impedence to the source terminal. Therefore, in figure 4, a further inverter 423 is provided. The output of inverter 422 is fed into the input of inverter 423 to generate a further signal corresponding to A ⊕ B. The output of inverter 423 is then fed into the source terminal of pass gate 415.

The embodiment of figure 4 has an extra inverter 423 in the path to generate a A ⊕ B signal. Where CIN is a carry bit that takes longer to generate than either A or B, any small reduction in the speed of generating A ⊕ B, due to this extra inverter, may not be critical. The embodiment of figure 4 has the advantage that by omitting pass gates 404 and 405, the amount of area needed for the circuit is less than that for the circuit of figure 3.

The circuits according to the present invention may be used for the addition of any three binary numbers, and may be used in any device which has a need to add three binary numbers together. It is not essential that the third input signal is specially selected, e.g. a carry input. Any binary input signal can be used as either the first, second or third input signal.

However, in order to take advantage of the reduced critical path for the third input signal, the third input signal may be chosen as a signal which takes longer to generate than either the first or the second input signal. The first and second signals may result from a faster calculation process than the third signal. For example, a piece of hardware may have three detectors, each generating a signal to be added, but where one of the signals requires more processing than the other two signals. This signal needing more processing may be used for the third input signal of the circuit.

In some applications adding three independent bits together, further provision may need to be made to deal with any carry bits arising during the addition. Standard methods known to a person skilled in the art may be used to deal with such carry bits.

Although other uses of the invention are possible, a major application of the invention is for an adder with fast carry-in. In this application, the first and second input signals correspond to individual bits to be added during a sum of two multi-bit numbers, and the third input signal may correspond to a carry input bit, generated by the previous column of the sum.

Embodiments of the present invention are suitable for standard cell technology in which the inputs and outputs have fixed input capacitance. The use of high input impedence devices such as inverters at the inputs and outputs of the pass gates facilities this.

While the invention has been described in terms of what are at present its preferred embodiments, it will be apparent to those skilled in the art that various changes can be made to the preferred embodiments without departing from the scope of the invention, which is defined by the claims.

CLAIMS:

1. A circuit for generating a sum bit representing the sum of three binary input signals; the circuit comprising:

first logic arranged to generate a first intermediate signal as the logical XOR of the first and second binary input signals and a second intermediate signal as the inverse of the logical XOR of the first and second binary input signals; and

second logic arranged to receive said first and second intermediate signals generated by said first logic, and to generate an output signal as the logical XOR of the first intermediate signal and the third binary input signal, said second logic comprising at least two pass gates, wherein:

a first gate terminal of a first of said pass gates is arranged to receive the third binary input signal, a second gate terminal of said first pass gate is arranged to receive the inverse of the third binary input signal, a first gate terminal of a second of said pass gates is arranged to receive the inverse of the third binary input signal, and a second gate terminal of said second pass gate is arranged to receive the third binary input signal;

input terminals of the first and second pass gates are connected to receive the first intermediate signal and the second intermediate signal respectively; and

output terminals of said pass gates are used to generate said output signal.

2. A circuit as claimed in claim 1, wherein the first logic includes a pair of high input impedence buffer components, a first of said buffer components being arranged to output the first intermediate signal, and a second of said buffer components being arranged to output the second intermediate signal.

3. A circuit as claimed in claim 2, wherein each of said high impedence buffer components comprises an inverter.

4. A circuit as claimed in any one of the previous claims, wherein said first logic includes at least two pass gates for use in the generation of said first and second intermediate signals.

5. A circuit as claimed in claim 4, wherein said at least two pass gates comprises a first pair of pass gates for use in the generation of said first intermediate signal and a second pair of pass gates for use in the generation of said second intermediate signal.

6. A circuit as claimed in claim 5, wherein said first logic includes a first inverter for inverting combined outputs of said first pair of pass gates to generate said first intermediate output, and a second inverter for inverting combined outputs of the second pair of pass gates to generate said second intermediate output.

7. A circuit as claimed in claim 4, wherein said at least two pass gates are connected to generate one of the first or second intermediate signals, and the first logic further comprises an inverter to generate the other of the first or second intermediate signals using said one of the first or second intermediate signals.

8. A circuit as claimed in claim 4, wherein said first logic circuit comprises a first inverter for inverting combined output of said at least two pass gates to generate said second intermediate signal and a second inverter for inverting the output of the first inverter for generating the first intermediate signal.

9. A circuit as claimed in any one of the previous claims, wherein said second logic comprises at least one inverter connected to said output terminals to generate said output signal.

10. A circuit as claimed in any one of the previous claims, further comprising third logic to generate an output carry bit using the inverse of said third binary input signal and at least one of the first and second intermediate signals.

11 A circuit as claimed in claim 10, wherein the third logic comprises a pair of pass gates.

12. A circuit as claimed in claim 11, wherein said third logic comprises at least one inverter connected to output terminals of said pass gates of the third logic to generate said output signal.

13. A circuit as claimed in claim 11 or claim 12, wherein the inverse of the third binary input is connected to an input terminal of one of the pass gates of the third logic, and wherein said input terminal of said one of the pass gates of the third logic is isolated from the input terminals of all other said pass gates.

14. A circuit as claimed in any previous claim, wherein said three inputs signals comprise first and second addition bits and a carry-in bit.

15. An adder circuit for adding together two multi-bit binary numbers, comprising a plurality of circuits according to any one of the previous claims.

16. A standard cell comprising the circuit as claimed in any one of the previous claims.

17. A circuit board comprising a plurality of the circuits as claimed in any one of the previous claims.

PRIOR ART

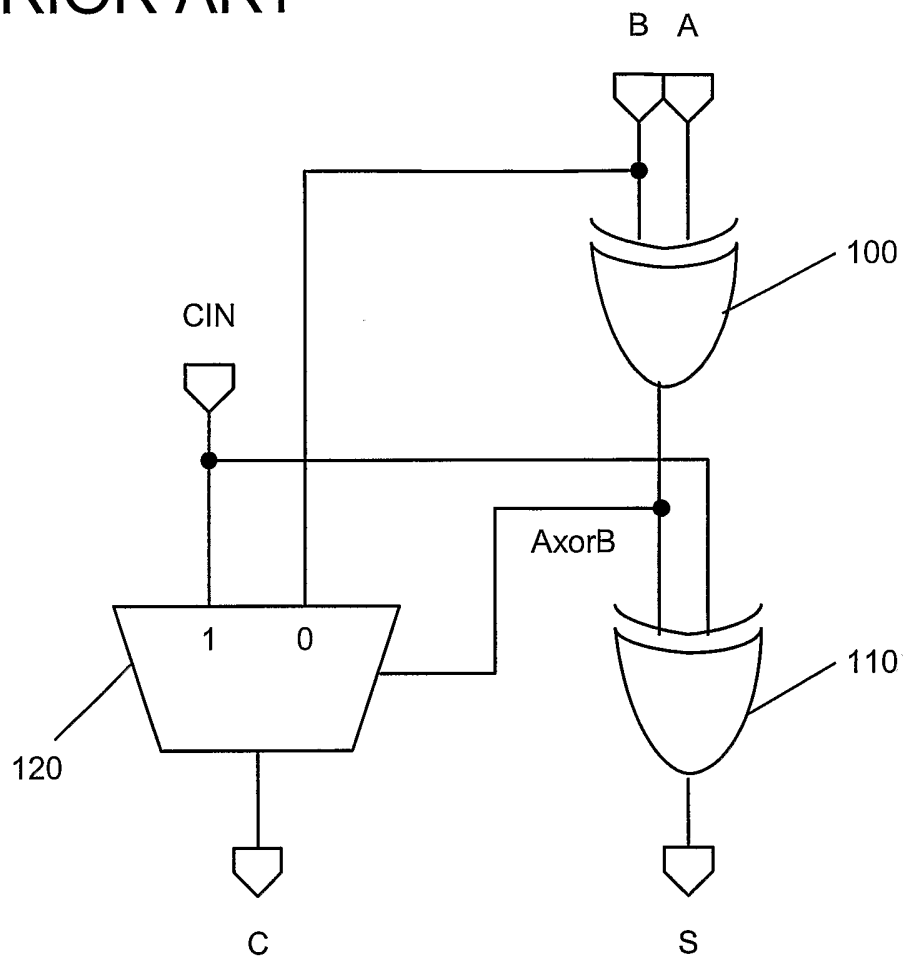
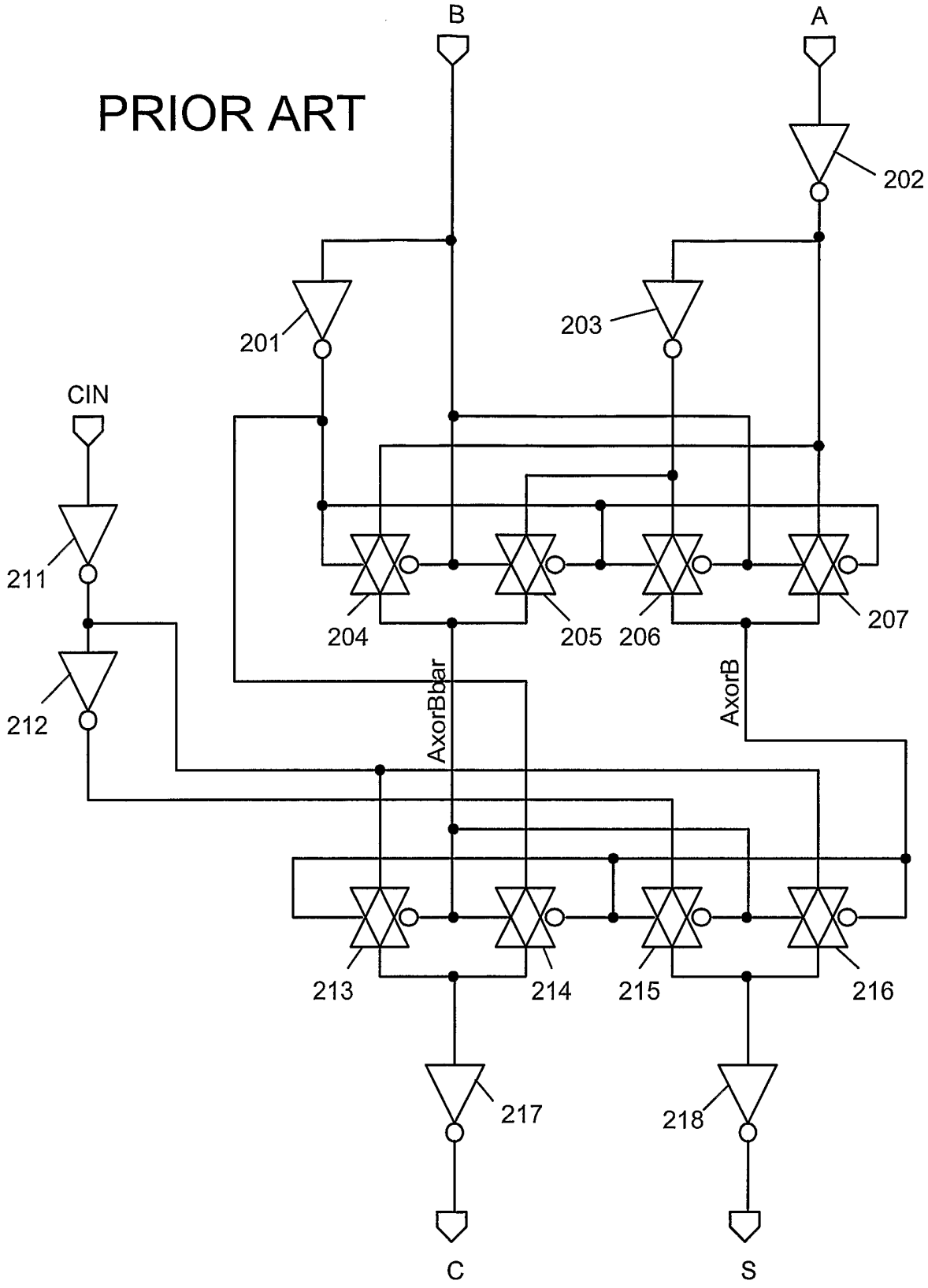


Figure 1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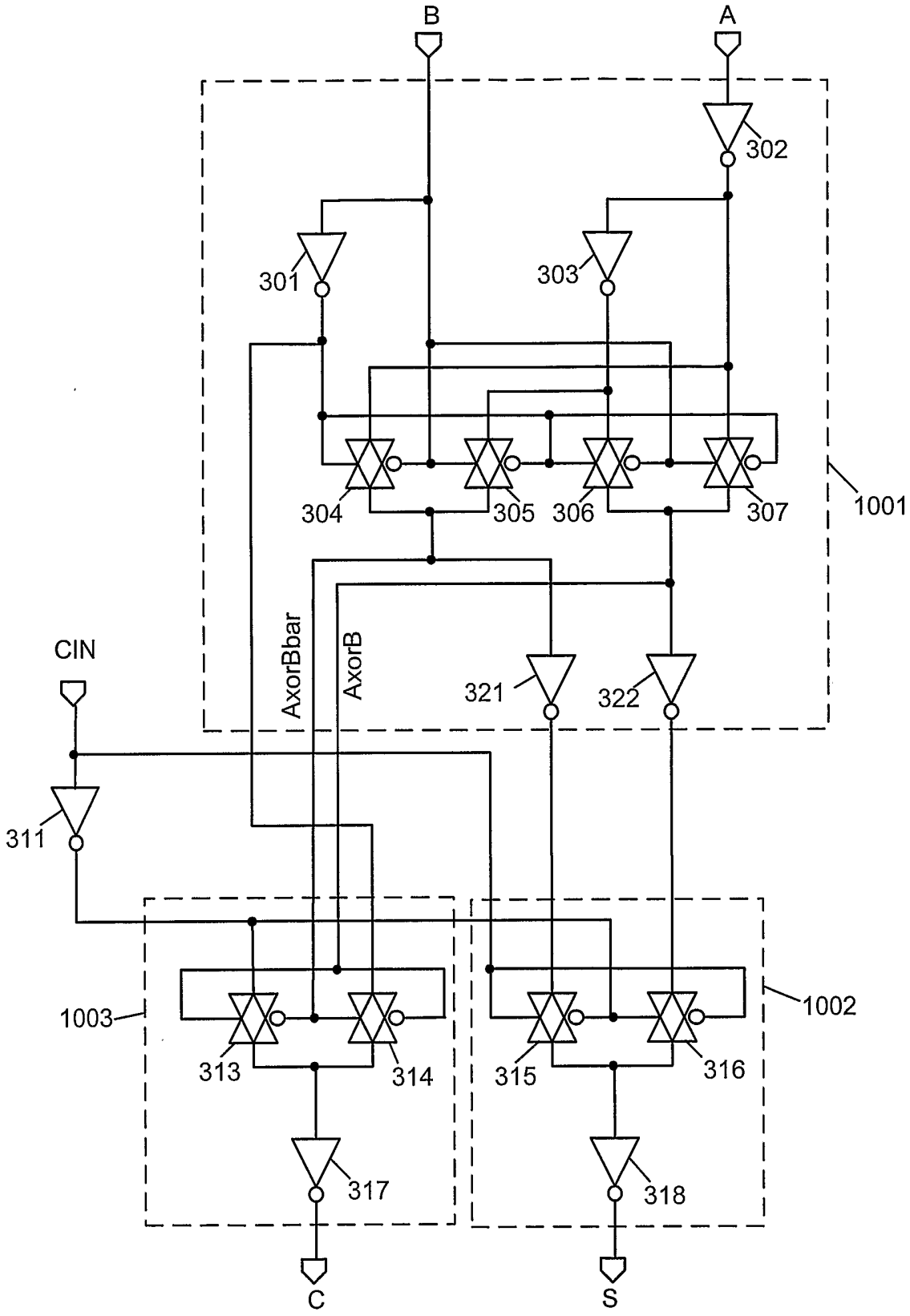
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1002
313
314
315
316
317
318
C
S

Figure 3

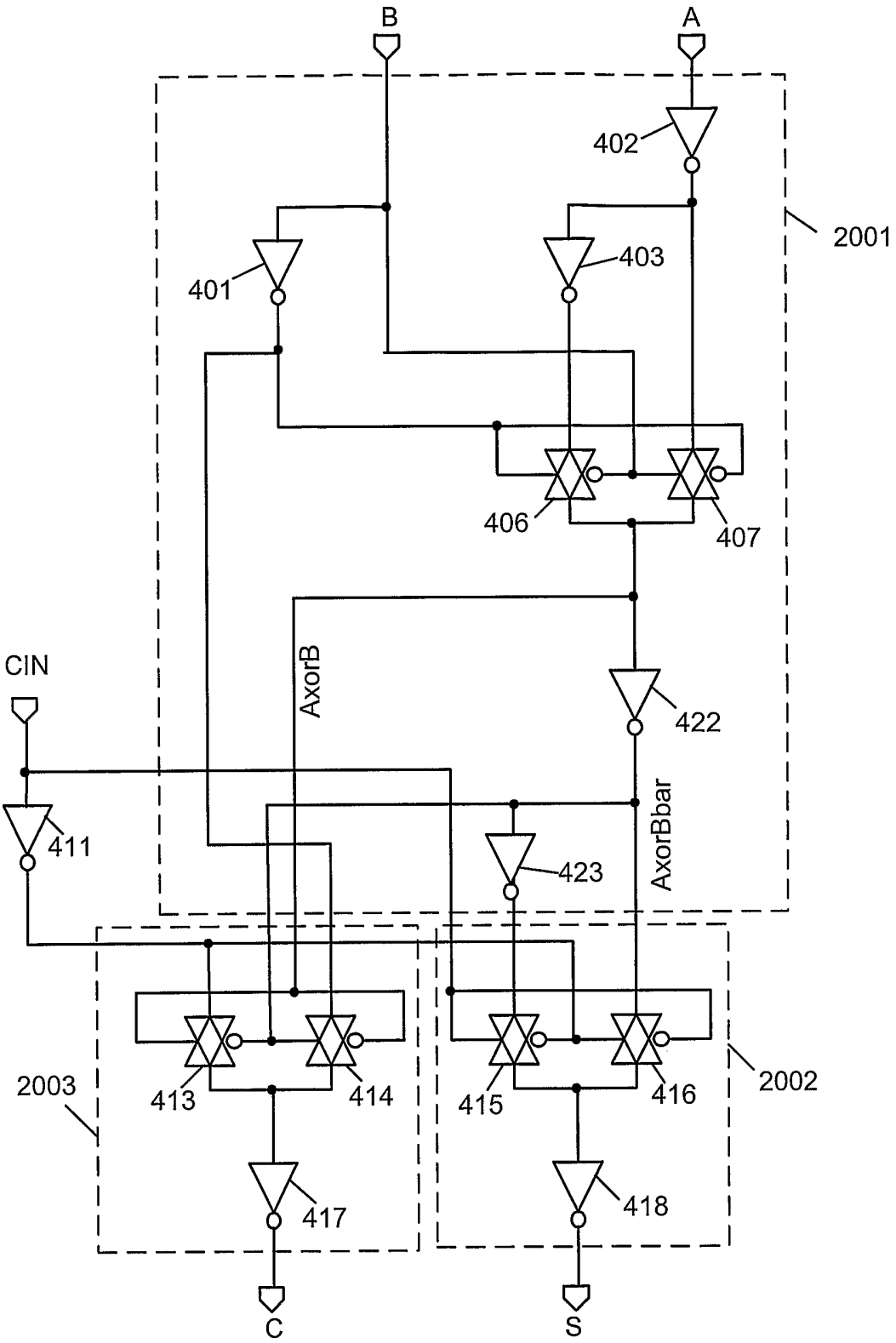
B
A
402
2001
401
403
406
407
CIN
AxorB
422
411
423
AxorBbar
2003
413
414
415
416
2002
417
418
C
S

Figure 4