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[54] HIGH SPEED TIMING GENERATOR

[52] U.S. Cl. 307/269; 328/63; 328/72

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[58] Field of Search 307/269; 328/63, 72

[56] References Cited

[73] Assignee: Teradyne, Inc., Boston, Mass.

U.S. PATENT DOCUMENTS

[21] Appl. No.: 15,403

4,586,005 4/1986 Crawford 331/1 A

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Primary Examiner—Margaret R. Wambach

Related U.S. Application Data

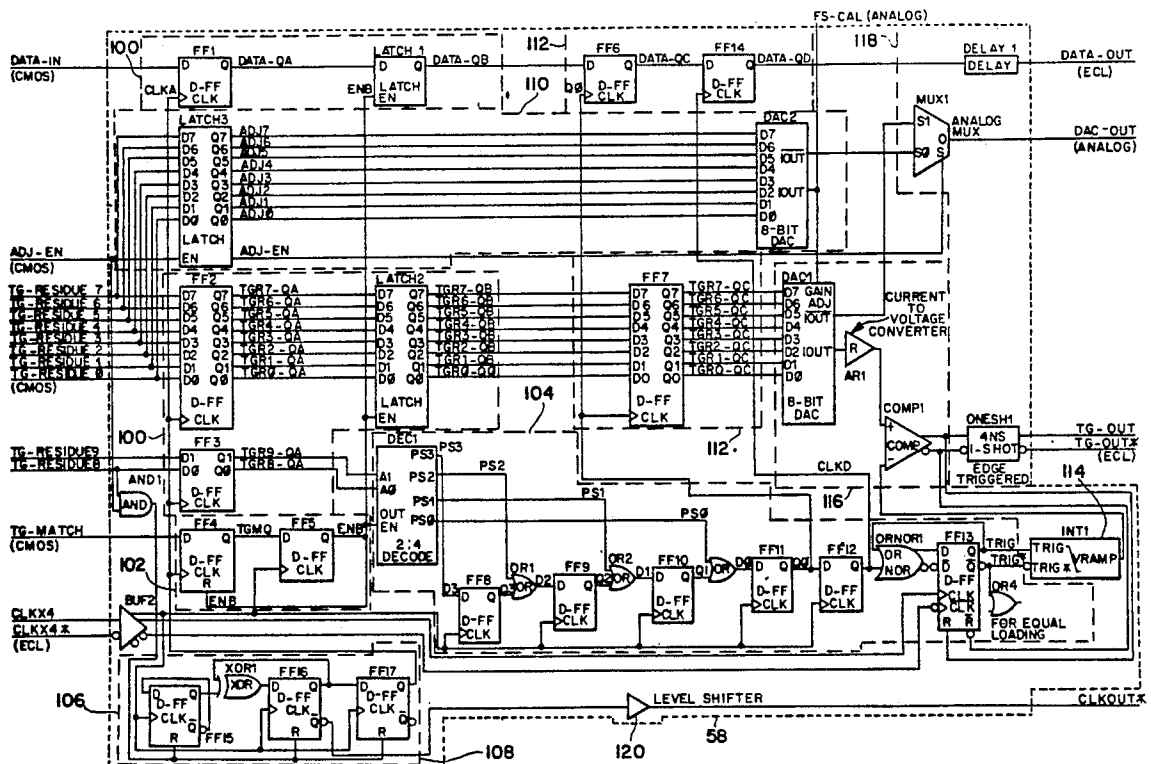
[60] Division of Ser. No. 605,977, Oct. 30, 1990, which is a continuation-in-part of Ser. No. 419,699, Oct. 11, 1989, abandoned.

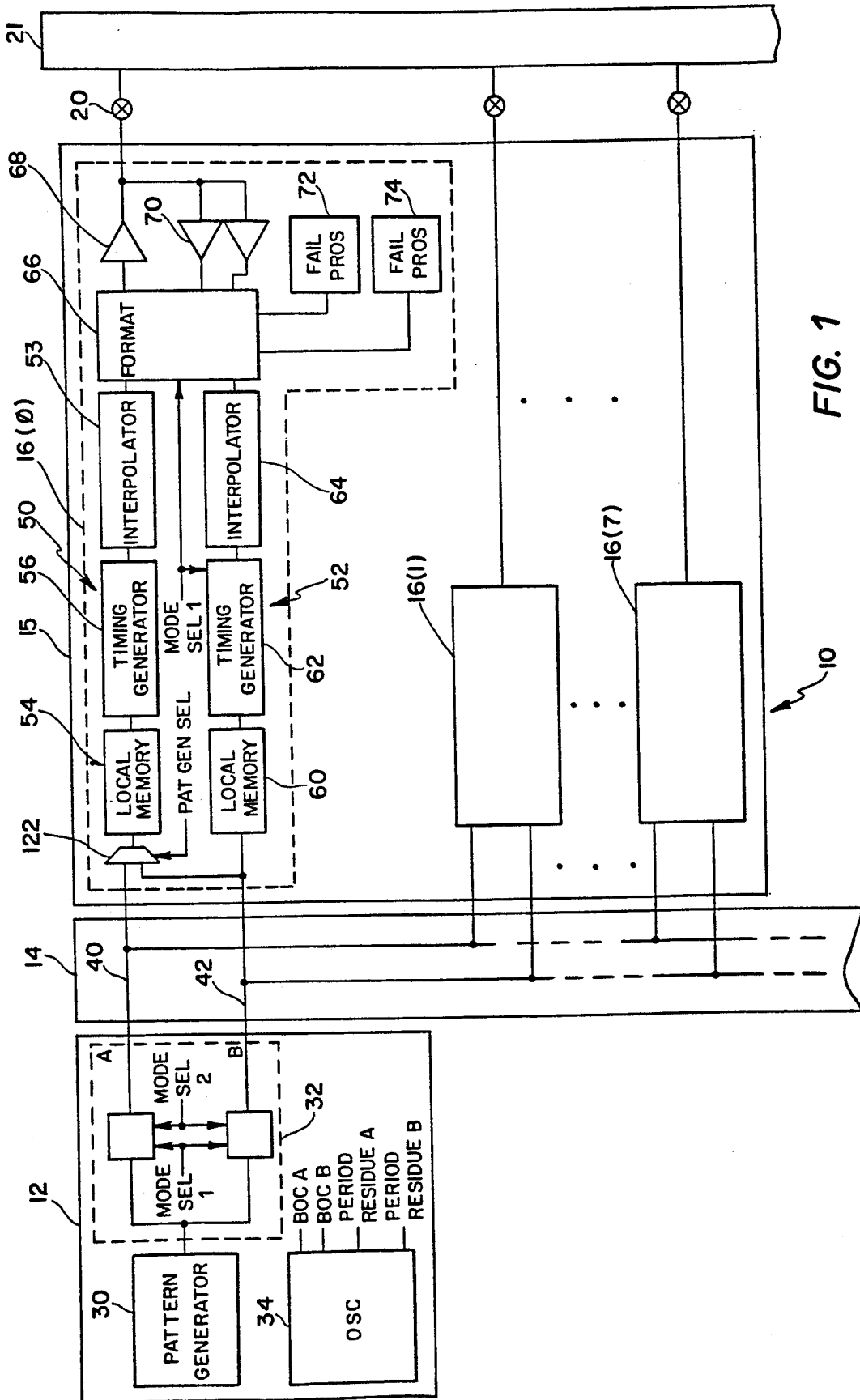
[57] ABSTRACT

"The present invention provides an interpolator circuit including a register, a pulse swallower, a ramping circuit and a compare circuit. The interpolator may be employed in a high speed timing generator".

[51] Int. Cl.⁵ H03K 5/13; H03K 17/26

7 Claims, 8 Drawing Sheets





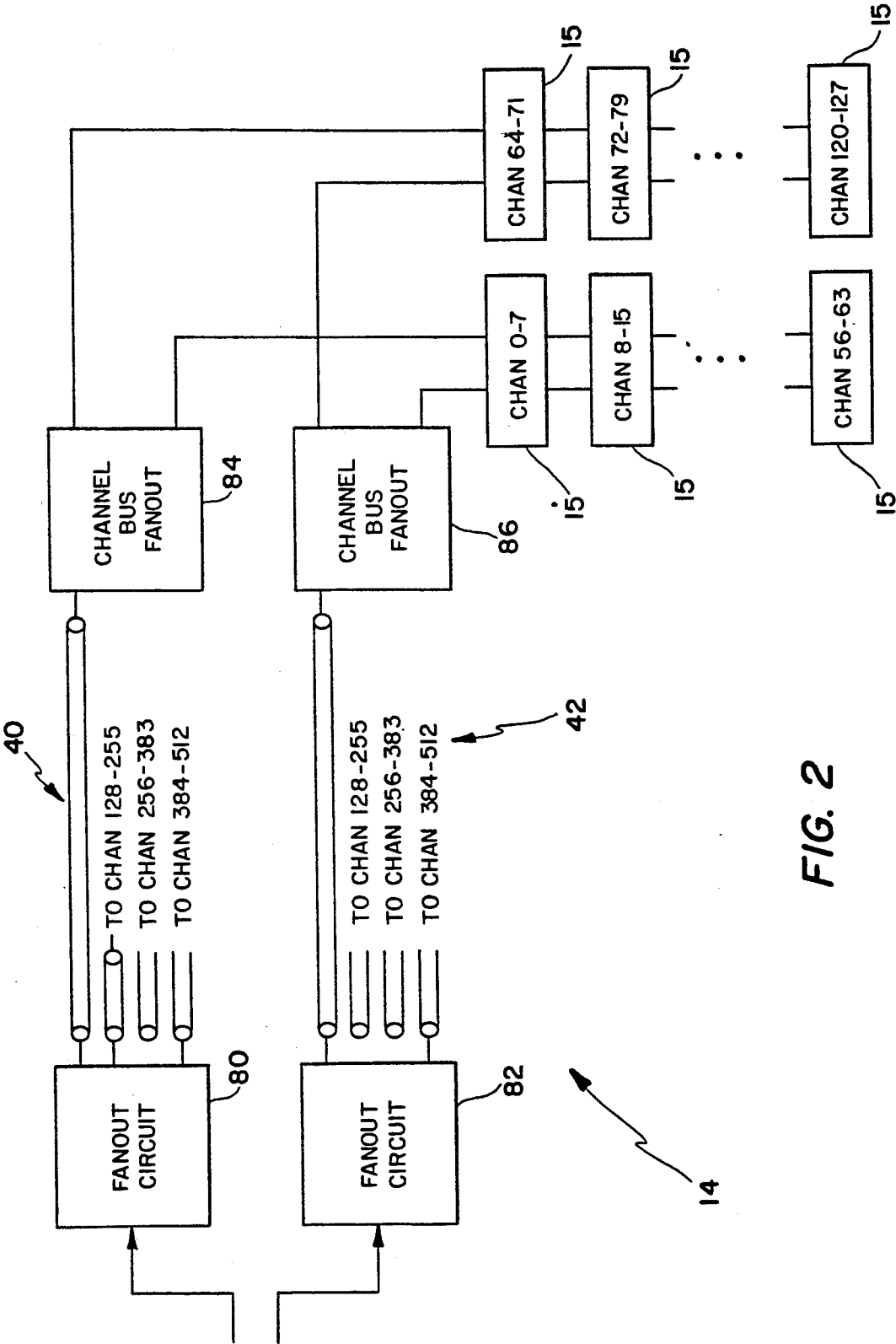
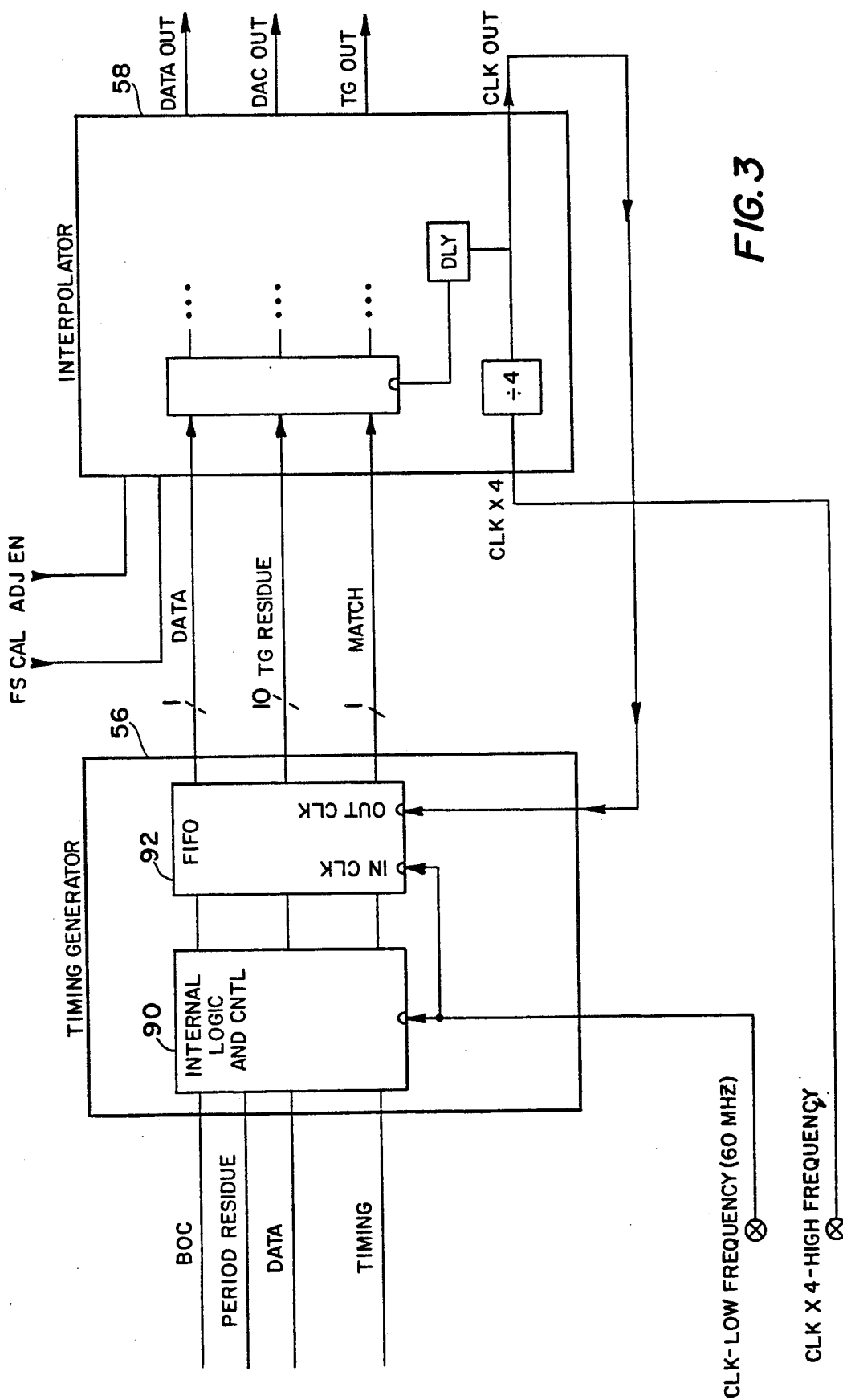


FIG. 2



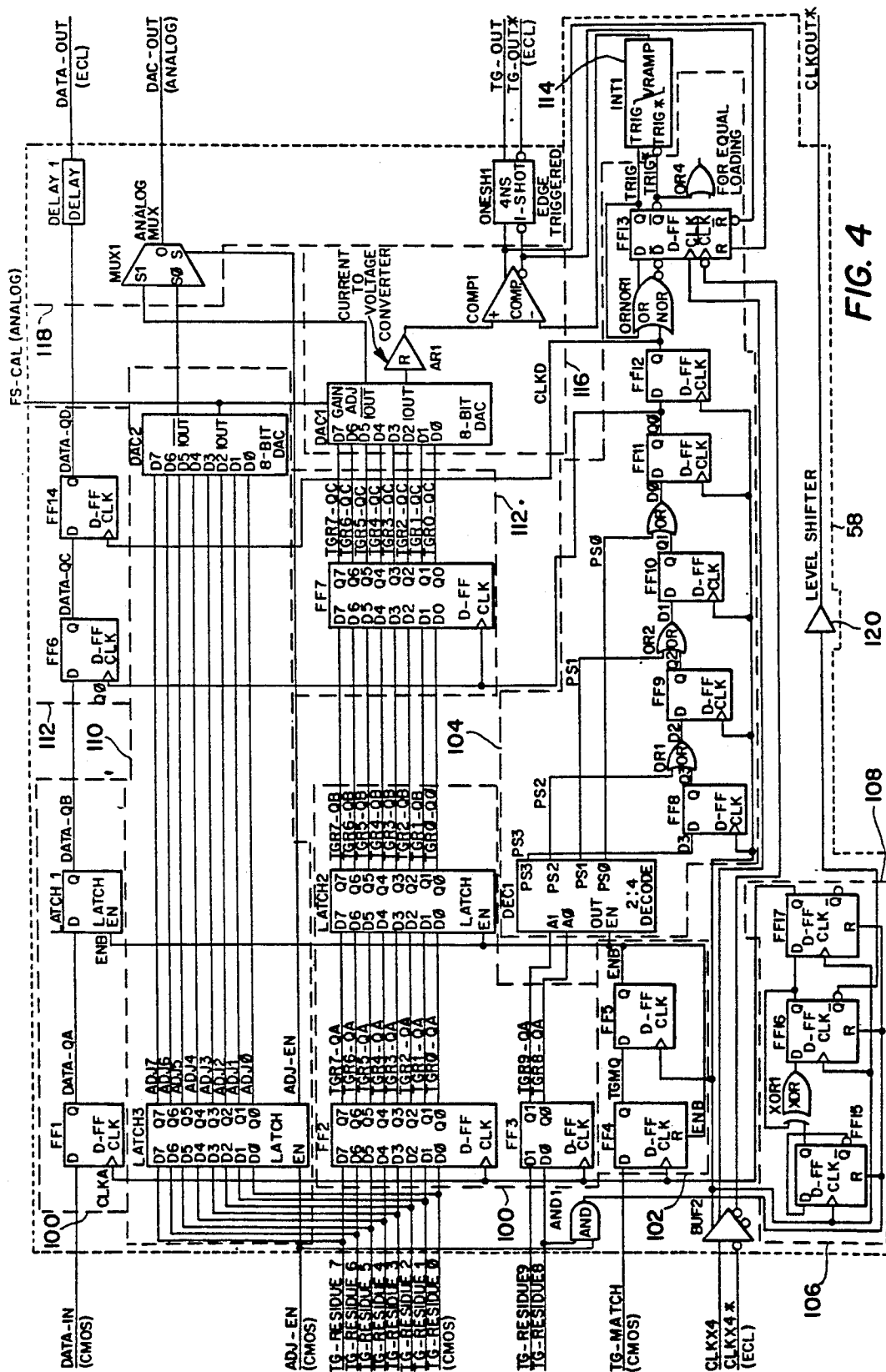
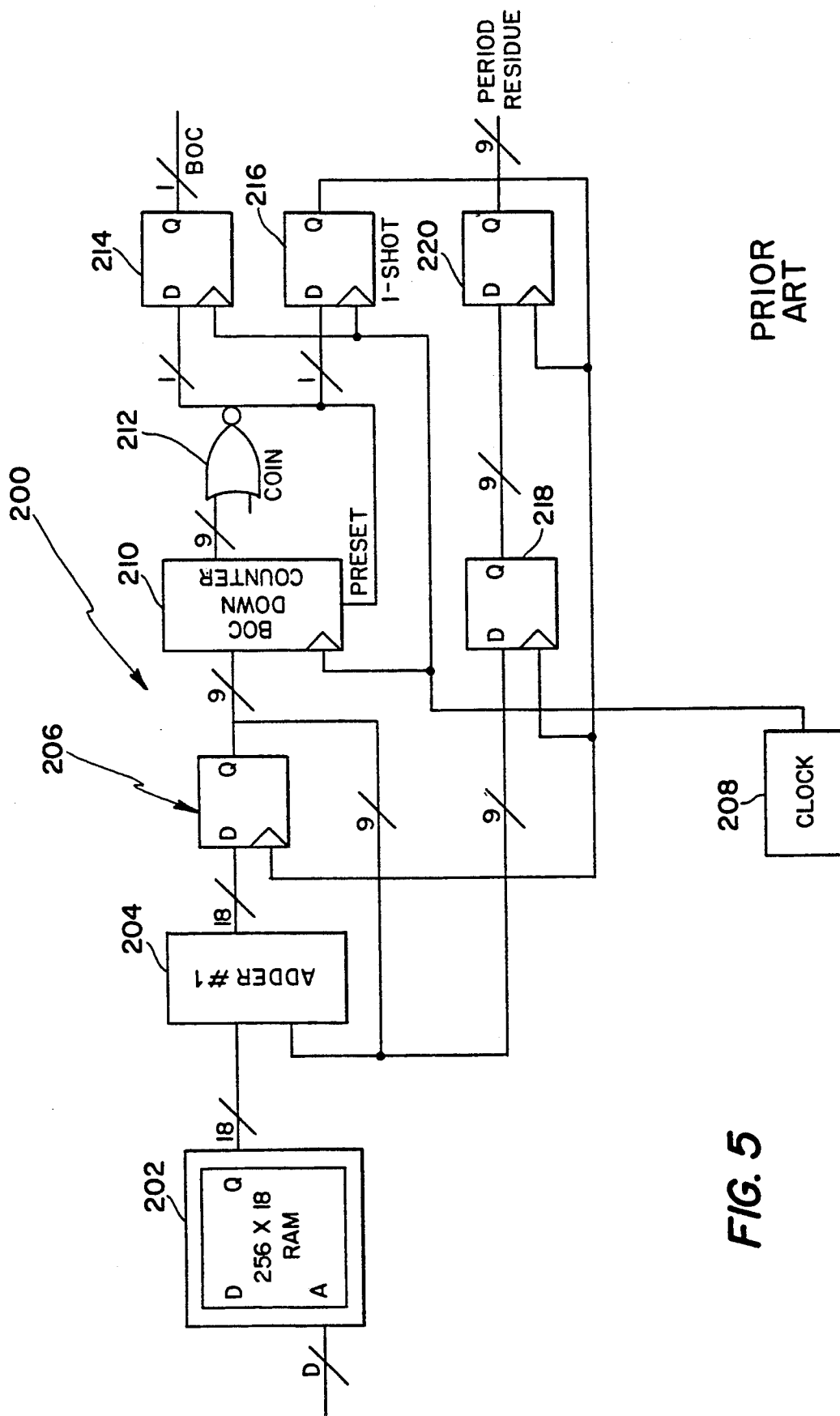
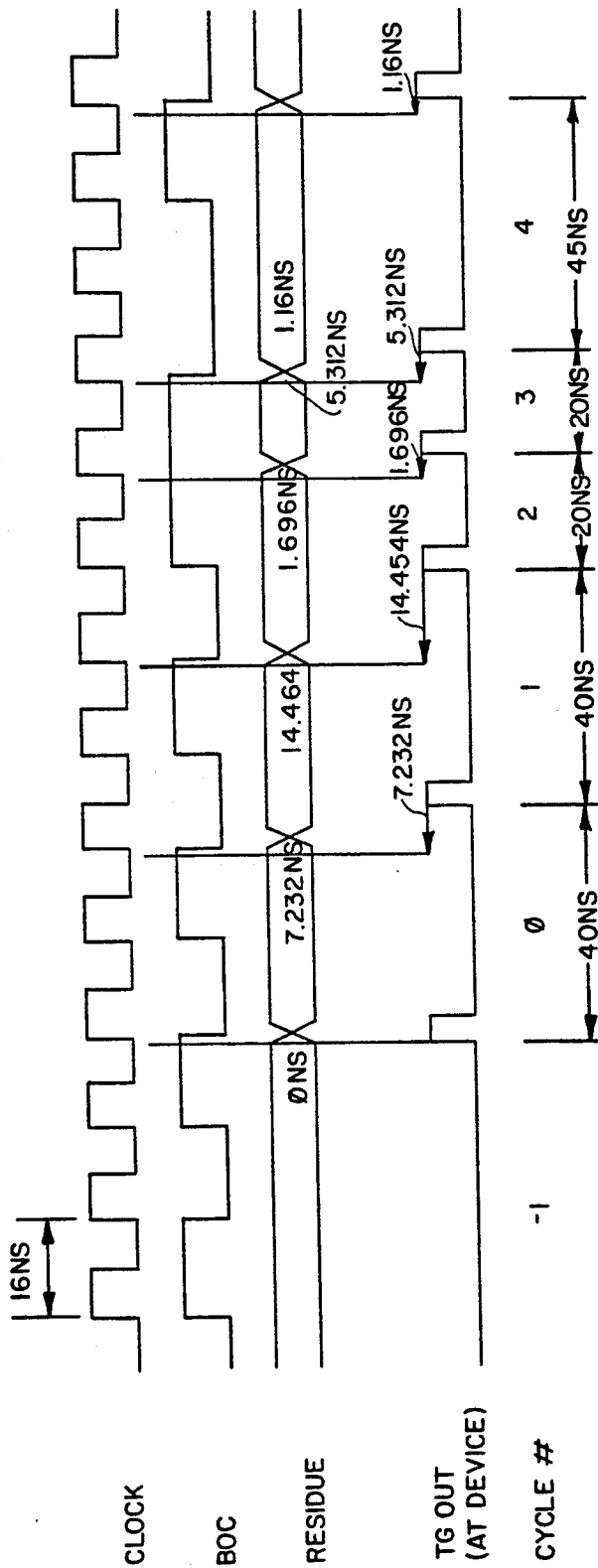


FIG. 4





CYCLE #	PERIOD (NS)	MSB'S	LSB'S	RESIDUE (NS)
-1*	32.768	32.768	0	0
0	40	32.768	7.232	7.232
1	40	32.768	7.232	14.464
2	20	16.384	3.616	1.696 + CARRY
3	20	16.384	3.616	5.312
4	45	32.768	12.232	1.16 + CARRY

FIG. 6 PRIOR ART

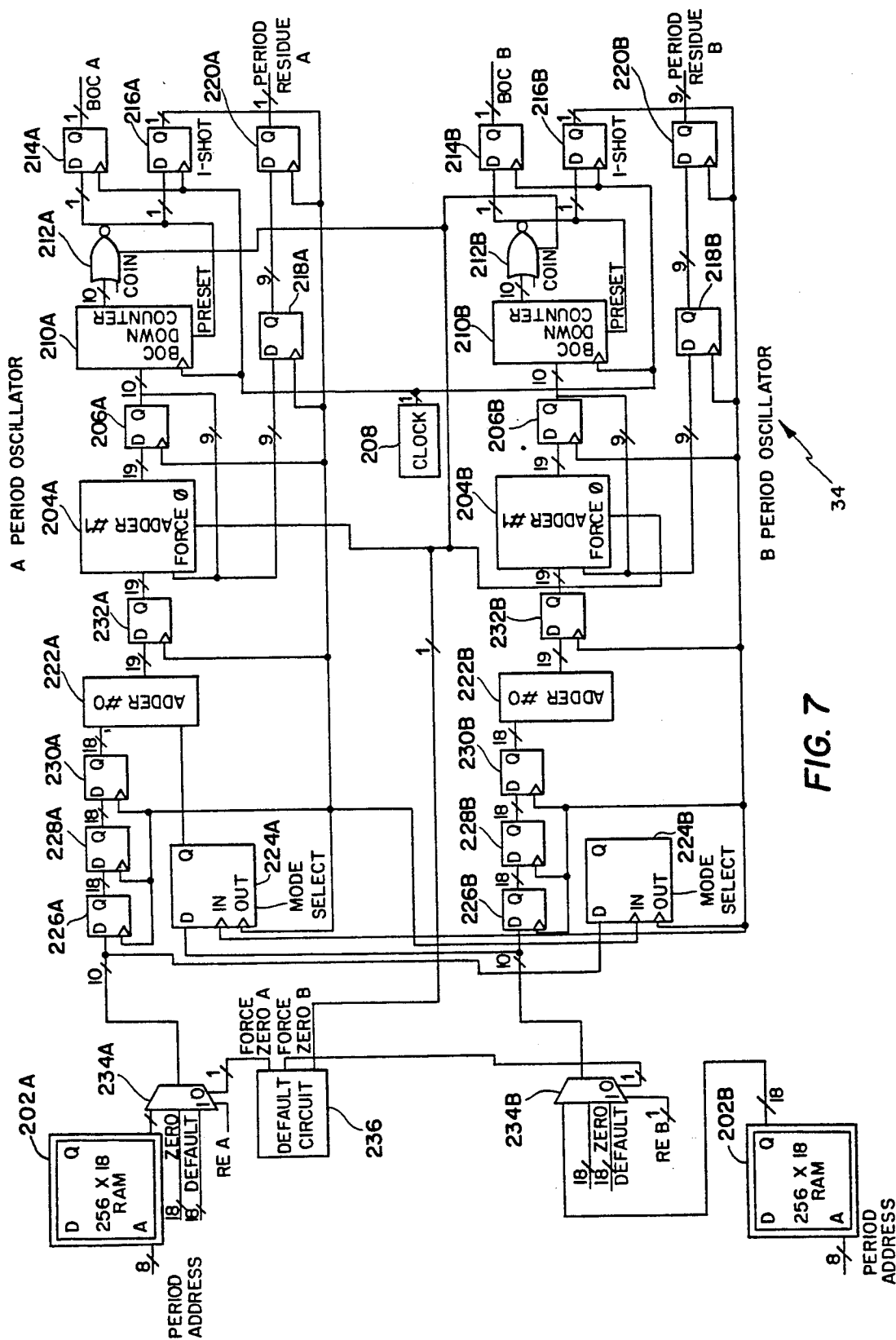
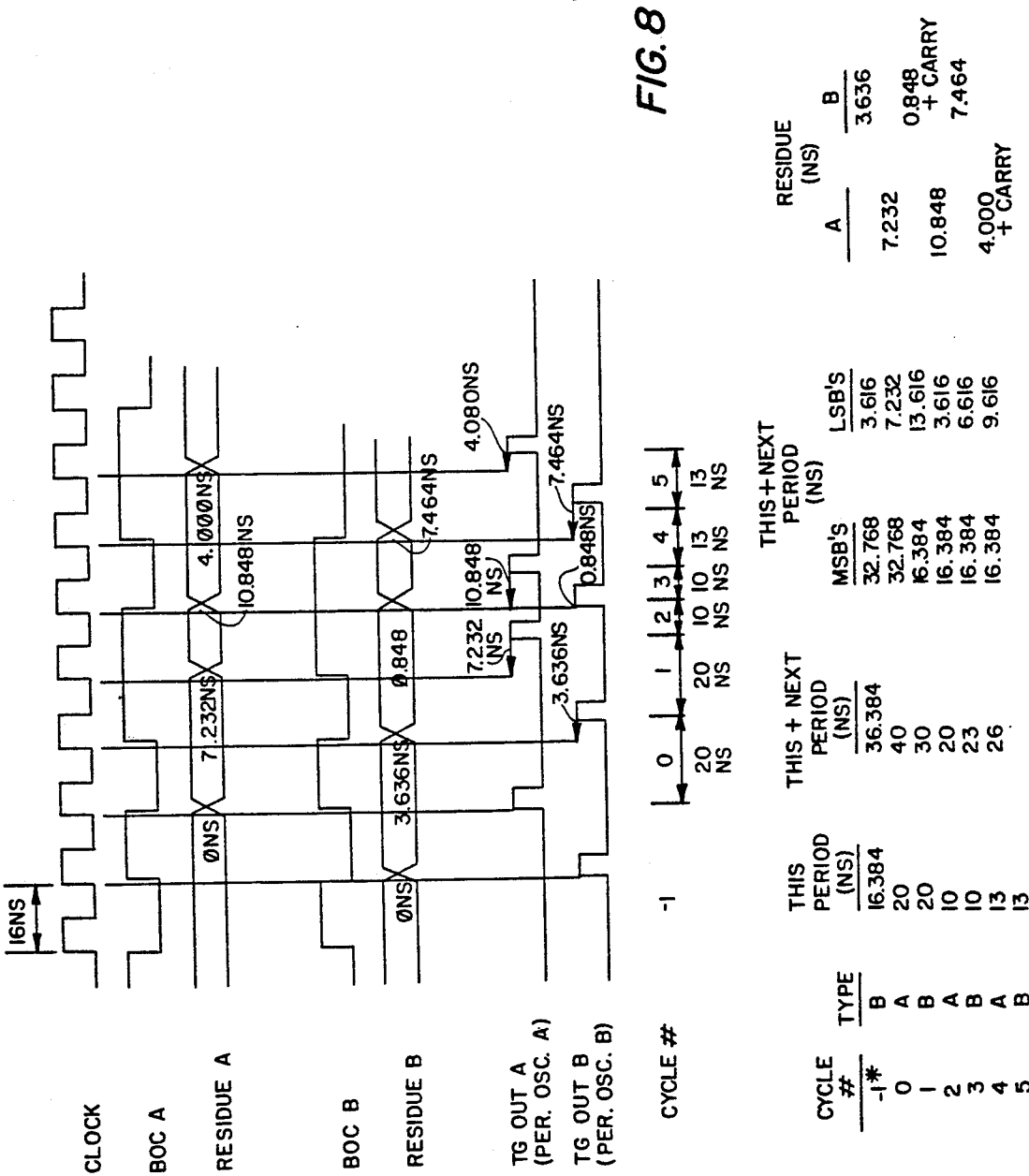


FIG. 7



HIGH SPEED TIMING GENERATOR

This application is a division, of application Ser. No. 605,977, filed Oct. 30, 1990, of Benjamin J. Brown and Peter A. Reichert for HIGH SPEED TIMING GENERATOR, which is a continuation in part of application Ser. No. 419,699, filed Oct. 11, 1989, of Benjamin J. Brown and Peter A. Reichert for HIGH SPEED TIMING GENERATOR, now abandoned.

BACKGROUND OF THE INVENTION

The invention relates to interpolators.

It is known to generate patterns which are used in automatic test equipment by providing a high speed pattern generator which generates address sequences which are sent to a plurality of local generator circuits. Each local generator circuit includes a high speed local memory, a pair of timing generators, a pair of corresponding interpolators, a high speed formatter and a high speed fail processor. The timing generators and interpolators run in an interleaved fashion, with one timing generator/interpolator set receiving and generating all even cycle information and the other set receiving and generating all odd information.

SUMMARY OF THE INVENTION

It has been discovered that providing a register circuit configured to receive and hold input timing data, a pulse swallower circuit configured to delay the timing data by an amount set forth by the timing generator, a ramping circuit configured to receive the pulse swallower output and to provide a ramping output upon receiving the pulse swallower output and a compare circuit configured to receive the input timing data and the ramping output and to provide output data when the ramping output equals the input timing data, provides an interpolator circuit which generates precisely timed output data based upon the input timing data.

In preferred embodiments the input timing data has one kind of logic level and the output data has another kind of logic level and the interpolator circuit includes a calibration circuit which provides an output which can be used in determining whether the interpolator circuit is operating properly.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The attached drawings illustrate the preferred embodiment, the structure and operation of which is then described.

DRAWINGS

FIG. 1 is a schematic block diagram of a high speed timing generator incorporating the invention.

FIG. 2 is a block diagram of a distribution circuit of the FIG. 1 timing generator.

FIG. 3 is a block diagram of timing generator and interpolator circuits of the FIG. 1 timing generator.

FIG. 4 is a schematic diagram of the FIG. 3 interpolator circuit.

FIG. 5 is a block diagram of a known period oscillator circuit.

FIG. 6 is a timing diagram for the FIG. 5 period oscillator circuit.

FIG. 7 is a block diagram of the period oscillator circuit of the FIG. 1 timing generator.

FIG. 8 is a timing diagram for the FIG. 7 period oscillator circuit.

STRUCTURE

Referring to FIG. 1, high speed timing generator system 10 includes pattern generator circuit 12, distribution circuit 14 and a plurality of channel cards 15, each including eight local generator circuits 16(0) to 16(7) (which are generally referred to by reference numeral 16). Each local generator circuit 16 provides a bit at node input 20 to device under test (DUT) 21.

Pattern generator circuit 12 includes conventionally designed high speed pattern generator 30 which provides address patterns at a frequency of 122.0703125 MHz (generally referred to as 120 MHz) and frequency divider circuit 32 which receives the high frequency patterns generated by pattern generator 30 and provides a pair of lower frequency address patterns, at outputs labelled A and B, which are half the frequency (i.e., 61.03515625 MHz, generally referred to as 60 MHz) of the high frequency address patterns generated by pattern generator 30. Pattern generator circuit 12 also includes a central period oscillator 34 which provides a pair of beginning of cycle (BOC) signals and a pair of multi-bit PERIOD RESIDUE signals to local generator circuits 16 via distribution circuit 14.

Frequency divider circuit 32 is controlled by two mode select inputs, MODE SEL 1 and MODE SEL 2. MODE SEL 1 can be set to a first value to cause divider circuit 32 to divide the address patterns into two differing patterns as described above, or to a second value to cause divider circuit 32 simply to produce at both outputs A and B the same frequency patterns generated by pattern generator 30. When MODE SEL 1 is set to the first value, pattern generator circuit 12 can be used in conjunction with channel cards 15 having dual-path local generator circuits 16 as shown in FIG. 1. When MODE SEL 1 is set to the second value, the same pattern generator circuit 12 can be used, as part of a lower-speed system, in conjunction with less costly channel cards that have only single-path local generator circuits connected to the A output of divider circuit 32.

MODE SEL 2 can be set to a first value, to cause divider circuit 32 to receive a single high-speed input from a single pattern generator 30 as shown in FIG. 1, or to a second value, to cause divider circuit 32 to receive two separate lower-speed inputs over two separate paths provided by two lower-speed pattern generators (not shown in FIG. 1 for the sake of simplicity). When MODE SEL 2 is set to this second value, MODE SEL 1 must also be set to its second value, thereby causing divider circuit 32 to produce at outputs A and B, without any division of the address patterns, the two respective signals received from the two pattern generators. When MODE SEL 2 is set to its second value, timing generator system 10 provides, at each node input 20 of device under test 21, a waveform having characteristics determined by either the signals provided over the A path or the signals provided over the B path, as selected by a pattern generator select input (PAT GEN SEL) that is applied to each local generator circuit 16 on a given channel card 15.

Distribution circuit 14 includes a pair of signal distribution paths 40, 42. Each signal distribution path 40, 42 includes a parallel-multibit bus which simultaneously provides the lower frequency addresses, as well as the BOC signals and the PERIOD RESIDUE signals, to the plurality of local generator circuits 16.

Each local signal generator 16 includes a pair of signal generating circuits 50, 52. Signal generating circuit 50 includes local memory 54, which receives information from distribution path 40 through multiplexer 122 and provides information to timing generator 56, and timing generator 56, which receives the information and provides a timing generator output to interpolator circuit 58. Likewise, signal generating circuit 52 includes local memory 60, which receives information from distribution path 42, timing generator 62 which receives information from local memory 60, and interpolator circuit 64, which receives information from timing generator 62. Although, for purposes of simplicity, only one timing generator and one interpolator are shown in each signal generating circuit, there are typically several timing generators and interpolators, and in a preferred embodiment there are six timing generators and interpolators in each signal generating circuit.

Interpolator circuits 58 and 64 provide signals to high speed formatter 66. Formatter 66 is a conventional emitter coupled logic (ECL) high speed formatter which receives timing pulses and data and provides a waveform indicating high or low at a particular time as well as a waveform indicating a drive or tristate condition at a particular time. Driver 68 receives the signal indicating high or low, compensates for any tri-state conditions, and provides an output to node 20, the output having the correct voltage levels for the particular device under test (DUT).

Dual detector 70 is also connected to node 20; dual detector 70 provides an output to high speed formatter 66. Dual detector 70 includes a comparator that compares a signal received from the device under test (DUT) with a high value, and a comparator that compares the signal with a low value. High speed formatter 66 is also connected to a pair of fail processors 72, 74.

Multiplexer 122 receives information from both distribution paths 40 and 42, and outputs information from one path or another based on the state of the PAT GEN SEL input, which is applied to each multiplexer 122 of each of the local generators 16 on a given channel card 15. Differing PAT GEN SEL inputs are applied to differing channel cards. PAT GEN SEL is used in conjunction with the MODE SEL 2 input to divider circuit 32, which causes divider circuit 32 to receive address patterns from two pattern generators, and with MODE SEL 1, which causes divider circuit 32 to output, without any division, address patterns from one pattern generator over distribution path 40 and address patterns from another pattern generator over distribution path 42. MODE SEL 1 prevents timing generator 62 from outputting any timing pulses, and causes formatter 66 to ignore any information received from signal generating circuit 52. Thus, PAT GEN SEL, in conjunction with MODE SEL 1 and MODE SEL 2, selects whether a given channel card 15 will output waveforms having characteristics determined by information provided over distribution path 40, or by information provided over distribution path 42.

Referring to FIG. 2, each distribution path 40, 42 of distribution circuit 14 includes two address/timing fanout circuits 80, 82 which each provide four parallel paths. Each parallel path of path 40 is connected to channel bus fanout circuit 84 via a transmission line assembly cable. Each paralleled path of path 42 is connected to channel bus fanout circuit 86 via a transmission line assembly cable. Accordingly, there are eight channel bus fanout circuits in all. Each pair of channel

bus fanout circuits 84, 86 is connected to 16 channel cards via backplane traces. Each channel card 15 contains eight channels, each channel including a local generator circuit 16. Accordingly, a distribution circuit 14 distributes signals to 512 local generator circuits, thus, system 10 provides 512 connections to a DUT.

Referring to FIG. 3, the interconnection between timing generator 56 and interpolator circuit 58 is shown. Timing generator 56 includes internal control logic 90 which is clocked by a low frequency (60 MHz) CMOS level CLK signal and first in, first out (FIFO) circuit 92, the input of which is clocked by CLK and the output of which is clocked by a low frequency CLKOUT signal. CLKOUT is generated by interpolator circuit 58. FIFO circuit 92 receives DATA, TG RESIDUE and MATCH inputs from control logic 90 and provides DATA, TG RESIDUE and MATCH outputs as the outputs of timing generator 56. Note that TG RESIDUE is a signal that is distinct from the PERIOD RESIDUE signals. Interpolator circuit 58 is clocked by a high frequency (240 MHz) CLKx4 signal; interpolator circuit 58 receives the 1-bit DATA signal, the 10-bit TG RESIDUE signal and the 1-bit MATCH signal from timing generator 56 as well as an analog interpolator calibration input (FS CAL) that is generated externally and an adjust enable input (ADJ EN). Interpolator circuit 58 uses the CMOS level DATA, TG RESIDUE and MATCH signals to provide a precisely delayed ECL pulse out (TG OUT), a bit of digital data (DATA OUT) which is delayed approximately the same amount as the precisely timed pulse out and has ECL levels and an analog test output (DAC OUT).

Referring to FIG. 4, interpolator circuit 58 is fabricated as a bi-polar integrated circuit and includes register circuit 100, enable circuit 102, pulse swallower circuit 104, divider circuit 106, delay circuit 108, calibration circuit 110, synchronizing circuit 112, ramping circuit 114, compare circuit 116 and output circuit 118.

Register circuit 100 includes flip flop FF1, which receives the CMOS level DATA IN signal from timing generator 56 and provides an ECL level DATA QA signal to LATCH 1, flip flop FF2, which receives eight bits of the CMOS level TG RESIDUE signal (Bits 0-7) from timing generator 56 and provides a eight bit ECL level TGR QA signal to LATCH 2, and flip flop FF3, which receives the remaining two bits of the TG RESIDUE signal (bits 8,9) from timing generator 56 and applies a two bit TGR QA signal to pulse swallower 104.

Enable circuit 102 includes flip flops FF4 and FF5. FF4 receives the CMOS level TG MATCH input and provides an ECL level TGMQ signal to FF5 which provides the enable (ENB) signal.

Pulse swallower circuit 104 includes 2:4 decoder (DEC1) which receives the two bit TGR QA signal from FF3 of register circuit 100 and the ENB signal from FF5 of enable circuit 102. DEC1 provides for output signals (PS0, PS1, PS2 and PS3). PS3 is provided to D flip-flop FF8, the output of which, Q3, is provided to OR gate OR1. OR1 also receives the PS2 signal and provides an input, D2, to D flip-flop FF9, the output of which is provided to OR gate OR2. OR2 also receives the PS1 signal and provides an input, D1, to D flip-flop FF10, the output of which is provided to OR gate OR3. OR3 also receives the PS0 signal and provides an input, DO, to D flip-flop FF11. FF11 provides an input to D flip-flop FF12 as well as to the clock input of flip-flop FF6 and flip flop FF7 of synchronizing circuit 112. The

output of FF12 is provided to differential ORNOR gate ORNOR1 as well as to the clock input of flip-flop FF14 of synchronizing circuit 112.

ORNOR1 provides an active high signal and an active low signal to fully differential D flip-flop FF13. FF13 provides differential signals TRIG and TRIG* to ramping circuit 114. The TRIG signal is also provided as the other input of ORNOR1 and, for equal loading, the TRIG* signal is provided as an input to OR4. The output of ramping circuit 114 is connected to the negative input to comparator COMPI of compare circuit 116.

Divider circuit 106 includes flip-flops FF15 and FF16 and exclusive-OR gate XOR1. FF15 and FF16 are configured as D flip-flops and are clocked by CLKX4 which is buffered by buffer BUF2. The Q output of FF15 is provided to XOR1, to which the Q output of FF16 is also provided. The Q' output of FF16 is shifted by level shifter 120 to provide the CLKOUT* signal which is fed back to timing generator 56. The Q output of FF16 is fed through flip-flop FF17 of delay circuit 108 to provide the clock CLKA for flip-flops FF1-4 of register circuit 100.

Calibration circuit 110 includes LATCH 3, which receives the eight bit TG RESIDUE 0-7 input and the adjust enable (ADJ EN) input and provides an eight bit ADJ output signal to 8-bit digital-to-analog converter DAC2, which provides an analog FS CAL output. FS CAL is an output of interpolator circuit 58 and is also provided to the GAINADJ input of DAC1. DAC2 also provides a complement output (IOUT1), which is connected to 2 to 1 analog multiplexer MUX1.

Synchronizing circuit 112 includes D flip-flop FF6, which receives the DATA QB signal from LATCH1, and D flip-flop FF7, which receives the eight bit TGR QB signal from LATCH 2. FF6 provides a DATA QC input to D flip flop FF14 which provides a DATA QD output signal. FF7 provides an eight bit TGR QC output signal to compare circuit 116.

Compare circuit 116 includes 8-bit digital-to-analog converter (DAC1) which receives the eight bit TGR QC output from FF7 of synchronizing circuit 112. DAC1 provides a current output (IOUT) to current-to-voltage converter AR1 and a complement current output (IOUT*) to 2-to-1 analog multiplexer MUX1. IOUT is connected to the positive input of COMP1. COMP1 provides a differential output signal which is provided to one-shot ONESHI of output circuit 118 and to the reset input of FF13.

Output circuit 118 includes MUX1, which provides the analog DAC OUT signal, delay line DELAY1, which provides the ECL DATA OUT signal, and ONESHI which provides the differential, ECL TG OUT and TG OUT* signals.

Before describing the period oscillator circuit shown in the timing generator circuit of FIG. 1, it will be helpful first to describe a known period oscillator circuit designed for use in a timing generator system without multiple, parallel data paths. Referring to FIG. 5, in period oscillator circuit 200, 256-times-18 bit random access memory 202 receives an 8-bit period address and produces an 18-bit period value. Adder 204 receives the 18-bit period value as one input, and receives as another input the nine least significant bits of the output of register 206, which receives the output of adder 204. The nine most significant bits of the output of register 206, which have a resolution of 16.384 nanoseconds (the period of clock 208), represent a digital part of the per-

iod value. The nine least significant bits of the output of register 206, which have a resolution of 32 picoseconds (16,384 picoseconds / 2^9), represent an analog part of the period value.

Beginning-of-cycle down counter 210 receives the nine most significant bits of the output of register 206 and produces a nine-bit output that counts down the number of upward edges of clock 208 specified by the nine input bits. Coincidence detector 212 receives the output of beginning-of-cycle down counter 210 and produces an output that is high only when the output of beginning-of-cycle down counter 210 is one or zero. The output of coincidence detector 212 is received as the preset input to beginning-of-cycle down counter 210. The beginning-of-cycle down counter loads the nine input bits from register 206 whenever the output of clock 208 goes high while the preset input is high, and the output counts down the upward edges of clock 208.

The output of coincidence detector 212 is received by flip-flop 214, which is clocked by upward edges of clock 208 and which produces as an output a beginning-of-cycle (BOC) signal. The output of coincidence detector 212 is received by one-shot 216, which is clocked by the output of clock 208. The output of one-shot 216 goes high whenever the output of clock 208 goes high while the output of coincidence detector 212 is high. The output of one-shot 216 remains high for approximately 8 nanoseconds (half of the period of clock 208). The output of one-shot 216 clocks register 206, register 218, which receives the nine least significant bits of the output of register 206, and register 220, which receives the output of register 218 and which produces as an output a PERIOD RESIDUE signal. The output of one-shot 216 also clocks a pattern generator that produces the 8-bit period addresses received by random access memory 202.

Referring to FIG. 6, BOC indicates which upward edge of the clock is to be used as a reference mark for the beginning of a cycle for the device under test (DUT). The vertical lines through the timing diagram represent the selected clock edges. A cycle begins at each upward edge of the clock that occurs while BOC is high, the cycle being delayed by a residual amount of time represented by the PERIOD RESIDUE signal. A timing generator receives both BOC and PERIOD RESIDUE and an interpolation circuit connected to the timing generator produces as an output the signal TG OUT, which for purposes of simplicity is shown going high at the beginning of each cycle. The point in time at which TG OUT goes high may actually be delayed by an amount of time programmed into the timing generator, the amount of time varying with each cycle. In an alternative embodiment, each of a pair of timing generators may receive both BOC and PERIOD RESIDUE and operate in an interleaved fashion, each of the timing generators being connected to one of a pair of interpolation circuits, with one interpolation circuit generating all even cycle information and another interpolation circuit generating all odd cycle information. The cycle boundaries of the waveform applied to the device under test (DUT) can be programmed to the 32 picoseconds resolution of the PERIOD RESIDUE signal. Note that before each burst begins, the period oscillator executes default periods of 32.768 nanoseconds (two clock periods). These default periods do not affect the device under test (DUT).

Referring to FIG. 7, in which components analogous to those in FIG. 5 are labelled as in FIG. 5 with suffixes

A and B, oscillator 34 according to the invention is designed for use in conjunction with the high-speed timing generator system of FIG. 1, which has multiple, lower-speed parallel data paths. Oscillator 34 does not require the use of expensive, high-speed, custom-manufactured integrated circuits, because the oscillator itself is divided into two lower-speed period oscillators A and B. Period oscillator A produces a BOC A and a PERIOD RESIDUE A signal for cycles 0, 2, 4, 6, etc. of each burst of period data, while period oscillator B produces a BOC B and a PERIOD RESIDUE B signal for cycles 1, 3, 5, 7, etc. of each burst. The BOC and PERIOD RESIDUE signals that define the beginning of cycle 2 are determined by the sum of the period value of cycles 0 and 1; the BOC and PERIOD RESIDUE signals that define the beginning of cycle 3 are determined by the sum of the period values of cycles 1 and 2; etc.

The period oscillators include random access memories 202A and 202B, which contain identical period value data. Random access memory 202A is addressed by period addresses provided by the A output of frequency divider circuit 32 (FIG. 1). Random access memory 202B is addressed by period addresses provided by the B output of frequency divider circuit 32.

An adder 222A or 222B within each oscillator must receive a period value from the oscillator's own random access memory and must receive from the random access memory of the other oscillator the next period value in the series of period values in the burst being executed. Note, however, that period oscillators A and B are clocked by differing clock signals from one-shots 216A and 216B respectively, and that these clock signals may sometimes occur simultaneously. Nevertheless, first-in-first-out pipeline-to-pipeline synchronizer circuits 224A and 224B, in conjunction with registers 226A, 228A, 230A, 226B, 228B, and 230B, ensure that the proper inputs are always present at adders 222A and 222B. Pipeline-to-pipeline synchronizer circuit 224B clocks in period values when the output of one-shot 216A goes high and clocks out period values when the output of one-shot 216B goes high immediately after the next occurrence of one-shot 216A going high. In some instances pipeline-to-pipeline synchronizer 224B may clock out period values when the output of one-shot 216B goes high simultaneously with the next occurrence of one-shot 216A going high, as long as the period value is clocked out three cycles after it is clocked in. In effect, therefore, pipeline-to-pipeline synchronizer 224B delays the period value from period oscillator A by one cycle less than the amount of time by which registers 226B, 228B, and 230B delay the period value from period oscillator B.

Likewise, pipeline-to-pipeline synchronizer circuit 224A clocks in period values when the output of one-shot 216B goes high and clocks out period values when the output of one-shot 216A goes high immediately after the next occurrence of one-shot 216B going high. In some instances pipeline-to-pipeline synchronizer 224A may clock out period values when the output of one-shot 216A goes high simultaneously with the next occurrence of one-shot 216B going high, as long as the period value is clocked out three cycles after it is clocked in. Pipeline-to-pipeline synchronizer circuits 224A and 224B enable oscillators A and B to calculate sums on the fly, without requiring the sums to be pre-stored in random access memories 202A and 202B. Consequently, oscillator 34 can be employed in auto-

matic test systems in which the pattern sequence, and hence the period value sequence, can vary due to the response of the device under test (DUT).

Pipeline-to-pipeline synchronizer circuits 224A and 224B receive a mode selection input that can be used to force the values at the outputs of the pipeline-to-pipeline synchronizers to zero, in order to permit period oscillators A and B to operate as two independent oscillators. Each of period oscillators A and B, when operating as an independent oscillator, operates at a maximum frequency that is half the maximum frequency of operation of the entire oscillator circuit when it operates as a single oscillator. The mode selection input is used in conjunction with the MODE SEL 1 input to divider circuit 32 (FIG. 1) to permit the pattern generator circuit 12 (FIG. 1) to be used in conjunction with channel cards having only single-path local generator circuits connected to the A output of divider circuit 32 and to the BOC A and RESIDUE A outputs of oscillator circuit 34. Alternatively, the mode selection input is used in conjunction with the MODE SEL 2 input to divider circuit 32 to permit the entire high-speed timing generator system to operate with two pattern generators and to provide, at each node input of the device under test, a waveform resulting from either the signals provided over the A path or the signals provided over the B path, as determined by pattern generator select inputs to each local generator.

Register 232A is provided between adders 222A and 204A, and register 232B is provided between adders 222B and 204B. These registers permit the use of adders that operate at half the speed that would be required if the registers were not present.

Multiplexers 234A and 234B receive period values provided by random access memories 202A and 202B, and receive period values of zero and default period values of 6.384 nanoseconds (one clock cycle). Multiplexers 234A and 234B are addressed by rank enable signals RE A and RE B from the pattern generator and by FORCE ZERO A and FORCE ZERO B from default circuit 236. The outputs of multiplexers 234A and 234B are connected to registers 226A and 226B respectively, and to pipeline-to-pipeline synchronizer circuits 224B and 224A respectively. Default circuit 236 also provides an input to adders 204A and 204B that forces the outputs of the adders to zero and an input to coincidence detectors 212A and 212B that forces the outputs of the coincidence detectors high. Before each burst of period values during the operation of the automatic test system, default circuit 236 resets and synchronizes oscillators A and B through multiplexers 234A and 234B in a manner described below.

The remaining components of oscillators A and B are analogous to the components shown in the circuitry of FIG. 5.

Referring to FIG. 8, BOC A and BOC B indicate which upward edges of the clock are to be used to as a reference mark for the beginning of even and odd cycles, respectively, for the device under test (DUT). Note that the clock signal that serves as a reference mark for the beginning of cycle 3 also serves as a reference mark for the beginning of cycle 4. Within a given local generator circuit 16 (FIG. 1), one timing generator receives both BOC A and PERIOD RESIDUE A, and an associated interpolation circuit produces as an output the signal TG OUT A, which is shown for simplicity going high at the beginning of each A cycle. Another timing generator receives both BOC B and PERIOD

RESIDUE B, and an associated interpolation circuit produces as an output the signal TG OUT B. The waveform applied to the device under test (DUT) depends upon the points in time at which either TG OUT A or TG OUT B goes high. Note that before each burst begins, each of period oscillators executes default periods of 32.768 nanoseconds (two clock periods). Consequently, the oscillator circuit as a whole executes default periods of 16.384 nanoseconds. These default periods do not affect the device under test (DUT).

OPERATION

Referring to FIG. 1, pattern generator 30 generates address patterns at a frequency of 120 MHz. This information is provided to frequency divider circuit 32 which receives the 120 MHz address pattern and provides two half speed (i.e., 60 MHz) address patterns to signal distribution paths 40, 42, respectively of distribution circuit 14. The half speed address patterns are cyclically, alternately provided to signal distribution paths 40, 42 by divider circuit 32, thus, divider circuit 32 functions as an alternator. Because the pattern is frequency divided prior to transmission to local generators 16, signal distribution paths 40, 42 need only be appropriate for transmitting signals having a frequency of 60 MHz rather than signals having a frequency of 120 MHz.

High speed timing generator 10 actually provides a 100 MHz signal at node 20; pattern generator 30 provides a 120 MHz signal to compensate for dead time of interpolator circuits 58, 64 (i.e., the amount of time taken by interpolator circuit 58 to provide a new edge) plus rising and falling calibration values. Interpolator circuits 58, 64 can refire every 16.384 ns; accordingly, generator 10 allows for a maximum difference of 3.616 ns between rising and falling calibration values in a 100 MHz generator 10.

At power-up and immediately before the start of each pattern burst, system 10 is resynchronized. More specifically, frequency divider circuit 32 is configured so that at power up, as well as when it is resynchronized, the first signal provided by frequency divider circuit 32 is provided at the output labelled A, and is sent over signal path 40. For a particular DUT, there may be between 10 to 200 pattern bursts for which system 10 is resynchronized. The period oscillator circuit 34 is resynchronized, in a manner described below, at the same time that the rest of the system is resynchronized.

Distribution circuit 14 provides the two half speed address patterns generated by divider circuit 32 to 512 channels. Each channel includes a local generator circuit 16 as shown in FIG. 1.

Referring to FIGS. 1 and 3, local memory 54 receives the half speed address pattern and, using look-up tables within memory 54, sends data to timing generator 56. This data includes a timing value (TIMING), and a data value (DATA). Timing generator 56 also receives one of the two beginning of cycle (BOC) signals and one of the two PERIOD RESIDUE signals from central period oscillator 34. Each timing generator, in internal logic and control 90, using BOC, PERIOD RESIDUE, TIMING, and DATA generates TG RESIDUE and MATCH signals to be sent to interpolator circuit 58. TG RESIDUE and MATCH are analogous to PERIOD RESIDUE and BOC, except that TG RESIDUE and MATCH define points in time that are delayed from the beginnings of cycles by amounts of time represented by the timing value (TIMING), and further de-

layed either by one of two calibration values. Internal logic and control 90 bases the selection of the calibration value on the value of DATA.

For a given timing generator, TG RESIDUE and MATCH represent either 1) the points in time at which formatter 66 is to place transitions in the waveform applied to the device under test (DUT), 2) the points in time at which formatter 66 indicates to driver 68 whether to begin or terminate applying the waveform to the device under test (DUT), 3) the points in time at which the outputs of dual detector 70 are latched, or 4) the points in time at which pin multiplexing is to occur. The value of DATA correspondingly represents either 1) whether a transition in the waveform will result in the waveform being high or the waveform being low, 2) whether formatter 66 is to indicate to driver 68 whether to begin or terminate applying the waveform to the device under test (DUT), or 3) whether a signal from the device under test (DUT) is expected to be high or low. In the fourth case, DATA is not used.

If DATA represents whether a transition in the waveform will result in the waveform being high or being low, then internal logic and control 90 of timing generator 56 must select between a "rising" calibration value corresponding to an amount of time needed to compensate for the skew in the waveform applied to the DUT that is due to a rising transition and a "falling" calibration value corresponding to an amount of time needed to compensate for the skew in the waveform that is due to a falling transition. Internal logic and control 90 selects either the "rising" calibration value or the "falling" calibration value by observing the data value (DATA). If DATA indicates that a transition in the waveform, if it occurs, will result in the waveform being at the high value, then it can be assumed that the transition will cause the skew due to a rising transition. Likewise, if DATA indicates that a transition in the waveform, if it occurs, will result in the waveform being at the low value, then it can be assumed that the transition will cause the skew due to a falling transition. Thus, by looking to the value of DATA, internal logic and control 90 can readily and conveniently determine which calibration value to use. Note that if the waveform is already at the high value (or the low value), and DATA indicates that a "transition" at a certain point in time will cause the waveform to remain at the high value (or the low value), then no transition in fact occurs. The calibration value is added digitally to the timing value and the period residue value by summation circuitry inside internal logic and control circuit 90, as is described in U.S. patent application Ser. No. 07/012,815, entitled "Timing Generator," filed Feb. 9, 1987 by George William Conner, assigned to Teradyne, Inc., now abandoned and incorporated in its entirety herein.

Likewise, if DATA represents whether formatter 66 is to indicate to driver 68 whether to begin or terminate applying the waveform to the device under test (DUT), then internal logic and control 90 of timing generator 56 must select between an "on" calibration value corresponding to an amount of time needed to compensate for the skew in the waveform applied to the DUT that is due to formatter 66 beginning to apply the waveform to driver 68, or by an "off" calibration value corresponding to an amount of time needed to compensate for the skew in the waveform that is due to formatter 66 terminating application of the waveform to driver 68. If DATA represents whether a signal from the device

under test (DUT) is expected to be high or low, then internal logic and control 90 of timing generator 56 must select between a "high" calibration value corresponding to an amount of time needed to compensate for the skew in the waveform that is caused by expecting the signal received from the device under test (DUT) to be high, and a "low" calibration value corresponding to an amount of time needed to compensate for the skew in the waveform that is caused by expecting the signal received from the device under test (DUT) to be low.

Register 92 is used to synchronize DATA, TG RESIDUE and MATCH with interpolator circuit 58 because these signals are stored in register 92 using CLK, which logic 90 also uses, and are provided to interpolator 58 using CLKOUT, which is generated by interpolator 58. Interpolator circuit 58 generates CLKOUT by dividing the 240 MHz CLKX4 signal by four; this divided signal is also used for internally clocking portions of interpolator circuit 58. Referring to FIG. 4, divider circuit 106, in conjunction with delay circuit 108, functions as a free running clock for interpolator circuit 58. Delay circuit 108 provides a clock which is delayed by one period (approximately 4 nsec) to the internal circuitry of interpolator circuit 58.

In operation, as long as TG MATCH is low, interpolator circuit 58 is idle because TG MATCH being low causes ENB of enable circuit 102 to be low. When ENB is low, DEC 1 provides all low outputs and LATCH 1 AND LATCH 2 remain at their previous state.

When TG MATCH goes high, enable circuit 102 functions as a one shot, providing a 4.096 nsec pulse. More specifically, when TG MATCH goes high, TGMQ goes high on the next clock from FF17. With TGMQ high, the next clock from BUF2, which is clocking at four times the frequency of the clock from FF17, causes ENB to go high. When ENB goes high LATCH 1, LATCH2 and DEC1 are enabled and FF4 is reset, causing TMGQ to go low, which causes ENB to go low on the next clock cycle. With LATCH 1, LATCH 2 and DEC1 enabled, data are transferred from FF1, FF2 and FF3 to LATCH1, LATCH 2 and DEC1 respectively. This data remains until TG MATCH goes high again.

When enable ENB goes high, pulse swallower circuit 104 receives the two most significant bits of TG RESIDUE. More specifically, these bits provide the inputs for DEC1. DEC1 provides a high output on one of lines PS0-3 depending on the value of TGR8 QA and TGR9 QA. Pulse swallower circuit 104 provides 0-12.288 nsec of delay, thus allowing ramping circuit 114 to only be required to ramp between 0-4.080 nsec rather than between 0-16.368 nsec. More specifically, if both TGR8 QA and TGR9 QA are low, then PS0 is high and PS1-3 are low. Thus, a high need only be clocked through two flip flops (FF11 and FF12) before reaching ORNOR1. Conversely, if both TGR8 QA and TGR9 QA are high, the PS3 is high and PS0-2 are low. Thus, a high is clocked through five flip-flops (FF's 8-12) before reaching ORNOR1. The additional three flip-flops provide an additional 12 nsec of delay.

When a high is provided as the output of FF11 of pulse swallower circuit 104, flip-flops FF6 and FF7 of synchronizing circuit 112 are clocked; thus, providing the DATA QC output to FF14 and the eight least significant bits of TG RESIDUE to digital-to-analog converter DAC1. DAC1 provides an analog output, which is converted to a voltage and provided to the "+" input

of COMP1. This input remains constant until FF7 is next clocked.

When a high is provided as the output of FF12 of pulse swallower circuit 104, flip-flop FF14 of synchronizing circuit 112 is clocked and fully differential flip-flop FF13 is provided with a high. The output of FF14 is delayed by DELAY 1 to substantially the same as that of TG OUT and TG OUT*. On the next edge from BUF2, FF13 provides an edge which causes ramping circuit INT1 to start ramping. This ramping signal continues until it equals the voltage from current to voltage converter AR1. At this time, a differential edge is provided by COMP1 which causes ONESH1 to provide a precisely timed differential pulse.

In addition to providing TG OUT and DATA OUT, interpolator circuit 58 can be calibrated using an internal calibration circuit 110. More specifically, when the adjust enable input ADJ EN is high, LATCH 3 is enabled and the eight least significant bits of TG RESIDUE are provided to DAC 2. DAC 2 uses this information to adjust the gain of DAC1. The gain of DAC1 can also be adjusted by FS CAL, thus allowing the gain to be externally adjusted. ADJ EN also causes MUX1 to provide the IOUT complement output of DAC1 as the analog DAC OUT output. Accordingly, the output of DAC1 can be measured when a known signal is provided to it.

Referring to FIGS. 7 and 8, in period oscillator 34, before each burst of period information, default circuit 236 resets and synchronizes period oscillators A and B. The default circuit applies period values of zero to both oscillators by addressing multiplexers 234A and 234B with FORCE ZERO A and FORCE ZERO B, which cause the multiplexers to output period values of zero. Because coincidence detectors 212A and 212B are arranged to produce signals that are high only when the output of beginning-of-cycle down counter 210 is one or zero, it can be shown that the BOC A and BOC B signals are stuck high as long as the period value is zero. Consequently, both oscillators A and B are clocked on every clock cycle, once the period value of zero has been clocked through the pipelines. At the same point in time at which default circuit 236 addresses multiplexers 234A and 234B in order to cause period values of zero to be applied to the period oscillators, default circuit 236 also forces the outputs of adders 204A and 204B to zero, thereby clearing the PERIOD RESIDUE feedback loop, and forces coincidence detectors 212A and 212B high, thereby forcing BOC A and BOC B high. The outputs of the adders are kept at zero and the outputs of the coincidence detectors are kept high for an amount of time sufficient to permit the period value of zero to propagate through the pipelines. Once the period value of zero has passed through the pipelines, the adders are no longer forced to zero and the outputs of the coincidence detectors are no longer forced high.

Then default circuit 236 changes the state of FORCE ZERO B, which causes multiplexer 234B to output a default period of one clock cycle. On this clock cycle, multiplexer 234A still outputs a period value of zero. On the next clock cycle default circuit 236 changes the state of FORCE ZERO A. Thus, on this clock cycle and every subsequent clock cycle until the burst begins, default circuit 236 addresses both multiplexers 234A and 234B in a manner such that both multiplexers output the default period.

It can be shown that the first non-zero period value that beginning-of-cycle down counter 210A receives is

the default period value, whereas the first non-zero period value that beginning-of-cycle down counter 210B receives is twice the default period. Beginning-of-cycle down counters 210A and 210B receive these first non-zero period values on the same clock cycle. On all subsequent cycles of period oscillators A and B before the burst begins, each of beginning-of-cycle counters 210A and 210B receives a period value of twice the default period, and period oscillators A and B are clocked on alternating clock cycles. It is necessary to apply the first default period to the B oscillator, rather than apply the first default period to the A oscillator, because if the first default period were applied to the A oscillator, the rest of the high-speed data distribution system, which is designed in a manner such that it interprets the first simultaneous BOC A and BOC B after reset as marking an A cycle and the next B cycle, would interpret the output of the oscillator circuit as including two B cycles in a row.

When a burst begins, a rank enable A (RE A) signal is applied to multiplexer 234A, and simultaneously the first period address is applied to random access memory 202A, when the pattern generator is clocked by the output of one-shot 216A. Then a rank enable B (RE B) signal is applied to multiplexer 234B, and simultaneously the next period address is applied to random access memory 202B, when the pattern generator is clocked by the output of one-shot 216B. The rank enable signals cause the multiplexers to output the period values received from random access memories 202A and 202B.

Referring to FIG. 8, once a burst begins, one interpolation circuit within a given local generator circuit produces as an output the signal TG OUT A, which goes high at the beginning of each even cycle. Another interpolation circuit produces as an output the signal TG OUT B. The waveform applied to the device under test (DUT) depends upon the points in time at which either TG OUT A or TG OUT B goes high.

OTHER EMBODIMENTS

Other embodiments are within the following claims.

E.g., interpolator circuit 58 may be used in other systems in which precisely timed output data is desired. In such a system, interpolator circuit 58 may be reset by providing a high on both the ADJ EN and TG RESIDUE 8 lines. A high on both these lines causes AND gate AND1 to provide a high to the reset inputs of flip-flops FF15, FF16 and FF17, thus, resetting the clock signals which clock the entire circuit.

Also e.g., timing generator 10 may provide a signal which is faster than 100 MHz by reducing the maximum difference between rising and falling calibration values.

Also e.g., system 10 may have any number of signal distribution paths. In such a system, divider circuit 32

divides the high speed pattern into as many lower speed patterns as required. Thus, system 10 may be configured to address individual customers specific needs. E.g., if a customer needs an extremely fast system, then more signal distribution paths are provided, or if a customer needs a lower cost system, then the number of signal distribution paths is reduced.

What is claimed is:

1. An interpolator circuit for generating precisely timed output data based upon input timing data comprising
 - a register circuit configured to receive and hold said input timing data,
 - a pulse swallower circuit configured to delay said timing data by an amount set forth by said timing data,
 - said pulse swallower circuit providing a pulse swallower output after said delay,
 - a ramping circuit configured to receive said pulse swallower output and to provide a ramping output, said ramping output being initiated upon receiving said pulse swallower output, and
 - a compare circuit configured to receive said input timing data and said ramping output and to provide output data when said ramping output equals said input timing data.
2. The interpolator circuit of claim 1 wherein said input timing data includes a multibit word having more significant bits and less significant bits, and said pulse swallower circuit uses said more significant bits to determine said amount of delay.
3. The interpolator circuit of claim 1 wherein said compare circuit includes a digital to analog converter configured to receive said input timing data and to convert said input timing data to analog timing data, said analog timing data being compared to said ramping output.
4. The interpolator circuit of claim 1 wherein said input timing data has one kind of logic level and said output data has another kind of logic level.
5. The interpolator circuit of claim 4 wherein said one kind of logic level is CMOS and said another kind of logic level is ECL.
6. The interpolator circuit of claim 1 further comprising
 - a calibration circuit, said calibration circuit being configured to receive said input timing data and to provide a calibration output,
 - said calibration output being used to calibrate said interpolator circuit.
7. The interpolator circuit of claim 6 wherein said interpolator circuit can also be calibrated from an external calibration signal.

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