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Description

The present invention relates to a method for producing a rear emitter solar cell structure having a heterojunction, wherein

- to form an absorber of the rear emitter solar cell structure, a crystalline semiconductor substrate having a doping of a first conductivity type is provided;
- on a front side of the semiconductor substrate at least one front intrinsic layer is produced from an intrinsic, amorphous semiconductor material;
- on the at least one front intrinsic layer at least one front doping layer is produced from an amorphous semiconductor material having a doping of the first conductivity type, which is higher than the doping of the semiconductor substrate;
- on a rear side of the semiconductor substrate at least one rear intrinsic layer is produced from an intrinsic, amorphous semiconductor material;
- to form an emitter of the rear emitter solar cell structure having a heterojunction, on the at least one rear intrinsic layer, at least one rear doping layer is produced from an amorphous semiconductor material having a doping of a second conductivity type, which is opposite to the first conductivity type;
- at least one electrically conductive, transparent front conduction layer is produced on the at least one front doping layer;
- at least one electrically conductive, transparent rear conduction layer is produced on the at least one rear doping layer;
- a front contact is produced on the at least one electrically conductive, transparent front conduction layer; and
- a rear contact is produced on the at least one electrically conductive, transparent rear conduction layer.

The invention further relates to a rear emitter solar cell structure having a heterojunction, having

- an absorber made of a crystalline semiconductor substrate having a doping of a first conductivity type;
- at least one front intrinsic layer formed on a front side of the absorber and made of an intrinsic, amorphous semiconductor material;
- at least one rear intrinsic layer formed on a rear side of the absorber and made of an intrinsic, amorphous semiconductor material;

- at least one front doping layer formed on the at least one front intrinsic layer and made of an amorphous semiconductor material having a doping of the first conductivity type, which is higher than the doping of the absorber;
- an emitter of at least one rear doping layer formed on the at least one rear intrinsic layer and made of an amorphous semiconductor material having a doping of a second conductivity type, which is opposite to the first conductivity type;
- at least one electrically conductive, transparent front conduction layer formed on the at least one front doping layer;
- at least one electrically conductive, transparent rear conduction layer formed on the at least one rear doping layer;
- a front contact formed on the at least one electrically conductive, transparent front conduction layer, and
- a rear contact formed on the at least one electrically conductive, transparent rear conduction layer.

In addition, the invention relates to a device for producing a rear emitter solar cell structure having a heterojunction, having

- an absorber made of a crystalline semiconductor substrate having a doping of a first conductivity type;
- at least one front intrinsic layer formed on a front side of the absorber and made of an intrinsic, amorphous semiconductor material;
- at least one rear intrinsic layer formed on a rear side of the absorber and made of an intrinsic, amorphous semiconductor material;
- at least one front doping layer formed on the at least one front intrinsic layer and made of an amorphous semiconductor material having a doping of the first conductivity type, which is higher than the doping of the absorber;
- an emitter of at least one rear doping layer formed on the at least one rear intrinsic layer and made of an amorphous semiconductor material having a doping of a second conductivity type, which is opposite to the first conductivity type;
- at least one electrically conductive, transparent front conduction layer formed on the at least one front doping layer;
- at least one electrically conductive, transparent rear conduction layer formed on the at least one rear doping layer;

- a front contact formed on the at least one front conduction layer; and
- a rear contact formed on the at least one rear conduction layer.

A method for producing a solar cell with a heterojunction and a front emitter is known from the publication EP 2 682 990 A1. In the known method, a layer stack consisting of a front side amorphous intrinsic semiconductor layer and a front side amorphous doped semiconductor layer is first deposited on a front side of a semiconductor substrate having a doping of a first conductivity type. The front side amorphous doped semiconductor layer has a doping of a second conductivity type, which is opposite to the first conductivity type. A layer stack consisting of a rear amorphous intrinsic semiconductor layer and a rear-side amorphous doped semiconductor layer is then deposited on the rear side of the semiconductor substrate. The rear amorphous doped semiconductor layer has a doping of the same conductivity type as the semiconductor substrate.

A transparent, electrically conductive layer is then deposited on the front side as an anti-reflective layer without structuring and then an electrically conductive rear coating is applied to the rear side via a mask so that the electrically conductive rear coating is not deposited on the layer stack formed at the substrate edge and thus no electrically conductive layer makes electrical contact at the substrate edge. Finally, front and rear contacts are created.

This layer application sequence results in a layer sequence with alternating doping at the substrate side edge, i.e. an n-p-n^+ or a p-n-p^+ sequence with an anti-reflective layer on top of each. The publication EP 2 682 990 A1 points out that the layer deposition sequence described must be observed in order to achieve advantageous edge insulation in the solar cell to be formed. In particular, the front layer stack consisting of the front amorphous intrinsic semiconductor layer and the front amorphous doped semiconductor layer shall be deposited before the rear layer stack consisting of the rear amorphous intrinsic semiconductor layer and the rear amorphous doped semiconductor layer in order to reduce the risk of shunts occurring at the to avoid solar cell edges.

The document JP 2001044461 A proposes to avoid undesired solar cell edge short circuits on a front emitter solar cell structure having a heterojunction, first of all the layer stack consisting of an amorphous intrinsic semiconductor layer on the rear and an amorphous doped semiconductor layer on the rear only on an area that is smaller than

the semiconductor substrate area, i.e at a distance from the edge of the substrate. Only then should the layer stack consisting of a front side amorphous intrinsic semiconductor layer and a front side amorphous doped semiconductor layer be deposited onto the front side of the substrate.

A similar procedure is also described in publication US 2017/0207351 A1.

In contrast to the prior art cited above, the present invention is based on a heterojunction solar cell structure with a rear emitter. Compared to heterojunction solar cells with a front emitter, such solar cells have the advantage that the optoelectrical properties of the electrically conductive, transparent front conduction layer and the design of the front contacts are less stringent.

In such rear emitter heterojunction solar cells, it is customary in the prior art to first deposit the intrinsic semiconductor layer and the amorphous semiconductor layer doped with the same conductivity type as the semiconductor substrate on the substrate front intended for light incidence, and only then the intrinsic semiconductor layer and the other to form an amorphous semiconductor layer doped as the semiconductor substrate on the substrate rear side.

However, it has been shown that with the known rear emitter heterojunction solar cells, the shunt resistance and reverse current can assume considerable values, as a result of which the solar cell characteristics suffer.

It is therefore the object of the present invention to improve the solar cell electrical properties of rear emitter heterojunction solar cells.

In one aspect, this objective is achieved by a method of fabricating a rear emitter solar cell structure having a heterojunction, in which

- to form an absorber of the rear emitter solar cell structure, a crystalline semiconductor substrate having a doping of a first conductivity type is provided;
- on a front side of the semiconductor substrate at least one front intrinsic layer is produced from an intrinsic, amorphous semiconductor material;
- on the at least one front intrinsic layer at least one front doping layer is produced from an amorphous semiconductor material having a doping of the first conductivity type, which is higher than the doping of the semiconductor substrate;
- on a rear side of the semiconductor substrate at least one rear intrinsic layer is produced from an intrinsic, amorphous semiconductor material;

- to form an emitter of the rear emitter solar cell structure having a heterojunction, on the at least one rear intrinsic layer, at least one rear doping layer is produced from an amorphous semiconductor material having a doping of a second conductivity type, which is opposite to the first conductivity type;
- at least one electrically conductive, transparent front conduction layer is produced on the at least one front doping layer;
- at least one electrically conductive, transparent rear conduction layer is produced on the at least one rear doping layer;
- a front contact is produced on the at least one electrically conductive, transparent front conduction layer; and
- a rear contact is produced on the at least one electrically conductive, transparent rear conduction layer, wherein

the front and rear intrinsic layers and the front and rear dopant layers are generated in the following order:

- producing the at least one rear intrinsic layer on the rear side of the semiconductor substrate;
- then producing the at least one front intrinsic layer on the front side of the semiconductor substrate;
- then producing the at least one front doping layer on the at least one front intrinsic layer; and
- then producing the at least one rear doping layer on the at least one rear intrinsic layer.

Surprisingly, by the fact that in the method according to the invention first the intrinsic amorphous semiconductor layer is produced on the substrate rear side, i.e. the rear intrinsic layer, then the intrinsic amorphous semiconductor layer and the doped amorphous semiconductor layer on the substrate front side, and only then the amorphous semiconductor layer, doped semiconductor layer, i.e. the front doping layer, is formed on the substrate front side, the shunt resistance and the reverse current are significantly improved in all solar cells produced according to the invention. It has also been demonstrated by thermographic measurements that the leakage current over substrate edges is greatly reduced by the process sequence according to the invention. In addition, the quality of passivation of the solar cells produced according to the invention

increases, as evidenced by a higher open-circuit voltage and a better fill factor of the rear emitter heterojunction solar cells. In addition, the solar cell efficiency is increased by the procedure according to the invention.

In a favoured variant of the method according to the invention, an n-doped semiconductor substrate is used as the semiconductor substrate, an amorphous semiconductor material doped with phosphorus is used to generate the front doping layer, and an amorphous semiconductor material doped with boron is used to generate the rear doping layer. Since boron diffuses faster than phosphorus and therefore carries over faster than phosphorus in the equipment used to fabricate the rear emitter heterojunction solar cell structure, the deposition of the boron-doped rear dopant layer as the last layer in the deposition of the amorphous layers has a particularly positive effect on equipment cleanliness.

In a preferred embodiment of the process according to the invention, the formation of the at least one front intrinsic layer on the front side of the semiconductor substrate and the formation of the at least one front doping layer on the at least one front intrinsic layer are performed in processes taking place directly one after the other in one and the same layer deposition reactor. As a result, only a single layer deposition reactor is needed to fabricate the front intrinsic layer and the front dopant layer, which overall simplifies and makes less expensive the device for fabricating the rear emitter heterojunction solar cell structure.

In addition, a particularly good edge isolation of the rear emitter solar cell structure having heterojunction produced according to the invention results if the at least one electrically conductive, transparent rear conduction layer is deposited on the at least one rear doping layer at a distance from the side edge of the semiconductor substrate, so that an edge region on the rear side is not coated with the electrically conductive, transparent rear side conduction layer and there is no electrical contact between the electrically conductive, transparent rear conduction layer and the front conduction layer during all process steps for forming the electrically conductive, transparent rear conduction layer.

The objective is further achieved by a rear emitter solar cell structure having a heterojunction, having

- an absorber made of a crystalline semiconductor substrate having a doping of a first conductivity type;

- at least one front intrinsic layer formed on a front side of the absorber and made of an intrinsic, amorphous semiconductor material;
- at least one rear intrinsic layer formed on a rear side of the absorber and made of an intrinsic, amorphous semiconductor material;
- at least one front doping layer formed on the at least one front intrinsic layer and made of an amorphous semiconductor material having a doping of the first conductivity type, which is higher than the doping of the absorber;
- an emitter of at least one rear doping layer formed on the at least one rear intrinsic layer and made of an amorphous semiconductor material having a doping of a second conductivity type, which is opposite to the first conductivity type;
- at least one electrically conductive, transparent front conduction layer formed on the at least one front doping layer;
- at least one electrically conductive, transparent rear conduction layer formed on the at least one rear doping layer;
- a front contact formed on the at least one electrically conductive, transparent front conduction layer, and
- a rear contact formed on the at least one electrically conductive, transparent rear conduction layer, wherein

on one side edge of the rear emitter solar cell structure having a heterojunction, on an edge region of the semiconductor substrate, there is a layer sequence in the following order from the inside to the outside:

- the at least one rear intrinsic layer,
- thereupon the at least one front intrinsic layer,
- thereupon the at least one front doping layer and
- thereupon the at least one rear doping layer.

Due to the layer structure at the side edge, i.e. the edge region of the rear emitter solar cell structure, there is a significant improvement in the shunt resistance and the reverse current of the solar cells produced according to the invention compared to rear emitter solar cell structures which have a conventional layer structure at their side edge, in which the following layers are present from the inside to the outside in the following sequence or overlap in the following sequence:

- the at least one front intrinsic layer,

- thereupon on the at least one front doping layer,
- then the at least one rear intrinsic layer, and
- thereupon the at least one rear doping layer.

In a preferred embodiment of the rear emitter heterojunction solar cell structure according to the invention, the semiconductor substrate is an n-doped semiconductor substrate, the front doping layer is doped with phosphorus and the rear doping layer is doped with boron.

An advantageous embodiment of the rear emitter solar cell structure having heterojunction according to the invention is constructed in such a way that the at least one electrically conductive, transparent rear conduction layer is deposited on the at least one rear doping layer at a distance from the side edge of the semiconductor substrate, so that an edge area on the rear side is not in contact with the electrically conductive, transparent rear conduction layer and there is no electrical contact between the electrically conductive, transparent rear conduction layer and the front conduction layer.

The object is also provided by a device for producing a rear emitter solar cell structure having a heterojunction, having

- an absorber made of a crystalline semiconductor substrate having a doping of a first conductivity type;
- at least one front intrinsic layer formed on a front side of the absorber and made of an intrinsic, amorphous semiconductor material;
- at least one rear intrinsic layer formed on a rear side of the absorber and made of an intrinsic, amorphous semiconductor material;
- at least one front doping layer formed on the at least one front intrinsic layer and made of an amorphous semiconductor material having a doping of the first conductivity type, which is higher than the doping of the absorber;
- an emitter of at least one rear doping layer formed on the at least one rear intrinsic layer and made of an amorphous semiconductor material having a doping of a second conductivity type, which is opposite to the first conductivity type;
- at least one electrically conductive, transparent front conduction layer formed on the at least one front doping layer;
- at least one electrically conductive, transparent rear conduction layer formed on the at least one rear doping layer;

- a front contact formed on the at least one front conduction layer; and
- of a rear contact formed on the at least one rear conduction layer, wherein

the device for forming the at least one front intrinsic layer on the front side of the semiconductor substrate, the at least one rear intrinsic layer on the rear side of the semiconductor substrate, the at least one front dopant layer on the at least one front intrinsic layer and the at least one rear dopant layer on the at least one rear intrinsic layer comprises only three layer deposition strands, wherein

- a first layer deposition strand comprises at least one layer deposition reactor for generating the at least one rear intrinsic layer on the rear side of the semiconductor substrate;
- a second layer deposition strand comprises at least one layer deposition reactor for forming the at least one front intrinsic layer on the front side of the semiconductor substrate and for forming the at least one front dopant layer on the at least one front intrinsic layer; and
- a third layer deposition strand comprises at least one layer deposition reactor for producing the at least one rear dopant layer on the at least one rear intrinsic layer;

and wherein at least one substrate transport and turning system is provided between the first and second layer deposition strands and between the second and third layer deposition strands.

In contrast to the prior art, in the device according to the invention the semiconductor substrate first passes through the first layer deposition strand with the at least one layer deposition reactor for producing the at least one rear intrinsic layer, is then turned, only thereafter fed to the second layer deposition strand with the at least one layer deposition reactor for producing the at least one front side intrinsic layer on the front side of the semiconductor substrate and for producing the at least one front doping layer on the at least one front intrinsic layer, thereafter turned again and only finally transported into the third layer deposition strand with the at least one layer deposition reactor for producing the at least one rear doping layer on the at least one rear side intrinsic layer.

In a preferred embodiment of the device of the invention, the first layer deposition strand comprises a rear intrinsic layer deposition reactor for producing the at least one

rear intrinsic layer on the rear side of the semiconductor substrate; the second layer deposition strand comprises a single front layer deposition reactor for producing the at least one front intrinsic layer on the front side of the semiconductor substrate and the at least one front doping layer on the at least one front intrinsic layer; and said third layer deposition strand comprises a rear dopant layer deposition reactor for forming said at least one rear dopant layer on said at least one rear intrinsic layer; and said at least one substrate transport and turning system is provided upstream of said front side layer deposition reactor upstream of or in said second layer deposition strand.

Preferred embodiments of the present invention are explained in more detail below with reference to figures, wherein

Figures 1a to 1i: schematically illustrate partial steps of a process sequence of an embodiment of the method according to the invention for producing a rear emitter solar cell structure having a heterojunction on the basis of cross-sectional views of the layer sequence produced in each case;

Figure 2 schematically shows a layer stack formed at a side edge of an intermediate pro duct of a rear emitter solar cell structure having a heterojunction according to the invention after the intrinsic and amorphous semiconductor layers have been formed;

Figure 3 schematically shows a possible basic structure of a subsection of a device according to the invention for producing rear emitter solar cell structures having a heterojunction; and

Figure 4 schematically shows a further possible basic structure of a subsection of the device according to the invention for producing rear emitter solar cell structures having heterojunction.

Figures 1a to 1i schematically show partial steps of a process sequence of an embodiment of the method according to the invention for producing a rear emitter solar cell structure 1 having heterojunction, as shown schematically in cross section in Figure 1i, for example, on the basis of cross-sectional views of the layer sequence produced in each case. The thicknesses of the layers shown in the individual figures are not to scale. Although the ratio of the respective layer thicknesses to each other is also not shown to scale, if one layer is shown thinner than another, this layer is also typically thinner in reality.

In the figures, the side of the respective layered structure shown at the top is the front side and the side shown at the bottom is the rear side of the respective layered structure. The front side is the side into which light incidence is provided in the finished rear emitter solar cell structure 1.

Figure 1a schematically shows a crystalline semiconductor substrate 2 with air oxide layers 21, 22 formed on its front and rear surfaces. The semiconductor substrate 2 has a doping of a first conductivity type. In the embodiment shown, the semiconductor substrate 2 is an n-doped silicon substrate, but in other embodiments of the invention it may be formed of another semiconductor material and/or have p-doping. Preferably, the n-dopant is a phosphorus dopant, but may also be formed with at least one other and/or at least one additional dopant.

In the example shown, the air oxide layers 21, 22 are SiO_2 layers with a thickness between 0.2 and 3.0 nm.

The air oxide layers 21, 22 are automatically formed at the atmosphere on the semiconductor substrate 2, which has been previously cleaned. The semiconductor substrate 2 forms an absorber in the finished rear emitter solar cell structure 1.

Figure 1b shows the semiconductor substrate 2 of Figure 1a after a further process step in which the semiconductor substrate 2 is loaded into a device for the production of rear emitter solar cell structures 1 having heterojunction. Portions of examples of such a device 30, 40 are shown in Figures 3 and 4.

During charging, both sides of the semiconductor substrate 2 are exposed to the atmosphere at temperatures typically below 200 °C, so that air oxide layers 23, 24, i.e. in this case SiO_2layers with a thickness of 0.2 to 3.0 nm, are again formed on the front and rear sides of the semiconductor substrate 2, or the air oxide layers 21, 22 grow by the thickness of the air oxide layers 23, 24.

In a further method step of the method according to the invention, shown schematically in Figure 1c, at least one rear intrinsic layer 3 of at least one intrinsic, amorphous semiconductor material is deposited on the rear side of the semiconductor substrate 2 comprising the air oxide layers 21, 22, 23, 24. The deposition of the at least one rear intrinsic layer 3 is preferably carried out using a PECVD process.

In the step shown in Figure 1d, as the layered structure of Figure 1c is transported to the next layer deposition reactor and inverted, air oxide layers 25, 26 are again formed on the front and rear sides of the layered structure of Figure 1c. In the example shown,

the air oxide layers 25, 26 are SiO_2 layers with a thickness of 0.2 to 3.0 nm. The air oxide layer 25 grows directly on the air oxide layers 21, 23 already existing on the front side. The air oxide layer 26 grows on the deposited rear intrinsic layer 3.

After deposition of the rear intrinsic layer 3, at least one front intrinsic layer 4 of at least one amorphous intrinsic semiconductor material and at least one front doping layer 5 of at least one amorphous semiconductor material having a doping of the first conductivity type higher than the doping of the semiconductor substrate 2 are deposited on the front side of the semiconductor substrate 2 with the layers 21, 23, 25 thereon. This can be seen in figure 1e. Since the semiconductor substrate 2 is n-doped in the embodiment shown, the front doping layer 5 is also n-doped here, preferably doped with phosphorus.

The front intrinsic layer 4 can be deposited separately from the front dopant layer 5, in different layer deposition reactors. However, it is particularly advantageous if, as is done in the embodiment shown, the front dopant layer 5 is deposited directly after the front intrinsic layer 4 in one and the same layer deposition reactor without intermediate substrate handling. In this case, air oxide formation between the front intrinsic layer 4 and the front dopant layer 5 is avoided.

During the substrate handling required after this layer deposition or these layer depositions, during which substrate transport to the next layer deposition reactor and again turning of the substrate takes place, the generated layer structure shown schematically in Figure 1e again reaches atmosphere, whereby again air oxide layers 27, 28 grow on both sides of the layer structure, which is shown in Figure 1f. In the embodiment example, the air oxide layers 27, 28 are SiO_2layers with a layer thickness between 0.2 and 3.0 nm.

After further substrate handling, a rear doping layer 6 of an amorphous semiconductor material with a doping of a second conductivity type opposite to the first conductivity type is formed on the rear side of the layer array shown in Figure 1f. This is shown in Figure 1g. In the embodiment shown, the rear doping layer 6 is a p-doped amorphous silicon layer. Specifically, the p-dopant used in the example is a boron dopant, but may be a different dopant in other embodiments of the invention. The rear doping layer 6 forms the emitter of the rear emitter solar cell structure 1 having heterojunction to be formed, which is provided on it and described in the following.

The layered structure of Figure 1g is subsequently transported to at least one further layer deposition reactor, whereby the layered structure is again exposed to atmospheric conditions during transport. In turn, approximately 0.2 to 3.0 nm thin air oxide layers 29, 30 form on the front and rear sides of the layered structure, which can be seen in Figure 1h.

Then, as shown schematically in Figure 1i, electrically conducting transparent front and rear conduction layers 7, 8 are formed on the front and rear sides of the layered structure of Figure 1h. The electrically conductive transparent front and rear conduction layers 7, 8 are preferably made of electrically conductive transparent oxide (TCO). In the embodiment shown, the electrically conductive transparent front and rear conduction layers 7, 8 are indium-tin-oxide (ITO) layers.

The electrically conductive transparent rear conduction layer 8 is deposited on the at least one rear dopant layer 6 at a distance from the side edge 50 of the semiconductor substrate 2 in the shown embodiment. The deposition of the rear dopant layer 6 can, for example, be carried out via a mask. As a result, an edge region 51 on the rear side of the rear emitter solar cell structure 1 having heterojunction remains uncoated by the electrically conductive transparent rear conduction layer 8. Due to the structured deposition, there is no electrical contact between the electrically conductive, transparent rear conduction layer 8 and the front conduction layer 7, not even during the deposition of the electrically conductive, transparent rear conduction layer 8.

Finally, front and back contacts 9, 10 are produced on the electrically conductive, transparent front and back conduction layers 7, 8, respectively. In the exemplary embodiment shown, the front and rear contacts 9, 10 are made of silver and are provided in the form of fingers on the front and rear of the solar cell. However, they can also be formed from a different, electrically conductive material and/or applied in a different form.

As can be seen from the above, air oxide layers 21, 22, 23, 24, 25, 26, 27, 28, 29, 30 are formed during each substrate transport, which form barriers between the semiconductor substrate 2 and the intrinsic layers 3, 4 deposited thereon, between the rear intrinsic layer 4 and the rear doping layer 6, and between the front and rear doping layers 5, 6 and the front and rear conduction layers 7, 8, respectively, deposited thereon. These barriers impede the conduction carrier transport and thus degrade the solar cell properties of the rear emitter solar cell structure 1 having heterojunction to be formed.

By depositing the front doping layer 5 directly after the front intrinsic layer 4 in the same layer deposition reactor, as described above, such a barrier formation between the front intrinsic layer 4 and the front doping layer 5 could be avoided.

Furthermore, the process step sequence according to the invention, in which the boron-doped rear doping layer 6 is deposited as the last of the amorphous semiconductor layers, minimizes the diffusion out of boron, which has a higher diffusion coefficient than the phosphorus contained in the front doping layer 5, from the rear doping layer 6. This also has an advantageous influence on the solar cell properties of the rear emitter solar cell structure 1 having heterojunction to be formed.

As can be seen schematically in Figure 2, the procedure according to the invention also has other advantageous effects. Figure 2 shows schematically an intermediate product of the rear emitter solar cell structure 1 having heterojunction according to the invention from Figure 1i. While in Figures 1a to 1i the layer sequences forming at the solar cell edge have been omitted for the sake of clarity, in Figure 2 this layer sequence is shown particularly large after deposition of the amorphous semiconductor layers 3, 4, 5 and 6 and before formation of the further layers 7, 8, 9, 10.

Starting from the n-doped semiconductor substrate 2 in the exemplary embodiment shown, an n-i-i-n^+-p layer sequence results at the edge of the solar cell. In contrast, in the prior art, an n-i-n^+-i-p layer sequence results from the conventional process sequence. The double intrinsic layer 3, 4 on the edge or on the side edge of the semiconductor substrate 2 appears to protect the structure formed in particular against the formation of shunt resistances and leakage currents at the edge of the solar cell.

In the Figures 3 and 4 partial areas of possible plant concepts or devices 30, 40 for the production of rear emitter solar cell structures 1 having heterojunction, as they are described above, are shown schematically. The device 30, which is shown diagrammatically in some areas in Figure 3, and the device 40, which is shown in some areas in Figure 4, each have three layer deposition strands 31, 32 and 42 for the formation of the amorphous semiconductor layers 3, 4, 5, 6, 33.

At least one layer deposition reactor 36 for producing the at least one rear intrinsic layer 3 on the rear side of the semiconductor substrate 2 is provided in a first layer deposition strand 31.

In a second layer deposition strand 32 or 42, at least one layer deposition reactor 39, 41; 44 is provided for forming the at least one front intrinsic layer 4 on the front side

of the semiconductor substrate 2 and for forming the at least one front doping layer 5 on the at least one front intrinsic layer 4. In the device 40, the second layer deposition strand 42 has only a single front layer deposition reactor 44 for producing the at least one front intrinsic layer 4 on the front side of the semiconductor substrate 2 and the at least one front doping layer 5 on the at least one front intrinsic layer 4.

At least one layer deposition reactor 43 for producing the at least one rear doping layer 6 on the at least one rear intrinsic layer 3 is provided in a third layer deposition strand 33.

A substrate transport and turning system 37 is provided between the first layer deposition strand 31 and the second layer deposition strand 32 or 42 and between the second layer deposition strand 32 or 42 and the third layer deposition strand 33. In the devices 30, 40 only a single substrate transport and turning system 37 is provided, which is located in front of the front layer deposition reactor(s) 39, 41 or 44.

A lock mechanism 45 is provided between and before each of the individual stratified deposition reactors.

A loading and unloading device 35 is provided at the start of each layer deposition strand 31, 32 or 42, 33.

Patentkrav

1. Fremgangsmåde til fremstilling af en bagsideemitter-solcellestruktur (1) med en heteroovergang, ved hvilken der

- til dannelse af en absorber til bagsideemitter-solcellestrukturen (1) tilvejebringes et krystallinsk halvledersubstrat (2) med en dotering af en første ledningsevnetype;
- på en forside af halvledersubstratet (2) frembringes mindst et forsideintrinsiclag (4) af et intrinsict, amorft halvledermateriale;
- på det mindst ene forsideintrinsiclag (4) frembringes mindst et forsidedoteringslag (5) af et amorft halvledermateriale med en dotering af den første ledningsevnetype, der er højere end doteringen af halvledersubstratet (2);
- på en bagside af halvledersubstratet (2) frembringes mindst et bagsideintrinsiclag (3) af et intrinsict, amorft halvledermateriale;
- til dannelse af en emitter i bagsideemitter-solcellestrukturen (1) med heteroovergang på det mindst ene bagsideintrinsiclag (3) frembringes mindst et bagsidedoteringslag (6) af et amorft halvledermateriale med en dotering af en anden ledningsevnetype, der er modsat den første ledningsevnetype;
- på det mindst ene forsidedoteringslag (5) frembringes mindst et elektrisk ledende, transparent forsideledningslag (7);
- på det mindst ene bagsidedoteringslag (6) frembringes mindst et elektrisk ledende, transparent bagsideledningslag (8);
- på det mindst ene elektrisk ledende, transparente forsideledningslag (7) frembringes en forsidekontaktering (9); og
- på det mindst ene elektrisk ledende, transparente bagsideledningslag (8) frembringes en bagsidekontaktering (10),

kendetegnet ved,

at for- og bagsideintrinsiclagene (3, 4) og for- og bagsidedoteringslagene (5, 6) frembringes i følgende rækkefølge:

- frembringelse af det mindst ene bagsideintrinsiclag (3) på bagsiden af halvledersubstratet (2);
- derpå frembringelse af det mindst ene forsideintrinsiclag (4) på forsiden af halvledersubstratet (2);

- derpå frembringelse af det mindst ene forsidedoteringslag (5) på det mindst ene forsideintrinsiclag (4); og
- derpå frembringelse af det mindst ene bagsidedoteringslag (6) på det mindst ene bagsideintrinsiclag (3).

2. Fremgangsmåde ifølge krav 1, **kendetegnet ved, at** der som halvledersubstrat (2) anvendes et n-doteret halvledersubstrat, til frembringelse af forsidedoteringslaget (5) anvendes et med phosphor doteret amorft halvledermateriale, og til frembringelse af bagsidedoteringslaget (6) anvendes et med bor doteret amorft halvledermateriale.

3. Fremgangsmåde ifølge krav 1 eller 2, **kendetegnet ved, at** frembringelsen af det mindst ene forsideintrinsiclag (4) på forsiden af halvledersubstratet (2) og frembringelsen af det mindst ene forsidedoteringslag (5) på det mindst ene forsideintrinsiclag (4) foretages i processer, der foregår direkte efter hinanden i en og samme lagafsætningsreaktor (44).

4. Fremgangsmåde ifølge et af de foregående krav, **kendetegnet ved, at** det mindst ene elektrisk ledende, transparente bagsideledningslag (8) afsættes på det mindst ene bagsidedoteringslag (6) med en afstand til halvledersubstratets (2) sidekant (50), således at et randområde (51) på bagsiden af bagsideemitter-solcellestrukturen (1) med heteroovergang ikke er belagt med det elektrisk ledende, transparente bagsideledningslag (8), og der ved alle fremgangsmådetrin til dannelse af det elektrisk ledende, transparente bagsideledningslag (8) ikke består nogen elektrisk kontakt mellem det elektrisk ledende, transparente bagsideledningslag (8) og forsideledningslaget (7).

5. Bagsideemitter-solcellestruktur (1) med en heteroovergang med
- en absorber af et krystallinsk halvledersubstrat (2) med en dotering af en første ledningsevnetype;
- mindst et på en forside af absorberen dannet forsideintrinsiclag (4) af et intrinsict, amorft halvledermateriale;
- mindst et på en bagside af absorberen dannet bagsideintrinsiclag (3) af et intrinsict, amorft halvledermateriale;

- mindst et på det mindst ene forsideintrinsiclag (4) dannet forsidedoteringslag (5) af et amorft halvledermateriale med en dotering af den første ledningsevnetype, der er højere end absorberens dotering;
- en emitter af mindst et på det mindst ene bagsideintrinsiclag (3) dannet bagsidedoteringslag (6) af et amorft halvledermateriale med en dotering af en anden ledningsevnetype, der er modsat den første ledningsevnetype;
- mindst et på det mindst ene forsidedoteringslag (5) dannet elektrisk ledende, transparent forsideledningslag (7);
- mindst et på det mindst ene bagsidedoteringslag (6) dannet elektrisk ledende, transparent bagsideledningslag (8);
- en på det mindst ene elektrisk ledende, transparente forsideledningslag (7) dannet forsidekontaktering (9) og
- en på det mindst ene elektrisk ledende, transparente bagsideledningslag (8) dannet bagsidekontaktering (10);

kendetegnet ved,

at der på en siderand (50) af bagsideemitter-solcellestrukturen (1) med heteroovergang på et randområde af halvledersubstratet (2) foreligger en lagfølge i følgende rækkefølge indefra og udad:

- det mindst ene bagsideintrinsiclag (3),
- derpå det mindst ene forsideintrinsiclag (4),
- derpå det mindst ene forsidedoteringslag (5) og
- derpå det mindst ene bagsidedoteringslag (6).

6. Bagsideemitter-solcellestruktur med heteroovergang ifølge krav 5, **kendetegnet ved, at** halvledersubstratet (2) er et n-doteret halvledersubstrat, forsidedoteringslaget (5) er doteret med phosphor, og bagsidedoteringslaget (6) er doteret med bor.

7. Bagsideemitter-solcellestruktur (1) med heteroovergang ifølge krav 5 eller 6, **kendetegnet ved, at** det mindst ene elektrisk ledende, transparente bagsideledningslag (8) er afsat på det mindst ene bagsidedoteringslag (6) med en afstand til halvledersubstratets (2) sidekant (50), således at et randområde (51) på bagsiden af bagsideemitter-solcellestrukturen (1) med heteroovergang ikke er belagt med det elektrisk ledende, transparente bagsideledningslag (8), og der ikke består nogen elektrisk kontakt mellem det elektrisk ledende, transparente

bagsideledningslag (8) og forsideledningslaget (7).

8. Apparat (30, 40) til fremstilling af en bagsideemitter-solcellestruktur (1) med en heteroovergang med

- en absorber af et krystallinsk halvledersubstrat (2) med en dotering af en første ledningsevnetype;
- mindst et på en forside af absorberen dannet forsideintrinsiclag (4) af et intrinsict, amorft halvledermateriale;
- mindst et på en bagside af absorberen dannet bagsideintrinsiclag (3) af et intrinsict, amorft halvledermateriale;
- mindst et på det mindst ene forsideintrinsiclag (4) dannet forsidedoteringslag (5) af et amorft halvledermateriale med en dotering af den første ledningsevnetype, der er højere end absorberens dotering;
- en emitter af mindst et på det mindst ene bagsideintrinsiclag (3) dannet bagsidedoteringslag (6) af et amorft halvledermateriale med en dotering af en anden ledningsevnetype, der er modsat den første ledningsevnetype;
- mindst et på det mindst ene forsidedoteringslag (5) dannet elektrisk ledende, transparent forsideledningslag (7);
- mindst et på det mindst ene bagsidedoteringslag (6) dannet elektrisk ledende, transparent bagsideledningslag (8);
- en på det mindst ene forsideledningslag (7) dannet forsidekontaktering (9); og
- en på det mindst ene bagsideledningslag (8) dannet bagsidekontaktering (10);

kendetegnet ved,

at apparatet (30, 40) til frembringelse af det mindst ene forsideintrinsiclag (4) på forsiden af halvledersubstratet (2), det mindst ene bagsideintrinsiclag (3) på bagsiden af halvledersubstratet (2), det mindst ene forsidedoteringslag (5) på det mindst ene forsideintrinsiclag (4) og det mindst ene bagsidedoteringslag (6) på det mindst ene bagsideintrinsiclag (3) kun har tre lagafsætningsstrenge (31; 32 eller 42; 33), hvor

- en første lagafsætningsstreng (31) har mindst en lagafsætningsreaktor (36) til frembringelse af det mindst ene bagsideintrinsiclag (3) på bagsiden af halvledersubstratet (2);

- en anden lagafsætningsstreng (32 eller 42) har mindst en lagafsætningsreaktor (39, 41 eller 44) til frembringelse af det mindst ene forsideintrinsiclag (4) på forsiden af halvledersubstratet (2) og til frembringelse af det mindst ene forsidedoteringslag (5) på det mindst ene forsideintrinsiclag (4); og
- en tredje lagafsætningsstreng (33) har mindst en lagafsætningsreaktor (43) til frembringelse af det mindst ene bagsidedoteringslag (6) på det mindst ene bagsideintrinsiclag (3);

og hvor mindst et substrattransport- og -vendesystem (37) er tilvejebragt mellem den første og den anden lagafsætningsstreng (31, 32 eller 42) og mellem den anden og den tredje lagafsætningsstreng (32 eller 42, 33).

9. Apparat ifølge krav 8, **kendetegnet ved, at** den første lagafsætningsstreng (31) har en bagsideintrinsiclagafsætningsreaktor (36) til frembringelse af det mindst ene bagsideintrinsiclag (3) på bagsiden af halvledersubstratet (2); den anden lagafsætningsstreng (42) har en enkelt forsidelagafsætningsreaktor (44) til frembringelse af det mindst ene forsideintrinsiclag (4) på forsiden af halvledersubstratet (2) og det mindst ene forsidedoteringslag (5) på det mindst ene forsideintrinsiclag (4); og den tredje lagafsætningsstreng (33) har en bagsidedoteringslagafsætningsreaktor (43) til frembringelse af det mindst ene bagsidedoteringslag (6) på det mindst ene bagsideintrinsiclag (3); og det mindst ene substrattransport- og -vendesystem (37) er tilvejebragt før forsidelagafsætningsreaktoren (44) før eller i den anden lagafsætningsstreng (42).

Fig. 1a

Fig. 1b

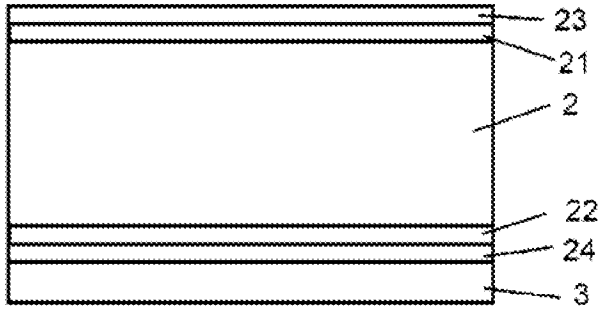

Fig. 1c

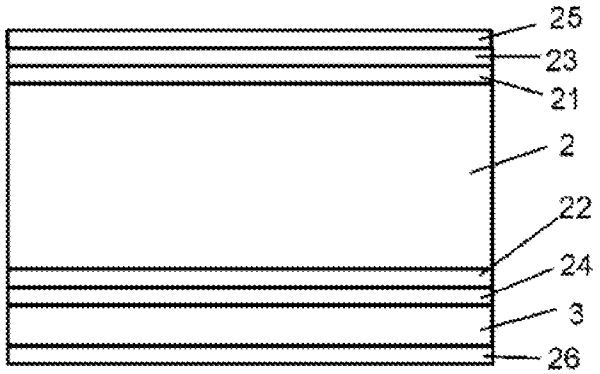

Fig. 1d

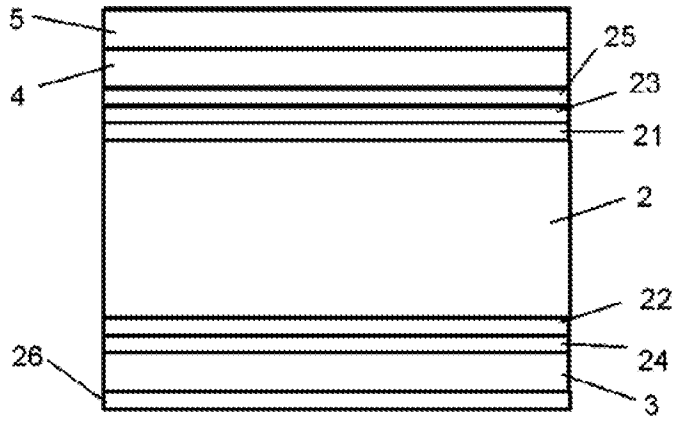

Fig. 1e

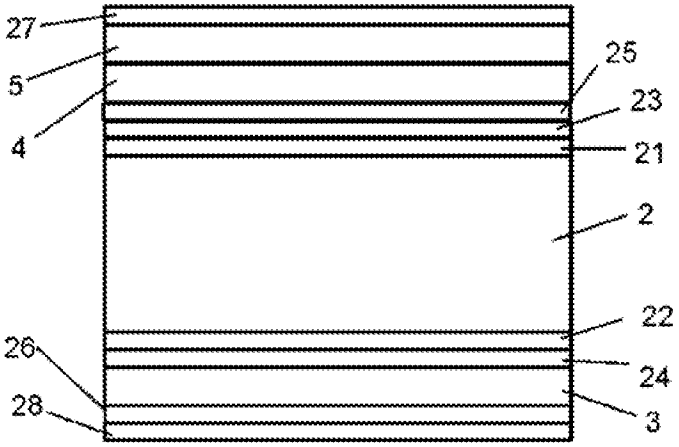

Fig. 1f

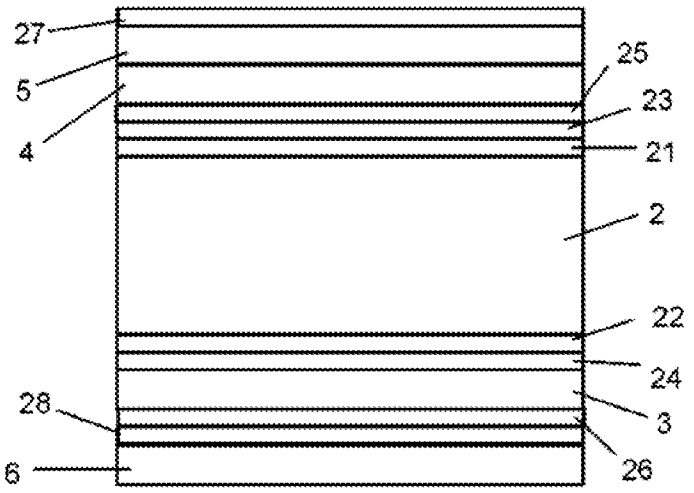

Fig. 1g

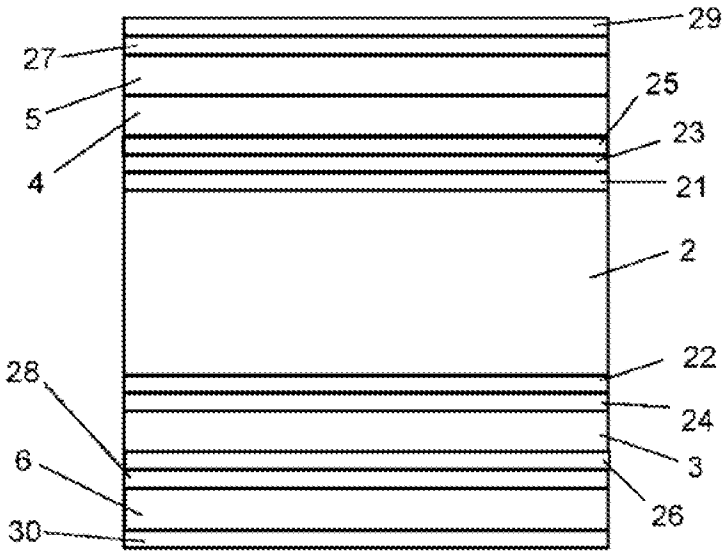
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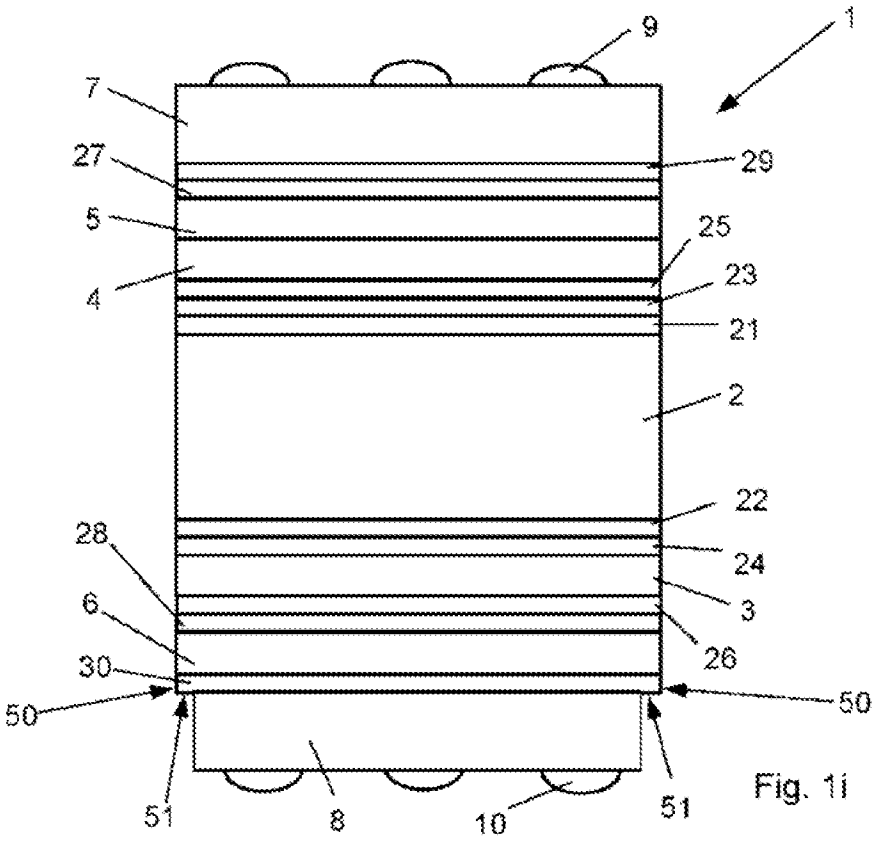
Fig. 1h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8
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51

Fig. 1i

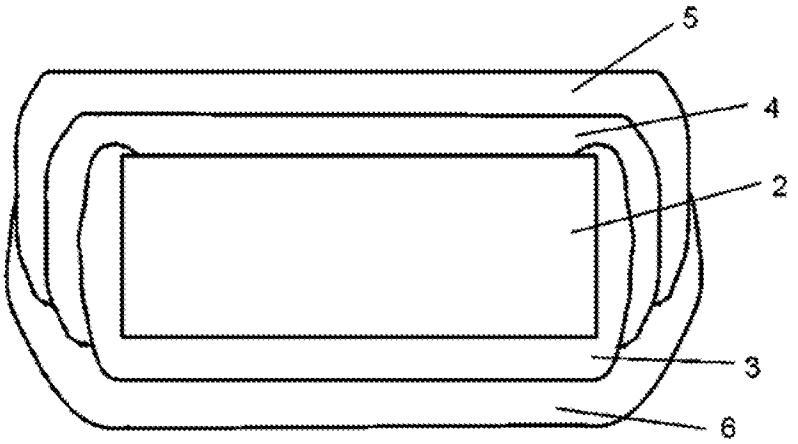
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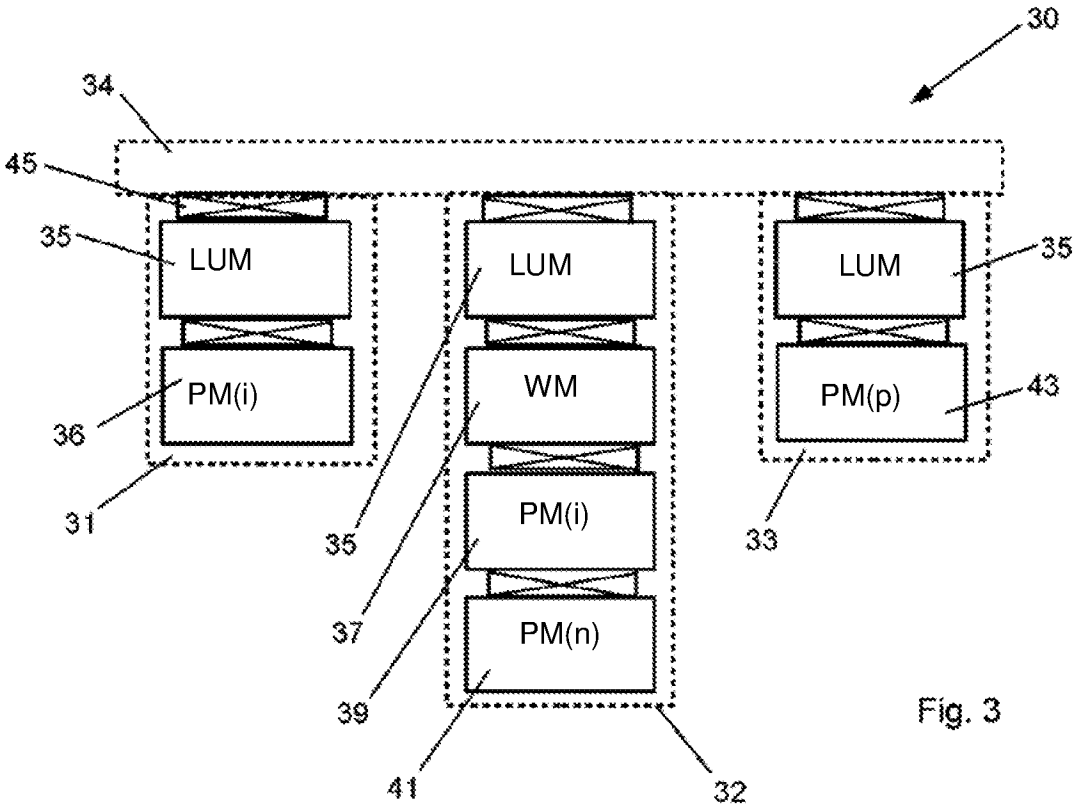
Fig. 2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45
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LUM
LUM
LUM
35
PM(i)
WM
PM(p)
43
36
31
35
PM(i)
33
37
PM(n)
39
41
32

Fig. 3

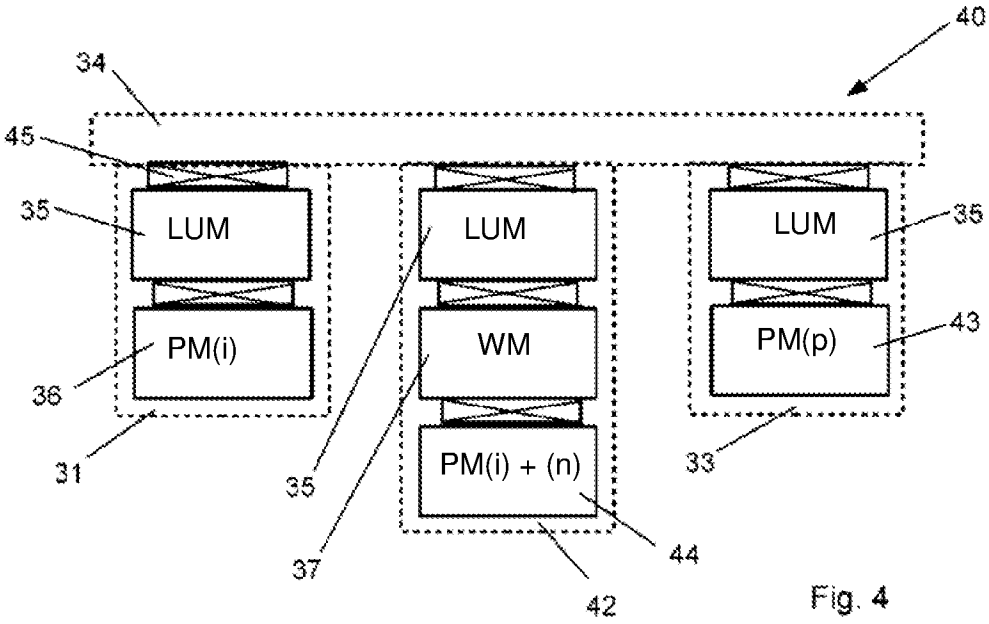

Fig. 4