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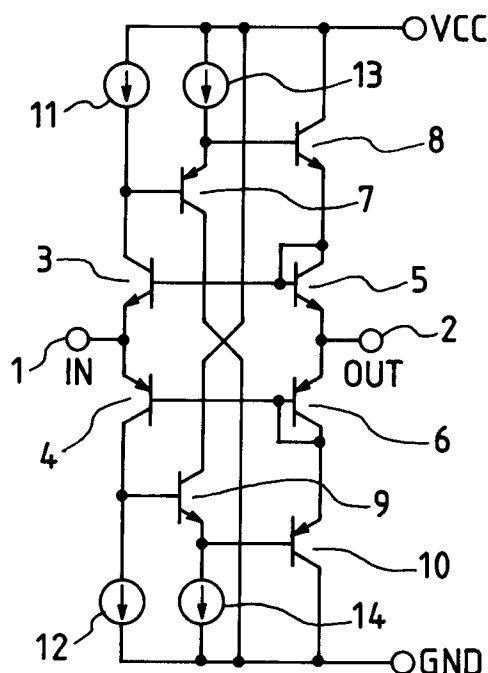
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Patentanwaltsbüro Tiedtke-Bühling-Kinne &
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W-8000 München 2(DE)(54) **Buffer circuit.**

(57) A buffer circuit provided with a transistor each on the input (1) and output (2) terminal sides, in which the transistor has been provided in order to keep constant a difference between a collector-emitter voltage of the input terminal side transistor (3,4) and that of the output terminal side transistor (5,6).

FIG. 2**EP 0 486 986 A1**

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a buffer circuit for use in, for example, impedance conversion, an input unit for current feedback type operational amplifiers and the like.

Related Background Art

Heretofore, the buffer circuit is composed of diode-connected transistors 15 and 16 which are opposite to each other in polarity, transistors 17 and 18 matching those transistors 15 and 16 respectively, and constant-current sources 19 and 20 for feeding constant current to the transistors 15 and 16 as shown in Fig. 1.

In the above conventional example, however, the transistors 15 and 17, and the transistors 16 and 18, for which matching is required respectively, are operated by a different C-E (Collector-Emitter) voltage. Therefore, an offset appears between input (IN) and output (OUT) due to the Early's effect of transistors, possibly causing a malfunction.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a buffer circuit obtained by solving the above problem of occurrence of such an offset.

It is a further object of the present invention to provide a buffer circuit provided with a transistor each on the input and output terminal sides, characterized in that the transistor has been provided in order to keep constant a difference between a collector-emitter (C-E) voltage of the input terminal side transistor and that of the output terminal side transistor, and to provide an operational amplifier having such a buffer circuit.

According to the present invention, the offset between the input and output terminals can be reduced for correct operations by the provision of a transistor which keeps constant the difference in the collector-emitter (C-E) voltage between transistors for which matching is required.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of a buffer circuit according to a conventional example;

Fig. 2 is a circuit diagram of a buffer circuit embodying the concept of the present invention; and

Fig. 3 is a circuit diagram of an input buffer for current feedback type operational amplifiers embodying the concept of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will hereinafter be described in detail with respect to embodiments thereof shown in the drawings.

(First Embodiment)

A preferred embodiment of the present invention is best shown in Fig. 2. In Fig. 2, numeral 1 is an input terminal, and numeral 2 is an output terminal. Transistors 3 and 4, which are opposite to each other in polarity, are connected with the input terminal 1, and are biased by constant-current sources 11 and 12 respectively. Transistors 5 and 6 are connected with the output terminal 2, and are diode-connected with a short between the base and the collector, requiring matching with those transistors 3 and 4 respectively. Transistors 7 and 8, and transistors 9 and 10 are used to keep constant the C-E voltage of the transistors 3 and 4, and the transistors 7 and 8 are biased by constant-current sources 13 and 14 respectively.

When an input voltage is applied to the input terminal 1, a voltage of the same value is output at the output terminal 2. At this time, the C-B (collector-base) voltage of the transistor 3 is kept down at 0 (V) by means of V_{be} of the transistors 7 and 8, and the C-E voltage of the transistor 3 is kept down at $1 \times V_{be}$ (V).

Similarly, the C-B voltage of the transistor 4 is kept down at 0 (V) by means of V_{be} of the transistors 9 and 10, and the C-E voltage of the transistor 4 at $1 \times V_{be}$ (V). Since the transistors 3 and 5, and the transistors 4 and 6 are operating at the same C-E voltage $1 \times V_{be}$ (V), there is no difference in operating current between the two due to the Early's effect, but an offset between the input and output terminals is very small. The circuit described above is integrated on a semiconductor substrate for formation.

(Second Embodiment)

Fig. 3 shows an example in which the above embodiment has been used as an input buffer for a current feedback type operational amplifier. In Fig. 3, numeral 21 is a forward input terminal, numeral 22 is a reverse input terminal, numerals 23 and 24 are current mirror circuits, numeral 25 is an output buffer, and numeral 26 is an output terminal.

An input current I_N flows through the reverse input terminal 22 by an input voltage applied to between the forward and reverse input terminals, and becomes a differential current between a current I_1 above and a current I_2 below the reverse input terminal 22. This differential current flows to

the output stage through current mirror circuits 23 and 24, is converted into a voltage at a point P, and is output at the output terminal 26 through an output buffer 25.

An offset between forward 21 and reverse 22 input terminals at this time is increased by the gain times and becomes an offset at the output terminal 26. When a buffer circuit according to the present invention is used as an input buffer, the offset between the forward 21 and reverse 22 input terminals becomes very small, and as a result, the offset at the output terminal 26 is also reduced. This operational amplifier consists of a semiconductor integrated circuit.

According to the present invention as described above, an offset between an input and output can be reduced by keeping down at a very small value a C-E voltage difference between transistors for which matching is required to each other for operation.

A buffer circuit provided with a transistor each on the input and output terminal sides, in which the transistor has been provided in order to keep constant a difference between a collector-emitter voltage of the input terminal side transistor and that of the output terminal side transistor.

Claims

1. A buffer circuit provided with a transistor each on the input and output terminal sides, wherein the transistor has been provided in order to keep constant a difference between a collector-emitter voltage of said input terminal side transistor and that of said output terminal side transistor.
2. A current feedback type operational amplifier wherein the input unit is provided with a buffer circuit according to Claim 1.
3. The buffer circuit according to Claim 1, wherein said buffer circuit constitutes a semiconductor integrated circuit.

FIG. 1
PRIOR ART

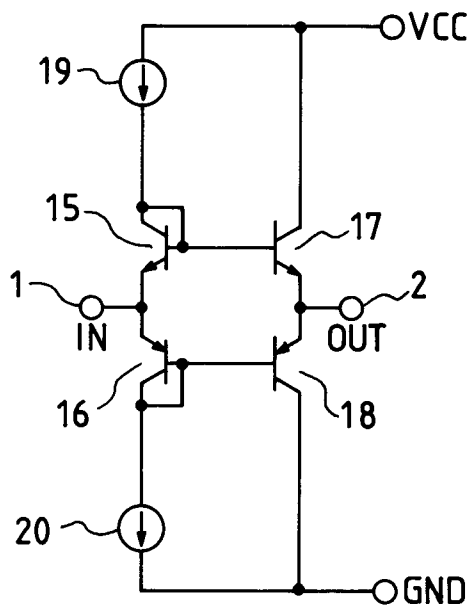


FIG. 2

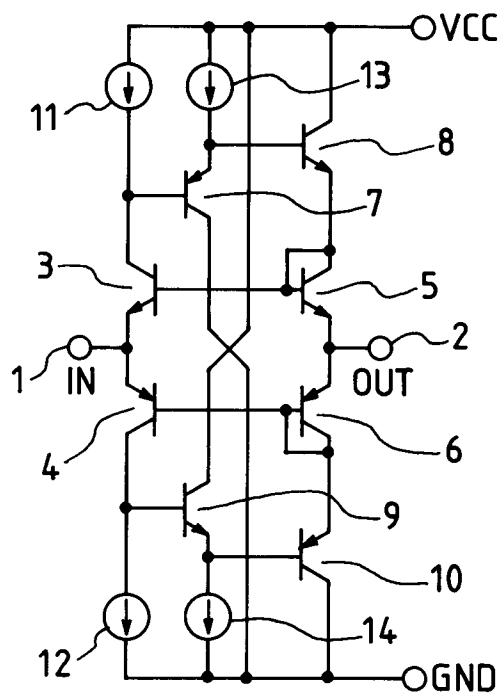
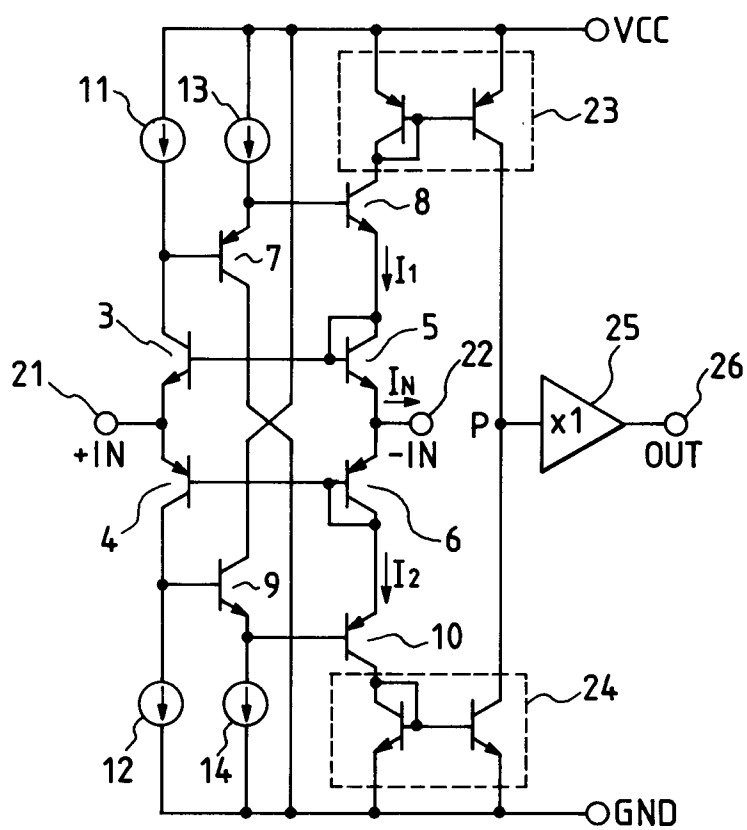


FIG. 3





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EUROPEAN SEARCH REPORT

Application Number

EP 91 11 9631

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	INTERNATIONAL JOURNAL OF ELECTRONICS, vol. 59, no. 6, December 1985, LONDON GB pages 771 - 777; G. NORMAND: 'Translinear current conveyors' * page 771, line 1 - page 774, line 9; figures 1-6 *	1-3	H03F3/343 H03F3/30 H03F1/30
X	INTERNATIONAL JOURNAL OF ELECTRONICS, vol. 57, no. 5, November 1984, LONDON GB pages 713 - 717; A. FABRE: 'An integrable multiple output translinear current convertor' * the whole document *	1-3	
A	ELECTRONIC DESIGN, vol. 35, no. 5, 5 March 1987, HASBROUCK HEIGHTS, NEW JERSEY pages 71 - 74; F. GOODENOUGH: 'Electronic Design Report ISSCC: ANALOG' * page 72, right column; figure 2 *	1-3	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H03F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 24 FEBRUARY 1992	Examiner TYBERGHIEN G.M.
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	