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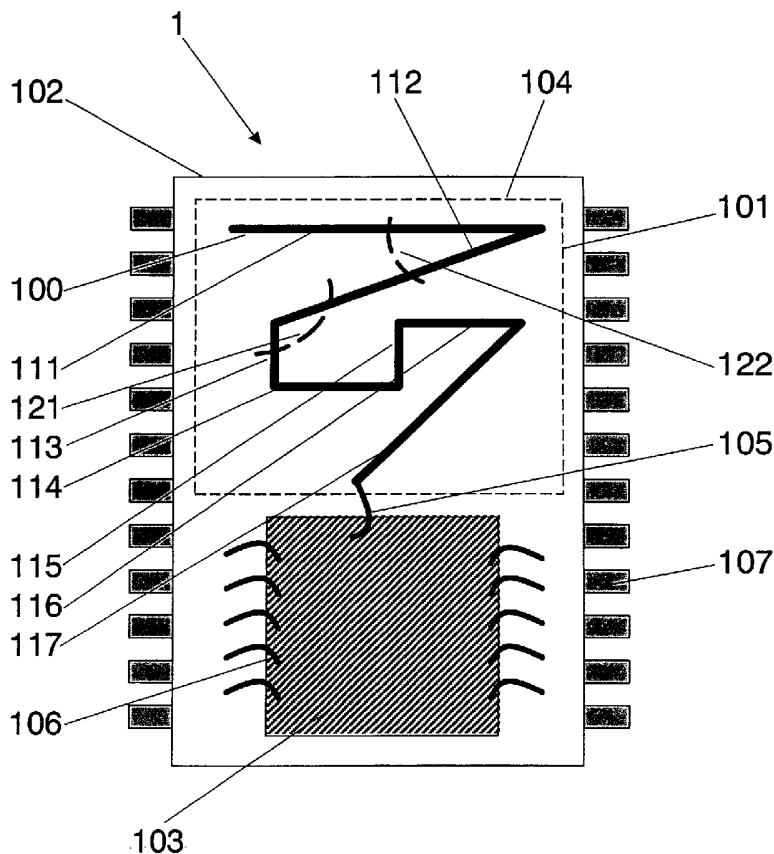
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(54) Title: INTEGRATED CIRCUIT PACKAGE INCLUDING MINIATURE ANTENNA



(57) Abstract: The present invention relates to an integrated circuit package comprising at least one substrate, each substrate including at least one layer, at least one semiconductor die, at least one terminal, and an antenna located in the integrated circuit package, but not on said at least one semiconductor die. The conducting pattern comprises a curve having at least five sections or segments, at least three of the sections or segments being shorter than one-tenth of the longest free-space operating wavelength of the antenna, each of the five sections or segments forming a pair of angles with each adjacent segment or section, wherein the smaller angle of each of the four pairs of angles between sections or segments is less than 180° (i.e., no pair of sections or segments define a longer straight segment), wherein at least two of the angles are less than 115°, wherein at least two of the angles are not equal, and wherein the curve fits inside a rectangular area the longest edge of which is shorter than one-fifth of the longest free-space operating wavelength of the antenna.

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INTEGRATED CIRCUIT PACKAGE INCLUDING MINIATURE ANTENNA

BACKGROUND OF THE INVENTION

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The present invention relates generally to novel integrated circuit packages that include a new family of miniature antennas in the package. The present invention allows the integration of a full wireless system into a single component.

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There is a trend in the semiconductor industry towards the so-called System on Chip (SoC) and System on Package (SoP) concepts. This means integrating as many components of an electronic system as possible (processors, memories, logic gates, biasing circuitry, etc.) into a single semiconductor chip (or "die") (SoC) or at least into a single integrated circuit package (SoP). The full integration of systems or subsystems into a single chip or package provides many advantages in terms of cost, size, weight, consumption, performance and product design complexity. Several electronics components for consumer applications, such as handsets, wireless devices, personal digital assistants (PDA) or personal computers are becoming more and more integrated into SoP/SoC products.

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The concept of integrating a full wireless system into a SoC/SoP device (FWSoc and FWSop) is especially attractive owing to the tremendous growth and success of cellular and wireless systems. In particular, there is a new generation of short/medium range wireless applications such as Bluetooth™, Hyperlan, IEEE802.11 and ultra wide band (UWB) systems where the progressive system integration into a single, compact product is becoming a key success factor (see for instance S.Harris and H.Johnston, "Handset industry debate Bluetooth chip options", WirelessEurope, May 2002). Recently, several vendors (for example www.infineon.com, www.st.com, www.epson.com www.csr.com) are offering SoC or SoP products for applications that integrate everything into the chip or package, except for the antenna. The reason the antenna is excluded is that its integration into the SoC or SoP is a major engineering challenge in the product development, mainly due to the reduced size of the commercial SoP and SoC packages and the well-known constraints on the performance of miniature antennas.

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There have been reported several attempts to integrate an antenna inside a semiconductor die or chip, which die or chip also includes an electronic system or

radio frequency (RF) front-end (see for example D. Singh, C. Kalliakis, P. Gardner, P.S. Hall, *Small H-Shaped Antennas for MMIC Applications*, IEEE Trans. on Antennas and Propagation, vol. 48, no. 7, July 2000; D.W. Griffin, A.J. Partfitt, *Electromagnetic Design Aspects of Packages for Monolithic Microwave Integrated Circuit-Based Arrays with Integrated Antenna Elements*, IEEE Trans. on Antennas and Propagation, vol. 43, no. 9 Sept. 1995; P.S. Hall, *System Applications: The Challenge for Active Integrated Antennas*, APS2000 Millenium Conference, April 2002; I. Papapolymerou, R.F. Drayton, L.P.B. Katehi, *Micromachined Patch Antennas*, IEEE Trans. on Antennas and Propagation, vol. 46, no. 2 Feb.. 1998; J. Zhao, S. Raman, *Design of Chip-Scale" Patch Antennas for 5-6GHz Wireless Microsystem*, Antennas and Propagation Society, 2001 IEEE International Sym , Volume: 2 , 2001 ; and U.S. Patent No. 6,373,447). These designs feature two important limitations: first the operating frequency must be large enough to allow a conventional antenna to fit inside the chip; second the antenna performance is poor in terms of gain, mainly due to the losses in the semiconductor material. According to D. Singh, et al., the smallest frequency in which an antenna has been integrated together with an electronic system inside the same was 5.98 GHz. Typical gains that have been achieved with such designs are around -10 dBi.

In general, there is a trade-off between antenna performance and miniaturization. The fundamental limits on small antennas were theoretically established by H. Wheeler and L.J. Chu in the middle 1940's. They stated that a small antenna has a high quality factor (Q) because of the large reactive energy stored in the antenna vicinity compared to the radiated power. Such a high quality factor yields a narrow bandwidth; in fact, the fundamental derived in such theory imposes a maximum bandwidth given a specific size of an small antenna. Related to this phenomenon, it is also known that a small antenna features a large input reactance (either capacitive or inductive) that usually has to be compensated with an external matching/loading circuit or structure. It also means that it is difficult to pack a resonant antenna into a space which is small in terms of the wavelength at resonance. Other characteristics of a small antenna are its small radiating resistance and its low efficiency (see R.C. Hansen, *Fundamental Limitations on Antennas*, Proc. IEEE, vol. 69, no. 2, February 1981).

Some antenna miniaturization techniques rely basically on the antenna geometry to achieve a substantial resonant frequency reduction while keeping

efficient radiation. For instance patent WO/0154225 discloses a set of space-filling antenna geometries (SFC) that are suitable for this purpose. Another advantage of such SFC geometries is that in some cases they feature a multiband response.

5 The dimension (D) is a commonly used parameter to mathematically describe the complexity of some convoluted curves. There exist many different mathematical definitions of dimension but in the present document the box-counting dimension (which is well-known to those skilled in advanced mathematics theory) is used to characterize some embodiments (see discussion on the mathematical concept of dimension in for instance W.E. Caswell and J.A. Yorke, *Invisible errors in dimension calculations: geometric and systematic effects*, Dimensions and Entropies in Chaotic Systems, G.Mayer-Kress edit., Springer-Verlag, Berlin 1989, second edition pp. 123-136, and K. Judd, A.I. Mees, *Estimating dimensions with confidence*, International Journal of Bifurcation and Chaos 1,2 (1991) 467-470).

15 It should be apparent that the present invention is substantially different from some prior-art designs called chip-antennas (see for instance H. Tanidokoro, N. Konishi, E. Hirose, Y. Shinohara, H. Arai, N. Goto, *1-Wavelength Loop Type Dielectric Chip Antennas*, Antennas and Propagation Society International Symposium, 1998, IEEE, vol. 4, 1998; *Electromagnetically coupled dielectric chip antenna*, Matsushima, H.; Hirose, E.; Shinohara, Y.; Arai, H.; Goto, N. Antennas and Propagation Society International Symposium, IEEE, Vol. 4, 1998). Those are typically single component antenna products that integrate only the antenna inside a surface-mount device. To achieve the necessary wavelength compression, those antennas are mainly constructed using high permittivity materials such as ceramics. The drawbacks of using such high permittivity materials are that the antenna has a very narrow bandwidth, the material introduces significant losses, and the manufacturing procedure and materials are not compatible with most current chip or package manufacturing techniques; therefore they do not currently include other components or electronics besides the antenna, and they are not suitable for a FWSoc or FWSop. On the contrary, the present invention relies on the specific novel design of the antenna geometry and its ability to use the materials that are currently being used for integrated circuit package construction, so that the cost is minimized while allowing a smooth integration with the rest of the system.

30 There have been recently disclosed some RF SoP configurations that also include also antennas on the package. Again, most of these designs rely on a

conventional microstrip, shorted patch or PIFA antenna that is suitable for large frequencies (and therefore small wavelengths) and feature a reduced gain. In the paper K. Lim, S. Pinel, M. Davis, A. Sutono, C. Lee, D. Heo, A. Obatoynbo, J. Laskar, E. Tantzaris. R. Tummala, *RF-System-On-Package (SOP) for Wireless Communications*, IEEE Microwave Magazine, vol. 3, no. 1, March 2002, a SoP including an RF front-end with an integrated antenna is described. The antenna comprises a microstrip patch backed by a cavity which is made with shorting pins and operates at 5.8 GHz. As mentioned in the paper, it is difficult to extend those designs in the 1-6 GHz frequency range where most current wireless and cellular services are located, mainly due to the size of conventional antennas at such large wavelengths. Another design for an antenna on a package is disclosed in Y.P. Zhang, W.B. Li, *Integration of a Planar Inverted F Antenna on a Cavity-Down Ceramic Ball Grid Array Package*, IEEE Symp. on Antennas and Propagation, June 2002. Although the antenna operates at the Bluetooth™ band (2.4GHz), the IC package is substantially large (15x15 mm) and the antenna performance is poor (gain is below -9dBi).

Patent application EP1126522 describes a particular double S-shaped antenna design that is mounted on a BGA package. Although no precise data is given on the package size in the application, typically, S-shaped slot antennas resonate at a wavelength on the order of twice the unfolded length of the S-shaped pattern. Again, this makes the whole package too large for typical wireless applications where the wavelength is above 120 mm. Also, this design requires a combination with high permittivity materials that, in turn, reduce the antenna bandwidth, increase its cost and decreases the overall antenna efficiency.

Regarding the package construction and architecture, there are several standard configurations depending mainly on the application. Some basic architectures are: single-in-line (SIL), dual-in-line (DIL), dual-in-line with surface mount technology DIL-SMT, quad-flat-package (QFP), pin grid array (PGA) and ball grid array (BGA) and small outline packages. Other derivatives are for instance: plastic ball grid array (PBGA), ceramic ball grid array (CBGA), tape ball grid array (TBGA), super ball grid array (SBGA), micro ball grid array BGA®. Some of these configurations are present in their CSP (Chip Scale Package) versions, wherein the semiconductor chip or die typically fills up to an 85% of the package area. The interconnection of those packages with the semiconductor chip or die can be done

with several standard processes and technologies as well, mainly wire-bonding, tape automated bonding and flip-chip. A description of several standard packaging architectures can be found in the websites of several package manufacturers, such as for instance www.amkor.com (see also L. Halbo, P. Ohlckers, *Electronic Components, Packaging and Production*, ISBN:82-992193-2-9).

In the last few years, several improvements in packaging technology have appeared mainly due to the development of Multichip Module (MCM) applications (see for instance N. Sherwani, Q. Yu, S. Badida, *Introduction to Multi Chip Modules*, John Wiley & Sons, 1995). Those consist of an integrated circuit package that typically contains several chips (*i.e.*, several semiconductor dies) and discrete miniature components (biasing capacitors, resistors, inductors). Depending on the materials and manufacturing technologies, MCM packages are classified in three main categories: laminated (MCM-L), ceramic (MCM-C) and deposited (MCM-D). Some combinations of them are also possible, such as MCM-L/D and other derivations such as Matsushita ALIVH. These MCM packaging techniques cover a wide range of materials for the substrate (for instance E-glass/epoxy, E-glass/polyimide, woven Kevlar/epoxy, s-glass/cyanate ester, quartz/polyimide, thermount/HiT^a epoxy, thermount/polyimide, thermount/cyanate ester, PTFE, RT-Duroid 5880, Rogers RO3000[®] and RO4000[®], polyolefin, alumina, sapphire, quartz glass, Corning glass, beryllium oxide and even intrinsic GaAs and silicon) and manufacturing processes (thick film, thin film, silicon thin film, polymer thin film, LTCC, HTCC).

SUMMARY OF THE INVENTION

The present invention relates generally to novel integrated circuit packages that include a new family of miniature antennas in the package. Also, the invention relates to several novel ways of arranging the materials and components of the package to include the antenna. The characteristic aspects of the invention are:

- the small size of the antenna, which allows the use of very small packages (such as for instance CSP packages) at typical wireless wavelengths;
- the antenna geometry that enables such a miniaturization;
- the arrangement of the antenna in the package, and

- the compatibility of the antenna design with virtually any state of the art packaging architecture.

The integrated circuit package of the present invention generally comprises an antenna in the form of a conducting pattern integrated in the package. One of the characteristic aspects of the invention is the geometry of the conducting pattern. The conducting pattern comprises a curve having at least five sections or segments, at least three of the sections or segments being shorter than one-tenth of the longest free-space operating wavelength of the antenna, each of the five sections or segments forming a pair of angles with each adjacent segment or section, wherein the smaller angle of each of the four pairs of angles between sections or segments is less than 180° (*i.e.*, no pair of sections or segments define a longer straight segment), wherein at least two of the angles are less than 115° , wherein at least two of the angles are not equal, and wherein the curve fits inside a rectangular area the longest edge of which is shorter than one-fifth of the longest free-space operating wavelength of the antenna. In some embodiments, the curve is arranged such that two of the angles are defined respectively in the clockwise and counter-clockwise directions at opposite sides of the curve to minimize the inductive coiling effect.

In some embodiments, SFC geometries can be used to shape a portion of the antenna included in the package, as long as the antenna geometry is arranged within the package according to the present invention. Although SFC geometries as described in WO/0154225 provide significant miniaturization capabilities, they have some drawbacks in terms of efficiency and input impedance that need to be corrected by using the special package and antenna geometry arrangements as disclosed in the present invention. In many cases, SFC antenna geometries described in WO/0154225 by themselves do not meet the optimum trade-off between antenna miniaturization and performance because of an excess of a number of segments, because there is a too tight requirement on the size of the segments (some times breaking the antenna geometry in 10 segments reduces the antenna efficiency), and because the angles between segments need to be arranged according to the present invention (at least two angles less than 115° , but it is not always necessary for all of them to be less than 115°) to fit and operate inside the package.

For those packages where the size is critical and the required degree of miniaturization is very high, the characteristic curve of the antenna will feature a

box-counting dimension larger than 1.17. For a further degree of miniaturization, the curve will be arranged such that its box-counting dimension ranges from 1.5 up to 3. For some embodiments, a curve having a box-counting dimension of about 2 is preferred.

5 The present invention applies to several antenna topologies, both balanced and unbalanced. In particular, monopoles, dipoles, loops, folded and loaded monopoles and dipoles and their slot or aperture equivalents (slot monopoles, slot dipoles, slot loops, folded and loaded slot monopoles and dipoles) are some of the structures that can be arranged according to the present invention. Other structures
10 include shorted and bent monopoles (L monopoles, IFA), multibranch structures, coupled monopoles and dipole antennas and again their aperture equivalents. All of them would include the characteristic pattern built on a component of the integrated circuit package according to the present invention.

 Another possible antenna configuration is a microstrip or patch antenna,
15 including their shorted versions (shorted patches and planar inverted F or PIFA structures); nevertheless for the planar cases a particular selection of the disclosed geometries should be considered to achieve the required degree of miniaturization. In particular, the characteristic pattern of the invention should include at least a curve with fifteen segments, with at least seven of the segments being shorter than
20 one-twentieth of the longest free-space operating wavelength of the antenna. The rest of the general conditions that conform the essential geometric aspects of the invention, as described above, apply to the microstrip patch and their shorted versions as well.

 The present invention is compatible with any of the current integrated and
25 integrated circuit package manufacturing techniques and architectures. For instance, tape bonding or flip-chip techniques could be used instead of wire bonding to interconnect the chip to the package. Also, a wide range of low-loss dielectric materials and single-layer or multi-layer manufacturing techniques such as the typical ones used in MCM-L, MCM-C and MCM-D or D/L techniques (for instance
30 HTCC, LTCC, lamination, thin and thick film processes) can be combined with the newly disclosed antenna geometry and package arrangements to implement the invention. Analogously, the invention is compatible with MCM electronic architectures that include two or more semiconductor chips inside a single package. The MCM packaging architectures are typical for the development of SoP solutions,

and for instance other RF passive and active components can be mounted on the package apart from the semiconductor dice. This means that in some embodiments of the invention, the antenna will not be directly connected to the semiconductor die as in the example of Figure 1, but through an RF front-end (including for instance filtering, biasing, mixing and amplifying stages) or other passive elements (transmission lines, baluns, matching networks and so on) mounted on the package.

The above description relates the main aspects of the invention that contribute to the antenna miniaturization and its efficient integration on an integrated circuit package. It should be noted that not every folded structure would provide the desired degree of antenna miniaturization; packing a large length of wire or conducting material in any arrangement will not provide always an efficient behavior of the antenna, due to coupling between segments and bends, and due to an inefficient use of the available space. The present invention provides the necessary degree of compactness to achieve the desired degree of integration of the antenna into the integrated circuit package.

Of course, depending on the application (for instance cellular GSM, DCS or PCS, BluetoothTM, WLAN, IEEE802.11a, IEEE802.11b, Hyperlan, Hyperlan2, UMTS, AMPS, WCDMA, DECT, UWB, CDMA-800, PDC-800, PDC-1500, KPCS, wireless chip interconnection, GPS, etc.), the requirements on the antenna in terms of bandwidth, impedance, efficiency, size and packaging density will be different. For every application there will be a trade-off on several of those parameters, and those trade-offs can always be met according to the essence and spirit of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows an embodiment of an integrated circuit package including an antenna formed from a conducting pattern having seven segments, according to the present invention.

Figure 2 shows an embodiment of an integrated circuit package including a dipole antenna, according to the present invention.

Figure 3 shows an embodiment of an integrated circuit package including a slot or aperture antenna, according to the present invention.

Figure 4 shows an embodiment of an integrated circuit package including a slot or aperture antenna, according to the present invention.

Figure 5 shows an embodiment of an integrated circuit package including a multibranch antenna, according to the present invention.

5 Figure 6 shows an embodiment of an integrated circuit package including a loop antenna, according to the present invention.

Figure 7A shows an embodiment of an integrated circuit package including a coupled dipole antenna, according to the present invention.

0 Figure 7B shows an embodiment of an integrated circuit package including an active monopole antenna and a parasitic monopole antenna, according to the present invention, both monopoles coupled through a close proximity region.

Figure 8A shows an embodiment of an integrated circuit package including an inverted F antenna (IFA), according to the present invention.

5 Figure 8B shows an embodiment of an integrated circuit package including an antenna curve that defines at least a portion of the perimeter of an area.

Figures 9A and 9B show an embodiment of an integrated circuit package including a solid conducting pattern combined with a curve, according to the present invention.

Figures 10A-10N show examples of prior art space-filling curves suitable for use in the integrated circuit packages of the present invention.

10 Figures 11A-11D show embodiments of integrated circuit packages including monopole antennas in the form of a Hilbert curve, according to the present invention.

Figures 12A-12E show embodiments of integrated circuit packages including dipole antennas, according to the present invention.

15 Figures 13A-13C show embodiments of integrated circuit packages including loop and slot antennas, according to the present invention.

Figure 14A shows an embodiment of an integrated circuit package including a slot monopole antenna, according to the present invention.

Figure 14B shows an embodiment of an integrated circuit package including a slot dipole antenna, according to the present invention.

30 Figure 15 shows an embodiment of an integrated circuit package including a monopole antenna and a grounding plane or ground counterpoise, according to the present invention.

Figures 16A-16E show conventional package architectures suitable for use in the integrated circuit packages of the present invention.

Figure 17 shows an embodiment of an integrated circuit package including an antenna having non-linear segments, according to the present invention.

Figure 18 shows a perspective view (above) and a top plan view (below) of an embodiment of an integrated circuit package including a multibranch monopole antenna, according to the present invention.

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Figure 19 shows a perspective view (above) and a top plan view (below) of an embodiment of an integrated circuit package including a monopole antenna, according to the present invention.

Figure 20 shows a perspective view (above) and a top plan view (below) of an embodiment of an integrated circuit package including a monopole antenna, according to the present invention.

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Figure 21 shows a perspective view (above) and a top plan view (below) of an embodiment of an integrated circuit package including a L-shaped monopole antenna, according to the present invention.

Figure 22 shows a top plan view of an embodiment of an integrated circuit package including a slot antenna, according to the present invention.

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Figure 23 shows examples of how the box-counting dimension is calculated, according to the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention relates to an integrated circuit package comprising at least one substrate, each substrate including at least one layer, at least one semiconductor die, at least one terminal, and an antenna located in the integrated circuit package, but not on the at least one semiconductor die. The antenna comprises a conducting pattern, at least a portion of which includes a curve, and the curve comprises at least five segments, each of the at least five segments forming an angle with each adjacent segment in the curve, at least three of the segments being shorter than one-tenth of the longest free-space operating wavelength of the antenna. Each angle between adjacent segments is less than 180° and at least two of the angles between adjacent sections are less than 115°, and wherein at least two of the angles are not equal. The curve fits inside a rectangular area, the longest side of the rectangular area being shorter than one-fifth of the longest free-space operating wavelength of the antenna.

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One of the advantages of the package arrangements of the present invention is that they allow a high package density including the antenna. In some embodiments such as for instance those shown in Figures 19 and 21, the antenna can be fitted in a rectangular area, the longest edge of which is shorter than one-twentieth of the longest free-space operating wavelength of the antenna. In some cases such as the one shown in Figure 21, the arrangement of the package in terms of layout, antenna and chip arrangement allows the whole package to be smaller than one-twentieth of the free-space operating wavelength.

One aspect of the present invention is the box-counting dimension of the curve that forms at least a portion of the antenna. For a given geometry lying on a surface, the box-counting dimension is computed in the following way: first a grid with boxes of size L1 is placed over the geometry, such that the grid completely covers the geometry, and the number of boxes N1 that include at least a point of the geometry are counted; secondly a grid with boxes of size L2 (L2 being smaller than L1) is also placed over the geometry, such that the grid completely covers the geometry, and the number of boxes N2 that include at least a point of the geometry are counted again. The box-counting dimension D is then computed as:

$$D = -\frac{\log(N2) - \log(N1)}{\log(L2) - \log(L1)}$$

In terms of the present invention, the box-counting dimension is computed by placing the first and second grids inside the minimum rectangular area enclosing the curve of the antenna and applying the above algorithm.

The first grid should be chosen such that the rectangular area is meshed in an array of at least 5 x 5 boxes or cells, and the second grid is chosen such that L2 = 1/2 L and such that the second grid includes at least 10 x 10 boxes. By the minimum rectangular area it will be understood such area wherein there is not an entire row or column on the perimeter of the grid that does not contain any piece of the curve. Thus, some of the embodiments of the present invention will feature a box-counting dimension larger than 1.17, and in those applications where the required degree of miniaturization is higher, the designs will feature a box-counting dimension ranging from 1.5 up to 3, inclusive. For some embodiments, a curve having a box-counting dimension of about 2 is preferred. For very small antennas, that fit for example in a rectangle of maximum size equal to one-twentieth of the longest free-space operating wavelength of the antenna, the box-counting

dimension will be necessarily computed with a finer grid. In those cases, the first grid will be taken as a mesh of 10 x 10 equal cells, while the second grid will be taken as a mesh of 20 x 20 equal cells, and then D is computed according to the equation above. In the case of small packages with of planar designs, *i.e.*, designs
5 where the antenna is arranged in a single layer on a package substrate, it is preferred that the dimension of the curve included in the antenna geometry have a value close to $D=2$.

In general, for a given resonant frequency of the antenna, the larger the box-counting dimension the higher the degree of miniaturization that will be achieved by
10 the antenna. One way of enhancing the miniaturization capabilities of the antenna according to the present invention is to arrange the several segments of the curve of the antenna pattern in such a way that the curve intersects at least one point of at least 14 boxes of the first grid with 5 x 5 boxes or cells enclosing the curve. Also, in other embodiments where a high degree of miniaturization is required, the curve
15 crosses at least one of the boxes twice within the 5 x 5 grid, that is, the curve includes two non-adjacent portions inside at least one of the cells or boxes of the grid.

An example of how the box-counting dimension is computed according to the present invention is shown in Figures 23A and 23B. An example of a curve 2300
20 according to the present invention is placed under a 5 x 5 grid 2301 and under a 10 x 10 grid 2302. As seen in the graph, the curve 2300 touches $N1=25$ boxes in grid 2301 while it touches $N2=78$ boxes in grid 2302. In this case the size of the boxes in grid 2301 is twice the size of the boxes in 2302. By applying the equation above it is found that the box-counting dimension of curve 2302 is, according to the present
25 invention, equal to $D=1.6415$. This example also meets some other characteristic aspects of some preferred embodiments within the present invention. The curve 2300 crosses more than 14 of the 25 boxes in grid 2301, and also the curve crosses at least one box twice, that is, at least one box contains two non adjacent segments of the curve. In fact, 2300 is an example where such a double crossing occurs in 13 boxes
30 out of the 25 in 2301.

The package arrangements in which the antenna is built on a single layer of a package substrate are very convenient in terms of cost because a single mask can be used for processing the antenna pattern on such a layer. In some embodiments (such as for instance those shown in Figures 1, 2, 4, 5, 18, 19, 20,

and 21) the antenna is arranged in a single layer and fed in one tip of the curve, such that no conductor crossing over the curve is required. Although not required, a further simplification and cost reduction is achieved by means of those embodiments in the present invention wherein the antenna and the chip are mounted on the same layer of a package substrate.

It is noted that, according to the present invention, the antenna structure is not limited to a planar structure, because the package can include several portions or parts of the antenna in multiple layers or components of the package. The layers can be optionally interconnected by means of several vias and viaholes. A preferred arrangement in several embodiments comprises repeating a similar antenna pattern on two or more layers within at least one of the package substrates, and interconnect such similar conducting patterns for the antenna at one or more points. Typically a preferred point for interconnecting such similar layers will be the feeding point. This way the current splits symmetrically on every layer so that the ohmic resistance of the overall antenna is lower and the antenna is more efficient. A simple, low-cost version of such an arrangement comprises a package including a single substrate, the substrate including an conducting antenna pattern at both sides, the patterns being connected by at least one via.

In other embodiments, two or more conducting patterns for the antenna structure are located on two or more layers of the package substrate, but those patterns are different. At least one of the patterns includes the curve of the present invention with at least five segments, while the conducting pattern or patterns in the other layer or layers are used to modify the antenna impedance and impedance bandwidth, the antenna resonant frequency, the radiation pattern, or a combination of those antenna parameters at the same time.

Other embodiments where the antenna structure is split on several parallel layers consists on an active-parasitic arrangement. That is, the package includes a plurality of dielectric layers within one or more substrates of the package, wherein the package includes at least a first conducting pattern for the antenna in a first of the layers, the first conducting pattern on the first layer being coupled or connected to the semiconductor die. Such a first conducting pattern that is fed by the die is the active element of the antenna arrangement. In this arrangement, the package includes at least a second conducting pattern on at least a second layer of any of the substrates, the second conducting pattern being capacitively or inductively

coupled to the first conducting pattern of the antenna, the second conducting pattern acting as a parasitic element for the antenna. As an example, the antennas on the package embodiments shown in Figures 1-6, 11-15 and 17-22 could become the active antenna in such an active-parasitic antenna arrangement, wherein at least an additional antenna pattern on a parallel layer on the same or other substrate would act as the parasitic element or elements of the antenna structure. The effect of such parasitic elements is primarily an increase in the bandwidth and efficiency of the antenna, together with a finer tuning of the input impedance to match the output of the output amplifier connected to the antenna.

An active-parasitic arrangement can be done in such a way that any of the package embodiments in the present invention is coupled to an external antenna by means of inductive or capacitive coupling or a combination of both. This way the antenna set inside the package becomes the active antenna and the external antenna becomes a parasitic antenna for the active antenna inside the package.

In the case of non-planar, multi-layer or volumetric structures for the antenna pattern within the package, the box-counting algorithm can be computed by means of a three-dimensional grid, using parallelepiped cells instead of rectangular and meshes with $5 \times 5 \times 5$ cells and $10 \times 10 \times 10$ or $20 \times 20 \times 20$ cells respectively. In those cases, such a curve can take a dimension larger than two and in some cases, up to three.

Figure 1 shows one embodiment according to the present invention. The package layout is arranged such that the die 103 is displaced with respect to the center of the substrate 102 to allocate the antenna 100 in the area 101. According to the present invention, the maximum side length of rectangular area 101 is the longest operating wavelength for the antenna divided by five. This particular embodiment includes a monopole antenna with a single radiating arm 100. The arm is formed by five or more segments (seven segments 111 through 117 in this particular example) with at least two angles such as 121 and 122 being less than 115° . Although not required, it is preferred that at least two of the angles that are less than 180° degrees are defined in the clock-wise and counter clock-wise directions at the opposite sides of the curve (right side for 121, left for 122). The antenna curve 100 is fed through a connection 105 to a pad on the semiconductor die, such a connection including, but not limited to, a wire bond. Other wire bonds, or similar connections, can be used to connect the die with the external circuitry by

means of the pins 107. As is well known in the art, because a monopole antenna is an unbalanced, asymmetrical structure, it requires that one of the two RF terminals of the die 103 be connected to an external ground plane by means of at least one of the terminals 107. Also, in this particular embodiment, area 101 must be free of any conductor material below or above the antenna pattern 100, at least in 50% of the surface above or below area 101. In similar embodiments, the only metal that is placed below or above the antenna pattern are the conductors (such as for instance wire bonds or metal strips) interconnecting the die and the package terminals. This condition is also preferred for the printed circuit board or PCB hosting the FWSoc module.

A similar embodiment such as the one including a monopole in Figure 1, could include a folded monopole instead. For arranging the antenna within the package as a folded monopole, the free-end of the monopole will be connected by means of a conductor to a grounding terminal of the package.

Figure 2 shows another embodiment of the present invention where the package 2 includes a dipole antenna 200 according to the present invention. Such a dipole antenna has two radiating arms 201 and 202 and is fed by a differential input/output terminal 105, which is provided by a couple of close conductors such as for instance two wire bonds. Other suitable feeding means could include two conducting strips placed on the same layer as the antenna, the two strips reaching directly or by means of a via hole, the solder balls of a flip-chip, or the pad connection region of a flip-chip connected by means of tape automatic bonding (TAB). The substrate 102 can be a single layer or a multilayer one, but in any case it leaves a clearance with no conducting material on at least a 50% of the area 101 where the antenna is enclosed, in any of the layers above or below the layer on which the antenna is lying.

Figure 3 shows an embodiment of the present invention that includes an slot or aperture antenna in the package 3. The slot comprises a gap or slit 300 which is formed on a conducting pattern 303 placed on at least one of the layers of the package substrate, the pattern covering at least a 50% of the layer surface where the antenna is lying on. In the present example the conducting pattern covers the whole footprint of the package (except for the slot, of course, defining the antenna), although this is not required. Optionally, this conducting pattern 303 can be grounded to an external ground on the printed circuit board to which the package is

mounted, by means of one or more terminals of the package like 107. To feed the slot antenna, two conducting terminals 301 and 302 are connected for instance by means of two wire bonds 105 to the die 103. Another possible way of feeding such an antenna comprises placing two conductor strips patterned on a parallel layer to the antenna layer, and connecting the two strips to a couple of points at each side of the slot by means of a via. In any case, each of the two conducting terminals 301 and 302 will be placed at opposite sides of the curve forming the slot. An alternative non-symmetrical, unbalanced feeding scheme for the antenna comprises a microstrip transmission line crossing over or below the slot. Such a microstrip transmission line can be formed so that the conducting pattern including the slot is the ground plane for the microstrip line, while the other part of the transmission line is the conducting strip lying on a parallel layer above or below the conducting pattern.

Another example of an slot embodiment is disclosed in Figure 4. In this particular case, the slot 400 intersects the perimeter of the conducting pattern where the slot is located at one point 401. In other words the slot is not completely surrounded by conducting materials as in the case of the package depicted in Figure 3. As in the embodiment shown in Figure 3, the slot is fed at the two opposite sides of the curve by means of two terminal conductors 405 and 406. In some applications, the slot embodiment is preferred over the monopole or dipole arrangements shown in Figures 1 and 2 because radiation efficiency is quite higher (current flows all over the pattern and not necessarily only along the curve). Also, the impedance can be controlled by moving the feeding terminals 405 and 406 to different points along the antenna perimeter.

One of the advantages of using slot antennas according to the present invention is that the antenna can be built over a different substrate or layer than the die. The layer or substrate including the slot antenna can be fed by means of for instance one or more vias, viaholes, vertical conductors or posts from the substrate or layer including the die. In such an arrangement, the surface covered by the conducting pattern where the slot is printed can be maximized, reaching for instance an area larger than an 80% of the overall footprint of the antenna package. An example of a package architecture including the arrangement could be based on a similar package to item 45 in Figure 16. The slot antenna can be for instance mounted in one of the layers 1612, while the die 1601 is lying on a multilayer substrate 1611. Although Figure 16 describes a wire-bonding technique for the die,

in many applications a flip-chip is preferred. The advantage of a flip-chip is that the connections are facing down substrate 1611, such that the top side of the die facing the upper substrates (such as 1612) where the slot antenna is mounted can include a conducting surface that shields and protects the die from the fields within the antenna.

Figure 5 shows a multibranch antenna structure on a package 5, where several curves, with not necessarily the same lengths, intersect each other at some points. In particular, the antenna 500 includes three arms 501, 502, 503, each of them being in the form of a curve according to the present invention. In this particular example the antenna takes the form of a monopole as in Figure 1, with a single feeding port connected to the die by means of connection 105 and one or more connections within terminals 107 connected to an external ground plane. By adjusting the number and length of the antenna arms the frequency response of the antenna can be tailored. In general, for a wide-band behavior, the length from the tips of the arms to the feeding point of the antenna will be similar. For a multiband response with no overlapping between frequency bands, the length of each arm is associated mainly with the center frequency of a particular band within the antenna response. Such a multibranch arrangement is also compatible with, but not limited to, a dipole, an inverted F antenna, or a slot antenna.

Figure 6 discloses a package 6 including a loop antenna 600 according to the present invention. In this case, the curve defines the perimeter of a loop, with two points of the loop providing the differential input terminal that is connected to the die by means of 105. Again, for an improved performance of the system, the package will be typically arranged such that the layers above or below the layer on which the antenna 600 is located will leave a clearance with no metallization or conducting material in at least a 50% of orthogonally projected area 101 on any of the layers above or below. Analogously, the package might be operated such that the PCB where the package or module is located leaves such a clearance on any layer including a metallization.

Package 7 in Figure 7A includes coupled dipole antenna 700 with two arms 701 and 702 which are coupled together by means of a close proximity region 704. According to the present invention, the minimum distance between conductors in 704 should be less than one-tenth of the longest free-space operating wavelength of the antenna. Figure 7B discloses another embodiment where the package 75

includes an active monopole 751 and a parasitic monopole 752, the parasitic monopole being grounded to an external ground plane or ground counterpoise by means of at least one of the terminals of the package such as for instance 753. Also, the package will include at least another terminal within the set of terminals 107 to externally ground one of the RF voltage references of die 103. Two conducting parts of the antenna such as the active monopole 751 and the parasitic one 752 are coupled by means of a close proximity region 754 such that the minimum distance between conductors in 704 should be less than one-tenth of the longest free-space operating wavelength of the antenna.

Figure 8A discloses a package 8 including an inverted F antenna (IFA). Similar to the previous disclosed embodiments, the die 103 is displaced from the center of the package 102 to leave an area 101 where the conducting pattern of the antenna is located. In the same way as in the previous embodiments, this pattern can be located in the layer of the package that supports the die or chip 103, or, in the case of a multilayer substrate, can be located in any of the parallel layers of the substrate 102. In case the antenna is located in a different layer than the die, it can always be connected to the proper terminal 105 of the chip by means of a via hole crossing one or multiple layers. In this embodiment, the antenna 800 is grounded at one of its tips by means of at least one of the terminals 107 of the package, such as for instance 803. Also, the antenna is fed at one intermediate point of the antenna curve by means of a connection 105 such as for instance a wire bond or a conducting strip reaching a solder ball on a flip-chip.

Figure 8B shows another embodiment of the present invention. In this case, package 85 includes an antenna curve 851 that defines at least a portion of the perimeter of an area 850, the area being filled by a conducting material. A point within area 850, such as for instance a point in region 852, is chosen as the feeding point and is connected by means of a conductor to the die 103. Such a conducting pattern can be used in many different ways. It can constitute a monopole and in this case the RF ground reference of chip 103 will be connected to an external conducting ground by means of at least one of the terminals 107 of the package. For a monopole configuration it is required that, above and below the layer on which the antenna is located, any projection of area 101 enclosing the conducting antenna pattern on any of the layers of the package or on any of the layers of an external substrate where the package is mounted leaves a clearance with no metallization at

least on 50% of the projected area 101. When more than 50% of the area below 101 is filled with a conducting material, the antenna becomes a microstrip or patch antenna according to the present invention, the conducting material being the ground for the microstrip or patch antenna. The antenna also becomes a planar inverted F antenna (PIFA), if additionally, at least one short to ground is placed at any point within the conducting antenna pattern. In the case of either a microstrip or patch arrangement, or in the PIFA case, the ground covering more than 50% of the area underneath the antenna is preferred. Such a ground can be included in any of the layers of a substrate 102 supporting the antenna and/or the chip 103, or alternatively it can be included in the external substrate or PCB supporting the package.

In the case of any microstrip or patch arrangement (including a PIFA arrangement), the characteristic pattern of the invention should include a curve with at least fifteen segments, with at least seven of them being shorter than one-twentieth of the free-space operating wavelength of the antenna, according to the present invention. This is necessary to achieve the desired degree of miniaturization that allows the integration of the antenna in a small area. The rest of the general conditions that conform the essential geometric aspects of the invention, as described above, apply to the microstrip patch and their shorted versions as well.

The geometry of the antenna in the present invention is not limited to being completely shaped by the characteristic curve of at least five segments. The curve needs only to define a portion or an aspect of the geometry, such as for instance a portion of the conducting strip or wire in case of a wire antenna such as a monopole or a dipole or an IFA, a portion of the slit in case of an slot or aperture antenna, a portion of the antenna perimeter in case of a patch antenna. For instance Figures 9A and 9B generally describe two examples 9 and 10 of packages including two antenna arrangements within the package, where a solid conducting pattern 910 and 911 is combined with the curves 920 and 921, but wherein the curves 920 and 921 do not define the entire antenna shape.

Figures 10A through 10N are examples of prior art space filling curves for antenna designs. Other types of multiband antennas that also feature a reduced size are multilevel antennas disclosed in WO/0122528.

Figures 11A through 11D show four examples of preferred embodiments of the invention. All four package examples 26 through 29 include a monopole

antenna according to the present invention. In package 26 in Figure 11A, the die 103 is displaced from the center of the package to leave space for including the antenna pattern 1100. In this particular example, the antenna pattern 1100 is defined by a space-filling Hilbert curve 14. The die 103 has one connection to the antenna pattern by means of a conductor 1104, while the second RF terminal is connected to at least one of the terminals of the package such as for instance 1101 by means of a conductor 1102.

Another monopole antenna arrangement is shown in package 27 in Figure 11B. One of the main differences between package 26 in Figure 11A and package 27 in Figure 11B is that the antenna pattern 1120 in Figure 11B is arranged along the longer side of the package so that the overall antenna length is maximized inside the package. This results in an increased radiation resistance, bandwidth and efficiency for the antenna. For this purpose, the SFC curve 14 has been modified to provide the characteristic elongated shape 1120. Although the antenna pattern in this embodiment has been shown with a particular example of SFC such as 14, an analogous embodiment maximizing the antenna length could be arranged by using any of the general curves according to the present invention.

In Figure 11C, package 28 contains another example of a monopole, where a maximum use of the available substrate surface is combined with a maximum length for the antenna pattern. The curve is split into two parts 1130 and 1132, both parts being connected by means of a conducting segment 1131. This arrangement is optimized by placing the die 103 as close as possible to one of the corners of the package. In this embodiment, the rectangular area that encloses the antenna pattern also encloses the die or chip 103. It is clear from this embodiment that it is not necessary in the present invention for the antenna and the die to be mounted in separate, non-overlapping rectangular areas.

Although package 29 in Figure 11D looks similar to package 28 in Figure 11C, in fact it includes a different architecture for the antenna in the package. The antenna arrangement in Figure 11D is a multibranch monopole, with a first arm 1140 and a second arm 1141, the arms being connected by means of the conducting segment 1142. Arm 1140 has one of its tips connected to the die 103, while the other tip is left free with no connection. For such an embodiment, the efficiency of the antenna is improved when the length and shape of the arm 1141 is the same as the portion of the arm 1140 that goes from the connection to segment 1142 to the

free tip of the arm. This is because the current intensity on the antenna is split on two equal arms, such that the ohmic resistance is divided by two, at least in the section of the antenna that covers from segment 1142 to the tips of the two arms of the antenna. It should be noted that the area that encloses the antenna is maximized with respect to the available area on the package; this provides an increased bandwidth and efficiency to the antenna behavior as well.

It can be seen that antenna curve in Figures 11A or 11B features a box-counting dimension larger than 1.5; in particular the dimension of this curve is between 1.9 and 2.1. It can be seen as well that if rectangle 101 is covered by a grid of 5 x 5 equal boxes, then the curve will cross more than 14 of the 25 boxes (about a 75% of the boxes would be crossed).

Also, it can be seen that at least one of the boxes would be crossed at least twice by the curve defining the antenna pattern. Such characteristic aspects for the antenna arrangement (a high box-counting dimension, a maximum surface usage, combined with a large number of small segments being connected to shape a very long curve) is especially suitable when a higher degree of miniaturization is required; for instance when the longest side of the rectangular area 101 is to be shorter than one-twentieth of the longest free-space operating wavelength.

Figure 12 shows several package embodiments including dipole antennas. In Figure 12B, package 31, the two equal arms of the dipole 1221 and 1222 are shaped according to a curve of the present invention, and are fed by a pair of conductors 1220. Another dipole arrangement is shown in Figure 12A, included on package 30. In this case, each of the arms are placed at opposite sides of the chip such that the overall antenna size from the free tip of one arm to the other free tip of the other arm is maximized. This provides an improved radiation resistance, bandwidth and efficiency. This can be further improved by arranging the dipole as shown in package 32 in Figure 12C, which is a multibranch dipole. There, every arm of the dipole is split into two curves 1230 and 1231 in the first arm and 1232 and 1233 in the second arm such as the current intensity is divided by two, and the overall loss resistance is halved. The two branches of each arm are connected by means of the conducting segment 1234 and 1235, respectively. In such an arrangement the dipole length is maximized together with the transversal size of the dipole such that the overall bandwidth and efficiency of the antenna is maximized.

In Figures 12D and 12E, packages 33 and 34 can be used when the antenna is desired to operate in a folded dipole mode. In package 33, the dipole enclosed in area 1241 is equal to the dipole enclosed in area 1242, except in that the one in 1242 is fed at its center by means of a pair of conductors connected to the chip or die. Both dipoles are connected at the tips, as generally done in a folded dipole arrangement. Another possible arrangement of the two dipoles defining the folded dipole structure is shown Figure 12E in areas 1251 and 1252 of package 34. The advantage of a folded dipole structure is that the input impedance of the dipole is increased with respect to a non-folded structure, and also the bandwidth of the antenna is improved.

It can be seen that the antenna geometries on packages 33 and 34 in Figures 12D and 12E form a closed loop, and therefore can define a loop antenna as well. Those structures can operate as folded dipoles or as loop antennas depending on the operating frequency and excited mode. This means that the antenna can also be operated as a multimode antenna, which can be used for instance to integrate in the same package two different communication or wireless services operating at two different frequency bands.

Other examples of loop antennas for an integrated circuit package according to the present invention are described in Figures 13A-C. In Figure 13A, package 35 includes a conductive curve 1301 constructed by means of several Hilbert-like sections around the semiconductor die 103. The loop is fed by means of a differential input/output port formed by a pair of conductors 1302. Again, such an arrangement maximizes both the perimeter and the area covered by the loop. The box-counting dimension of this curve is between 1.9 and 2, providing a high package density for operation at very low frequencies. This is another example of an embodiment where the die is placed inside the rectangular area enclosing the conducting pattern of the antenna. To protect the chip from the intense magnetic field flowing inside the loop, the chip can include a conductive layer shielding at least one of its surfaces. For this purpose, a flip-chip arrangement would be preferred.

Package 36 in Figure 13B is the dual version of the package 35 shown in Figure 13A, where the loop takes the form of an slot on a conducting pattern in any of the substrate layers supporting the die. The same advantages in terms of package density and maximum usage of the available surface are obtained in this

case. The feeding scheme of such a loop is also differential, with one conductor 1311 connected to the conducting region inside the loop, while a second conductor 1312 is placed at the opposite side of the curve, on the outer conducting area. As shown in Figure 13C, the two conductors 1321 and 1322 do not need to be close together on the same side of the die, they can be for instance at opposite sides. Depending on the relative position of the two conductors, the impedance will change, which is useful for tuning the antenna to match the required output impedance of the output RF amplifier inside the die.

Package 38 in Figure 14A is the dual version of the monopole in Figure 11B. It shares the same advantages in terms of maximizing efficiency and radiation resistance due to maximum use of available length. In fact, it can be seen as a combination of package 27 in Figure 11B and package 4 in Figure 4. Like package 4 in Figure 4, the antenna is a slot, and that the slot intersects the perimeter of the conducting pattern including the slot at one point. Other combinations are possible, such as for instance including the two tips of the slot inside the conductive pattern supporting the slot, as in Figure 3, or having both ends intersecting the perimeter of the pattern as shown in package 39 in Figure 14B.

Figure 15 displays a package including a monopole antenna 1501. In this example, a part of the grounding plane or ground counterpoise 1502 is placed on the same layer as the antenna, in such a way that it does not overlap the rectangular area 1505 in which the monopole arm 1501 is enclosed. The antenna is fed through one conductor 1503. In this particular embodiment, it is shown how the tip of the monopole 1504 can be put close to the ground plane 1502. This would provide some capacitive loading to the antenna that contributes to the overall antenna miniaturization.

Figures 16A-16E describe, without any limiting purposes, several examples of conventional package architectures (items 41, 42, 43, 44, 45) for integrated circuits. All of them share some common part arrangements. In most of the cases a semiconductor die or chip 1601, 1606 is attached to a substrate or laminate 1610, which is one of the most important parts of the package. Such a substrate or laminate acts as a mechanical support for the semiconductor die or chip, contributes to the heat removal from the chip, and provides several terminals 1603, 1604 to electrically connect the chip with the outside world. The chip and the package can be interconnected in many ways. A most common way is by means of wire bonds

1602, although other techniques such as for instance, tape bonding or flip-chip technologies are possible. The package is usually enclosed in a plastic mold or encapsulated 1615 to protect the chip and the interconnections with the terminals.

5 Item 41 in Figure 16A is an example of a package architecture where the terminals are pin connections. Such pin connections are common in DIL, DIL-SMT, QFP and PGA packages. Usually such pins surround the perimeter of the package and are connected to the chip directly by means of wire bonds or by conducting strips on top of the package substrate. In some cases, a metal frame includes both terminals and conducting strips that are connect (usually by thermocompression)
10 through wire bonds to the chip. In the case of a PGA package, the terminals are not only arranged around the perimeter of the package but in a 2D grid array underneath the package. This is typically employed when a high terminal count for both the chip and the package are required.

15 Items 42, 43, 44 and 45 in Figures 16B-D show several examples of BGA packages, wherein the pin terminals are replaced by solder balls 1604. Such an interconnection technique is also characteristic in flip-chip architectures (see items 43 and 44), wherein the chip is connected to the package by an analogous scheme. In a flip-chip arrangement, the chip is mounted upside-down, with connections facing down the packages substrate or laminate. In such an arrangement, the
20 interconnection is done by means of a grid of conducting balls or bumps 1605.

The market pressure for reducing the size and cost of integrated circuit packages has resulted in a set of new architectures to increase the functionality of the chips while reducing the footprint of the package. Item 44 in Figure 16D shows a chip-scale package (CSP), wherein the package is shrunk to almost match the
25 reduced footprint of the chip.

Other means of increasing the package density include the use of multilayer structures within one or several substrates in the package. Item 45 in Figure 16E is an example of a package architecture where a plurality of dielectric layers 1611 are attached to each other to form the substrate that supports the chip. Every layer on
30 the substrate can support several metallizations and conducting strips to interconnect the chip 1601 with terminals 1604, or to other chips or electrical components (such as for instance resistors, capacitors, inductors, filters, mixers, amplifiers, oscillators, etc.) mounted on the substrate. Such metallizations on the layers can be interconnected by means of vias and via holes 1614. Additionally,

other laminates or substrates 1612 can be included above or below the chip to support additional components or chips. Again, such additional substrates can be interconnected with other substrates by means of vias and via holes.

5 Although the segments that make up the curve forming the antenna of the present invention are shown as being linear in the Figures, the present invention is not limited to curves formed only from linear segments. One or more of the segments making up the antenna curve of the present invention may be non-linear, up to and including all of the segments of the antenna curve. For example, as shown in Figure 17, curve 1702 includes several non-linear segments. When the
0 antenna curve of the present invention includes at least one non-linear segment, the shortest distance between any point on the curve having the at least one non-linear segment and an identical curve formed entirely of linear segments is less than one-tenth of the longest free-space operating wavelength of the antenna. This is true no matter how many non-linear segments are in the curve. As depicted in Figure 17,
15 curve 1701 (shown in dashed lines) represents an all-linear curve that is identical in shape to curve 1702, which has non-linear segments. The shortest distance between any point on curve 1702 and curve 1701 is less than one-tenth of the longest free-space operating wavelength of the antenna.

20 Additional examples of how the package can be arranged according to the present invention are shown in Figures 18 through 21. Figure 18 shows a multibranch monopole arrangement, with two identical arms 1801 and 1802 which are symmetrically arranged on the two halves of the package substrate. The die 1805 is displaced from the center of the substrate 1803 of the package but it is located near the center point of one of the substrate edges. This allows the two
25 arms to symmetrically grow from the segment 1807. The area covered by the antenna is maximized, while keeping a maximum length of the two curves to allow efficient antenna size compression. In particular, a grid of 5 x 5 cells over the package would include a portion of the curve in about at least an 80% of the cells. The box-counting dimension of the curve is close to 2.

30 The embodiment in Figure 18 shows a semiconductor die 1805 which includes at least two RF connections 1804 and 1806 for the antenna. Connection 1806 is made at the input of the double-branch structure, while connection 1804 is connected to one of the terminals 1808 of the package by, for instance, a via hole on substrate 1803 and a conducting strip in a second layer of the substrate 1803

that connects the via hole with at least one of the terminals 1808. Terminal 1808 would be connected to an external ground-plane, such as for instance a conducting layer on a printed circuit board or PCB. Although wire bonds are shown as an example in Figure 18, it will be clear to one skilled in the art that other interconnection arrangements (such as for instance flip-chip or TAB) could be used as well to interconnect the chip 1803 with the terminals on the package 1808.

An embodiment with an antenna arrangement such as that shown in Figure 18, could be used for instance to package an antenna operating at 2 GHz in a package smaller than 10 x 10 mm (that is a package with a size smaller than one-fifteenth of the free-space operating wavelength of the antenna). This is not considering the potential extra reduction in size obtainable by combining such an antenna design with a high dielectric constant substrate for 1803. This means that conventional, low-cost package materials such as polyimide compounds could be used instead of using a higher-cost, higher permittivity dielectric material. On the other hand, some extra miniaturization of the antenna and the package can be achieved if the package is made of a high permittivity material, at the expense of some extra losses (less efficiency) and some narrowing of the electrical bandwidth. Applications for such an embodiment could be for instance a FWSoc for Bluetooth™, for WLAN IEEE802.11 or for UMTS/3G-WCDMA.

Figure 19 shows another example of embodiment according to the present invention. The package includes a monopole antenna, the monopole antenna including a single radiating arm, the arm being fed at one point. The die provides one connection to the antenna and one connection to an external ground. In this case the package is arranged in a rectangular geometry, providing approximately one half of the package for the antenna and the other half for the die. For maximum size compression, a box-counting dimension of about 2 is desired for the antenna curve. This arrangement would allow, for instance, a FWSoc systems operating around 2 GHz (including, but not limited to, FWSoc for Bluetooth™, for WLAN IEEE802.11 or for UMTS/3G-WCDMA) to be packaged in a module smaller than 10 x 5 mm. In this case as well, the minimum rectangle enclosing the antenna has the longest side smaller than the corresponding longest free-space operating wavelength divided by 30.

For very small packages, such as for instance, a squared package of a size around one-thirtieth of the longest free-space operating wavelength of the antenna,,

other embodiments provide efficient solutions according to the present invention. In Figure 21 for example, the chip or die is arranged near a corner of the package, such that an 'L' shaped area is left free on the package substrate for the conductive pattern of the antenna. In such an arrangement, a monopole defined by a single radiating arm, the arm taking the shape of a curve 2102 according to the present invention is used. It is preferred that a first tip 2101 of the curve is near the edge of the package at one end of the L-shaped area, while the free tip 2100 of the monopole is left at the other end of the area. A box-counting dimension of about 2 is preferred for achieving such a high package density.

For some slightly larger packages (for instance a square package of side length around one-tenth of the longest free-space operating wavelength of the antenna), it is preferred that the antenna pattern includes a smaller number of segments, yet fills as much as possible the available space. A package including a monopole antenna with such characteristics is shown in Figure 20. In this embodiment, the monopole includes two equal radiating arms 2000 and 2001 that are interconnected by a point which in turn is used to feed the antenna by means of a conductor 2002. As in other monopole configurations, second conductor is used to connect the second RF output or ground reference for the chip to an external ground reference. A wirebond is connected to a via hole 2003. The via hole 2003 connects the wirebond to a strip that runs on another layer until it reaches at least one of the terminals of package that will be connected to an external ground.

An alternative embodiment for a package according to the present invention is shown in Figure 22. Here the antenna is a slot 2200 on a conducting pattern 2204, the pattern completely covering a layer of package substrate except for the slot. Optionally, some via holes are used to interconnect other layers above or below the conducting pattern. Preferably, the conducting pattern 2204 is connected to one or several of the package interconnections to allow the connection of the pattern to an external ground. In this embodiment, slot 2200 has one of the tips 2201 intersecting the external perimeter of the conducting pattern 2204. The other tip 2202 is completely surrounded by the pattern 2204. Again the antenna is fed by a pair of conductors, such as for instance a couple of wire bonds, each of the conductors being connected at some point at each of the sides of the slot. Also, a high box-counting dimension (of about 2) is required to achieve such a high package

density, and the curve preferably is chosen to cross at least 75% of the boxes within the smallest 5 x 5 grid that covers the antenna.

Those skilled in the art will notice that, although for the sake of clarification most of the previous embodiments are described in the Figures in a wire bond configuration, those embodiments are compatible with other chip interconnection techniques, such as for instance flip-chip or tape bonding techniques. Also, the present invention allows several ways for interconnecting the chip and the terminal or terminals of the package. One possible way according to the present invention comprises arranging several conducting strips on at least a different layer than the conducting antenna pattern. To minimize the coupling between the strips and the interconnections between the chip and the package terminals, it is preferred when possible to arrange such strips such that every crossing of the strips over or below any segment of the antenna structure is made in a perpendicular direction. In those packages where the terminals form a two-dimensional array of terminals (such as for instance in those packages within the families of ball grid arrays, and pin grid arrays), the present invention discloses an advantageous way of arranging the antenna curve and the package terminals such a minimum interference occurs. Such an arrangement consisting of choosing an antenna geometry wherein the curve includes a number of segments according to the present invention, wherein those segments form a 90° angle with adjacent segments at least at the region on top of the array of terminals, the antenna geometry being chosen so that the antenna curve follows a path along a rectangular mesh where the lines of the mesh are equidistant from the terminal pins or balls. A non-limiting example of curves that allow such arrangement are curves based on Hilbert, Peano, SZ and ZZ geometries. It becomes clear that other curves including 90° bends such as those in Figures 11, 12, 13, 14, 15, 18, 19, 20, 21, or 22 could be used for that purpose as well.

Although the previous embodiments show a direct feeding of the antennas from the chip, other feeding schemes are allowed within the present invention. For instance, other passive or active components such as resistors, capacitors, inductors, filters, resonators, transmission lines, baluns, mixers, diplexers, amplifiers or other RF networks could be placed between the antenna and the chip. This can be enabled through many different packaging architectures and techniques such as for instance any of the multi-chip module techniques such as MCM-L, MCM-C, MCM-D or MCM-D/L.

One particular way of connecting the antennas of the previous embodiments with the chip or intermediate RF networks is by means of capacitive coupling. Capacitive coupling is provided by two conductors placed in close proximity but not in direct contact, the conductors being ohmically connected to the antenna and to the chip or intermediate RF network, respectively. For instance, the two conductors can consist of two pads on a substrate of the package, the pads being either coplanar or lying one on top of the other on separate layers of the substrate. In other embodiments, such a coupling can be provided by a pad on the chip and a pad on the substrate connected to the antenna pattern.

Another possible feeding scheme for the antenna is by means of inductive coupling, wherein a loop of current connected to the chip is coupled to a loop within the antenna conducting pattern. Both loops, the one connected to the chip and the one in the antenna, can be lying on the same layer of the substrate, or alternatively they can be aligned one on top of one another on separate layers either within the same substrate or in different substrates within the same package, to maximize coupling between both loops.

It should be clear that the chip and antenna arrangements shown in the Figures, and others within the spirit of the present invention, can be arranged in several kinds of package topologies. For instance, many of the DIL topologies shown can be exchanged with SIL, QFP, PGA and BGA packages. In general, there is no limitation for any of the antenna designs shown in the present invention for combination with any kind of standard package topologies: single-in-line (SIL), dual-in-line (DIL), DIL-SMT, quad-flat-package (QFP), pin grid array (PGA), ball grid array (BGA) and its derivatives PBGA, CBGA, TBGA, SBGA, BG A.

Another possible way of arranging the conducting pattern of the antenna is building it in or upon the plastic mold encapsulating the whole package. The pattern can be for instance connected to the chip by means of a capacitive or inductive coupling to a conducting element on one of the package substrates, the conducting element comprising for instance a radiating arm of the antenna, or a reactive loop or pad of the substrate connected to the die or to an RF component or network connected to the die. The conducting pattern of the antenna can be built on such a plastic mold by several means, such as for instance a two-shot injection process, a co-injection process, an insert molding process or an MID process.

Although a multiband antenna such as for instance a multibranch antenna can be used within the package when several services or operating frequency bands are to be integrated in the same system, it is clear that other options within the present invention include arranging two or more antennas within the same package. For instance, those two or more antennas according to the present invention can be arranged in the same substrate layer, in different layers within the same substrate, in different substrates or even in the substrate and in the plastic casing of the package. One possible arrangement for a two antenna package includes two similar antennas wherein each one is fed independently, and wherein one conducting pattern is rotated 90° with respect to the other antenna pattern. This provides an effective means for integrating a polarization diversity communication system inside a single package.

The packaging techniques including an RF antenna according to the present invention provide an effective means of compressing the size of a wireless system such that it becomes feasible to integrate such a system in a small package. For instance, the present invention enables packaging a system operating within the 0.5 to 5.5 GHz frequency band in an area smaller than 10 x 10 mm. For instance, a package such as that shown in Figure 21 can integrate a full wireless system operating at the ISM 2.4 GHz band in an area smaller than 16 mm², without requiring the use of expensive high permittivity materials. This opens the scope for many new applications for systems such as for instance Bluetooth™, IEEE802.11a, IEEE802.11b, Hyperlan, Hyperlan2, UMTS, GSM900, GSM1800, PCS1900, AMPS, WCDMA, DECT, and GPS.

Any of the antenna designs arranged according to the present invention can be integrated also inside the semiconductor die. Although this possibility increases the cost of the system, it can be convenient at higher frequencies where the whole system is to be integrated inside the chip (SoC). Also, the same designs inside the package could be used as a single antenna component without the chip.

The package arrangements of the present invention can find application also in many other different environments. This way, one or several antennas inside the package can be used to power the chip by coupling the electromagnetic energy captured by the antenna to the biasing circuitry of the chip. This becomes advantageous for those packages that are to be used in very low-consumption devices or where they only need to react to an external electromagnetic signal

interrogating the system inside the package, such as it is the case in radio frequency identification systems (RFID).

5 Other possible uses of the package beside communication or wireless systems are sensors. In some embodiments the package integrates a sensor or sensing system besides the chip and the antenna. In other cases the antenna itself is used a sensing device for some type of electromagnetic signal or physical magnitude. When this is combined with a remote feeding scheme as described above, such packages can become specially suitable for low-cost applications where the sensor is to be located in remote areas with a difficult access. This includes sensors inside human bodies or animals, sensor inside cars, sensors inside 0 tires or chemical containers, sensors for dangerous environments such as flammable or explosive gases, or liquids. Some of the physical properties that could be sensed in those arrangements include, but are not limited to: temperature, pressure, tension, traction, acceleration, vibration, distance, speed, rotation, light 5 intensity, electromagnetic field intensity, chemical concentration of a chemical component inside a material, electromagnetic or acoustic doppler shift or motion.

Is to be understood that even though various embodiments and advantages of the present invention have been described in the foregoing description, the above 10 disclosure is illustrative only, and changes may be made in details, yet remaining within the spirit and scope of the present invention, which is to be limited only by the appended claims.

CLAIMS

1. An integrated circuit package comprising:
- at least one substrate, each substrate including at least one layer;
- 5 at least one semiconductor die;
- at least one terminal;
- an antenna located in said integrated circuit package but not on said at least one semiconductor die, said antenna comprising a conducting pattern, at least a portion of which includes a curve, wherein said curve comprises at least five segments, each of said at least five segments forming a pair of angles with each adjacent segment in said curve, at least three of said segments being shorter than one-tenth of the longest free-space operating wavelength of said antenna;
- 0 wherein the smaller angle of the pair of angles between adjacent segments is less than 180° and at least two of said smaller angles between adjacent segments are less than 115° , wherein at least two of smaller said angles are not equal; and
- 5 wherein said conducting pattern fits inside a rectangular area, the longest side of said rectangular area being shorter than one-fifth of the longest free-space operating wavelength of said antenna.
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2. An integrated circuit package as defined in claims 1 or 2, wherein said at least two angles that are less than 115° are defined in the clockwise and counter-clockwise directions at opposite sides of said curve.
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3. An integrated circuit package as defined in claims 1 or 2 wherein said conducting pattern fits inside a rectangular area, the longest side of said rectangular area being shorter than one-twentieth of the longest free-space operating wavelength of said antenna.
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4. An integrated circuit package as defined in claim 1, 2 or 3, wherein at least one of said segments is non-linear;
- wherein the shortest distance between any point on said curve having said at least one non-linear segment and an similarly-shaped curve formed entirely of

linear segments is less than one-tenth of the longest free-space operating wavelength of said antenna.

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5. An integrated circuit package as defined in claims 1, 2, 3 or 4, wherein said curve has a box-counting dimension larger than about 1.17, said box-counting dimension being computed by means of a first and a second rectangular grid, said grids fitting inside the smallest rectangular area enclosing said curve; wherein said first grid comprises at least 5 x 5 equal-sized cells; and wherein said second grid is the same size as said first grid, but with four times the number of cells, said cells of said second grid being scaled down by a factor of two with respect to the cells of said first grid.
 6. An integrated circuit package as defined in claims 1, 2, 3 or 4, wherein said curve has a box-counting dimension between 1.5 and 3, inclusive, said box-counting dimension being computed by means of a first and a second rectangular grid, said grids fitting inside the smallest rectangular area enclosing said curve; wherein said first grid comprises at least 5 x 5 equal-sized cells; and wherein said second grid is the same size as said first grid, but with four times the number of cells, said cells of said second grid being scaled down by a factor of two with respect to the cells of said first grid.
 7. An integrated circuit package as defined in claims 1, 2, 3 or 4, wherein said curve has a box-counting dimension of about 2, said box-counting dimension being computed by means of a first and a second rectangular grid, said grids fitting inside the smallest rectangular area enclosing said curve; wherein said first grid comprises at least 5 x 5 equal-sized cells; and wherein said second grid is the same size as said first grid, but with four times the number of cells, said cells of said second grid being scaled down by a factor of two with respect to the cells of said first grid.

8. An integrated circuit package as defined in claims 1, 2, 3 or 4, wherein said curve has a box-counting dimension between 1.1 and 3, inclusive, said box-counting dimension being computed by means of a first and a second rectangular grid, said grids fitting inside the smallest rectangular area enclosing said curve;
5 wherein said first grid comprises at least 10 x 10 equal-sized cells; and wherein said second grid is the same size as said first grid, but with four times the number of cells, said cells of said second grid being scaled down by a factor of two with respect to the cells of said first grid.
- 0 9. An integrated circuit package as defined in claims 5, 6 or 7, wherein said curve crosses at least 14 of the 25 equal cells of said first grid.
10. An integrated circuit package as defined in claims 5, 6 or 7, wherein said curve crosses at least one of said 25 equal cells of said first grid at least twice.
5
11. An integrated circuit package as defined in any one of claims 1-9, wherein at least a portion of said curve is a space-filling curve.
12. An integrated circuit package as defined in claim 11, wherein said space-filling
10 curve is a Hilbert curve or a Peano curve.
13. An integrated circuit package as defined in claim 11, wherein said space-filling curve is selected from the group consisting of SZ, ZZ, HilbertZZ, Peanoinc, Peanodec, and PeanoZZ.
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14. An integrated circuit package as defined in any one of claims 1-13, wherein said curve is formed on a single plane in said integrated circuit package, and wherein said first curve does not intersect itself at any point.
- 30 15. An integrated circuit package as defined in any one of claims 1-13, wherein at least two of said segments of said curve are located on different layers within said integrated circuit package, said segments being connected by one or more vias.

16. An integrated circuit package as defined in claim 15, wherein said two segments located on different layers are located on opposite sides of a two-sided layer within said integrated circuit package.
- 5 17. An integrated circuit package as defined in any one of claims 1-3 or 15, wherein said two segments located on different layers are located on two different substrates within said integrated circuit package.
18. An integrated circuit package as defined in any one of claims 1-17, wherein said
conducting pattern is a first conducting pattern, wherein said package includes at
least a second conducting pattern having two ends;
wherein one of the two ends is connected to a point on said first conducting
pattern; and
wherein said conducting patterns fit together inside a rectangular area, the
longest side of said rectangular area being shorter than one-fifth of the longest
free-space operating wavelength of said antenna.
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19. An integrated circuit package as defined in any one of claims 1-18, wherein said
curve is the radiating arm of a monopole antenna, said radiating arm including at
least one feeding point;
wherein said at least one feeding point is connected to said at least one
semiconductor die either directly, or indirectly by means of a passive or active
RF network; and
wherein said integrated circuit package includes at least one ground terminal to
connect the package and at least an RF connection of said semiconductor die
to a ground plane or ground counterpoise.
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20. An integrated circuit package as defined in claim 19, wherein said monopole
antenna is a folded monopole antenna.
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- 5 21. An integrated circuit package as defined in any one of claims 1-18, wherein said curve defines at least a portion of at least one of the two radiating arms of a dipole antenna, said two arms including at least one feeding point on each arm, wherein said at least two feeding points are connected to said at least one semiconductor die either directly, or indirectly by means of a passive or active RF network.
- 10 22. An integrated circuit package as defined in claim 21, wherein said dipole antenna is a folded dipole antenna.
- 15 23. An integrated circuit package as defined in any one of claims 1-18, wherein said curve is a slot in a conducting pattern, said pattern covering at least 50% of at least one of said layers of at least one of said substrates within said integrated circuit package.
- 20 24. An integrated circuit package as defined in claim 23, wherein said slot includes two feeding points, said points defining a differential input/output terminal; wherein each of said two feeding points is placed at opposite sides of said slot, said feeding points being fed by two conductors, said two conductors being either wire bonds, or conducting strips formed on the layer of the substrate containing said slot.
- 25 25. An integrated circuit package as defined in claims 23 or 24, wherein said slot is fed by a conducting strip, said conducting strip being located on a substrate layer above or below the layer on which the slot is located; and wherein said conducting strip crosses over the slot at at least one point.
- 30 26. An integrated circuit package as defined in claims 23, 24, or 25, wherein said slot is completely surrounded by the conducting material of said conducting pattern.
27. An integrated circuit package as defined in claims 23, 24, or 25, wherein said slot intersects the perimeter of said conducting pattern at at least one point of said perimeter.

28. An integrated circuit package as defined in any one of claims 23-27, wherein said conducting pattern is connected to at least one terminal of said integrated circuit package, said at least one terminal being adapted for connection to an external ground plane or ground counterpoise.

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29. An integrated circuit package as defined in any one of claims 1-18, wherein said first curve is at least a portion of the radiating arm of an inverted F antenna; wherein said radiating arm includes at least one feeding point on said curve, said at least one feeding point being connected to said at least one semiconductor die either directly, or indirectly by means of a passive or active RF network;

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wherein said radiating arm is connected to a first ground terminal of said integrated circuit package, wherein said first ground terminal is adapted for connection to an external ground plane or ground counterpoise; and

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wherein said integrated circuit package includes a second ground terminal which is adapted for connecting said at least one semiconductor die to said external ground plane or ground counterpoise.

30. An integrated circuit package as defined in any one of claims 1-18, wherein said antenna comprises at least two radiating arms, wherein said at least two radiating arms are coupled together in a region wherein the distance between said at least two radiating arms is shorter than one-tenth of the longest free-space operating wavelength of said antenna.

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31. An integrated circuit package as defined in claim 30, wherein said arms comprise the two radiating arms of a dipole antenna.

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32. An integrated circuit package as defined in claim 30, wherein said curve comprises first and second radiating arms, wherein said first radiating arm includes at least one feeding point, said at least one feeding point being connected to said at least one semiconductor die either directly, or indirectly by means of a passive or active RF network; wherein said integrated circuit package includes at least one grounding terminal to connect the package to a ground plane or ground counterpoise, and

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wherein said at least one semiconductor die is connected to a first grounding terminal of said integrated circuit package;

wherein said second radiating arm is a parasitic element having no feeding point, but having a grounding point that is connected to a second grounding terminal in said integrated circuit package; and

wherein said first and second grounding terminals are adapted for connection to an external ground plane or ground counterpoise.

33. An integrated circuit package as defined in any one of claims 1-18, wherein said curve is at least a portion of a closed curve, said closed curve defining a loop antenna, or a slot-loop antenna.

34. An integrated circuit package as defined in any one of claims 1-18, wherein said conducting pattern defines at least a portion of the perimeter of the radiating surface of a microstrip, patch or planar inverted F antenna; said curve comprising at least fifteen segments, wherein at least seven of said segments are shorter than one-twentieth of the longest free-space operating wavelength of said antenna; wherein said conducting pattern includes at least one feeding point, said at least one feeding point being connected to said at least one semiconductor die either directly, or indirectly by means of a passive or active RF network; and wherein said integrated circuit package is mounted over an external ground plane or ground counterpoise so that said ground plane or ground counterpoise completely covers the area underneath said integrated circuit package.

35. An integrated circuit package as defined in claim 35, wherein said conducting pattern is formed on a first substrate layer in said integrated circuit package; wherein said integrated circuit package includes a second conducting pattern located on a second substrate layer in said integrated circuit package; said second conducting pattern acting as the ground plane for said microstrip, patch or planar inverted F antenna.

36. An integrated circuit package as defined in any one of claims 1-35, wherein the connections between said at least one semiconductor die and said at least one terminal of said integrated circuit package are a plurality of conducting strips.
- 5 37. An integrated circuit package as defined in any one of claims 1-36, wherein said curve is located on the top surface of said at least one substrate; and wherein said at least one semiconductor die is mounted on the same substrate surface as said curve.
- 0 38. An integrated circuit package as defined in any one of claims 1-36, wherein said integrated circuit package includes at least one substrate having a plurality of layers; wherein said curve is located on at least two of said layers.
- 15 39. An integrated circuit package as defined in any one of claims 1-36, wherein said curve is located on at least one of said layers of said substrates; wherein said integrated circuit package includes at one additional conducting pattern; and wherein said additional conducting pattern modifies a property of said antenna, the antenna property being selected from the group consisting of the impedance and impedance bandwidth, the antenna resonant frequency, the antenna radiation pattern, and combinations thereof.
- 20 40. An integrated circuit package as defined in any one of claims 1-36, wherein said integrated circuit package includes at least two substrates; wherein said curve is located on the top surface of one of said substrates; and wherein said at least one semiconductor die is mounted on a different substrate surface from said curve; and wherein said curve and said at least one semiconductor die are located on parallel surfaces.
- 30 41. An integrated circuit package as defined in any one of claims 1-36, wherein the integrated circuit package does not include any metallization above or below the

antenna conducting pattern, except for wires or strips used to connect the at least one semiconductor die with the terminals of said integrated circuit package.

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42. An integrated circuit package as defined in any one of claims 1-36, wherein the integrated circuit package includes at least one additional metallization located on a substrate layer parallel to the substrate layer on which the curve is located, wherein the area containing said additional metallization covers less than 50% of the rectangular area enclosing said curve.
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43. An integrated circuit package as defined in any one of claims 23-28, wherein said slot antenna is located on a first substrate in said integrated circuit package; wherein said at least one semiconductor die is located on a second substrate in said integrated circuit package, said two substrates being connected by at least one via or post; and
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- wherein the minimum area containing said slot antenna covers at least 80% of the total footprint of said integrated circuit package.
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44. An integrated circuit package as defined in claim 43, wherein said at least one semiconductor die is a flip-chip, said flip-chip including a shielding conducting layer at the opposite face of the terminals, and wherein said slot antenna is positioned over said flip-chip so that said flip-chip is located between said first and second substrates.
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45. An integrated circuit package as defined in any one of claims 1-36, wherein the connections between said at least one semiconductor die and the terminals of said integrated circuit package are located on a first layer of a substrate in said integrated circuit package;
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- wherein said curve is located on the same substrate as said connections, but on a different layer of said substrate that is parallel to the first layer of said substrate where said connections are located.
46. An integrated circuit package as defined in any one of claims 1-45, wherein each time a conducting strip on said first layer crosses above or below said curve on

said second layer, the conducting strip and the curve lie in a direction perpendicular to one another.

- 5 47. An integrated circuit package as defined in any one of claims 1-36, wherein said integrated circuit package includes a two-dimensional array of pins or solder balls on a first layer of at least one substrate in said integrated circuit package and wherein said curve is located on a different layer above said first layer; wherein said two-dimensional array of pins or solder balls fits inside a rectangular grid having the same number of cells as there are pins or solder balls in the two-dimensional array, wherein each pin or solder ball is located in the center of a cell of the rectangular grid so that the grid is equidistant from each of said pins or solder balls; wherein all of said angles between adjacent segments of said curve are 90° , so that said curve follows a path along said rectangular grid between said pins or solder balls.
- 10 48. An integrated circuit package as defined in any one of claims 1-36, wherein said curve is repeated in two or more layers within at least one of the substrates of said integrated circuit package, and wherein all of said curves are connected through at least one via at the feeding points of said curves.
- 15 49. An integrated circuit package as defined in any one of claims 1-36, wherein said at least one semiconductor die and said curve are connected through capacitive coupling, said coupling being provided by two conducting elements separated by a dielectric material, each of said conducting elements being connected ohmically to said curve and said at least one semiconductor die, respectively.
- 20 50. An integrated circuit package as defined in any one of claims 1-36, wherein said conducting pattern is a first conducting pattern located on a first layer of at least one of said substrates in said integrated circuit package, said first conducting pattern being coupled or connected to said at least one semiconductor die; wherein said integrated circuit package includes at least a second conducting pattern located on a second layer of said substrate, said second curve being

capacitively or inductively coupled to said first conducting pattern, said second conducting pattern acting as a parasitic element for said first curve.

51. An integrated circuit package as defined in any of the preceding claims, wherein
5 said curve is adapted for electromagnetic coupling to an external antenna, said external antenna acting as a parasitic antenna for said curve.
52. An integrated circuit package as defined in any one of claims 1-51, wherein said
10 integrated circuit package is constructed by a technique selected from the group consisting of MCM-L, MCM-C, MCM-D, and MCM-D/L.
53. An integrated circuit package as defined in any one of claims 1-51, wherein said
15 integrated circuit package is selected from the group consisting of single-in-line, dual-in-line, DIL-SMT, quad-flat-package, pin grid array, ball grid array, PBGA, CBGA, TBGA, SBGA, and BGA.
54. An integrated circuit package as defined in any one of claims 1-51, wherein said
20 integrated circuit package is encapsulated in plastic;
wherein said curve is located on said plastic encapsulating said integrated circuit package; and
wherein said curve is capacitively coupled to a second curve located in said integrated circuit package, or to said at least one semiconductor die.
55. An integrated circuit package as defined in claim 54, wherein said curve is formed
25 on said plastic encapsulating said integrated circuit package by a technique selected from the group consisting of a two-shot injection process, a co-injection process, an insert molding process and an MID process.
56. An integrated circuit package as defined in any one of claims 1-55, wherein said
30 integrated circuit package is smaller than 10 mm by 10 mm, and said antenna is resonant at a frequency between 0.5 and 5.5 GHz.

57. An integrated circuit package as defined in any one of claims 1-55, wherein said integrated circuit package is smaller than 100 square millimeters, and said antenna is resonant at a frequency between 0.5 and 5.5 GHz.
- 5 58. An integrated circuit package as defined in any one of claims 1-55, wherein said integrated circuit package is smaller than 16 square millimeters, and said antenna is resonant at a frequency of 2.4 GHz.
- 10 59. An integrated circuit package as defined in any one of claims 1-55, wherein said antenna operates for a system selected from the group consisting of Bluetooth™, IEEE802.11a, IEEE802.11b, Hyperlan, Hyperlan2, UMTS, GSM900, DCS, GSM1800, PCS1900, CDMA-800, PDC-800, PDC-1500, KPCS, AMPS, WCDMA, DECT, UWB and GPS.
- 15 60. An integrated circuit package as defined in any one of claims 1-59, wherein said integrated circuit package contains or is integrated in a sensor for measuring a parameter selected from the group consisting of temperature, pressure, tension, traction, acceleration, vibration, distance, speed, rotation, light intensity, electromagnetic field intensity, chemical concentration of a chemical component
- 20 inside a material, electromagnetic or acoustic doppler shift or motion.

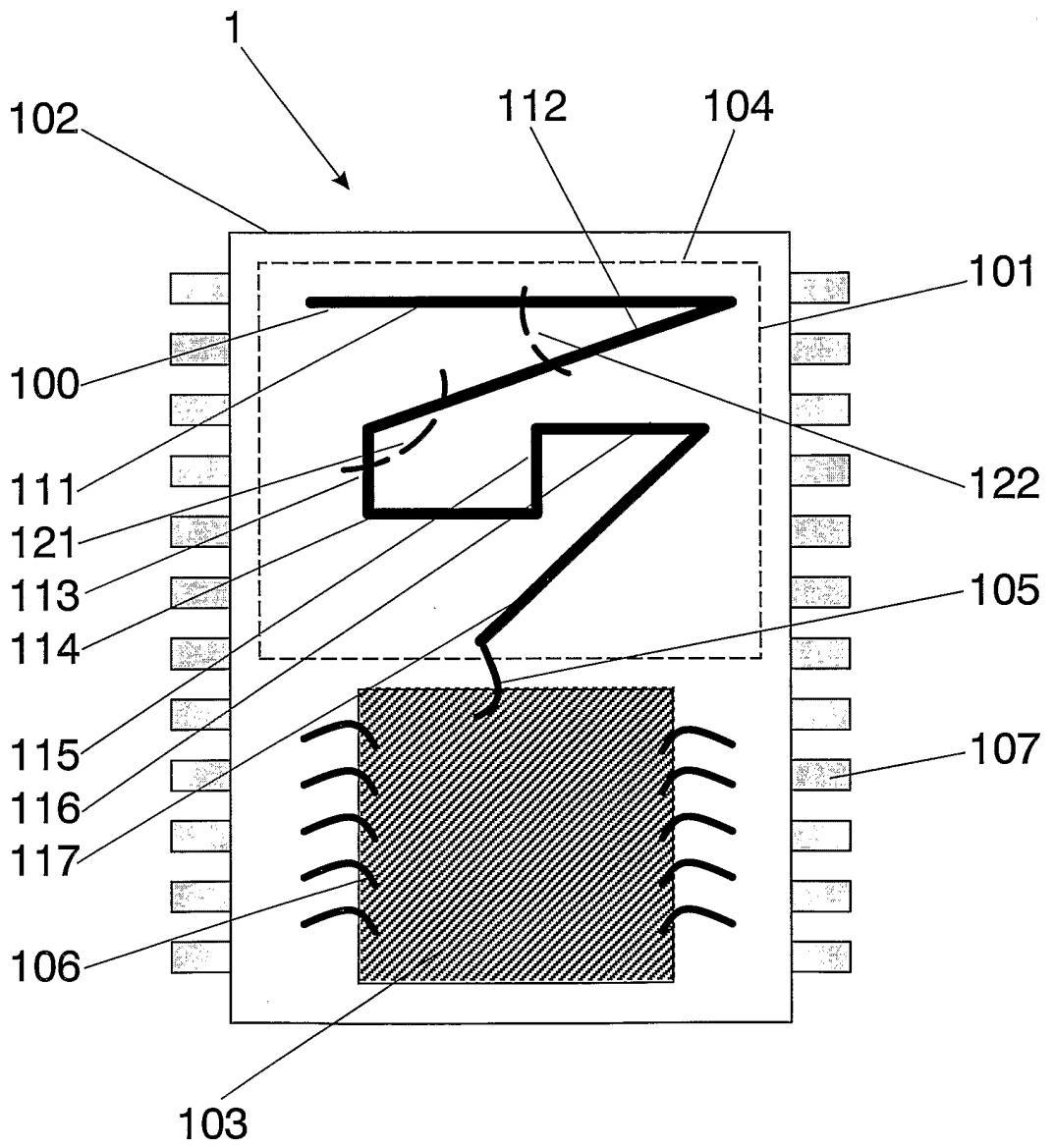


FIG.1

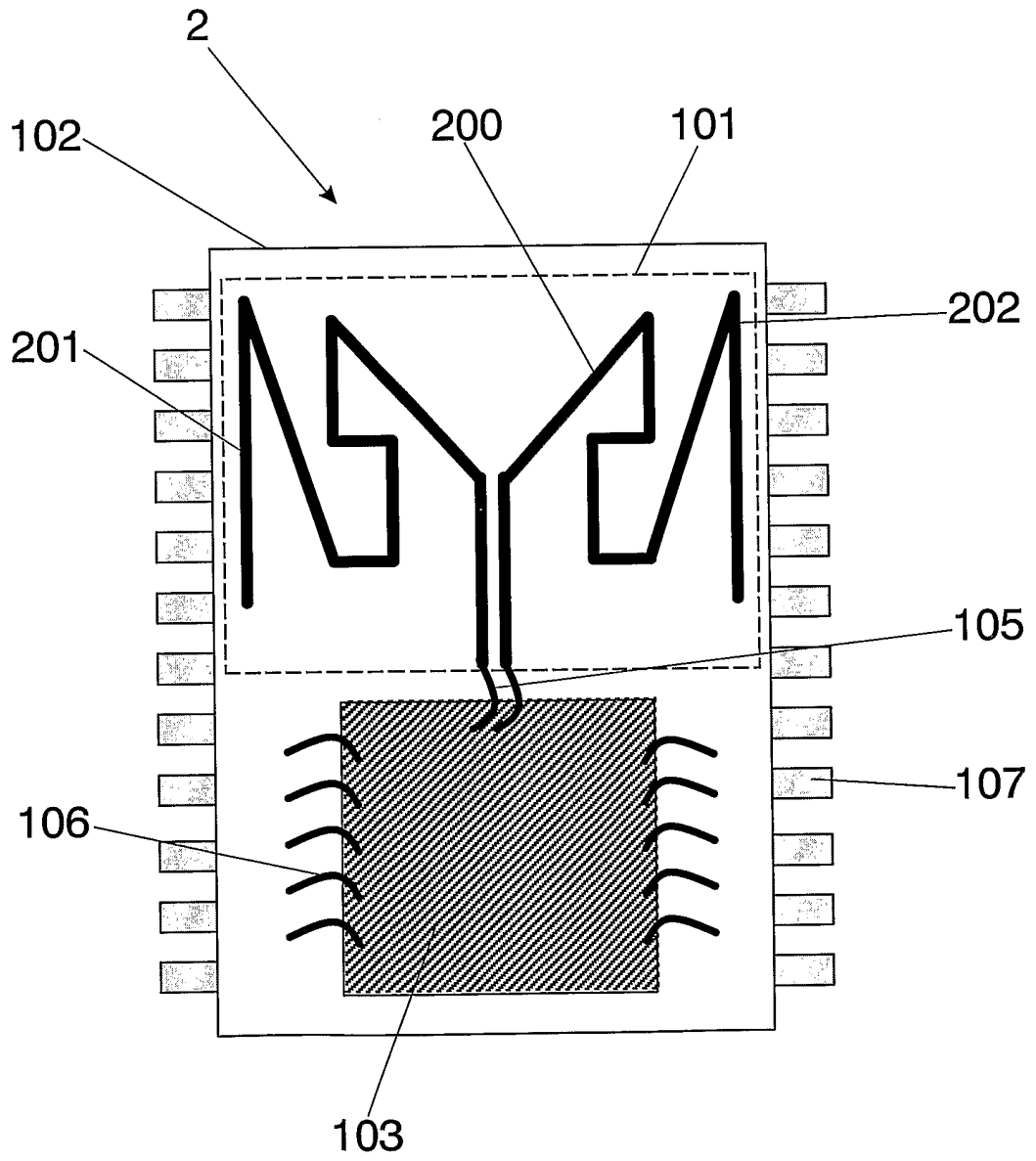


FIG.2

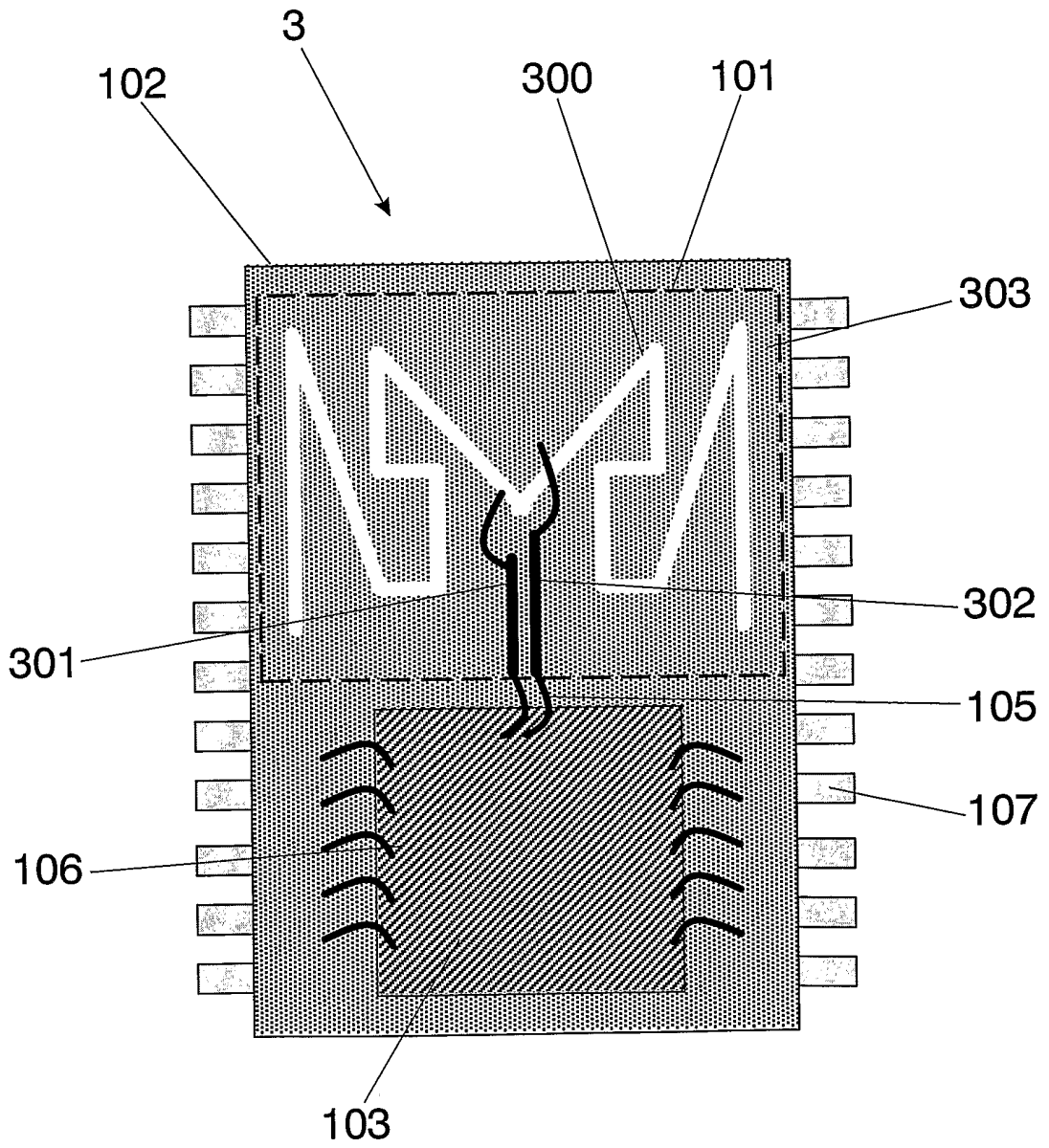


FIG.3

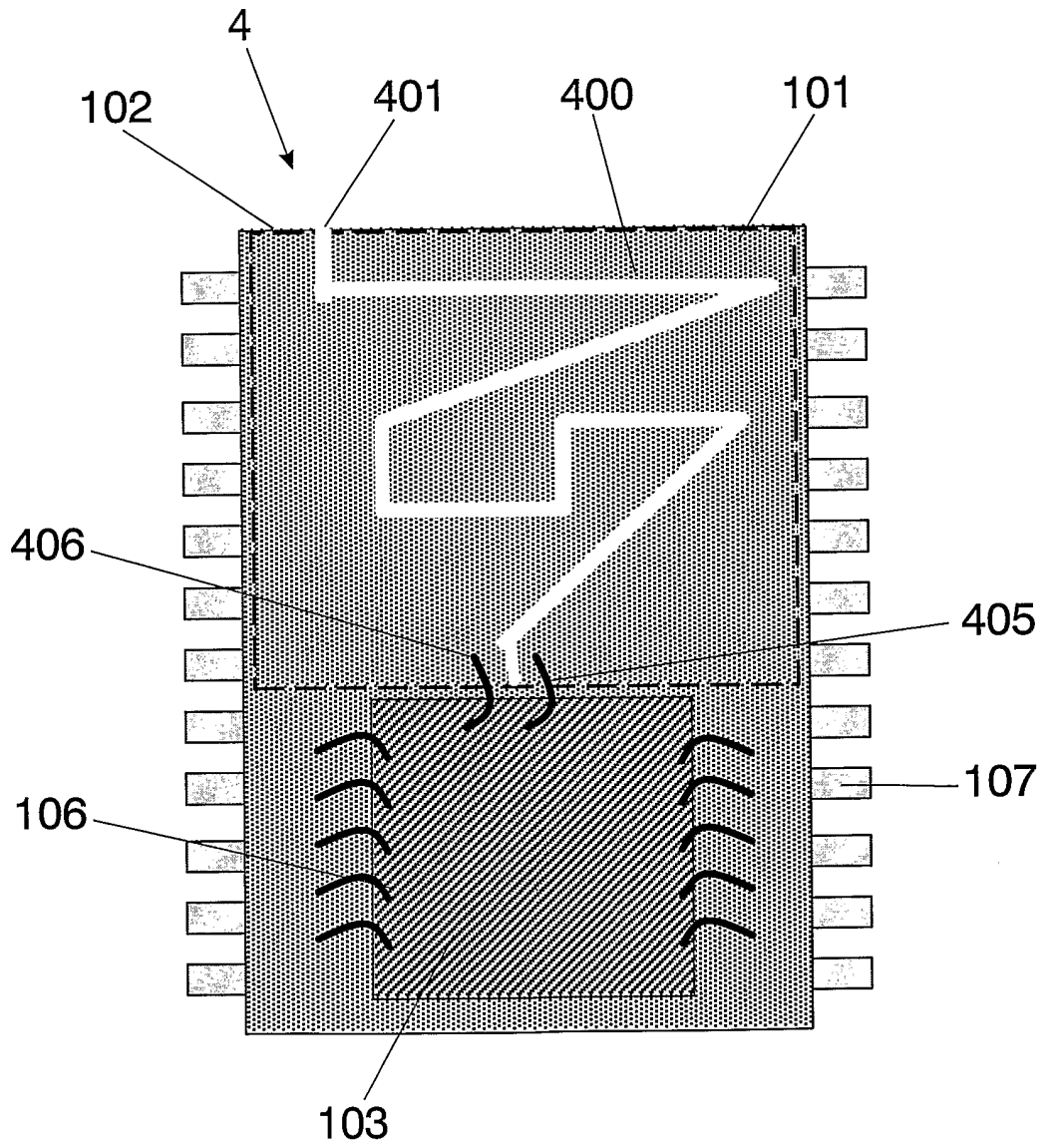


FIG.4

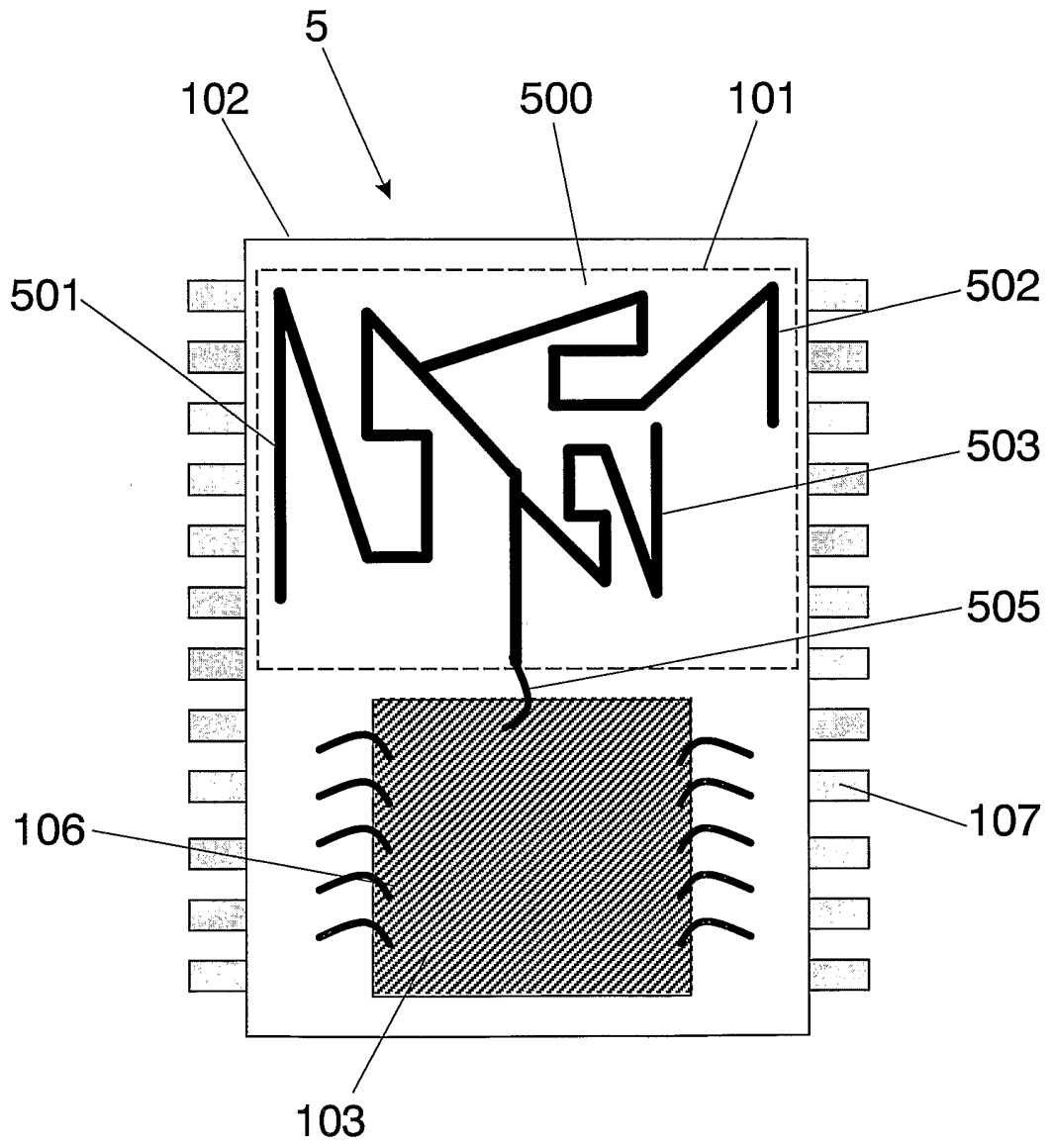


FIG.5

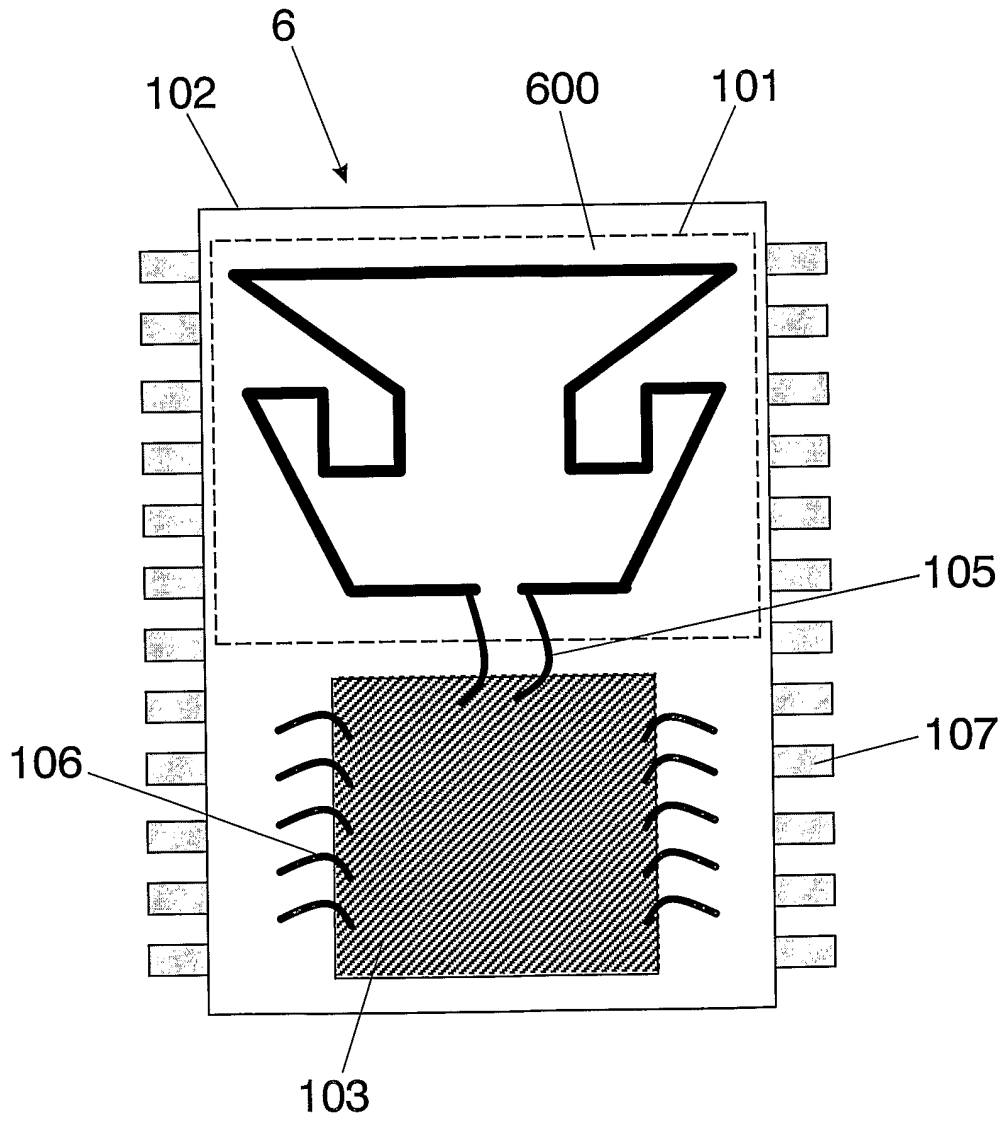


FIG. 6

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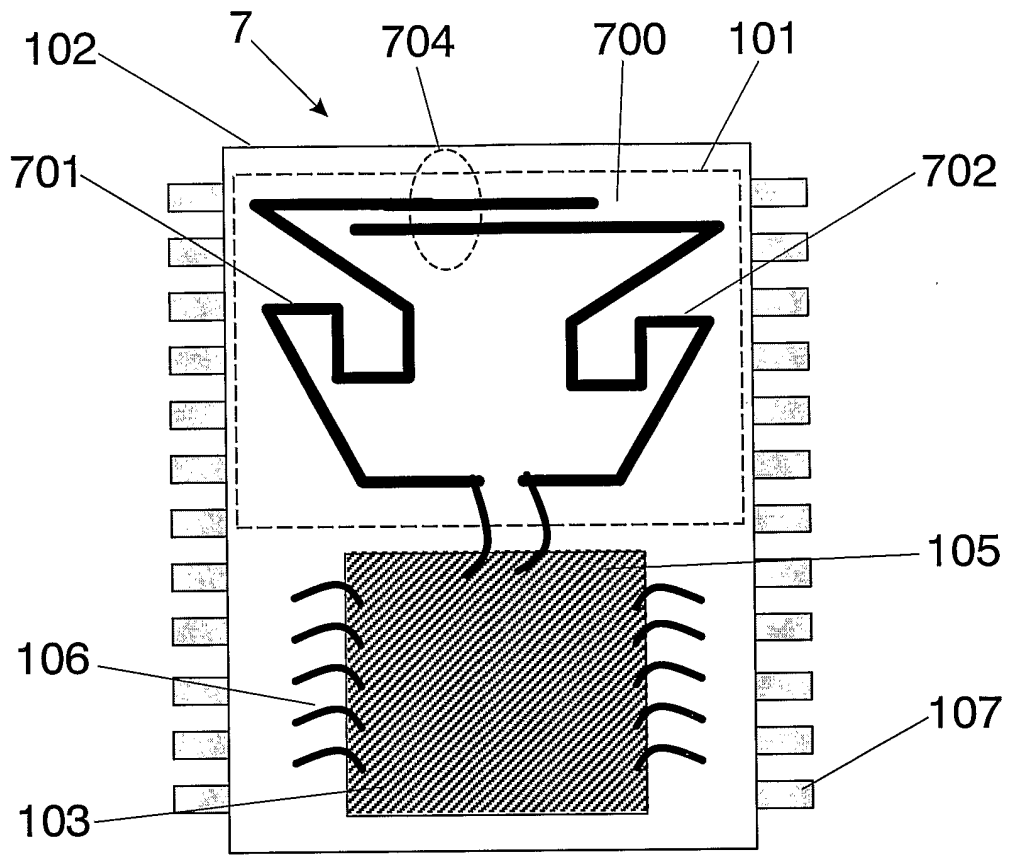


FIG. 7A

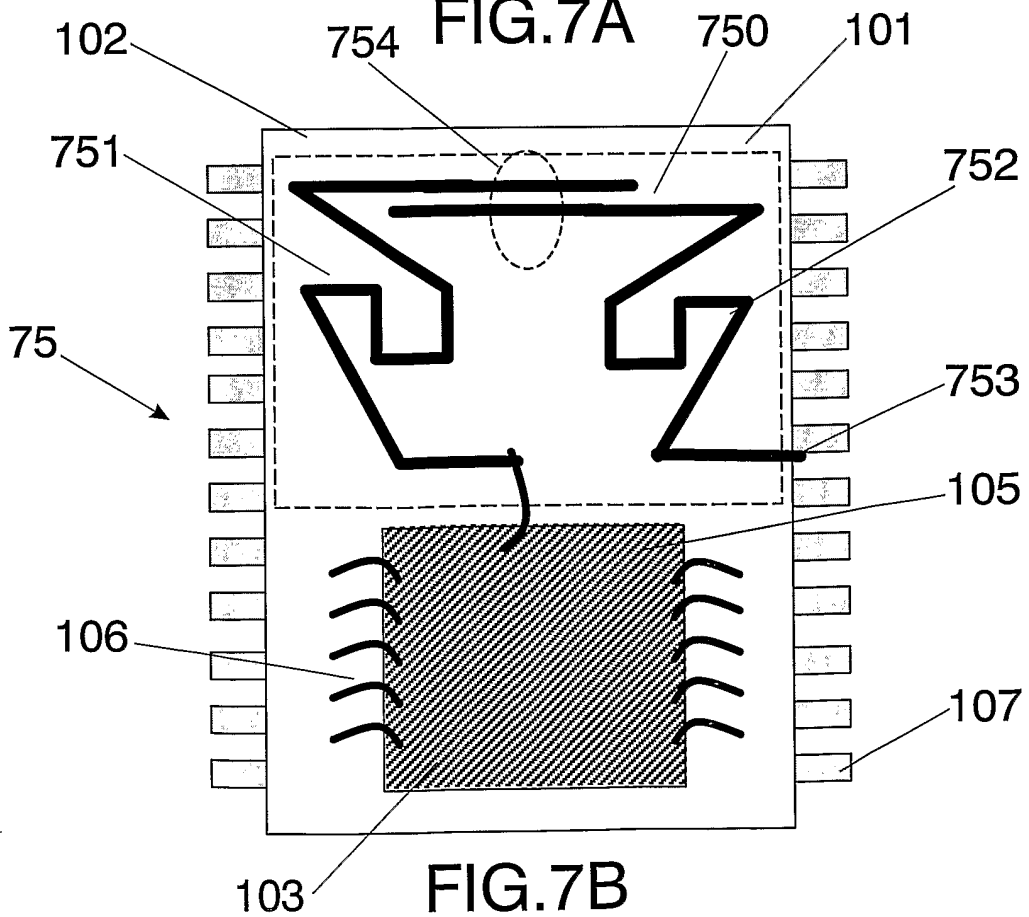


FIG. 7B

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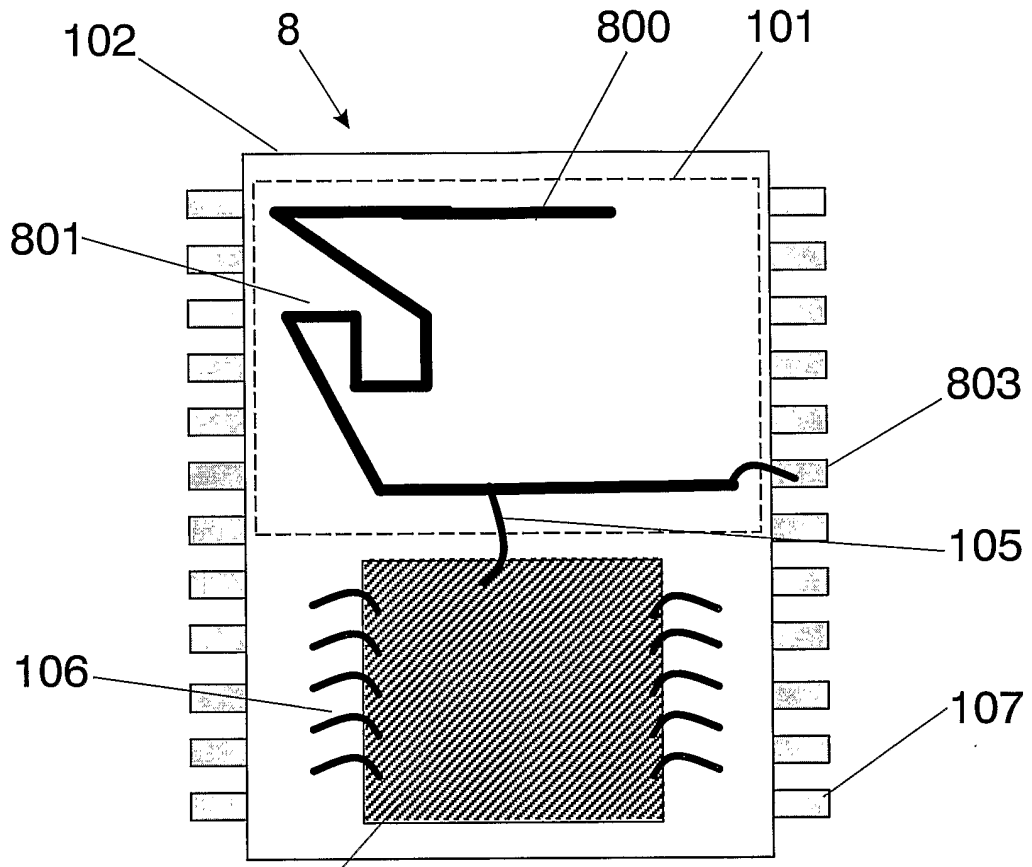


FIG. 8A

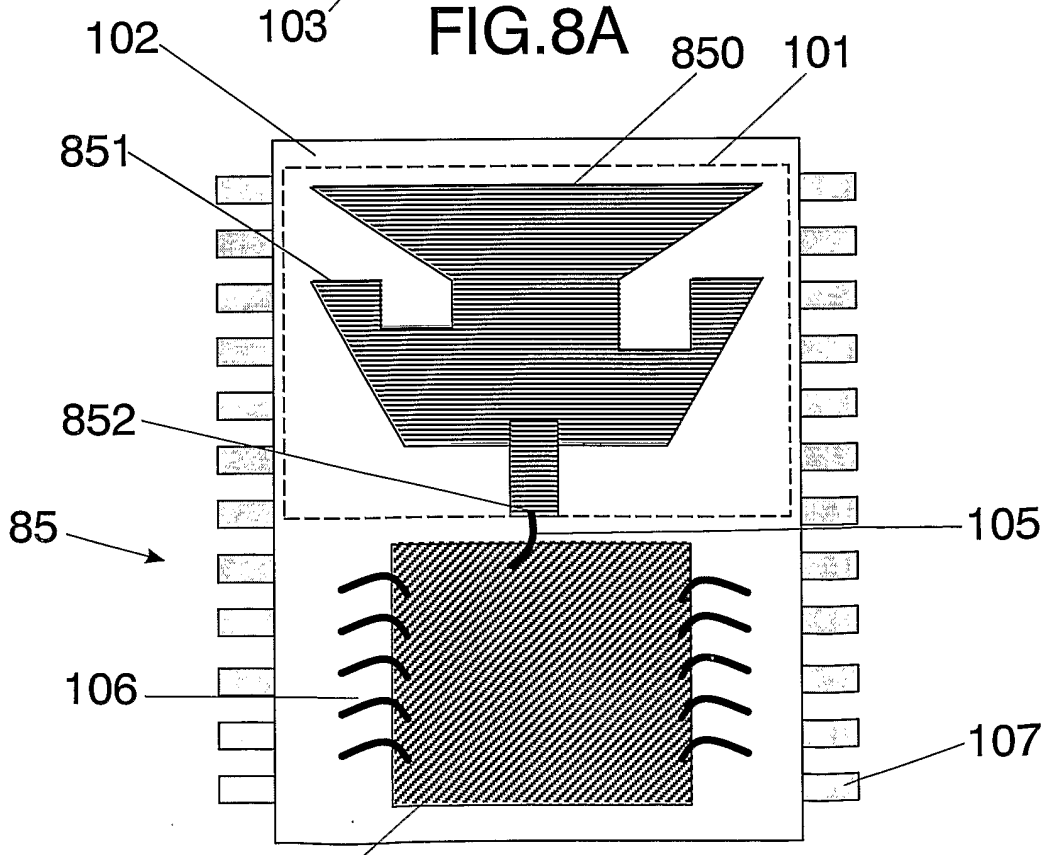


FIG. 8B

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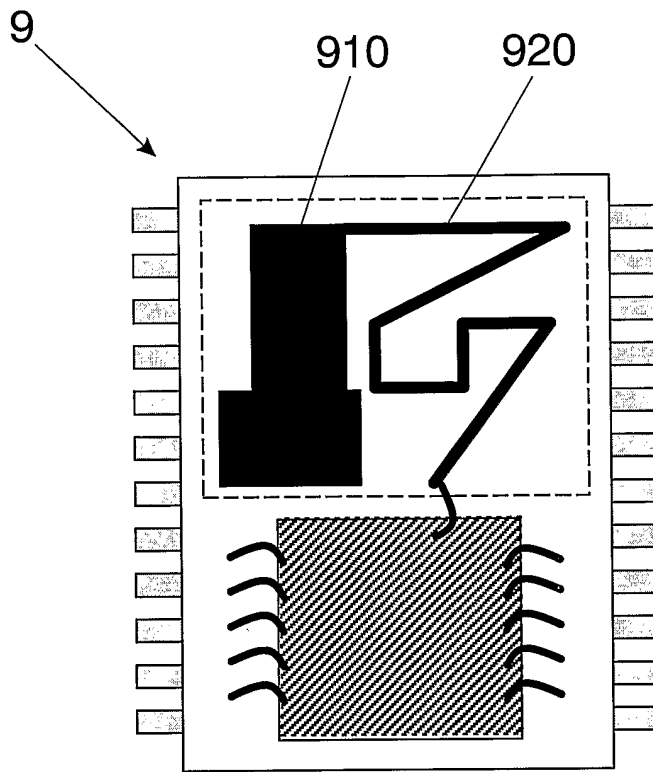


FIG. 9A

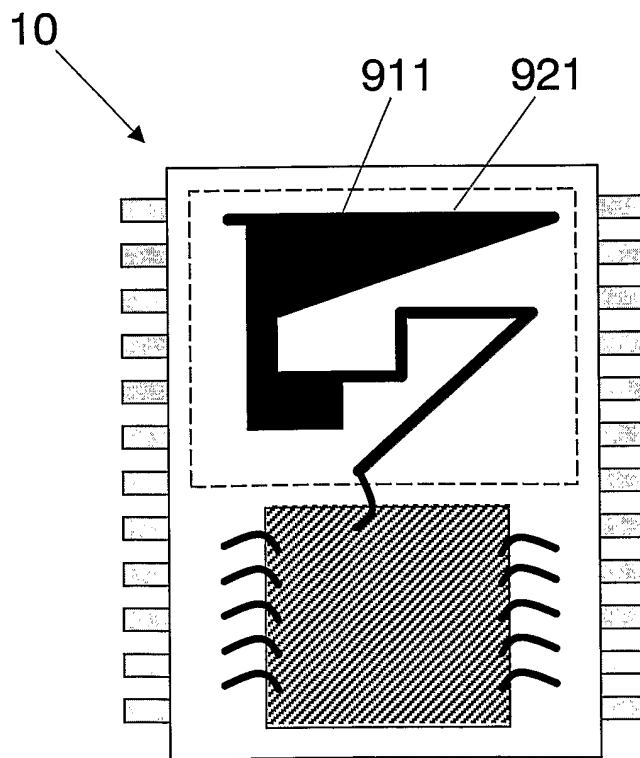


FIG. 9B

FIG.10A

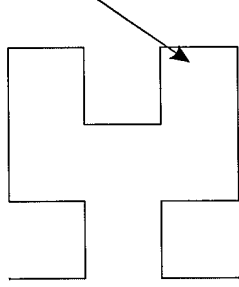


FIG.10B

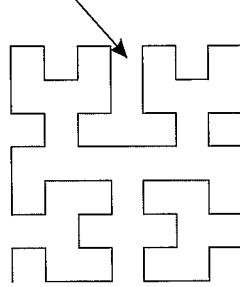


FIG.10C

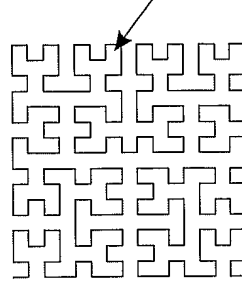


FIG.10D

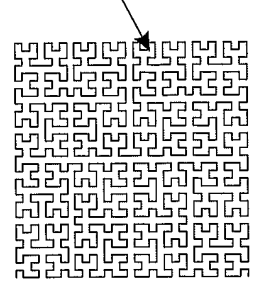


FIG.10E

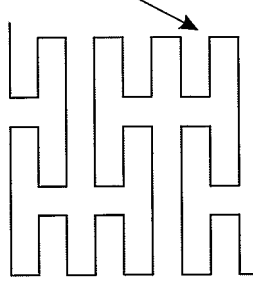


FIG.10F

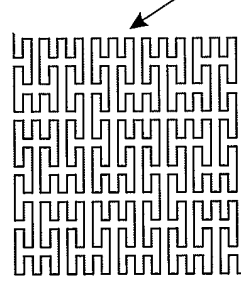


FIG.10G

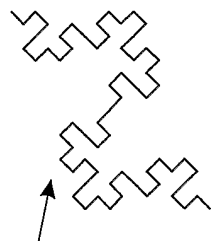
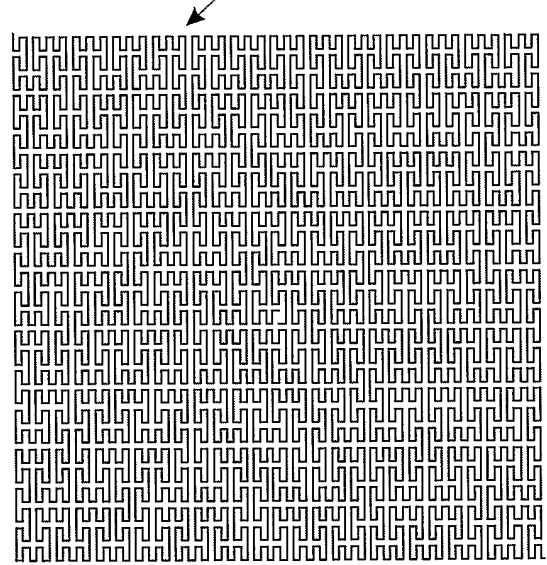


FIG.10H

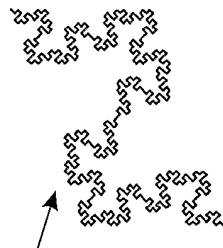


FIG.10I

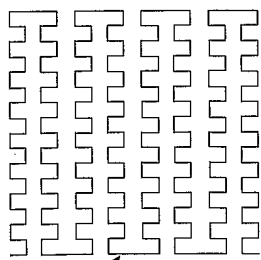


FIG.10J

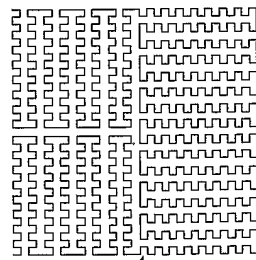


FIG.10K

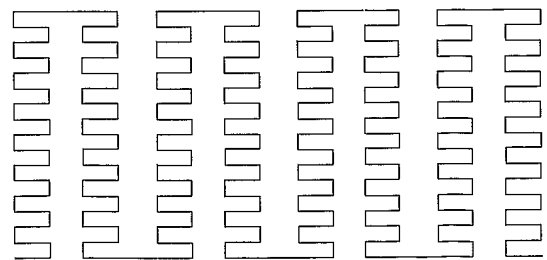


FIG.10L

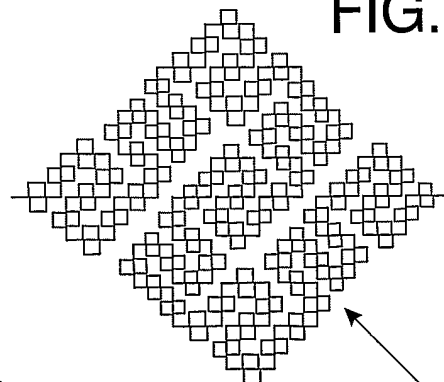


FIG.10

FIG.10N

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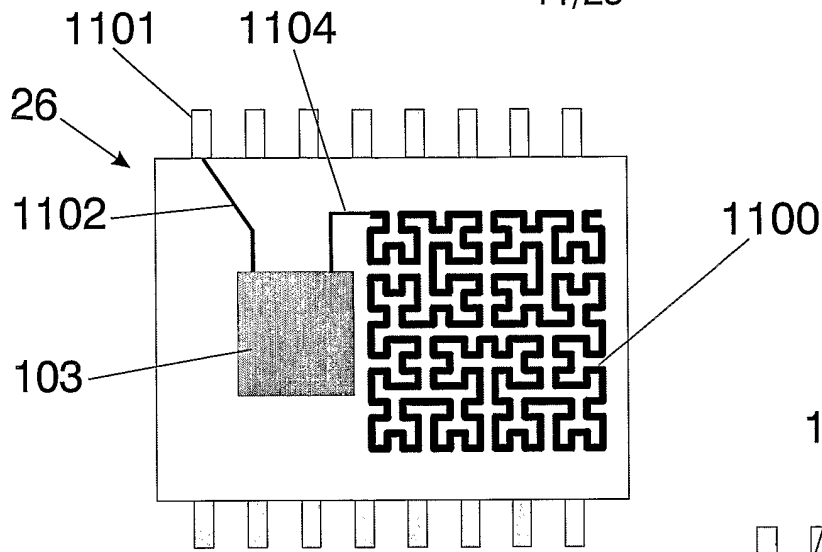


FIG. 11A

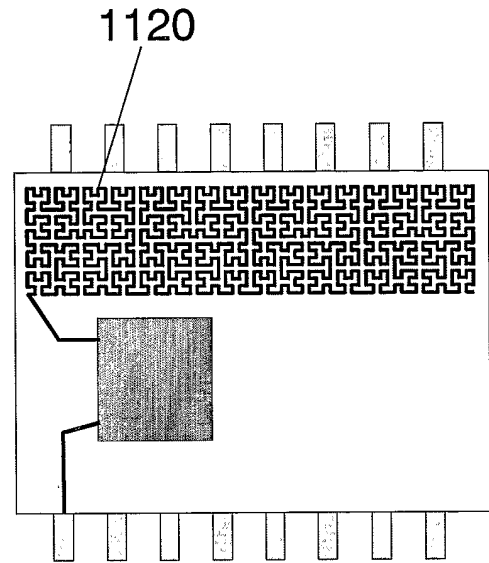


FIG. 11B

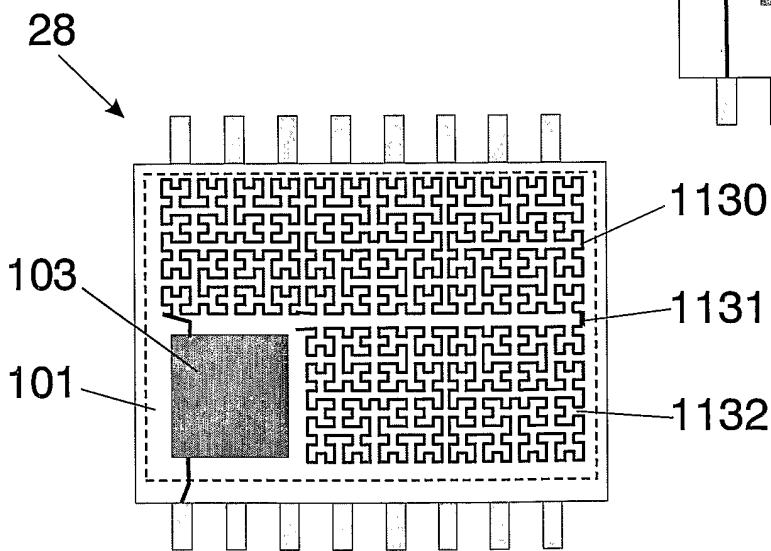


FIG. 11C

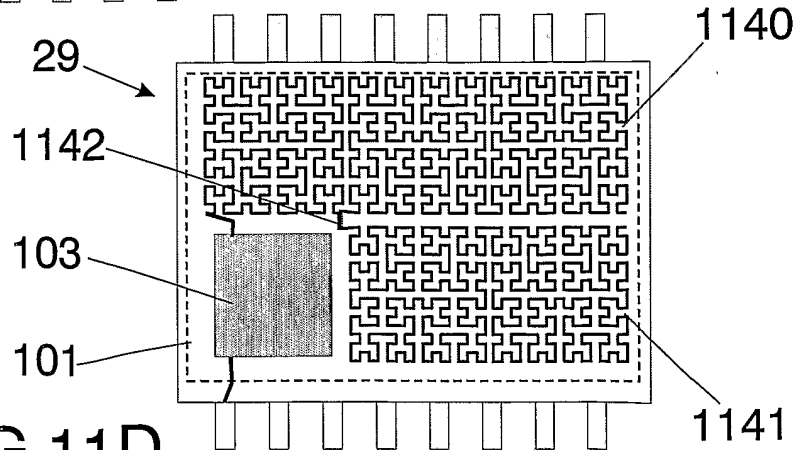


FIG. 11D

FIG. 11

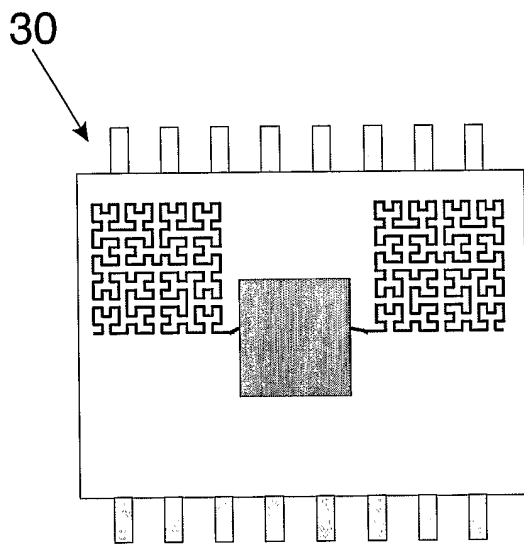


FIG. 12A

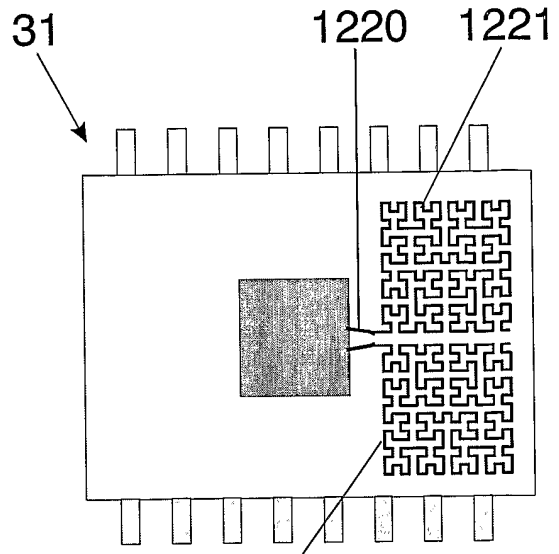


FIG. 12B

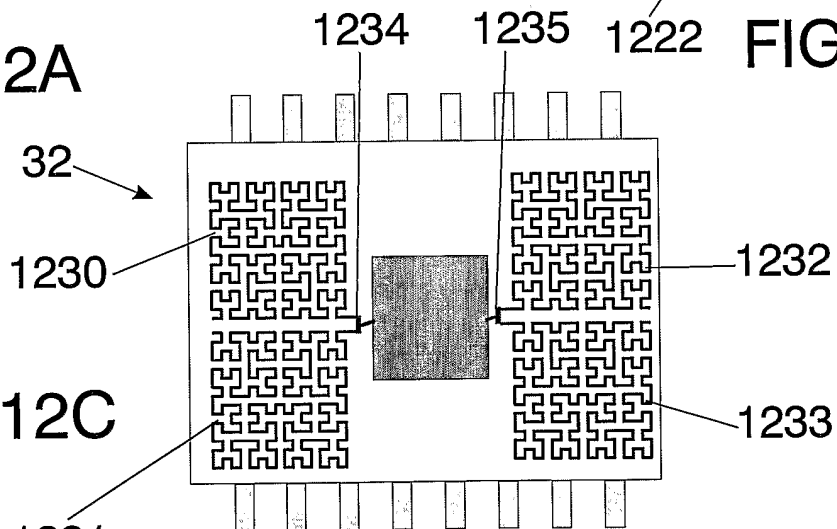


FIG. 12C

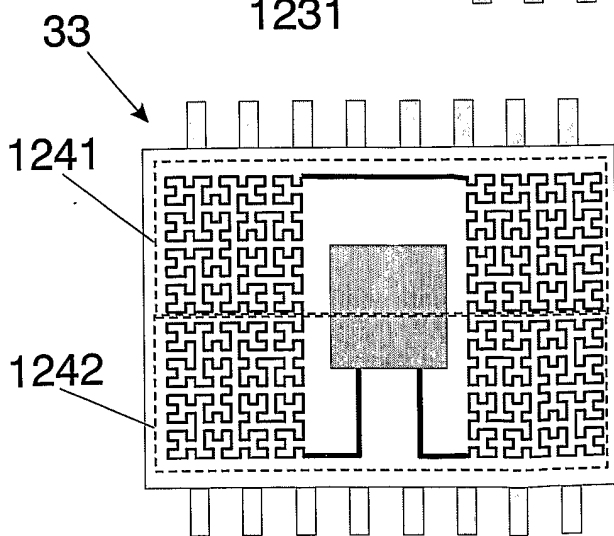


FIG. 12D

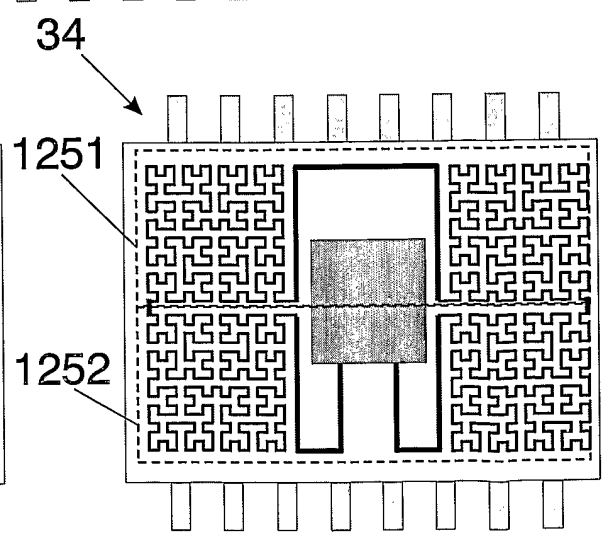
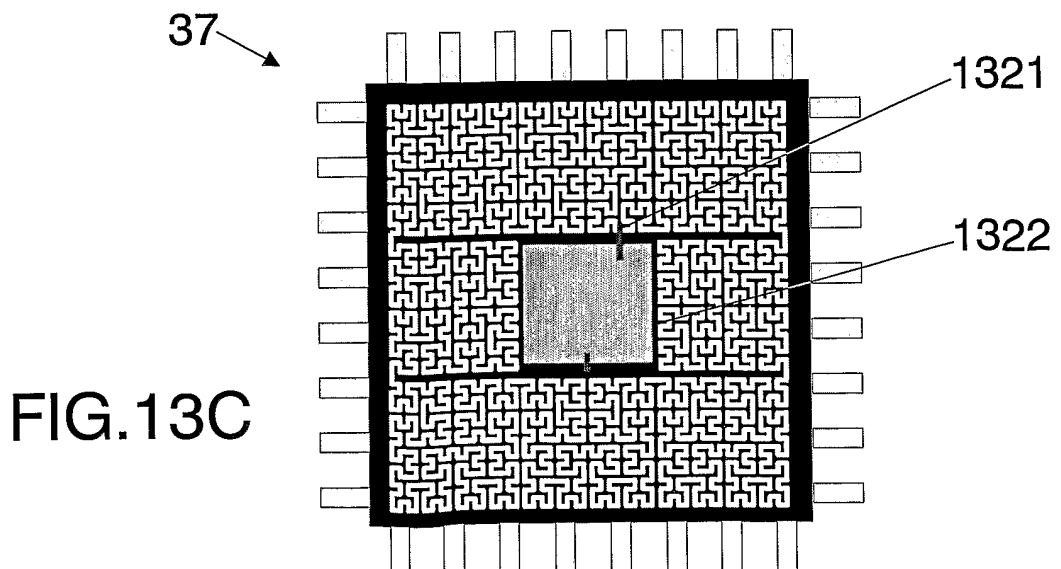
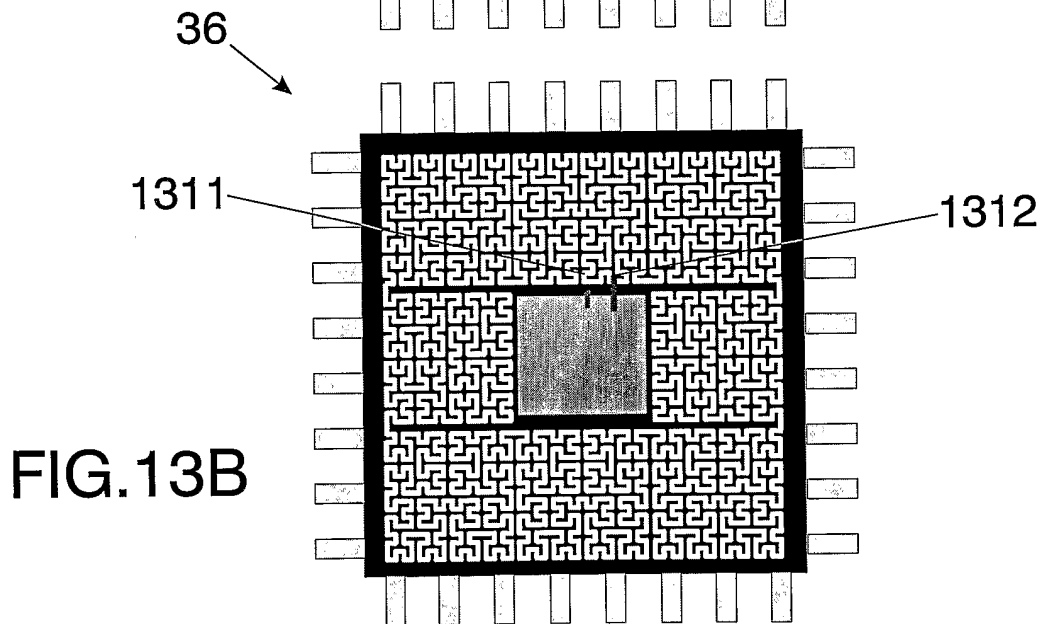
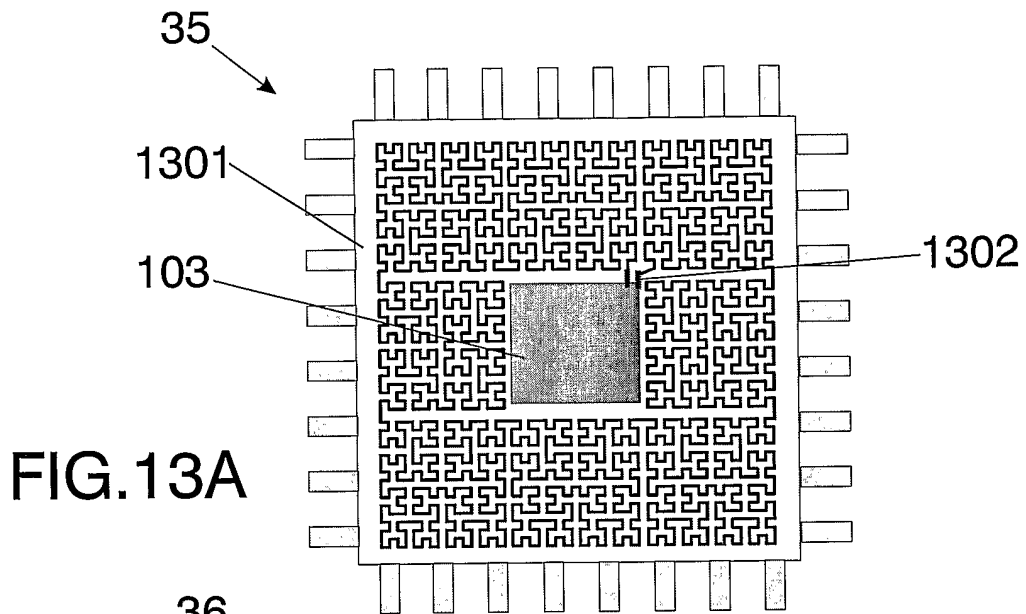


FIG. 12E

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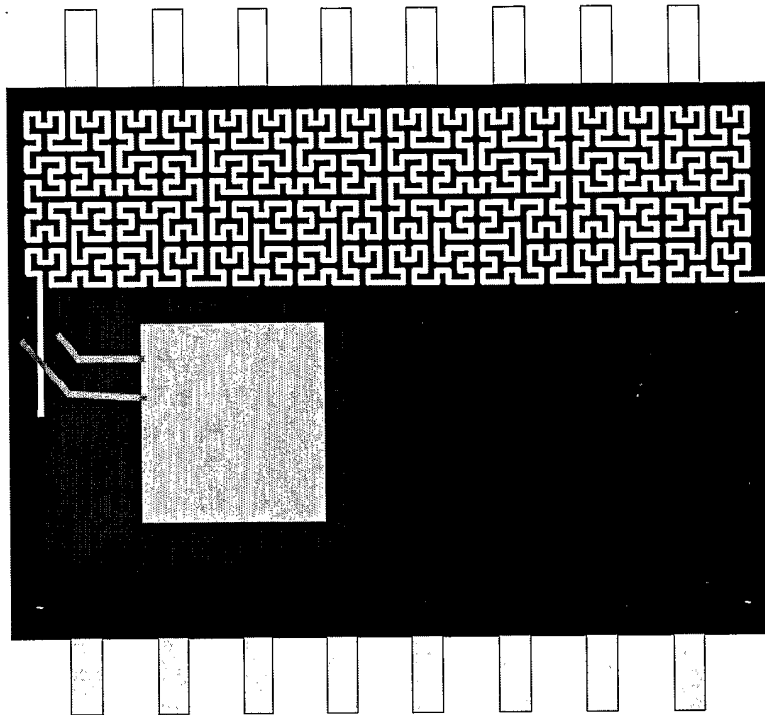


FIG. 14A

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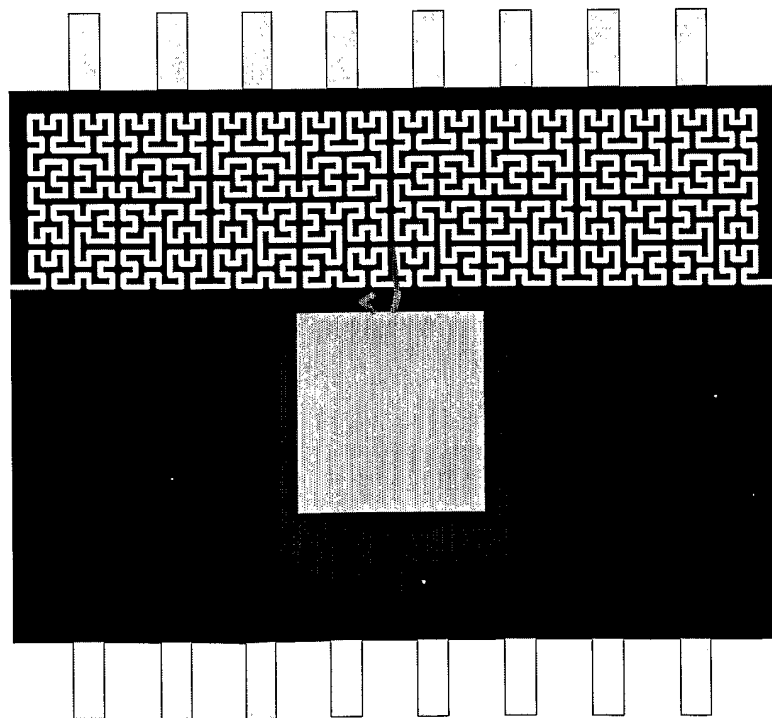


FIG. 14B

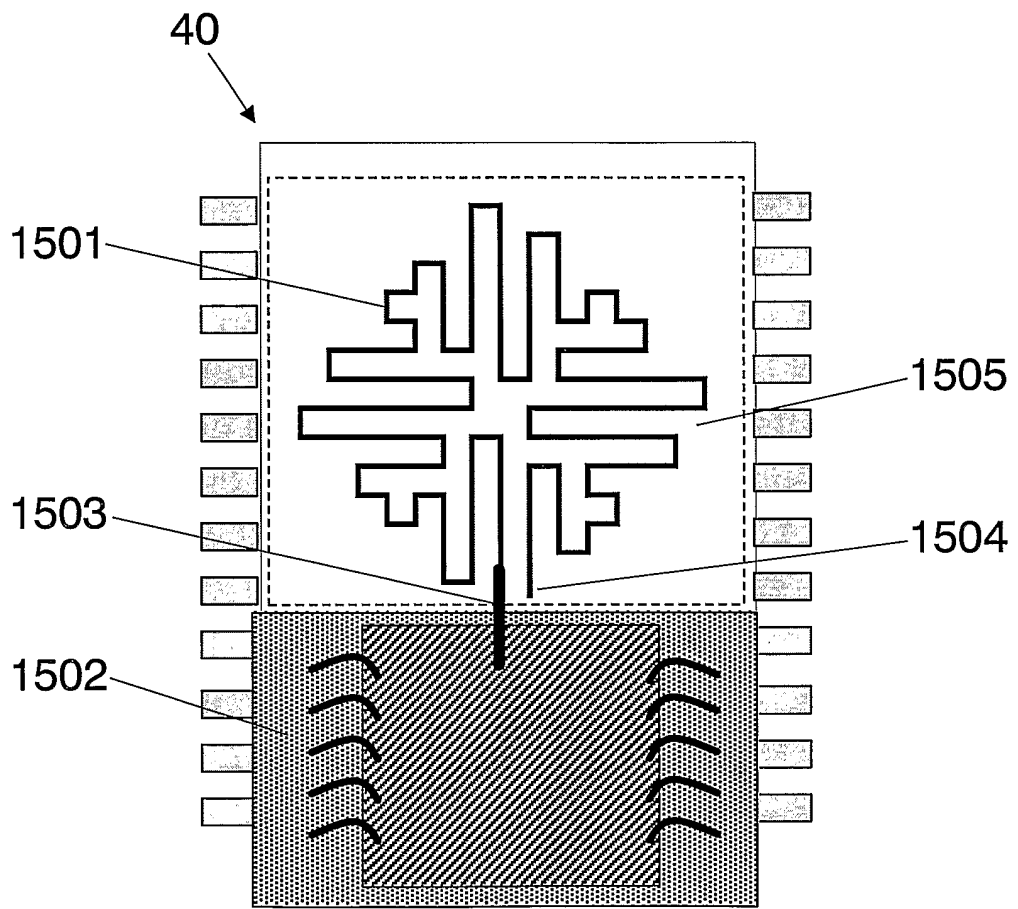


FIG.15

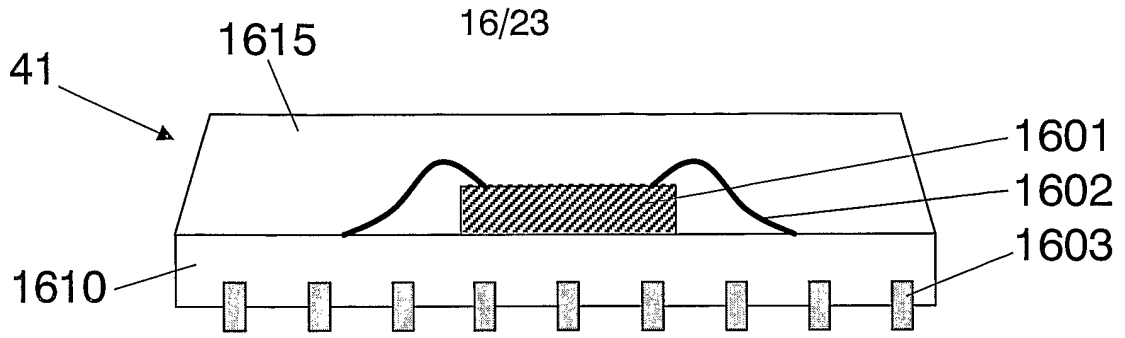


FIG. 16A

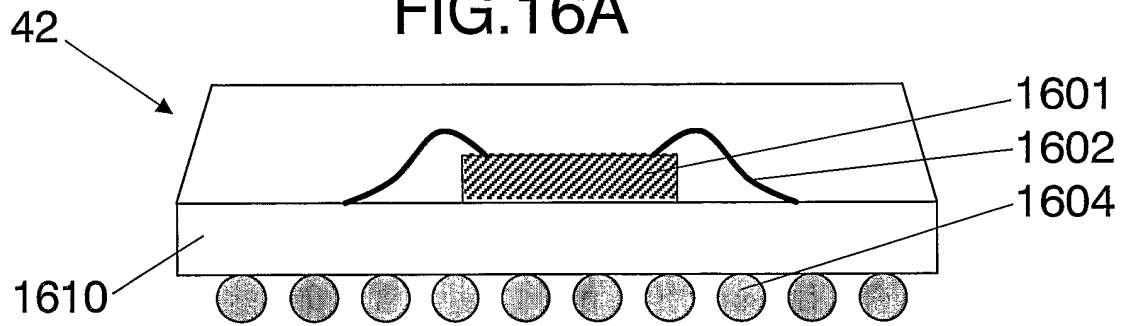


FIG. 16B

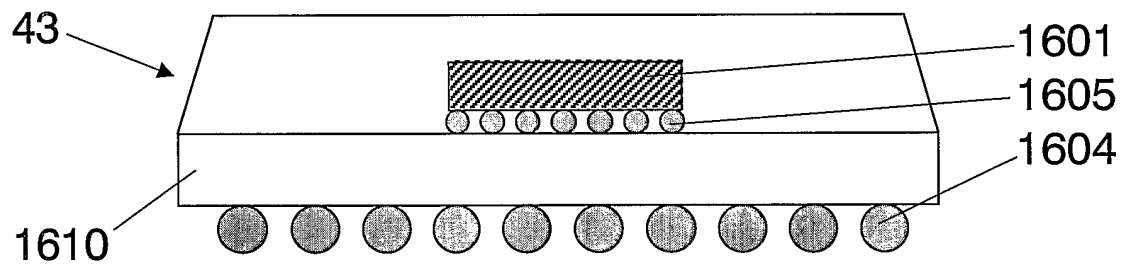


FIG. 16C

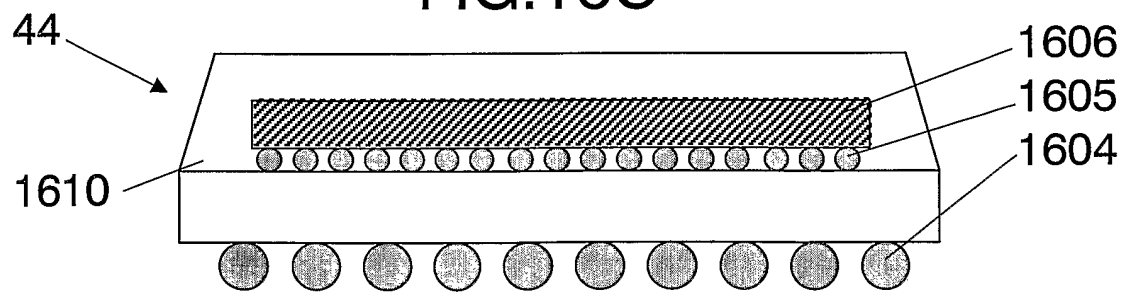


FIG. 16D

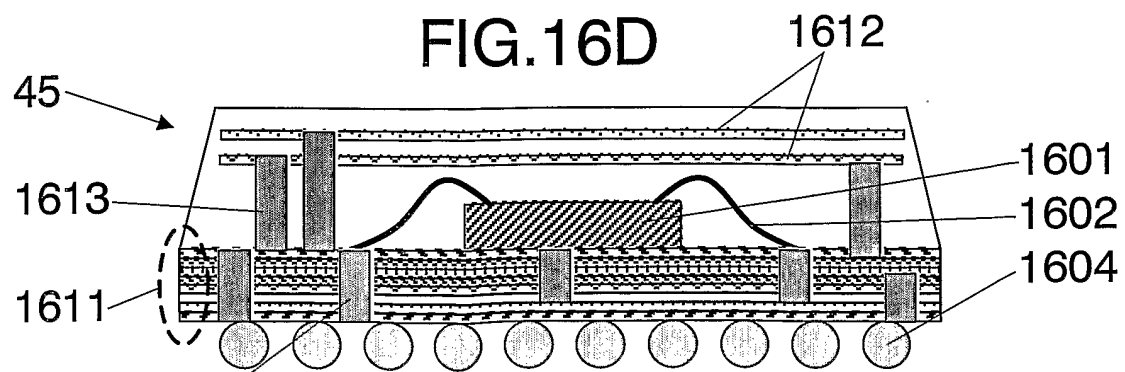


FIG. 16E

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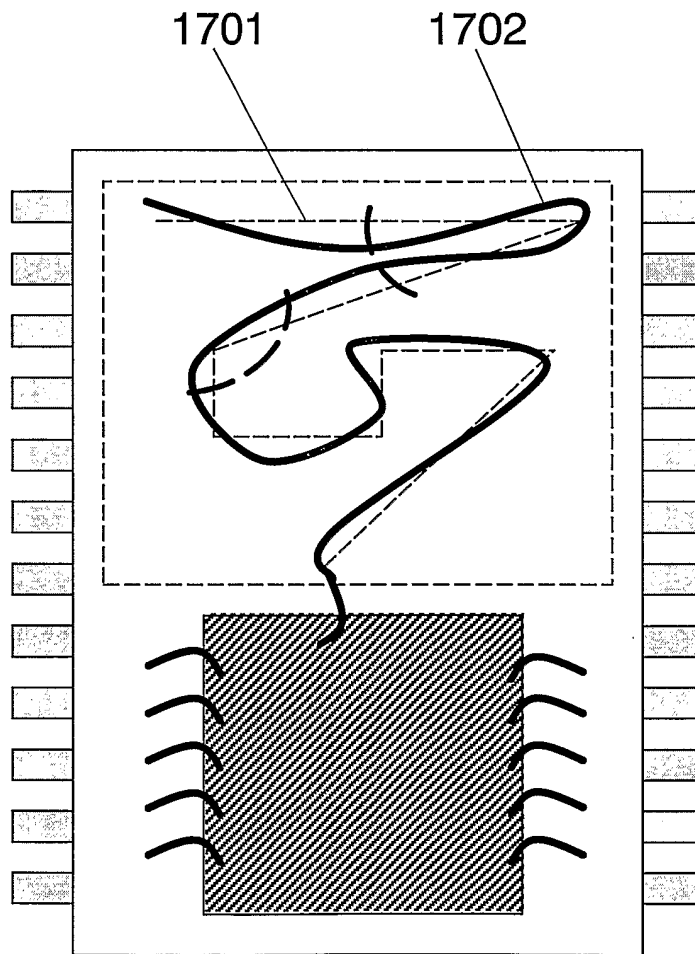


FIG.17

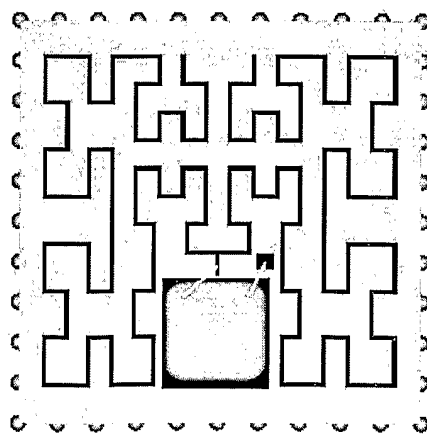
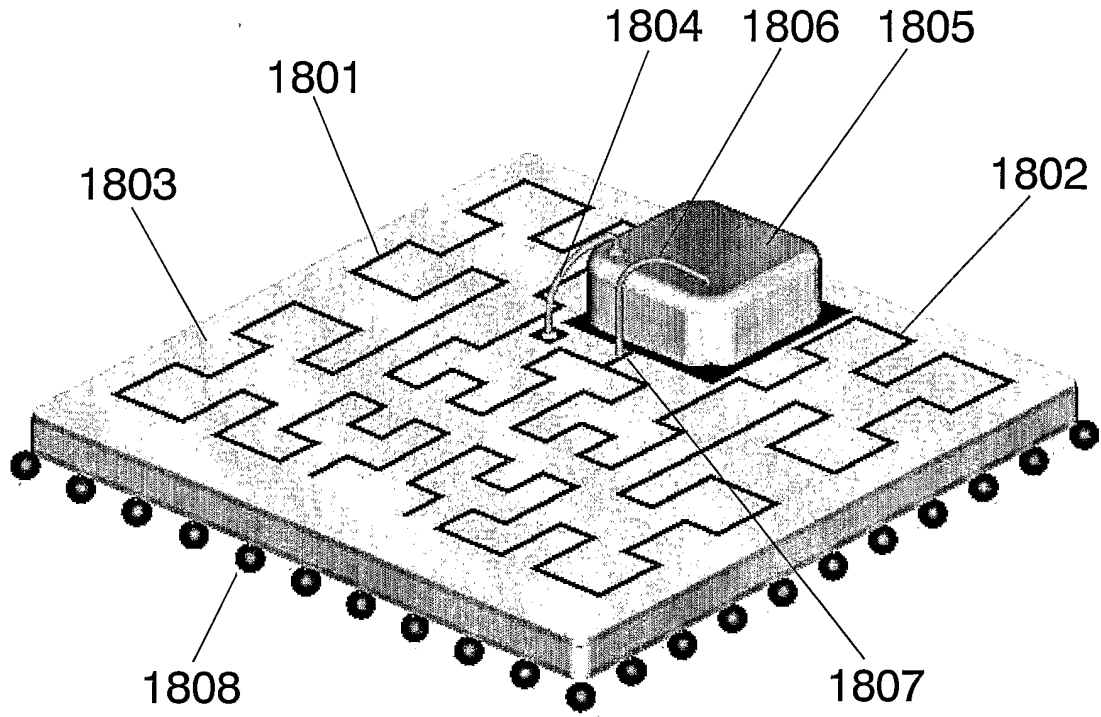


FIG.18

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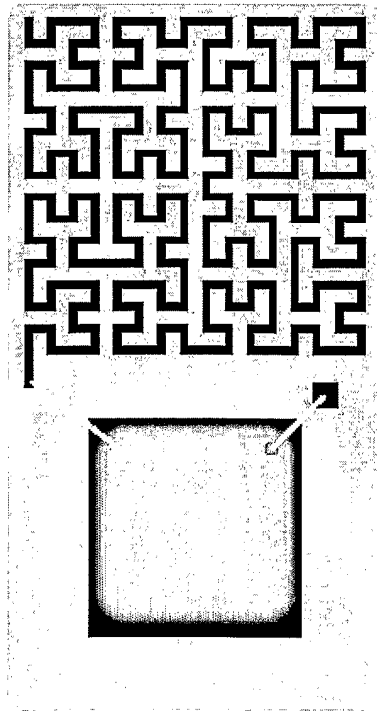
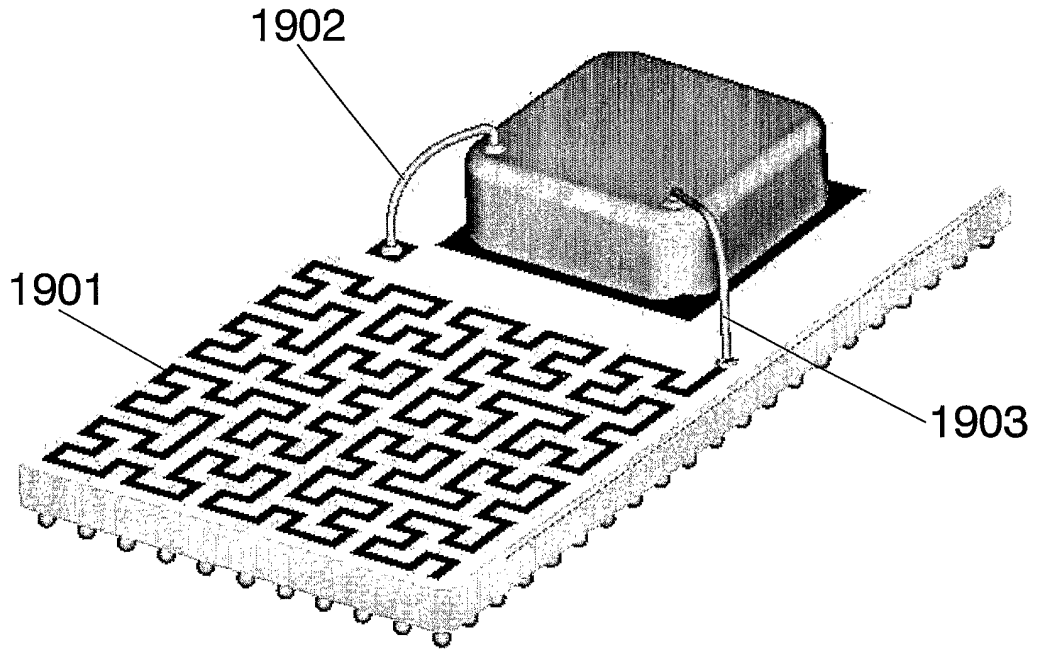


FIG.19

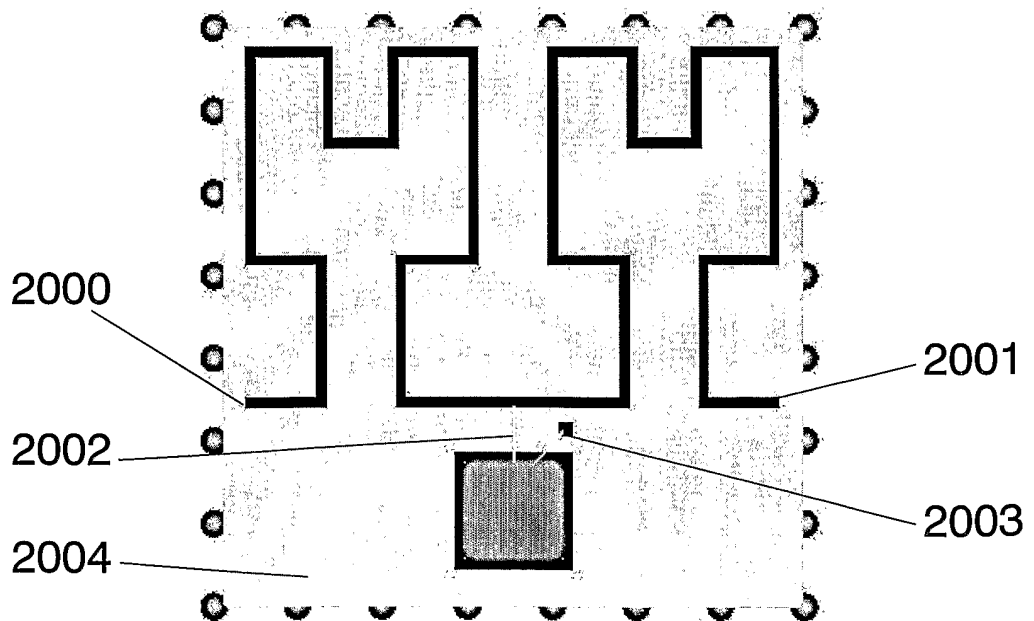
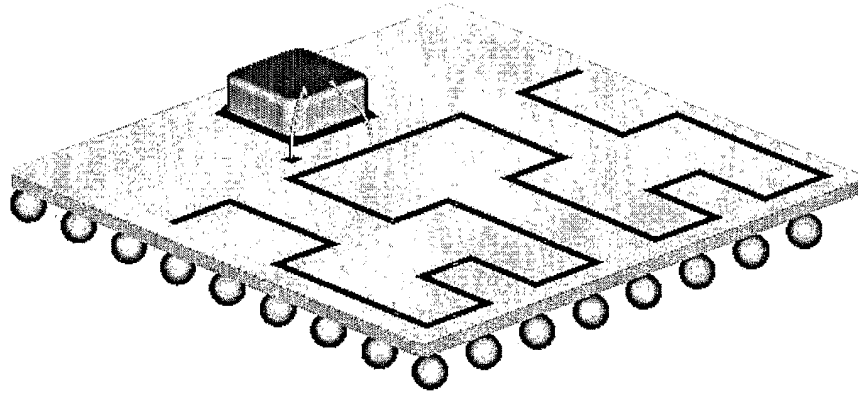


FIG.20

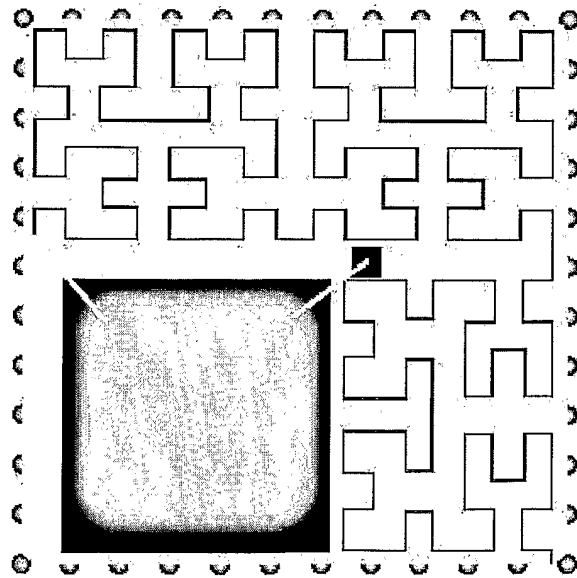
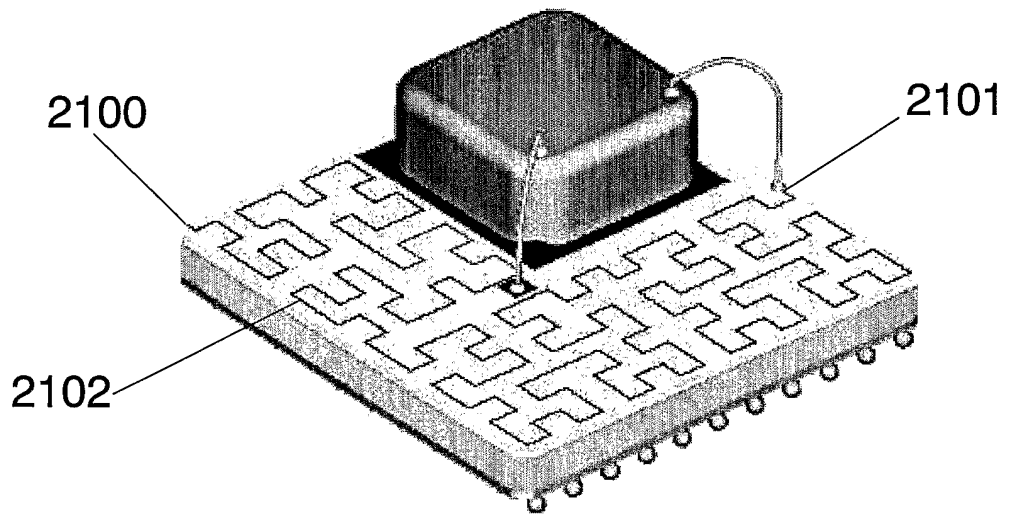


FIG.21

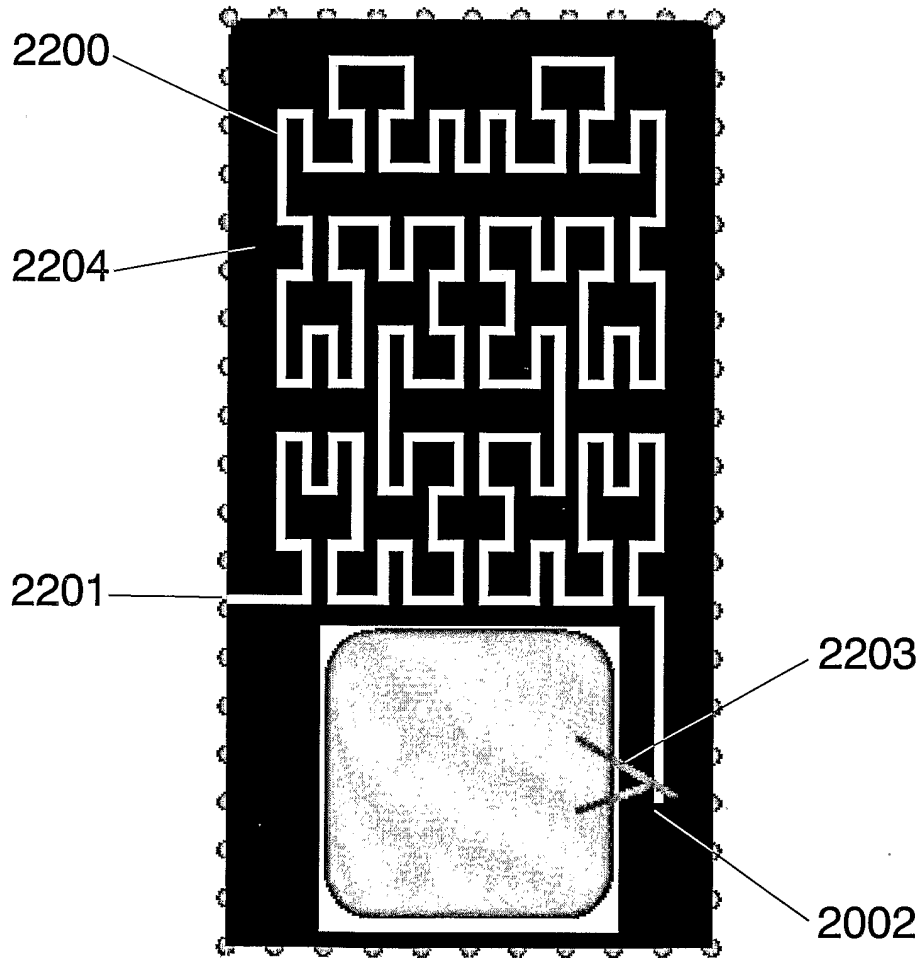


FIG. 22

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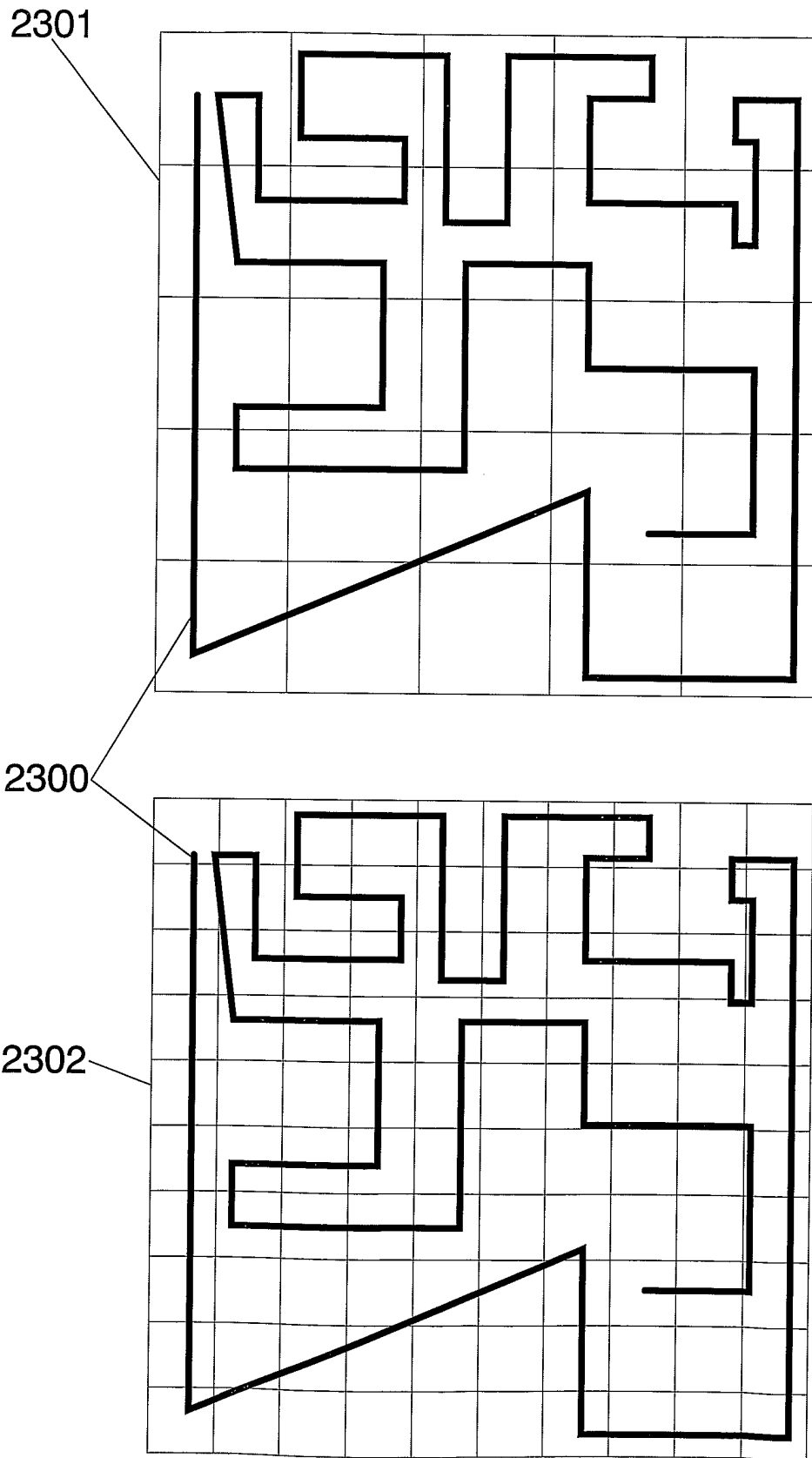


FIG.23

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 02/12427

A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H01Q1/38				
According to International Patent Classification (IPC) or to both national classification and IPC				
B. FIELDS SEARCHED				
Minimum documentation searched (classification system followed by classification symbols) IPC 7 H01Q				
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched				
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data, PAJ				
C. DOCUMENTS CONSIDERED TO BE RELEVANT				
Category ^o	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
Y	WO 01 54225 A (FRACTUS S A ;ANGUERA PROS JAIME (ES); PUENTE BALIARDA CARLES (ES);) 26 July 2001 (2001-07-26) page 1, line 6 -page 18, line 19; figures 1-25 abstract ---	1-60		
Y	EP 1 126 522 A (CIT ALCATEL) 22 August 2001 (2001-08-22) abstract; figures 1,2 column 1, line 3 -column 5, line 56 ---	1-60		
Y	US 6 320 543 B1 (MARUHASHI KENICHI ET AL) 20 November 2001 (2001-11-20) abstract; figures 1-8 column 1, line 6 -column 7, line 48 ---	1-60		
-/--				
<input checked="" type="checkbox"/> Further documents are listed in the continuation of box C.				
<input checked="" type="checkbox"/> Patent family members are listed in annex.				
^o Special categories of cited documents :				
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"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family			
Date of the actual completion of the international search <p style="text-align: center; font-weight: bold;">26 June 2003</p>	Date of mailing of the international search report <p style="text-align: center; font-weight: bold;">28. 07. 2003</p>			
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer <p style="text-align: center; font-weight: bold;">ROLAND LANDSTRÖM/MN</p>			

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 02/12427

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6 424 315 B1 (GLENN THOMAS P ET AL) 23 July 2002 (2002-07-23) abstract; figures 1A-6 column 1, line 35 -column 5, line 57 ---	1-60
Y	US 6 285 342 B1 (DUAN DAH-WEIH ET AL) 4 September 2001 (2001-09-04) column 1, line 10 -column 7, line 21 abstract; figures 2-11 -----	1-60

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 02/12427

Patent document cited in search report	A	Publication date	Patent family member(s)	Publication date
WO 0154225	A	26-07-2001	WO 0154225 A1 AU 3150000 A EP 1258054 A1	26-07-2001 31-07-2001 20-11-2002
EP 1126522	A	22-08-2001	EP 1126522 A1 CN 1369914 A JP 2001292026 A US 2001052645 A1	22-08-2001 18-09-2002 19-10-2001 20-12-2001
US 6320543	B1	20-11-2001	JP 2000278009 A	06-10-2000
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