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(71) Applicant
The Plessey Company plc

(Incorporated in the United Kingdom)

Vicarage Lane, Ilford, Essex, IG1 4AQ, United Kingdom

(72) Inventor
Ian Phillips

(74) Agent and/or Address for Service
F E Elliott
The Plessey Company plc, Intellectual Property Department, Vicarage Lane, Ilford, Essex, IG1 4AQ, United Kingdom

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(58) Field of search
UK CL (Edition J) **G4A AEF, H1K KGB KMA**
INT CL⁴ **G06F, G11C, H01L**

(54) **An integrated circuit having a patch array**

(57) The integrated circuit has at least one patch array (B) built into a spare space on the integrated circuit. The patch array is brought into use when faults are discovered during the manufacturing process to enable the manufacturing process to continue. The patch array consists of a gate array, and may be metalised into gate patterns to assist in testing.

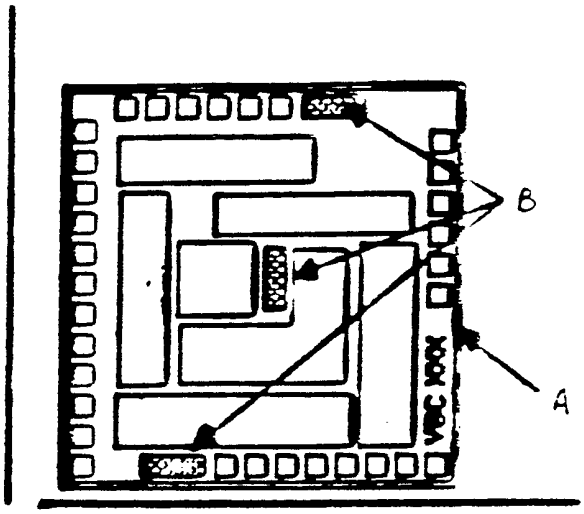

Fig. 1.

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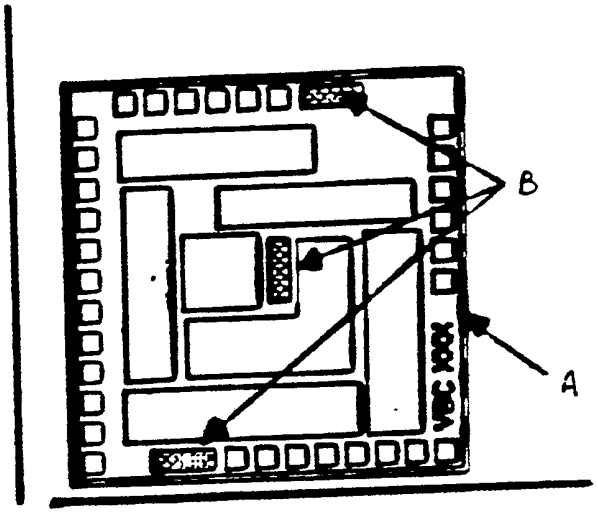

Fig. 1.

AN INTEGRATED CIRCUIT HAVING A PATCH ARRAY

The present invention relates to an integrated circuit having a patch array.

Full custom or cell based integrated circuits are more expensive to process for two main reasons.

There are only a limited set of masking stages involved in the characterisation of a gate array, typically three, whereas a cell/custom design involves a complete set of masks, typically thirteen.

The gate array base layers, known as mirrors, benefit in cost from the total volume of them produced, rather than the customers requirements only.

Custom integrated circuits, as gate arrays are inevitably wrong in some minor detail at the first, and often subsequent attempts are also wrong. For a custom circuit the cost of any change inevitably requires the generation of a complete set of new masks. The consequence for the gate array is the same, but, having only a limited mask set, the cost is lower and so is the cycle time.

Accordingly, an aim of the present invention is to provide integrated circuits having at least one patch array which is brought into use when a fault is discovered during the manufacturing process.

According to the present invention there is provided an integrated circuit having a plurality of base layers and a pluality of metalisaiton layers and at least one patch array built into a spare space on the integrated circuit, said patch array being brought into

use when a fault is discovered during the development process, to enable the manufacturing process to continue on the base layers.

An embodiment of the invention will now be described with reference to the accompanying drawing in which:

Figure 1 shows an integrated circuit layout having space-filling patch arrays.

The flexibility of a gate array is due to the layout of a field of usable transistors, plus a family of 'lay-on' metal patterns to characterise them into convenient logic functions. Thus any logic function can be implemented by changing only the metal layers. The cost however is silicon inefficiency and gate arrays are usually larger for a given function.

Most custom or cell based designs are very compact for most of their area, but there usually are 'gaps' where 'odd' shaped blocks fit together. As a percentage of the overall chip they are small, but then so too are the usual initial errors.

The invention is concerned with the provision in available spaces on any custom/cell designed integrated circuit A, small patches of gate array B. They would be connected to source and drain voltage supplies, or provision made to do so, and may initially be metalised into 'harmless' gate patterns, to aid testing.

Their use becomes apparent when a fault is discovered on the first and subsequent batches processed.

Because the patch arrays are little sections of gate array, a large set of 'cell' metalisation options are available, these can be used to provide the level of correction usually required at this stage of manufacture. Further, because the changes, which can be quite

extensive, only involve changing the metal layers, the cost and timescale becomes comparable with that of gate arrays.

Further, as customers purchasing the initial silicon are confident of getting working product from the 'base layers' of their initial design, they can at little risk commit larger initial batches, holding back a quantity at a 'pseudo-mirror' stage, thus in his turn gaining the cost benefit of scale.

The above description is not intended to limit the scope of the present invention, for example some designs involving small individual changes, such as address fields, could be designed intending to use the patch arrays for these variants.

CLAIMS

1. An integrated circuit having a plurality of base layers and a plurality of metalisation layers and at least one patch array built into a spare space on the integrated circuit, said patch array being brought into use when a fault is discovered during the manufacturing process, to enable the development process to continue on the base layers.

2. An integrated circuit as claimed in claim 1, wherein the patch array consists of a gate array.

3. An integrated circuit as claimed in claim 2, wherein the array is metalised into 'harmless' gate patterns to assist in testing.

4. An integrated circuit as claimed in claim 3, wherein the gate array is used to provide level correction.

5. An integrated circuit substantially as hereinbefore described.

6. An integrated circuit substantially as hereinbefore described with reference to Figure 1.

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