AU/PCT
4819 BKB

(CONVENTION. Company.) Form 8

COMMONWEALTH OF AUSTRALIA

Patents Act 1952-1969

DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT OR PATENT OF ADDITION

(1) Here insert (in full) Name of Company.

In support of the Convention Application made by(1) Telefonaktiebolaget LM Ericsson, S-126 25 STOCKHOLM SWEDEN a company organized under the laws of Sweden (hereinafter referred to as the applicant) for a Patent for an invention entitled:(2) METHOD FOR AVOIDING LATENT ERRORS IN A LOGIC NETWORK FOR MAJORITY SELECTION OF BINARY SIGNALS

(2) Here insert title of Invention.

(3) Here insert full Name and Address, of Company official authorized to make declaration.

We ~~I~~(3) Mr Tage Lövgren, Mickelsbergsvägen 134, S-126 63 HÄGERSTEN of SWEDEN and Mr Åke Stavling, Högbergsgatan 11, 2trp, S-116 45 STOCKHOLM SWEDEN

do solemnly and sincerely declare as follows:

1. We are ~~I am~~ authorised by the applicant for the patent to make this declaration on its behalf.

2. The basic application as defined by Section 141 of the Act was made in(4) Sweden on the 12th day of May 1989, by ELLEMTEL Utvecklings Aktiebolag ~~on the xxxx day of xxxxxx 19xxxx by xxxx~~

(4) Here insert basic Country or Countries followed by date or dates and basic Applicant or Applicants.

3.(5) Mr Tord Lennart Haulin, Hammarbygatan 52, S-753 24 UPPSALA SWEDEN

(5) Here insert (in full) Name and Address of Actual Inventor or Inventors.

is/~~are~~ the actual inventor of the invention and the facts upon which the applicant is entitled to make the application are as follow:

The applicant is the assignee of Mr Tord Lennart Haulin and the applicant has the consent of the said ELLEMTEL Utvecklings Aktiebolag

4. The basic application referred to in paragraph 2 of this Declaration was ~~not~~ the first application made in a Convention country in respect of the invention the subject of the application.

DECLARED at Stockholm, Sweden

this 20th day of November 1990

TELEFONAKTIEBOLAGET LM ERICSSON

(6) Signature.

(6) Åke Stavling Tage Lövgren

(12) PATENT ABRIDGMENT (11) Document No. AU-B-56740/90
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 622029

(54) Title
A METHOD FOR AVOIDING LATENT ERRORS IN A LOGIC NETWORK FOR MAJORITY SELECTION OF BINARY SIGNALS

International Patent Classification(s)
(51)[5] **G06F 011/18**

(21) Application No. : **56740/90** (22) Application Date : **03.05.90**

(87) PCT Publication Number : **WO90/13869**

(30) Priority Data

(31) Number	(32) Date	(33) Country
8901723	12.05.89	SE SWEDEN

(43) Publication Date : **29.11.90**

(44) Publication Date of Accepted Application : **26.03.92**

(71) Applicant(s)
TELEFONAKTIEBOLAGET LM ERICSSON

(72) Inventor(s)
TORD LENNART HAULIN

(74) Attorney or Agent
WATERMARK PATENT & TRADEMARK ATTORNEYS , Locked Bag 5, HAWTHORN VIC 3122

(56) Prior Art Documents
US 4583224
US 4555721
US 4468574

(57) Claim

1. A method for avoiding latent errors in a logic network for majority selection of binary signals in a triplicated system, in which the logic network includes a plurality of separate logic devices for performing logic operations, e.g. NAND- and/or NOR-operations, and in which each of the separate logic devices includes parallel-connected semi-conductor components, each of which receives a respective logic input signal, and further includes series-connected semi-conductor components, each of which receives a respective logic input signal, c h a r a c t e t e r i z e d by repeatedly switching each of said logic devices (21-24, 31-34, 71-74, 81-84, 91-94, 101-104) in a manner such that those semi-conductor components which were parallel-connected are switched so as to be series-connected and vice versa, whereby each of said logic devices will perform alternately logic operations which are dual correspondences of one another, e.g. NAND- and NOR-operations, with the aid of the same semi-conductor components (41-46, 51-56) in respective devices in both instances, and whereby, in practice, majority selection will be effected alternately with the aid of two mutually different logic networks, each being the dual correspondence of the other.

UPI DATE 29/11/90 APPLN. ID 56740 / 90

PCT AOJP DATE 10/01/91 PCT NUMBER PCT/SE90/00290

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G06F 11/18

A1

(11) International Publication Number: WO 90/13869

(43) International Publication Date: 15 November 1990 (15.11.90)

(21) International Application Number: PCT/SE90/00290

(22) International Filing Date: 3 May 1990 (03.05.90)

(30) Priority data:
8901723-0 12 May 1989 (12.05.89) SE

(71) Applicant: TELEFONAKTIEBOLAGET LM ERICSSON [SE/SE]; S-126 25 Stockholm (SE).

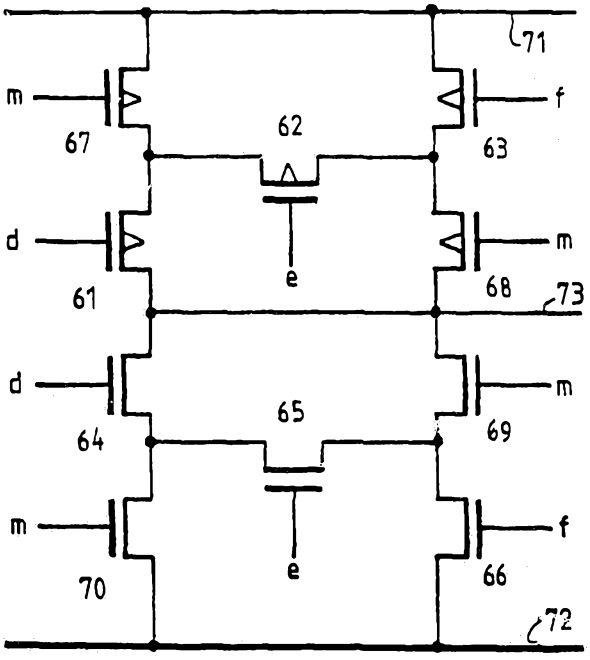
(72) Inventor: HAULIN, Tord, Lennart ; Hammarbygatan 52, S-753 24 Uppsala (SE).

(74) Agents: LÖVGREN, Tage et al.; Telefonaktiebolaget LM Ericsson, S-126 25 Stockholm (SE).

(81) Designated States: AU, BR, CA, FI, JP, KR, NO.

Published
With international search report.

(54) Title: A METHOD FOR AVOIDING LATENT ERRORS IN A LOGIC NETWORK FOR MAJORITY SELECTION OF BINARY SIGNALS



(57) Abstract

A method for avoiding latent errors in a logic network for majority selection of binary signals in a triplicated system. Errors which result from errors or faults in one of two or more parallel-connected transistors of one or more separate logic devices included in the logic network are avoided by repeatedly switching each of the separate logic devices in a manner such that transistors which were parallel-connected become series-connected, and vice versa. As a result, these devices will perform alternately logic operations which are the dual correspondence of one another, e.g. NAND- and NOR-operations with the aid of the same transistors (61-66) in both instances. Thus, in practice, majority selection will be performed alternately with two mutually different logic networks, which are the dual correspondence of each other.

A METHOD FOR AVOIDING LATENT ERRORS IN A LOGIC NETWORK FOR MAJORITY SELECTION OF BINARY SIGNALS

TECHNICAL FIELD

The invention relates to a method for avoiding latent errors in a logic network for majority selection of binary signals in a tripled system, in which the logic network includes a plurality of separate logic devices for carrying-out logic operations, for instance NAND- and/or NOR-operations, and in which each of the separate logic devices includes parallel-connected semi-conductor components, each of which receives a respective logic input signal, and also series-connected semi-conductor components, each of which receives a respective logic input signal.

BACKGROUND ART

Triplicated digital systems are sometimes used in, for instance, telecommunication systems for safety reasons. In this respect, there are used three parallel branches in which identical operations are carried out. Downstream of given function blocks incorporated in said branches, a majority selection is made between mutually corresponding output signals from the three function blocks. Consequently, the malfunction of one of said three function blocks will have no significance. The system is thus tolerant to single errors and to multiple errors which do not overlap one another in time and space.

In order for a faulty or erroneous system function to be discovered, it is necessary to use the function concerned. System functions which remain unused over long periods of time can be encumbered with one or several latent errors which are not discovered and reported. Majority selection functions are additionally prone to this drawback, since this function is not tested until an error has occurred. In normal cases, i.e. when the function blocks are error-free, the output signals from the function blocks which correspond to one another in the three branches are equal. Consequently, latent errors may be present in

the devices which carry out majority selection, these errors remaining undiscovered for as long as the function blocks are error-free and produce mutually identical output signals.

The devices which carry out majority selection comprise, for instance, logic networks composed of separate logic devices, e.g. NAND and/or NOR-gates, which contain, inter alia, two or more parallel-connected and series-connected transistors. A fault in such a transistor will normally remain undiscovered until a particular type of error occurs in a separate function block, which may not occur for a very long time, wherewith overlapping errors resulting in system malfunction may occur.

DISCLOSURE OF THE INVENTION

The problem of latent errors due to errors or faults in one of two or more series-connected or parallel-connected transistors in the separate logic devices of the logic networks for majority selection is avoided by repetitive switching in each of said logic devices. Switching is effected such that transistors which were parallel-connected become series-connected, and vice versa. Consequently, the logic devices will carry-out alternately logic operations which have respective dual correspondence, e.g. NAND- and NOR-operations, with the aid of the same transistors in both cases. In this way, a switch is made between two logic networks which are the dual correspondence of one another, and in practice the majority selection will be effected alternately with two mutually different logic networks. Because transistors which were connected in parallel become connected in series, and vice versa, an interruption or a short circuit in one of the transistors or its control line will be discovered when the transistor is connected in series instead of in parallel, or vice versa.

The invention is characterized by the features set forth in the following Claims.

BRIEF DESCRIPTION OF DRAWINGS

The invention will now be described in more detail with reference to the accompanying drawings, in which Figure 1 illustrates part of a triplicated system; Figures 2 and 3 illustrate two different exemplifying embodiments of a device for majority selection incorporated in the system shown in Figure 1; Figure 4 illustrates an example of realizing a NAND-gate included in the device illustrated in Figure 2; Figure 5 illustrates an example of realizing a NOR-gate included in the device illustrated in Figure 2; Figure 6 illustrates an example of a controllable logic device which can be included in a device for majority selection; and Figures 7-10 illustrates four further examples of a device for majority selection.

BEST MODES OF CARRYING OUT THE INVENTION

Figure 1 illustrates a part of a triplicated system. The reference signs 11a-11c identify three mutually identical function blocks, each located in a respective branch of three mutually identical branches. Each function block may, for instance, consist of a circuit board having a plurality of components, although, as will be understood, the block may consist of units which are larger or smaller than a circuit board. In normal circumstances, each of the blocks 11a-11c will receive mutually similar input signals and produce mutually similar output signals, a-c. Each of the output signals a-c is applied to a respective one of three devices 12a-12c for majority selection. Each of these devices produces an output signal equal to the value occurring on the majority, i.e. at least two, of the outputs from the blocks 11a-11c. Consequently, the output signals from the majority selection devices 12a-12c will be mutually similar, even if one of the blocks 11a-11c is faulty. The output signals from the majority selection devices 12a-12c is applied to a respective one of three new function blocks 13a-13c, the output signals of which are, in turn, applied to three new majority selection devices 14a-14c. It will be

understood that the number of function blocks between two majority selection devices can vary.

It should be mentioned that a report to the effect that an error has occurred in one of the function blocks can be readily reported automatically, by comparing each of the output signals from the three function blocks of mutual correspondence with the output signal from the device which has carried out the majority selection between the signals. This comparison can be effected, for instance, with the aid of EXOR-gates. The error, however, may have occurred in the majority selection device concerned.

Figure 2 illustrates a first example of realizing a majority selection device. This device consists of three NAND-gates 21-23, which obtain the signals a and b, b and c, and a and c respectively on the inputs thereof. Thus, with these references, the majority selection device corresponds to one of the devices 12a-12c in Figure 1. The gates 21-23 produce output signals d-f, which are applied to a NAND-gate 24, which in turn produces an output signal g.

Figure 3 illustrates another example of realizing a majority selection device. In this case, the NAND-gates in the device illustrated in Figure 2 have been replaced with NOR-gates 31-34. The output signals produced by said gates are referenced h-k.

It can be mentioned that the logic networks shown in Figures 2 and 3 are the dual correspondence of one another.

It will be seen from the following truth table that both the output signals g and k coincide with the majority of the input signals a-c for different values thereof.

a b c	d e f	g	h i j	k
000	111	0	111	0
001	111	0	100	0
010	111	0	001	0
011	101	1	000	1
100	111	0	010	0
101	110	1	000	1
110	011	1	000	1
111	000	1	000	1

Figure 4 illustrates an exemplifying embodiment of a NAND-gate. This gate corresponds to the gate 24 in Figure 2 and thus has three inputs, which receive the signals d-f. The gate includes three parallel-connected P-type CMOS-transistors 41-43 and three series-connected N-type CMOS-transistors 44-46. A high and a low supply-voltage is applied to conductors 47 and 48 respectively. The gate output consists of a conductor. Each of the P-transistors 41-43 conducts for low control-voltage, i.e. for a zero, whereas each of the N-transistors 44-46 conduct for high control-voltage, i.e. for a one. Consequently, the output signal will be low, i.e. zero, only when all input signals d-f are high, i.e. ones. In other cases, the output signal will be high, i.e. a one. This is in agreement with a logic NAND-condition.

Each of the gates 21-23, which have only two inputs, can also be realized as the gate shown in Figure 4, although with the modification that two inputs are connected together.

As before mentioned, the latent error can be present in a majority selection device of said kind, due to the fact that one or two of the parallel-connected transistors are faulty and that the fault has not been discovered. Provided that the input signals are the same, a permanent break-down in one or two of the parallel-connected transistors will go undiscovered. An error or fault which occurs as a permanent short-circuit in one of the series-connected transistors will also go undiscovered. The input signals to a majority selection device will be mutually the same when the

three mutually corresponding function blocks connected to the input side of the majority selection device are error free and when the nearest preceding majority selection device is also error free.

As will be understood from the aforegoing, the majority selection can also be effected with a NOR-gate network according to Figure 3. Figure 5 illustrates an embodiment of a NOR-gate. This gate corresponds to the gate 34 of the Figure 3 embodiment and has three inputs. The gate is constructed of transistors similar to those of the NAND-gate 24 according to Figure 4. The transistors connected in parallel in the Figure 4 embodiment are, however, connected in series in the Figure 5 embodiment and are referenced 51-53, whereas the transistors connected in series in Figure 4 are connected in parallel in Figure 5 and are referenced 54-56. High and low supply-voltage and the output of the gate are connected to conductors 57-59. When all input signals h-j have the value zero, each of the series-connected P-transistors 51-53 become conductive and none of the parallel-connected N-transistors 54-56. The gate output-signal will then be a one. In other cases, the output signal is a zero, which agrees with a logic NOR-condition.

This gate may also have a latent fault, due to the fact that one or two of the parallel-connected or series-connected transistors is faulty, without this fault being detected while the input signals are mutually the same.

It can be mentioned that NAND- and NOR-functions are the dual correspondence of one another.

Figure 6 illustrates an example of a controllable logic device which can be included in a majority selection device. The logic device includes ten CMOS transistors, of which five, 61-63 and 67-68, are P-type transistors, and five, 64-66 and 69-70, are N-type transistors. The transistors 61-63 and 64-66 receive input signals d-f which correspond to the same signals in the NAND-gate 24 according to Figures 2 and 4. The transistors 67-70 receive a control signal m, which alternates between a zero and a one. High

supply-voltage, low-supply voltage and the output of the logic device are applied to conductors 71, 72 and 73 respectively.

The transistors 67-68 are conductive when the control signal m is a zero, under which condition the transistors 69-70 will be non-conductive. Consequently, in practice, the transistors 61-63 will be connected in parallel between the high supply-voltage and the output 73. The lower half of the Figure is, in practice, reduced at the same time to a series-connection of the transistor 64-66 between the output and the low supply-voltage. The logic device thus corresponds in this case to the NAND-gate illustrated in Figure 4.

When the control signal m is a one, the transistors 67-68 will, instead, be non-conducting, whereas the transistors 69-70 are conducting. In this way, the upper half of the Figure is reduced to a series-connection of the transistors 61-63, whereas the transistors 64-66 are connected in parallel. Thus, the logic device will in this case correspond to the NOR-gate shown in Figure 5.

By permitting the control signal m to assume the values zero and one alternately, the controllable logic device according to Figure 6 will function alternately as a NAND-gate and as a NOR-gate. Four controllable logic devices of this kind can be used as separate NAND-gates in a majority selection device according to Figure 2 or 3. The gates which have only two inputs are therewith realized advantageously as a three-input gate, although with two inputs connected together. By using four controllable logic devices of the kind illustrated as a majority selection device according to Figure 2 or 3, majority selection will at times be carried out with four NAND-gates and at times with four NOR-gates. Thus, in practice, majority selection is effected alternately with two mutually different logic networks, each of which is the dual correspondence of the other. Since the same transistors are used in both instances and since the transistors which were parallel-connected in the one instance are series-connected in the other instance, and vice versa, a fault in one of the transistors or the connections thereto will no longer be latent. This is explained by

the fact that any interruption in one of the transistors will be discovered when it is switched to a series-connection, while any short circuit will be discovered when it is switched to a parallel-connection. Naturally, some form of arrangement is required for reporting the fault or error automatically, for example an arrangement which includes EXOR-gates in accordance with the aforegoing.

When the controllable logic device according to Figure 6 functions as a NAND-gate, current will pass through respective transistors 62 and 65 in a first direction, whereas when the logic device functions as a NOR-gate, the currents will, instead, pass in the opposite direction. This makes CMOS-transistors suitable for inclusion in a device of this kind. Such transistors namely have good current conductivity in both directions.

The majority selection devices need not necessarily be comprised of solely NAND-gates or solely NOR-gates. A study of the majority selection device illustrated in Figure 2 will show that the output signal g with logic algebra can be designated g = ((a x b)' x (b x c)' x (a x c)')', where the primes signify inversion. The expression can be converted, with the aid of de Morgan's theorems, to g = a x b + b x c + a x c, which corresponds to a logic network of the kind illustrated in Figure 7. This network comprises three AND-gates 71-73 and one OR-gate 74.

In practice, NAND and NOR-gates are preferred to AND- OR-gates respectively. Consequently, a network according to Figure 7 is often realized in practice instead of a network according to Figure 8. In this network, the AND-gates 71-73 of the Figure 7 embodiment have been replaced with NAND-gates 81-83, each having a respective inverter 85-87, and the OR-gate 74 has been replaced with a NOR-gate 84, having an inverter 88. Each of the gates 81-84 can consist of a controllable logic device according to Figure 6. In this case, the control signal m applied to the logic devices which are intended to function as NAND-gates shall be a zero, whereas the control signal applied to the logic device intended to function as a NOR-gate shall be a one.

By simultaneously switching the control signals from zero to one, and vice versa, there is obtained a logic network which is the dual correspondence of the network illustrated in Figure 8. One such dual network is illustrated in Figure 9. Compared with the Figure 8 embodiment, the NAND-gates 81-83 have thus been replaced with NOR-gates 91-93 and the NOR-gate 84 has been replaced with a NAND-gate 94. The output signal of the network is referenced n. It will be seen that each NOR-gate, e.g. 91, with its inverter, e.g. 85, can be replaced by an OR-gate, and that the NAND-gate 94, with its inverter 88, can be replaced with an AND-gate. This corresponds to a logic network illustrated in Figure 10, where the gates are referenced 101-104. The output signal can be designated:
$n = (a + b) \times (b + c) \times (a + c)$, which with the aid of de Morgan's theorems can be converted to $n = ((a + b)' + (b + c)' + (a + c)')'$. This expression coincides with the expression obtained with a logic network having four NOR-gates in accordance with Figure 3, which has the same function as the logic network according to Figure 2. Thus, the majority selection function can also be carried out with logic networks according to Figures 8 and 9, for instance, each of these logic networks consisting of both NAND and NOR gates.

The logic networks illustrated in Figures 7 and 10 are also the dual correspondence of one another.

When the transistors 61-63 of the logic device according to Figure 6 are N-type transistors instead of P-type transistors, and when the transistors 64-66 are P-type transistors instead of N-type transistors, said device will effect logic AND- or OR-operations instead of NAND- or NOR-operations. More specifically, the logic device will function as an OR-gate when the transistors 61-63 are connected in parallel and the transistors 64-66 are connected in series and as an AND-gate in the converse case. This enables the logic device to be used to switch between the AND-OR-networks according to Figures 7 and 10. These types of network, however, must be provided with amplifiers in order to be used in practice.

As will be understood, the logic device illustrated in Figure 6 can be modified to include two plus two transistors having control electrodes connected to the inputs of the logic device. In this way, there is obtained logic gates having two inputs instead of three. As will be understood from the aforegoing, however, this is not necessary, since two of the three inputs can, instead, be mutually connected with the intention of obtaining a gate having two inputs.

The gates and the logic device according to Figures 4-6 are made up of CMOS-transistors. However, other semiconductor components may be used instead of CMOS-transistors.

C L A I M S

1. A method for avoiding latent errors in a logic network for majority selection of binary signals in a triplicated system, in which the logic network includes a plurality of separate logic devices for performing logic operations, e.g. NAND- and/or NOR-operations, and in which each of the separate logic devices includes parallel-connected semi-conductor components, each of which receives a respective logic input signal, and further includes series-connected semi-conductor components, each of which receives a respective logic input signal, c h a r a c t e r i z e d by repeatedly switching each of said logic devices (21-24, 31-34, 71-74, 81-84, 91-94, 101-104) in a manner such that those semi-conductor components which were parallel-connected are switched so as to be series-connected and vice versa, whereby each of said logic devices will perform alternately logic operations which are dual correspondences of one another, e.g. NAND- and NOR-operations, with the aid of the same semi-conductor components (41-46, 51-56) in respective devices in both instances, and whereby, in practice, majority selection will be effected alternately with the aid of two mutually different logic networks, each being the dual correspondence of the other.

2. A method according to Claim 1, c h a r a c t e r i z e d by effecting majority selection alternately with four logic NAND-devices (21-24) and four logic NOR-devices (31-34).

3. A method according to Claim 1, c h a r a c t e r i z e d by effecting said majority selection in the one instance with three logic NAND-devices (81-83), each having a respective following inverter (85-87) and a logic NOR-device (85) with a following inverter (88), and in the second instance with three logic NOR-devices (91-93), each having a respective following inverter (85-87), and a logic NAND-device (94) with a following inverter (88).

4. A method according to Claim 1, c h a r a c t e r i z e d by effecting said majority selection alternately with the aid, in the

one instance, of three logic AND-devices (71-73) and a logic OR-device (74), and in the other instance with the aid of three logic OR-devices (101-103) and a logic AND-device (104).

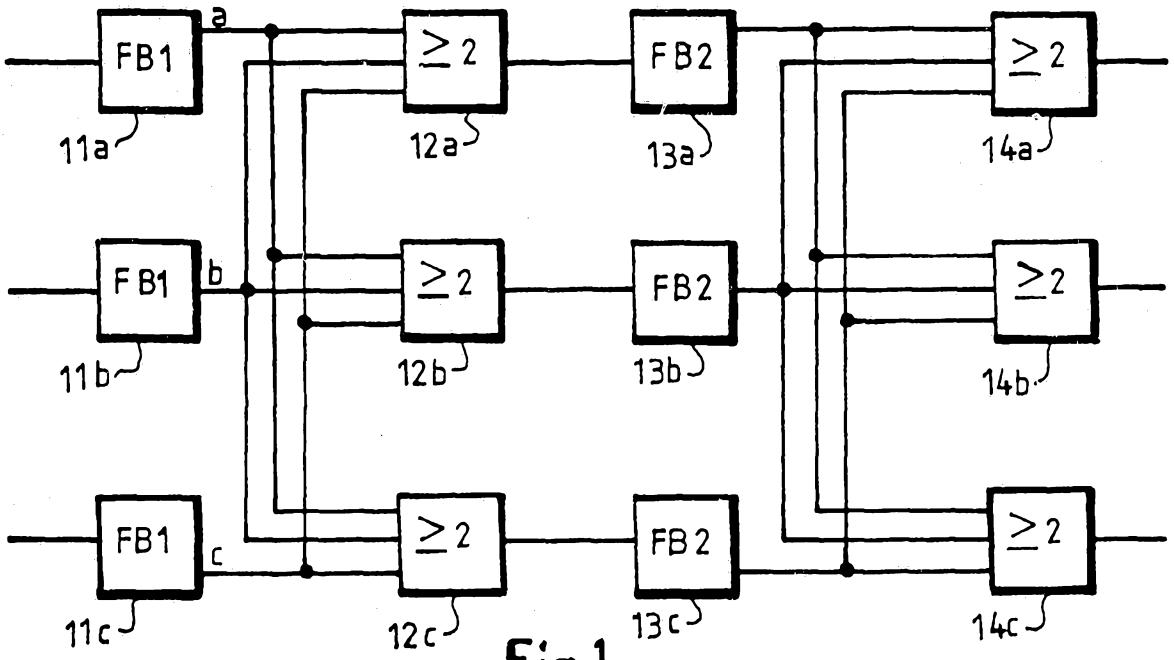

FB1
a
≥2
FB2
≥2
11a
12a
13a
14a
FB1
b
≥2
FB2
≥2
11b
12b
13b
14b
FB1
c
≥2
FB2
≥2
11c
12c
13c
14c

Fig.1

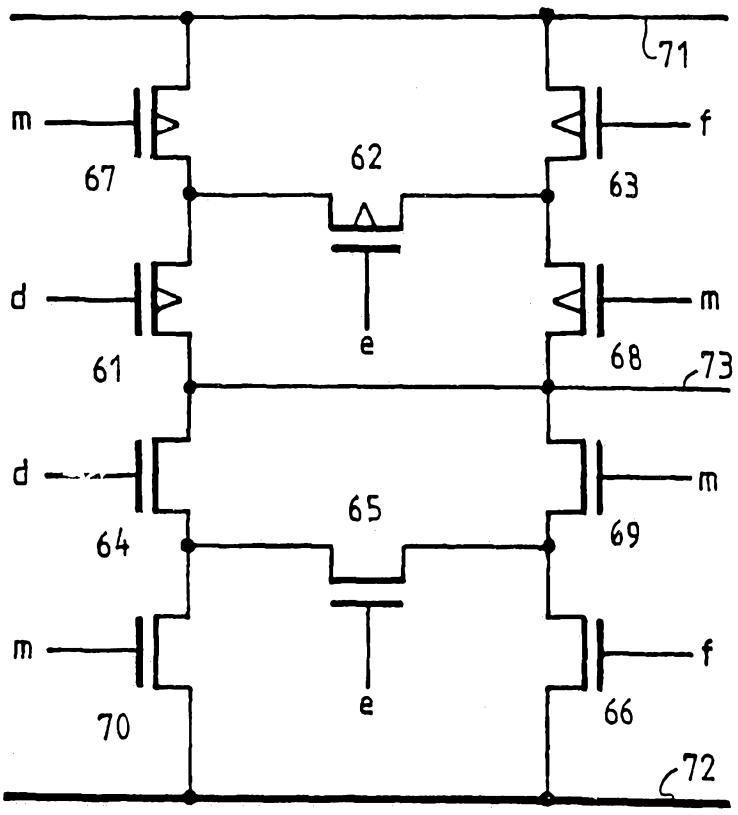

71
m
f
67
62
63
d
m
e
61
68
73
d
m
65
64
69
m
f
e
70
66
72

Fig.6

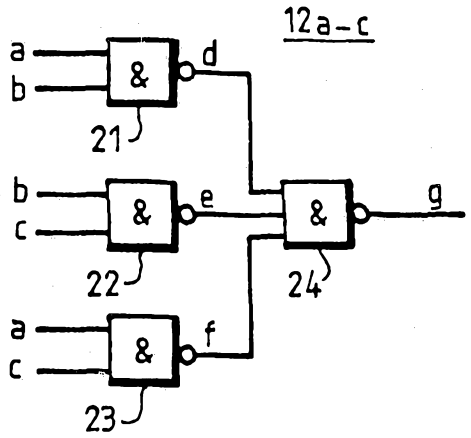


Fig.2

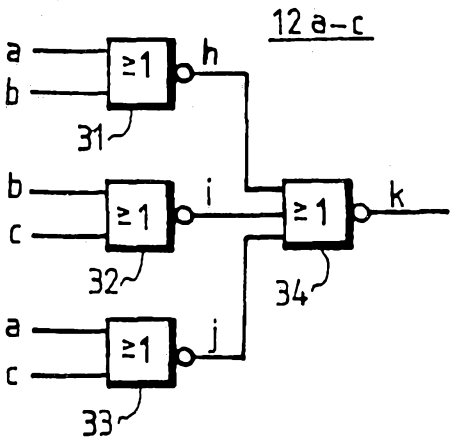


Fig.3

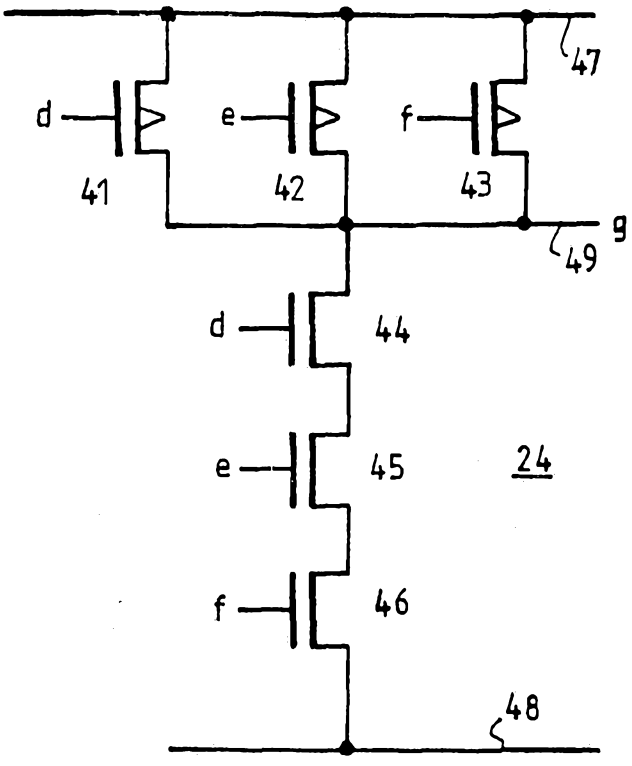


Fig.4

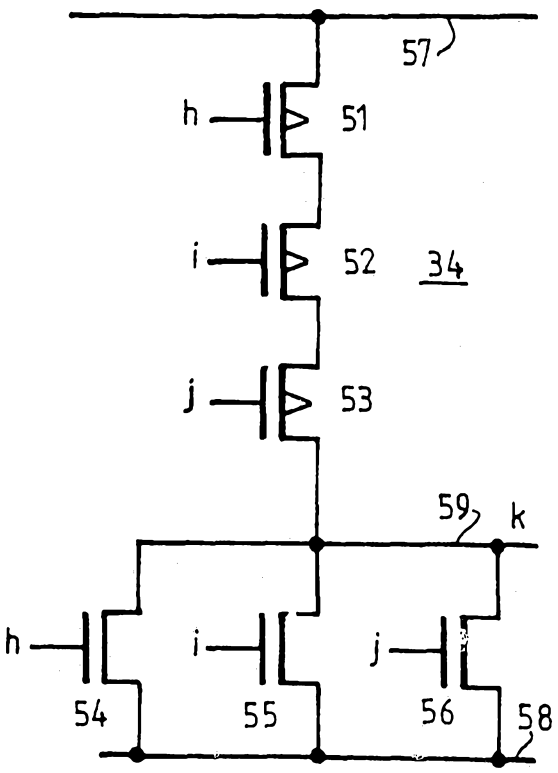


Fig.5

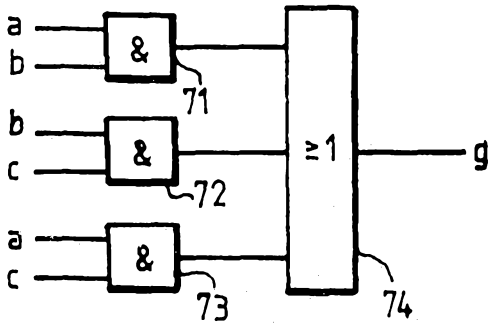


Fig.7

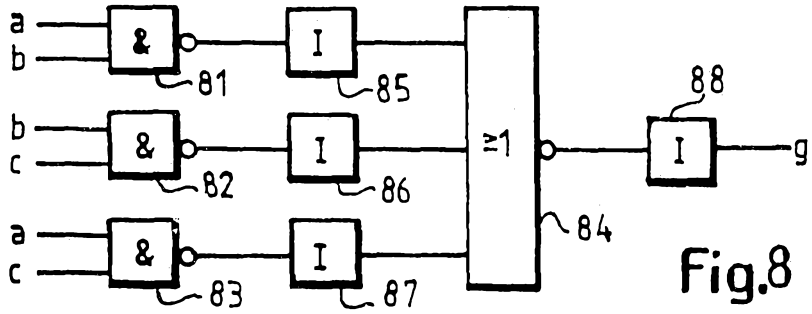


Fig.8

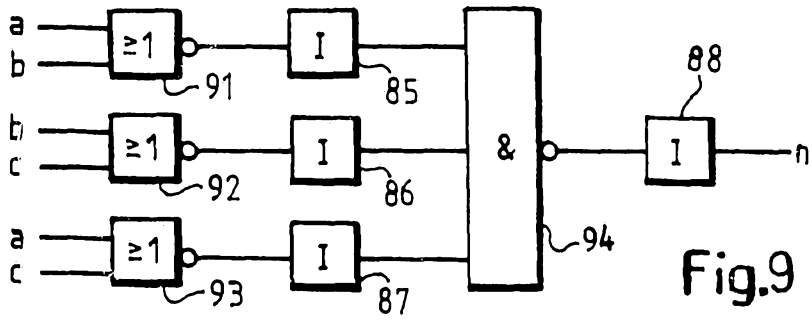


Fig.9

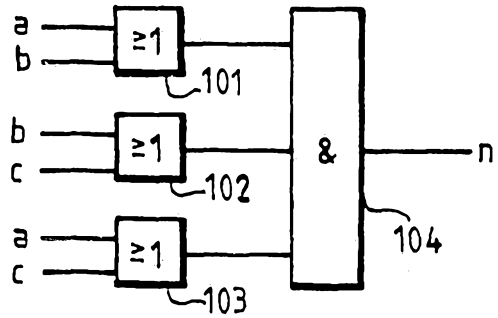


Fig.10

INTERNATIONAL SEARCH REPORT

International Application No PCT/SE 90/00290

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC5: G 06 F 11/18

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
IPC5	G 06 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in Fields Searched[8]

SE,DK,FI,NO classes as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category *	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	US, A, 4583224 (ISHII ET AL) 15 April 1986, see column 1, line 11 - line 18; column 1, line 62 - line 68; column 2, line 2 - line 6; figures 2-6 --	1-4
A	US, A, 4468574 (ENGELER ET AL) 28 August 1984, see figures 2,4,5 --	1-4
A	US, A, 4555721 (BANSAL ET AL) 26 November 1985, see figures 22,25 --	1-4
A	GB, A, 2093614 (THE PLESSEY COMPANY LIMITED) 2 September 1982, see figure 2 --	1-4

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
10th August 1990	1990 -08- 14
International Searching Authority	**Signature of Authorized Officer**
SWEDISH PATENT OFFICE	RUNE BENGTSSON

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	US, A, 4375683 (WENSLEY) 1 March 1983, see figures 1-7 --	1-4

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. PCT/SE 90/00290

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the Swedish Patent Office EDP file on 90-06-27
The Swedish Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4583224	86-04-15	EP-A-B- 0109602	84-05-30
		JP-A- 59085153	84-05-17
US-A- 4468574	84-08-28	NONE	
US-A- 4555721	85-11-26	DE-A- 3279194	88-12-08
		EP-A-B- 0066068	82-12-08
		JP-A- 57192081	82-11-26
		US-A- 4467518	84-08-28
GB-A- 2093614	82-09-02	NONE	
US-A- 4375683	83-03-01	NONE	