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(54) **Title**: SWITCHED CAPACITOR AMPLIFIER

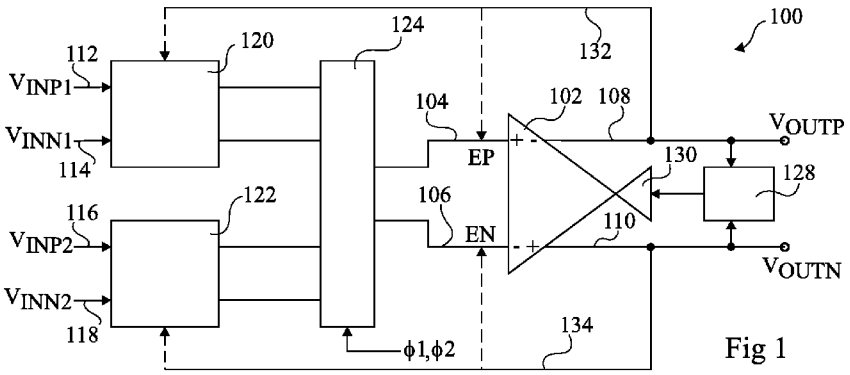

Fig 1

(57) **Abstract**: The invention concerns a switched capacitor amplifier having an amplification unit (102) adapted to amplify a differential signal; a first switched capacitor block (120) including a first plurality of capacitors operable to sample a first differential input signal during a first sampling phase and to drive the amplification unit during a first drive phase; and a second switched capacitor block (122) comprising a second plurality of capacitors operable to sample a second differential input signal during a second sampling phase and to drive the amplification unit during a second drive phase.

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SWITCHED CAPACITOR AMPLIFIER

FIELD OF THE INVENTION

The present invention relates to a switched capacitor amplifier, and in particular to a switched capacitor amplifier having two phases of operation.

BACKGROUND OF THE INVENTION

Switched capacitor amplifiers generally comprise an amplifier stage coupled to a number of switched capacitors, which are switched in order to sample an input voltage at the input of a circuit during a first phase, and then to supply, during a subsequent phase, the signal to an amplifier stage to be amplified.

In differential switched capacitor amplifiers it is generally an aim to control a common mode output of the amplifier at a fixed voltage, at the same time as providing a high static gain in order to ensure a high linearity of the differential amplifier. However, in known switched capacitor amplifiers, it is hard to obtain both of these aims.

Furthermore, such switched capacitor amplifiers tend to be inefficient in terms of power consummation.

SUMMARY OF THE INVENTION

It is an aim of embodiments of the present invention to at least partially address one or more drawbacks of known switched capacitor amplifier circuits.

According to one aspect of the present invention, there is provided a switched capacitor amplifier comprising: an amplification unit adapted to amplify a differential signal; a first switched capacitor block comprising a first plurality of capacitors operable to sample a first differential input signal during a first sampling phase and to drive the amplification unit during a first drive phase; a second switched capacitor block comprising a second plurality of capacitors operable to sample a second differential input signal during a second sampling phase and to drive the amplification unit during a second drive phase.

According to an embodiment of the present invention, the first switched capacitor block alternates between the first sampling phase and the first drive phase, and the second switched capacitor block alternates between the second sampling phase and the second drive phase.

According to an embodiment of the present invention, the switched capacitor amplifier comprises control circuitry for generating first and second timing signals for controlling the first and second switched capacitor blocks for example such that the first drive phase occurs during the second sampling phase and such that the second drive phase occurs during the first sampling phase.

According to an embodiment of the present invention, the first switched capacitor block is adapted to couple the first plurality of capacitors to first differential inputs of the switched capacitor amplifier during the first sampling phase and to a pair of differential input terminals of the amplification unit during the first drive phase; and the second switched capacitor block is adapted to couple the second plurality of capacitors to second differential inputs of the switched capacitor amplifier during the second sampling phase

and to the pair of differential input terminals of the amplification unit during the second drive phase.

According to another embodiment of the present invention, during the first sampling phase the first switched capacitor block is adapted to couple the first plurality of capacitors between the first differential inputs and a first reference voltage level.

According to another embodiment of the present invention, the switched capacitor amplifier further comprises a feedback control block adapted to provide a common mode feedback signal to the amplification unit based on differential output signals of the amplification unit.

According to another embodiment of the present invention, the feedback control block comprises a first resistor having a first terminal coupled to a first differential output terminal of the amplification unit and a second resistor having a second terminal coupled to a second differential output terminal of the amplification unit, and a comparator comprising a first input coupled to the second terminals of the first and second transistors and a second input coupled to receive a reference voltage.

According to another embodiment of the present invention, the switched capacitor amplifier further comprises feedback capacitors coupled between differential input and output terminals of the amplification unit during the first and second drive phases.

According to another embodiment of the present invention, the amplification unit comprises a two-stage differential amplifier.

According to another embodiment of the present invention, the amplification unit is a chopper amplifier.

According to another embodiment of the present invention, the switched capacitor amplifier is adapted to perform an integration of the first and/or second differential input signal.

According to a further aspect of the present invention, there is provided a system comprising input circuitry arranged to provide at least one differential input signal; and the above switched capacitor amplifier coupled to the input circuitry to receive the at least one differential input signal.

According to a further aspect of the present invention, there is provided an analog to digital converter comprising input circuitry arranged to provide at least one differential input signal; and the above switched capacitor amplifier coupled to the input circuitry to receive the at least one differential input signal.

According to a further aspect of the present invention, there is provided an integrated circuit comprising the above switched capacitor amplifier.

According to a further aspect of the present invention, there is provided a method of amplification comprising: controlling a first switched capacitor block to sample a first differential input signal during a first sampling phase and to drive an amplification unit during a first drive phase; and controlling a second switched capacitor block to sample a second differential input signal during a second sampling phase and to drive the amplification unit during a second drive phase, wherein the first and second drive phases do not overlap.

According to an embodiment of the present invention, the first and second differential input signals are identical to each other, while according to another embodiment of the present invention, the first and second differential input signals are independent of each other.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other purposes, features, aspects and advantages of the invention will become apparent from the following detailed description of embodiments, given by way of illustration and not limitation with reference to the accompanying drawings, in which:

Figure 1 illustrates a switched capacitor amplifier according to an embodiment of the present invention;

Figure 2 illustrates a switched capacitor amplifier according to a further embodiment of the present invention;

Figure 3 illustrates an amplifier unit of the switched capacitor amplifier of Figure 1 in more detail according to a further embodiment of the present invention;

Figure 4 illustrates an amplifying unit of the switched capacitor amplifier of Figure 1 in more detail according to an embodiment of the present invention;

Figure 5 illustrates a switched capacitor amplifier according to yet a further embodiment of the present invention;

Figure 6 illustrates timing of first and second phases of the switched capacitor amplifier according to embodiments of the present invention; and

Figure 7 illustrates an electronic device comprising a switched capacitor amplifier according to embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates a switched capacitor amplifier 100. As illustrated, amplifier 100 comprises an amplification unit 102, having differential positive and negative inputs 104 and 106 respectively, and differential negative and positive outputs 108 and 110 respectively. In particular, the amplification unit is arranged to be driven by one differential input signal at a time, and thus comprises a single pair of differential inputs and outputs. The amplifier circuit comprises a pair of differential input terminals 112 and 114, and a pair of differential input terminals 116 and 118. Input terminals 112 to 118 receive input voltage signals V_{INP1}, V_{INN1}, V_{INP2} and V_{INN2} respectively.

Input terminals 112 and 114 are coupled to the inputs of a switched capacitor block 120, which comprises a number of switched capacitors (not shown in Figure 1). Input terminals 116 and 118 are coupled to the input nodes of a switched capacitor block 122, which also comprises a number of switched capacitors

(not shown in Figure 1). The switched capacitor blocks 120 and 122 each comprise differential outputs coupled to a switch block 124. Switch blocks 120, 122 and 124 are controlled by timing signals Ø1 and Ø2. These timing signals select when the differential outputs of the switch capacitor block 120 or the differential outputs from the switched capacitor block 122 are coupled the differential input terminals 104 and 106 of the differential amplification unit. The timing signals Ø1 and Ø2 are for example generated by control circuitry (not shown in Figure 1).

The output terminals 108 and 110 of the amplification unit 102 provide differential output signals V_{OUTP} and V_{OUTN} of the circuit. VOUTP has opposite phase to input signal EN of the amplification unit, while VOUTP has opposite phase to input signal EP of the amplification unit. These signals are also provided to a feedback control block 128, which is coupled to outputs 108 and 110 and generates a control signal based on these signals to a comparator 130 of the amplification unit 102. This control signal provides common mode feedback, allowing the common mode of the output signals to be controlled.

As illustrated by lines 132 and 134, the output terminals 108 and 110 of the amplification unit 102 are provided as feedback signals to the amplification unit inputs 104, 106 or to the switched capacitor blocks 120 and 122, depending on the type of amplification that is to be performed by the switched capacitor amplifier.

In operation, each of the switched capacitor blocks 120 and 122 operates having a sampling phase, during which the input signals on the inputs 112 and 114 or 116 and 118 are coupled to capacitors to sample the input voltages. Furthermore, each of the switched capacitor blocks 120, 122 operates having a drive phase, during which capacitors in the block are coupled to the inputs of the amplification unit 102, to drive the amplification unit. The sampling and drive phases in each of the blocks 120, 122 alternates, and the sampling and drive phases of the two blocks 120, 122 are offset with respect to each other,

so that only one of the blocks is driving the amplification unit at any one time. The timing can be arranged for example such that while one block is sampling the input, the other block is driving the amplification unit, and vice versa.

The differential input signals V_{INP1} and V_{INP2}, and V_{INN1} and V_{INN2} may be different to each other, allowing two differential signals to be amplified by the same differential amplifier, or V_{INP1} could be the same signal as the V_{INP2}, while the input signal V_{INN1} is the same signal as V_{INN2}, allowing the sampling rate of the input differential signal to be doubled.

Figure 2 illustrates the switched capacitor amplifier 100 of Figure 1 in more detail according to one embodiment.

In this embodiment, the differential input signals to the switched capacitor blocks are the same as each other. The circuit comprises the same amplification unit 102 as shown in Figure 1, having the same input terminals 104, 106 and output terminals 108, 110 and these will not be described again in detail. The circuitry forming the switched capacitor blocks 120, 122 and switch 124 will now be described.

Input terminal 202 is coupled to a node 208 by a switch 210 and a capacitor 212 coupled in series, and also, in parallel, by a switch 214 and a capacitor 216 coupled in series. In similar fashion, input terminal 204 is coupled to a node 218 by a switch 220 and a capacitor 222 coupled in series, and, in parallel, by a switch 224 and a capacitor 226 also coupled in series.

A node between switch 214 and capacitor 216 is coupled to a reference voltage VCM by a switch 228, while a node between the switch 220 and capacitor 222 is coupled to reference voltage VCM via a switch 230. The VCM reference voltage is a common mode voltage for example at a level halfway between the supply voltage level and a ground voltage level, although it could be at a different value as would be described in more detail below.

The node between switch 210 and capacitor 212 is coupled to the output terminal 108 of the amplification unit 102 by a switch 232, while the node between switch 224 and capacitor

226 is coupled to the output terminal 110 of the amplification unit 102 by a switch 234.

Nodes 208 and 218 are coupled together by a switch 236, and also, in parallel, by switches 238 and 240 coupled in series. A node 239 between switches 238 and 240 is coupled to a reference voltage VCM1.

Node 208 is also coupled to the input terminal 104 of the amplification unit 102 by a switch 242, while node 218 is coupled to the input terminal 106 of the amplification unit 102 by a switch 244.

Switches, capacitors and nodes 208 to 240 in Figure 2 perform the functions of the switched capacitor block 120 of Figure 1, while switches 242 and 244 form part of the switch block 124.

The lower half of Figure 2 illustrates switches, capacitors and nodes 208' to 240' which for the switched capacitor block 122 of Figure 1, and is identical in lay out to features 208 to 210, with the same reference numerals being used for like features with the addition of an apostrophe.

The output terminals 108 and 110 of the amplification unit 102 are also coupled together by resistors 250 and 252 connected in series. Resistors 250 and 252 preferably have the same resistance value, and the node between these two resistors, labelled 254 in Figure 2, is coupled to the comparator 130 of the amplification unit 102. Comparator 130 also receives the reference voltage VCM, and based on a comparison between VCM and the voltage at node 254, provides a common mode feedback signal for controlling the common mode provided by the amplification unit 102, as will be described in more detail below.

In operation, Ø1 and Ø2 have opposite phases to each other except during transitions. Switches controlled by Ø1 are ON when Ø1 is high, and OFF when Ø1 is low, and likewise switches controlled by Ø2 are ON when Ø2 is high, and OFF when Ø2 is low. When Ø1 is high, switched capacitor block 120 is controlled to same the differential input signal at inputs 202 and 204 by coupling one terminal of capacitors 212 and 216 to

input 202, and one terminal of capacitors 222 and 226 to input 204. At the same time, the other terminals of capacitors 212, 216, 222 and 226 are coupled together, and the reference voltage VCM1, and these capacitors are isolated from the inputs to the amplification unit 102. Thus the differences between V_{INP} and V_{INN} with respect to the reference voltage VCM1 are stored on capacitor pairs 212, 216 and 222, 226 respectively.

At the same time, while Ø1 is high, capacitors 212', 216', 222' and 226' are isolated from the inputs 202, 204. Furthermore, capacitors 212' is coupled between output 108 and input 104 of amplification unit 104, while capacitor 216' is coupled between VCM input 206 and input 104'. In a similar fashion, capacitors 226' is coupled between output 110 and input 106 of amplification unit 104, while capacitor 222' is coupled between VCM input 206 and input 106. Thus the amplification unit 102 is driven based on the voltages stored on capacitors 216' and 222' at the inputs of the amplification unit and on feedback capacitors 212' and 226'.

The gain of the amplification unit 102 can thus be expressed as:

$$(V_{OUTN}-V_{OUTP})/V_{IN} = (C_f + C_S)/C_f$$

wherein V_{OUTN} and V_{OUTP} are the output voltages of the amplification unit when driven by V_{IN}, which is the voltage difference between V_{INP} and V_{INN}. C_f is the value of the feedback capacitors 212, 226, 212' and 226', which for example all have equal capacitance. C_S is the value of the sampling capacitors 216, 222, 216' and 222', which also for example have equal capacitances.

The input common mode of the amplification unit 102 can be expressed as: $(V_{EP}+V_{EN})/2 \approx V_{EP} \approx V_{EN} = V_{CM1}$. This is equivalent to the input common mode of the amplifier 102 being fixed at the reference voltage V_{CM1}.

Figure 3 illustrates the amplification unit 102 of Figure 1 in more detail according to one embodiment, in which it comprises a two-stage amplifier.

A first stage of the amplifier comprises a differential pair comprising a transistor 302, which has a gate node coupled to input line 104, and a transistor 304, has a gate node coupled to input line 106. Transistors 302 and 304 each have source terminals coupled to a current source 306. The drain terminal of transistor 302 is coupled to a current source 308, while the drain terminal of transistor 304 is coupled to a current source 310.

A node 312 between transistor 302 and current source 308 is further coupled to the gate of a transistor 314, which has its source/drain nodes coupled between a supply voltage level V_{DD}, and a current source 316. The node between transistor 314 and current source 316 is also coupled to node 312 via a capacitor 317, and provides the output voltage V_{OUTP} of the amplification unit 102 on line 108. In a similar fashion, a node 322 between transistor 304 and current source 310 is coupled to the gate node of a transistor 324, which has its source/drain nodes coupled between a supply voltage level v_{DD} and a current source 326. The node between transistor 324 and current source 326 is also coupled to node 322 via a capacitor 327, and provides the output voltage V_{OUTN} of the differential amplification unit 102 on line 110. Transistors 314 and 324 provide the second stage of the amplification unit. Capacitors 317 and 327 provide stability to the amplifier.

Current sources 306, 316 and 326 are coupled to a ground voltage reference, for example at 0 V or a different voltage, while current sources 308 and 310 are coupled to a supply voltage, for example 2.8 V, although in alternative embodiments the ground and reference voltages could be swapped.

Common mode feedback resistors 250, 252 and comparator 130 are also shown in Figure 3, coupled as shown in Figure 2 between the output terminals 110 and 108. As illustrated, the output of comparator 130 is coupled to a node 330, which controls current sources 308 and 310, thereby controlling the current flow through the differential pairs 204 and 304 and

allowing the common mode voltage to be controlled at the reference voltage VCM.

Figure 4 illustrates an alternative embodiment of the amplification unit 102, in which the amplifier is a chopping amplifier, having two switching phases S1 and S2, and thereby allowing cancellation of both the offset voltage and the low frequency noise of the amplifier.

Again, the amplification unit 102 comprises a two-stage amplifier. The first stage comprises a differential pair 402, 404. The gate node of transistors 402 is coupled to both the input line 104 and the input line 106, via switches 406 and 408 respectively. Switch 406 is controlled by signal ØS1, while switch 408 is controlled by a signal ØS2, that is of opposite phase to ØS1. In a similar fashion, the gate terminal of transistor 404 is coupled to input line 106 via a switch 410, and to input line 104 via a switch 412. Switch 410 is controlled by the signal ØS1, while switch 412 is controlled by signal ØS2.

The source nodes of transistors 402 and 404 are coupled to a current source 414. The drain nodes of transistor 402 and 404 are coupled to a supply voltage V_{DD} via transistors 416 and 418 respectively. The node between transistors 402 and 416 is labelled 420, while the node between transistors 404 and 418 is labelled 421. The gate terminal of a PMOS transistor 422 is coupled to nodes 402 and 404 via respective switches 424 and 426 controlled by signals ØS1 and ØS2 respectively. The source/drain terminals of transistor 422 are coupled between a supply voltage V_{DD} and the output line 108 of the amplification unit, providing output voltage V_{OUTP}. The gate node of transistor 422 is also coupled output line 108 via a capacitor 428 to provide stability to the amplifier. Output line 108 is also coupled to a current source 430. In a similar fashion, the gate terminal of a transistor 432, is coupled to nodes 420 and 421 via respective switches 434 and 436 controlled by signals ØS2 and ØS1 respectively. The source/drain terminals of transistor 432 are coupled between a supply voltage V_{DD} and the output line 110 of the amplification unit, providing output

voltage V_{OUTN}. The gate node of transistor 432 is also coupled output line 110 via a capacitor 438 to provide stability to the amplifier. Output line 110 is also coupled to a current source 440.

As with the embodiments of Figures 2 and 3, common mode feedback control is provided by a pair of resistors 250, 252 coupled to output lines 108 and 110 and the comparator 130. In the embodiment of Figure 4, the output of comparator 130 is coupled to a node 442, which is coupled to the gate terminals of transistors 416 and 418.

While in Figure 4 current sources 414, 430 and 440 are coupled to a ground reference voltage, while transistors 416, 418, 422 and 432 are coupled to a supply voltage V_{DD}, in alternatively embodiments the ground and supply voltage levels could be swapped.

In operation, the control signals ØS1 and ØS2 are provided such that the circuit selects alternate inputs of the differential pair 402 and 404, while at the same time selecting alternate inputs of the output transistors 422 and 432. In this way, the offset voltage and low frequency noise of the amplifier can be improved.

As an example, in the case in which a single differential signal is processed by the amplifier, the timing signals can be chosen such that ØS1=Ø1 and ØS2=Ø2, or in the case that two different signals are processed, ØS1 and ØS2 could be at half the frequency of one of Ø1, Ø2. Obviously, precautionary measures can be taken for transitions.

Figure 5 illustrates an alternative embodiment of a switched capacitor amplifier 500, which rather than being a gain amplifier, is an integrator amplifier, used for example to implement a sigma-delta analog to digital converter. As with the gain amplifier, this amplifier may also operate with a single input signal or a pair of different input signals.

Features in Figure 5 which are the same as those in Figure 2 have been labelled with like reference numerals, and will not be described again in detail.

As illustrated, the switch capacitor amplifier 500 comprises input lines 502 and 504 for receiving a first differential input signal comprising signals V_{INP1} and V_{INN1} and second differential input lines 506 and 508 for receiving a differential input signal comprising signals V_{INP2} and V_{INN2}. The first and second differential input signals may be the same signals or different signals.

Input lines 208, 208' are also provided for receiving a common mode voltage VCM.

Input line 502 is coupled to node 208 via a switch 510 and a capacitor 512 coupled in series. A node 513 between switch 510 and capacitor 512 is furthermore coupled to the input line 206 via a switch 514. In a similar fashion, input line 504 is coupled to node 218 via a switch 516 and a capacitor 518 coupled in series. A node 519 coupled between switch 516 and capacitor 518 is furthermore coupled to input line 206 via a switch 520.

The circuitry coupling input lines 506 and 508 to nodes 208' and 218' is the same as described above between input lines 502, 504 and nodes 208, 218, and has been labelled with the same reference numerals with the addition of an apostrophe.

In this embodiment, feedback capacitors 522 and 524 are provided coupled directly between the output lines 108 and 110 and input lines 108 and 106 respectively.

Operation of the circuit of Figure 5 is similar to that of Figure 2, except that the output is integration amplification rather than gain amplification is performed.

In the circuits of Figures 2 and 5, two common mode voltages VCM and VCM1 are provided, generated by two voltage generators not illustrated.

The voltage reference VCM is provided to the comparator as well as to node 206. It is on this voltage reference that the output common mode of the amplifier is based: $(V_{OUTP}+V_{OUTN})/2=VCM$. The voltage VCM is generally chosen to be half the supply voltage in order to allow the output signal to have the maximum amplitude variation.

The voltage reference VCM1 is applied to node 239, and the input common mode voltage of the amplifier 102 is based on this reference voltage: (VEP+VEN)/2=VCM1. The voltage VCM1 is chosen such that the amplification unit 102 is adequately driven. The voltage level required for this will depend on the particular design of the amplification unit.

Figure 6 illustrates an example of the timing signal Ø1 and Ø2 according to one embodiment. As illustrated, each period of the timing signals Ø1, Ø2 comprises a high pulse 602, 604 respectively. The high pulse 602 for example corresponds to the drive phase during which switched capacitor block 122 drives the amplification unit 102, while the high pulse 604 corresponds to the drive phase during which switched capacitor block 120 drives the amplification unit 102. As illustrated, the timing signals Ø1, Ø2 are not high at the same time, and thus the drive phase of the switched capacitor block 120 does not overlap the drive phase of the switched capacitor block 122. Furthermore, as controlled by timing signal Ø1, the switched capacitor block 122 alternates between the sampling and drive phases, and as controlled by the timing signal Ø2, the switched capacitor block 120 alternates between the sampling and drive phases.

The timing shown in Figure 6 is just an example, and in alternative embodiments other forms of signals would be possible in which the rising and falling edges of signals Ø1 and Ø2 are offset with respect to each other.

Figure 7 illustrates an electronic circuit 700 comprising input circuitry 702, an amplifier block 704 and processing circuitry 706. Device 700 is for example any electronic device receiving or generating differential signals that need to be amplified, such as a mobile telephone, a hard disk drive for a PC or laptop, a laptop computer, set-top box, a games console, digital camera, digital radio etc. The input circuitry for example comprises any circuitry for receiving of reading a differential signal. The differential input signal is then provided to the amplifier block 704, which comprises the switched capacitor amplifier of Figures 1, 2 or 5, and may have

unity gain or positive or negative gain, and according to some embodiments may integrate the input signal. Such an amplifier could comprise the amplification unit of Figures 3 or 4. The differential output of the amplifier block 704 is provided to processing circuitry 706, which for example filters the signal, and/or provides other processing of the signal, before it is output, for example to speakers, a display or any other output means.

Thus a switched capacitor amplifier has been described. One advantage of the embodiments described herein is that common mode control is possible without short circuiting the input terminals of the amplification unit, and this means that a two-stage amplification unit may be provided, allowing greater gain and thus improved linearity when compared to a single stage amplifier. In particular, if the inputs of a first stage are short circuited, its outputs will be have a small differential caused by the first stage offset, and the second stage of the amplifier will be over-driven. In consequence, in such an amplifier, the outputs of the second stage will take a long time to return to the correct value and during this time supply consumption will be large. On the other hand, in the embodiments described herein, as the input terminals of the amplification unit are not short circuited and are always driven, the amplifier is always working and is always able to process the input signal, thereby improving power consumption.

A further advantage of the embodiments described herein is that, when the same differential input signal is applied to both switched capacitor blocks, the signal can be sampled twice as often as when only one switched capacitor block is provided, thereby reducing noise in the output signal, and allowing fall Nyquist operation. In particular, in some of the embodiments described herein, the amplification unit 102 processes the input signal during the two phases of the clock, preferably without dead time, resulting in twice the sampling rate for the same supply power consumption and substantially the same silicon area.

A further advantage of the embodiments described herein is that, when the differential input signals are different, independent signals, the same amplification unit can be used to amplify two signals. In this case, a switch can be provided at the output of the amplification unit, controlled by the timing signals Ø1, Ø2, to separate the two signals after amplification. In particular, in some of the embodiments described herein, the amplification unit 102 processes a first signal during the clock phase when Ø1 is high, and processes a second signal during the clock phase when Ø2 is high. This is preferably no dead time, as the signals are processed alternately, and current consumption and silicon area are substantially unchanged.

Having thus described illustrative embodiments of the invention, various alterations, modifications and improvements will readily occur to those skilled in the art.

The switches in Figures 2, 4 and 5 can be realised with transistors, as will be apparent to those skilled in the art, for example N or P channel MOS transistors.

While the amplification unit has been described comprising two stages, in alternative embodiments it could comprise only one stage, or more than two stages.

While in the example circuits of Figures 3 and 4 the differential pairs are illustrated as NMOS transistors, other types of transistors may be used. Furthermore, while the second stage comprises PMOS transistors, again other types of transistors could be used.

Such alterations, modifications and improvements are intended to be within the scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The invention is limited only as defined in the following claims and the equivalent thereto.

CLAIMS

1. A switched capacitor amplifier comprising:

an amplification unit (102) adapted to amplify a differential signal;

a first switched capacitor block (120) comprising a first plurality of capacitors operable to sample a first differential input signal during a first sampling phase and to drive said amplification unit during a first drive phase;

a second switched capacitor block (122) comprising a second plurality of capacitors operable to sample a second differential input signal during a second sampling phase and to drive said amplification unit during a second drive phase, wherein the first and second drive phases do not overlap.

2. The switched capacitor amplifier of claim 1, wherein the first switched capacitor block alternates between the first sampling phase and the first drive phase, and the second switched capacitor block alternates between the second sampling phase and the second drive phase.

3. The switched capacitor amplifier of claim 1 or 2, further comprising control circuitry arranged to generate a first timing signal for controlling the first switched capacitor block and a second timing signal for controlling the second switched capacitor block.

4. The switched capacitor amplifier of any of claims 1 to 3, wherein:

the first switched capacitor block is adapted to couple said first plurality of capacitors to first differential inputs (112, 114) of said switched capacitor amplifier during said first sampling phase and to a pair of differential input terminals (104, 106) of the amplification unit during the first drive phase; and

the second switched capacitor block is adapted to couple said second plurality of capacitors to second differential inputs (116, 118) of said switched capacitor amplifier during said second sampling phase and to said pair of

differential input terminals (104, 106) of the amplification unit during the second drive phase.

5. The switched capacitor amplifier of claim 4, wherein during said first sampling phase said first switched capacitor block is adapted to couple said first plurality of capacitors between the first differential inputs and a first reference voltage level (VCM1).

6. The switched capacitor amplifier of any of claims 1 to 5, further comprising a feedback control block (128) adapted to provide a common mode feedback signal to the amplification unit based on differential output signals (108, 110) of the amplification unit.

7. The switched capacitor amplifier of claim 6, wherein the feedback control block comprises a first resistor (250) having a first terminal coupled to a first differential output terminal (108) of the amplification unit and a second resistor (252) having a second terminal coupled to a second differential output terminal (110) of the amplification unit, and a comparator (130) comprising a first input coupled to the second terminals of the first and second resistors and a second input coupled to receive a reference voltage (VCM).

8. The switched capacitor amplifier of any of claims 1 to 7, further comprising feedback capacitors (212, 226, 212', 226', 522, 524) coupled between differential input and output terminals (108, 110) of the amplification unit during said first and second drive phases.

9. The switched capacitor amplifier of any preceding claim, wherein the amplification unit comprises a two-stage differential amplifier.

10. The switched capacitor amplifier of any preceding claim, wherein the amplification unit is a chopper amplifier.

11. The switched capacitor amplifier of any preceding claim, adapted to perform an integration of the first and/or second differential input signal.

12. A system comprising:

input circuitry (702) arranged to provide at least one differential input signal;

the switched capacitor amplifier of any of claims 1 to 11, coupled to the input circuitry to receive the at least one differential input signal.

13. An analog to digital converter comprising:

input circuitry (702) arranged to provide at least one differential input signal;

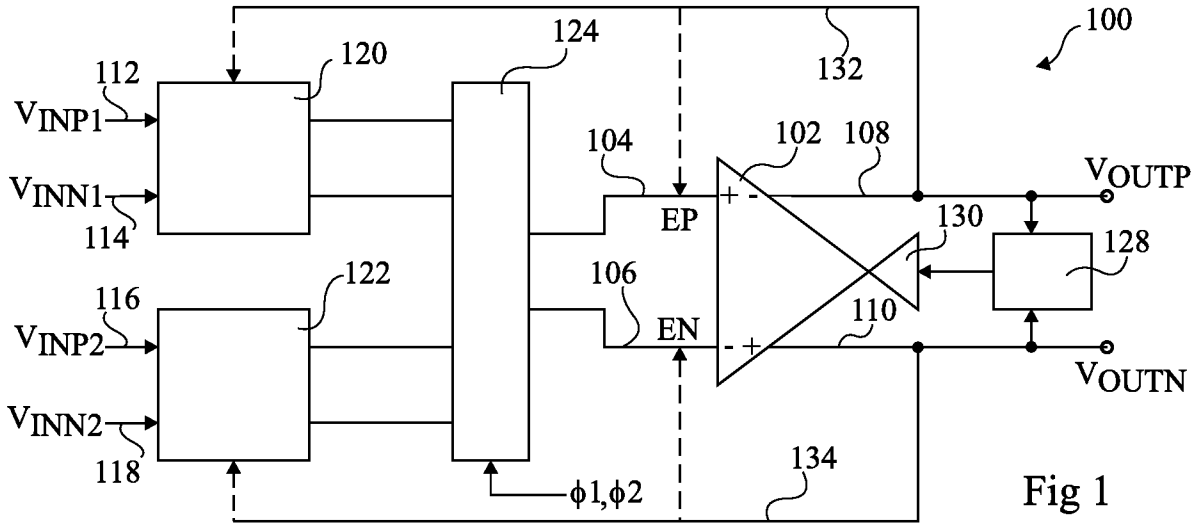
the switched capacitor amplifier of any of claims 1 to 11, coupled to the input circuitry to receive the at least one differential input signal.

14. An integrated circuit comprising the switched capacitor amplifier of any one of claims 1 to 11.

15. A method of amplification comprising:

controlling a first switched capacitor block (120) to sample a first differential input signal during a first sampling phase and to drive an amplification unit during a first drive phase; and

controlling a second switched capacitor block (122) to sample a second differential input signal during a second sampling phase and to drive the amplification unit during a second drive phase, wherein said first and second drive phases do not overlap.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104
102
108
VOUTP
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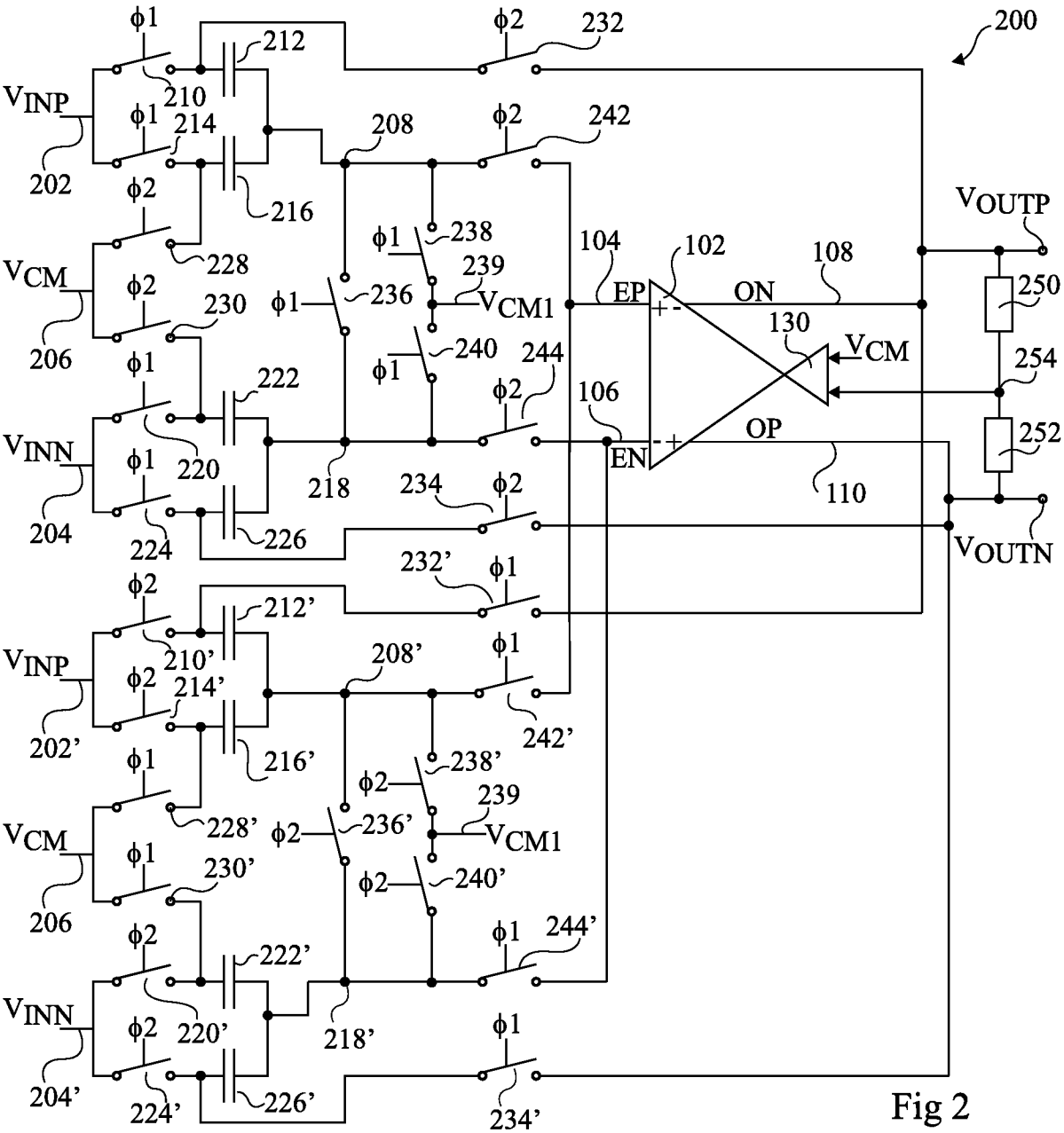
EN
110
VOUTN
VINN2
118
134
ϕ1,ϕ2

Fig 1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ϕ2
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242
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216
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236
VCM1
EP
ON
250
206
240
130
VCM
254
222
244
106
VINN
220
218
234
OP
252
204
224
226
110
VOUTN
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212'
210'
208'
242'
214'
202'
216'
238'
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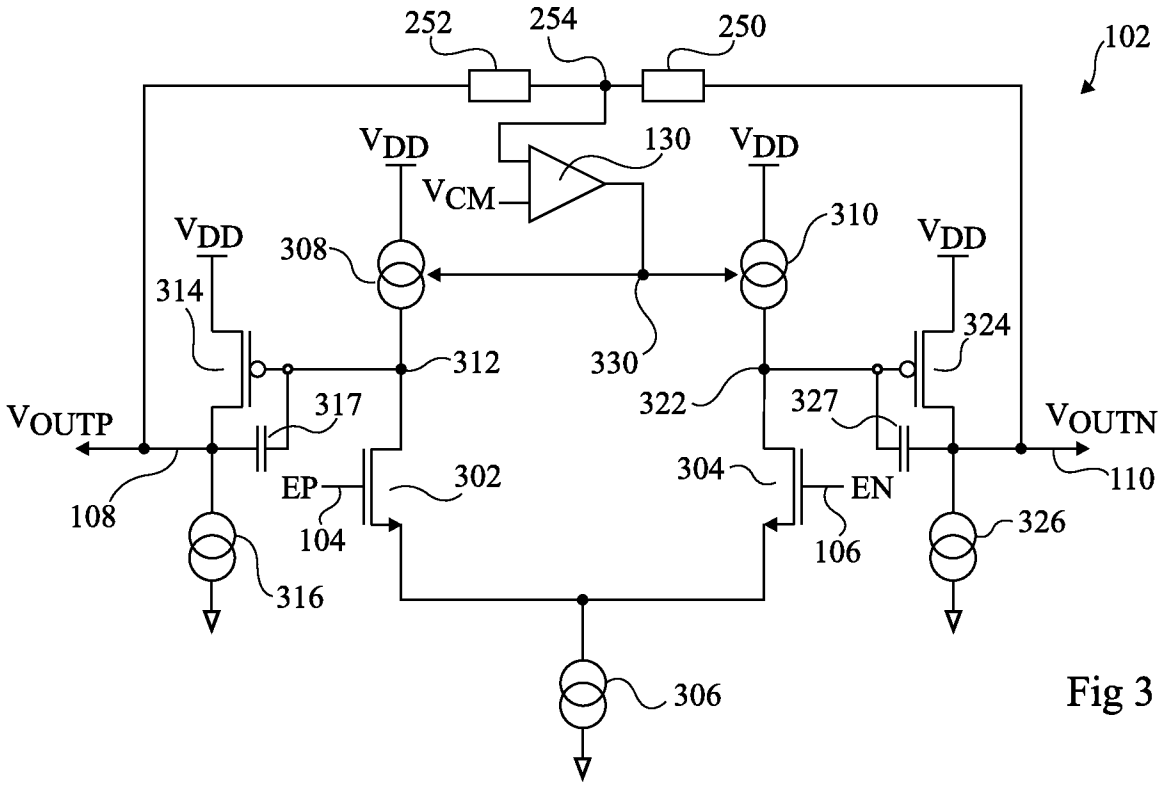
226'
224'
234'

Fig 2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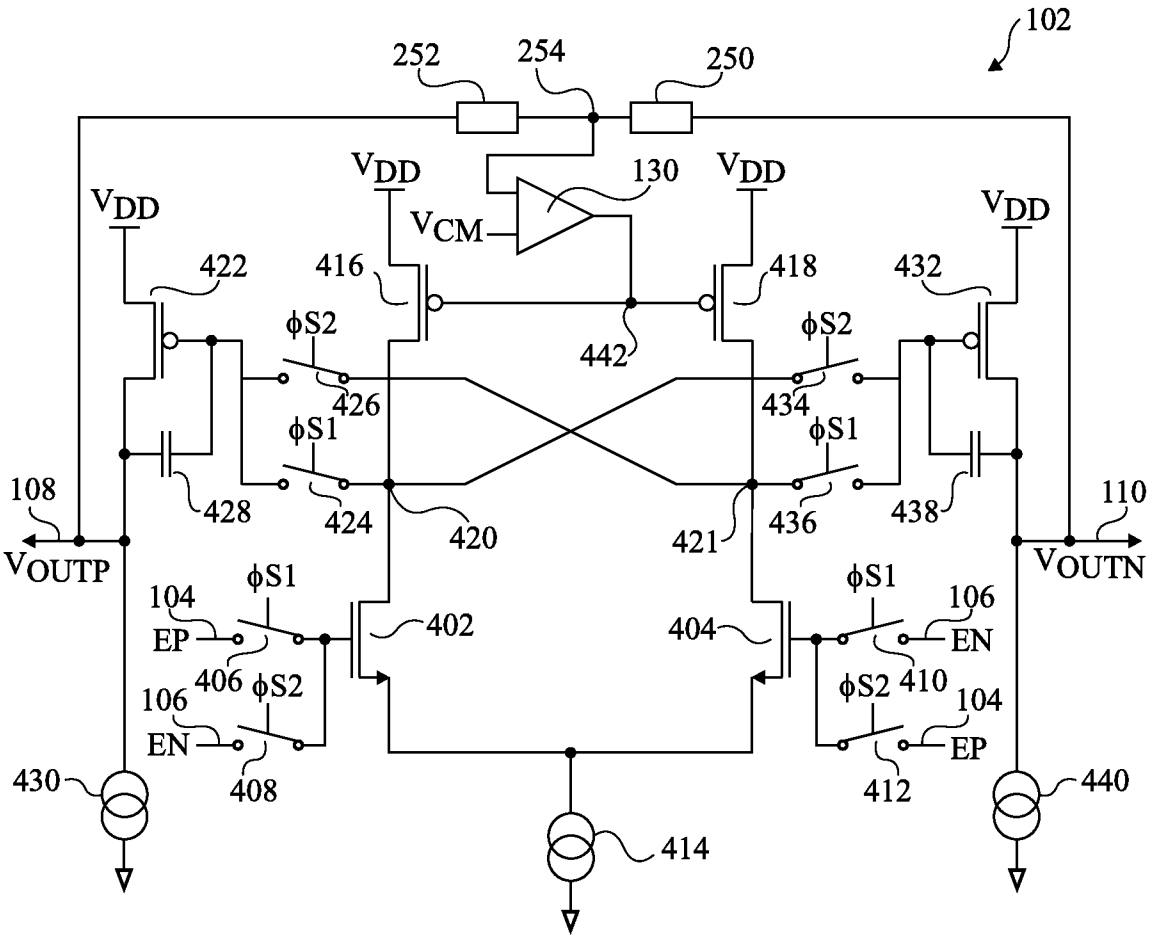
316
306

Fig 3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VDD
VCM
VDD
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418
432
ϕS2
ϕS2
442
426
434
ϕS1
ϕS1
108
428
424
420
421
436
438
110
VOUTP
VOUTN
ϕS1
ϕS1
104
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ϕS2
ϕS2
106
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EN
EP
408
412
430
440
414

Fig 4

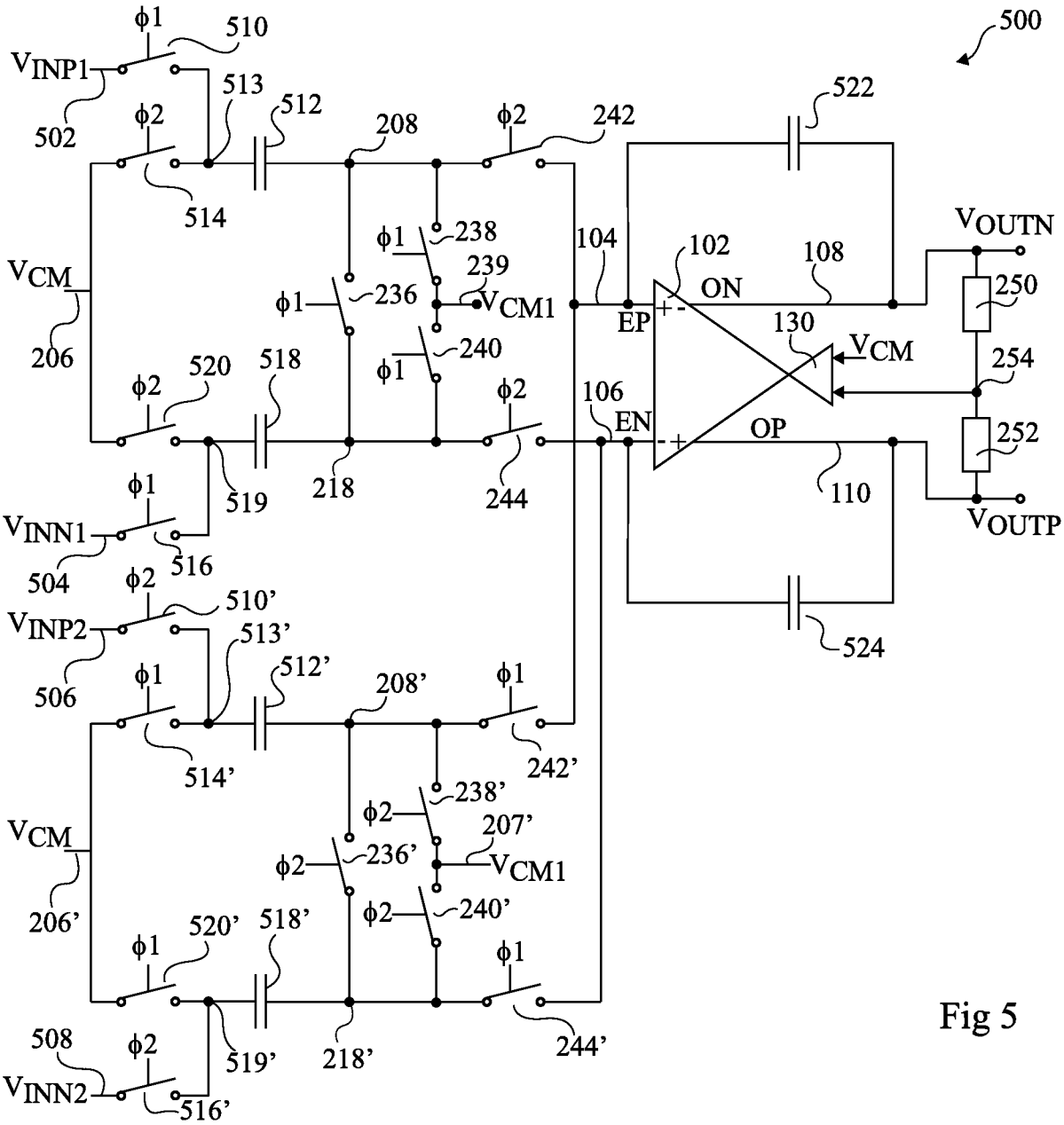

Fig 5

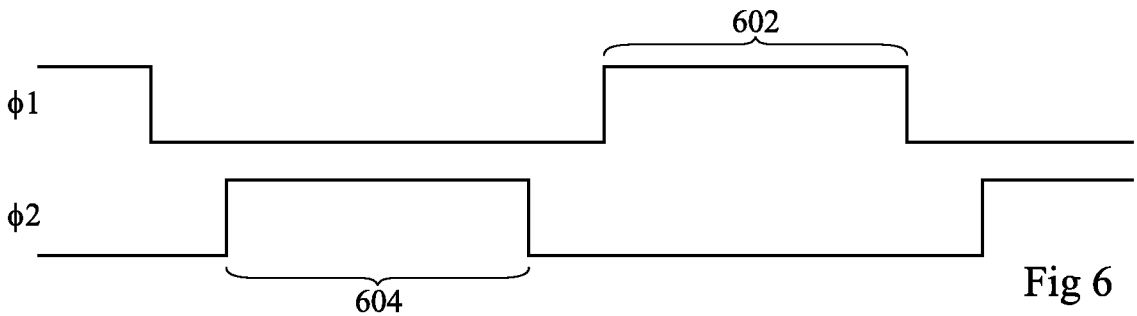

Fig 6

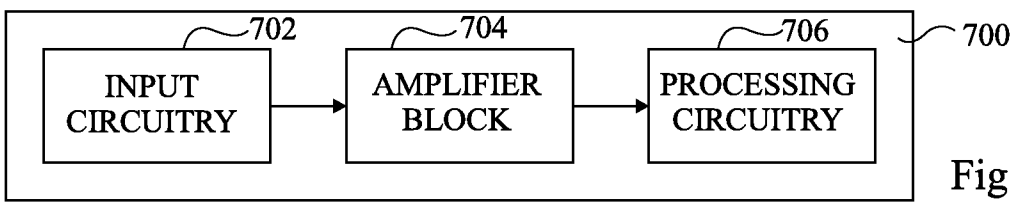

Fig 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/057734

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 973 536 A (MAEJIMA TOSHIO [JP]) 26 October 1999 (1999-10-26) column 4, line 7 - line 22; figures 4,5	1-5,8,9, 11-15
A	US 6 259 313 B1 (LEWICKI LAURENCE DOUGLAS [US]) 10 July 2001 (2001-07-10) column 5, line 19 - column 7, line 34; figure 7	1-15

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 July 2009	23/09/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kurzbauer, Werner

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/057734

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	TERTULIEN NDJOUNTCHE ET AL: "Improved Structures for Programmable Filters: Application in a Switched-Capacitor Adaptive Filter Design" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 46, no. 9, 1 September 1999 (1999-09-01), XP011013120 ISSN: 1057-7130 figures 4,8	1-15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2009/057734

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

see additonal sheet(s)

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-15

   A switched capacitor amplifier comprising two differential inputs and two capacitor blocks each operable to sample and to drive an amplification unit during corresponding sampling and drive phases, whereas the first and second drive phases do not overlap and each of the capacitor blocks alternates between a first and second sampling and drive phase.

   ---

2. claims: 6,7 (as far as they refer to claim 1)

   A switched capacitor amplifier comprising two differential inputs and two capacitor blocks each operable to sample and to drive an amplification unit during corresponding sampling and drive phases, whereas the first and second drive phases do not overlap, further comprising a feedback control block adapted to provide a common mode feedback signal.

   ---

3. claim: 8 (as far as it refers to claim 1)

   A switched capacitor amplifier comprising two differential inputs and two capacitor blocks each operable to sample and to drive an amplification unit during corresponding sampling and drive phases, whereas the first and second drive phases do not overlap, further comprising feedback capacitors.

   ---

4. claim: 9 (as far as it refers to claim 1)

   A switched capacitor amplifier comprising two differential inputs and two capacitor blocks each operable to sample and to drive an amplification unit during corresponding sampling and drive phases, wherein the amplification unit comprises a two-stage differential amplifier.

   ---

5. claim: 10 (as far as it refers to claim 1)

   A switched capacitor amplifier comprising two differential inputs and two capacitor blocks each operable to sample and to drive an amplification unit during corresponding sampling and drive phases, whereas the first and second drive phases do not overlap and wherein the amplification unit is a chopper amplifier.

   ---

6. claim: 11 as far as it refers to claim 1)

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

A switched capacitor amplifier comprising two differential inputs and two capacitor blocks each operable to sample and to drive an amplification unit during corresponding sampling and drive phases, whereas the first and second drive phases do not overlap and wherein the amplifier is adapted to perform an integration of the first / second signal.

---

7. claim: 13 (as far as refers to claim 1)

An analog to digital converter comprising an input circuitry providing a signal to a switched capacitor amplifier comprising two differential inputs and two capacitor blocks each operable to sample and to drive an amplification unit during corresponding sampling and drive phases, whereas the first and second drive phases do not overlap.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2009/057734

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5973536 A	26-10-1999	JP 3216490 B2	09-10-2001
		JP 9083301 A	28-03-1997
US 6259313 B1	10-07-2001	NONE	