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A semiconductor integrated circuit

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H3T 2B3 2T2X 2T3F 2T4 3J 4D 4H1 4H2 4S 5E HD

(56) Documents cited
None

(58) Field of search
H3T
Selected US specifications from IPC sub-class H03K

GB 2 177 866 B

FIG. 1

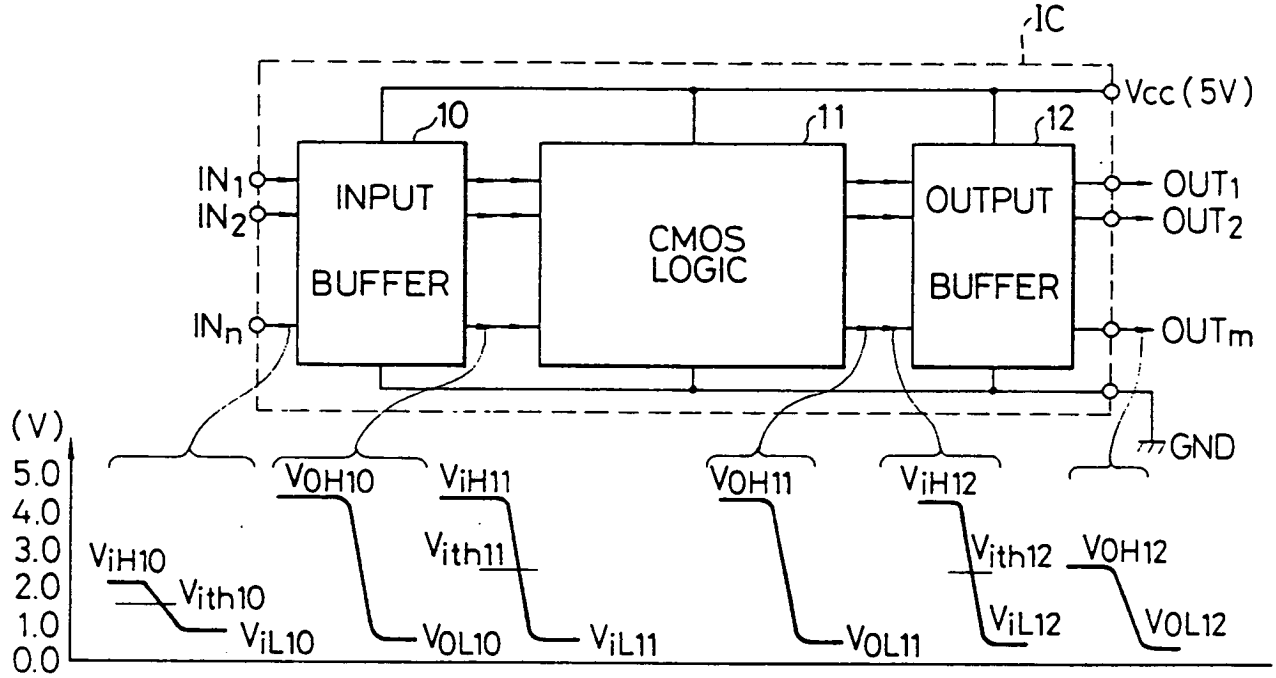
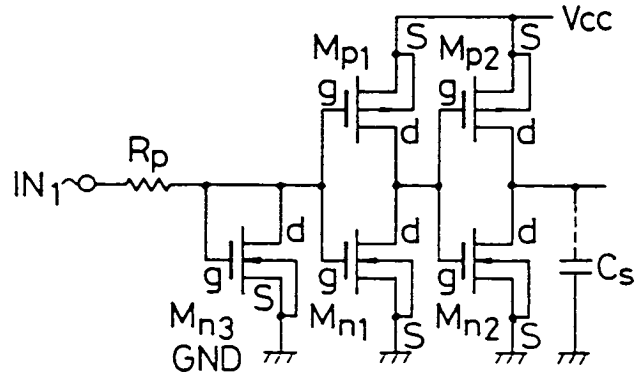

IC
Vcc (5V)
10
11
12
IN1
IN2
INn
INPUT BUFFER
CMOS LOGIC
OUTPUT BUFFER
OUT1
OUT2
OUTm
GND
(V)
5.0
4.0
3.0
2.0
1.0
0.0
VOH10
ViH11
VOH11
ViH12
ViH10
Vith11
Vith12
VOH12
Vith10
ViL10
VOL10
ViL11
VOL11
ViL12
VOL12

FIG. 2


Vcc
Mp1
Mp2
S
g
d
Rp
IN1
Cs
Mn3
Mn1
Mn2
GND

10

FIG. 3

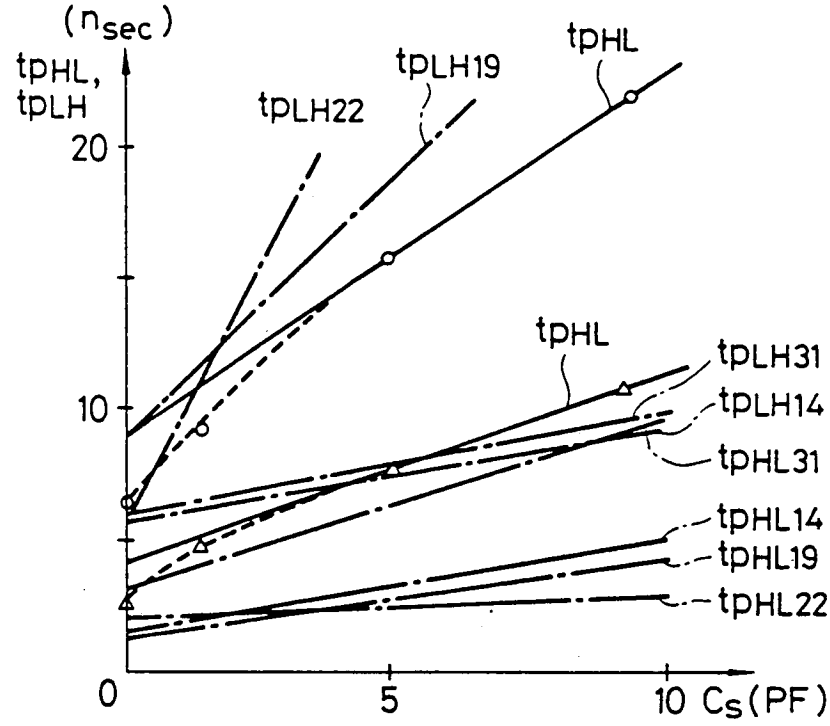

(nsec)
tpHL, tpLH
20
10
0
5
10 Cs(PF)
tpLH22
tpLH19
tpHL
tpHL
tpLH31
tpLH14
tpHL31
tpHL14
tpHL19
tpHL22

FIG. 4

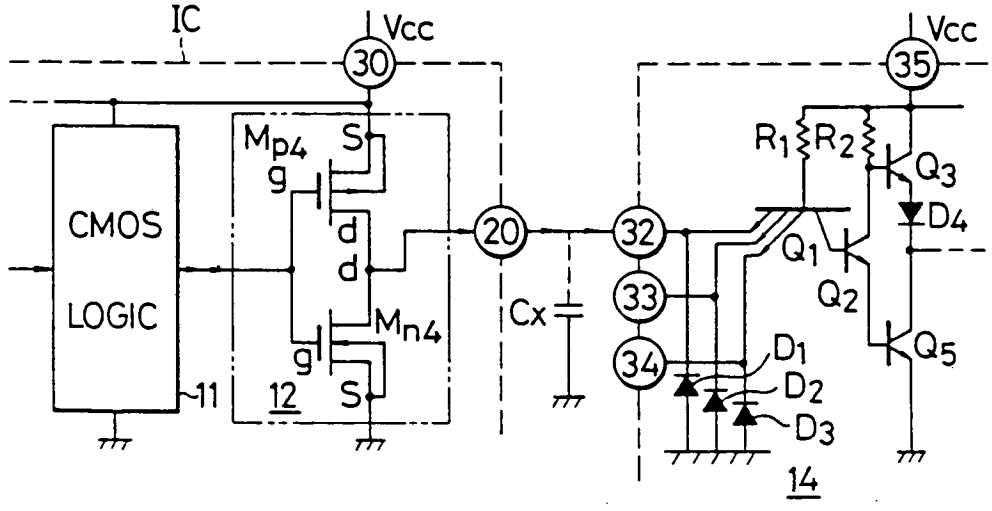

IC
Vcc
30
CMOS
LOGIC
11
Mp4
g
S
d
d
Mn4
g
12
S
20
Cx
32
33
34
Vcc
35
R1
R2
Q3
D4
Q1
Q2
Q5
D1
D2
D3
14

FIG. 5

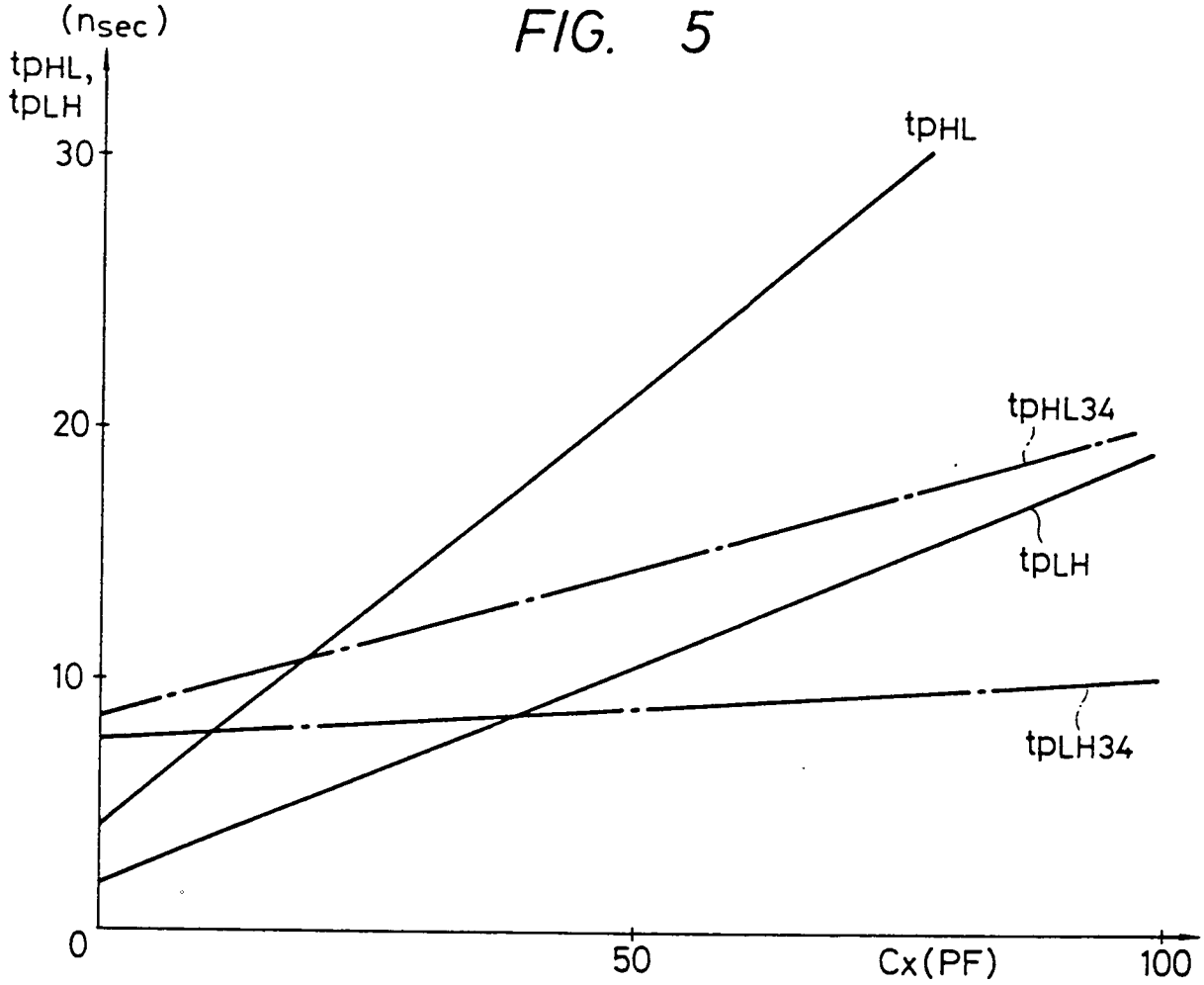
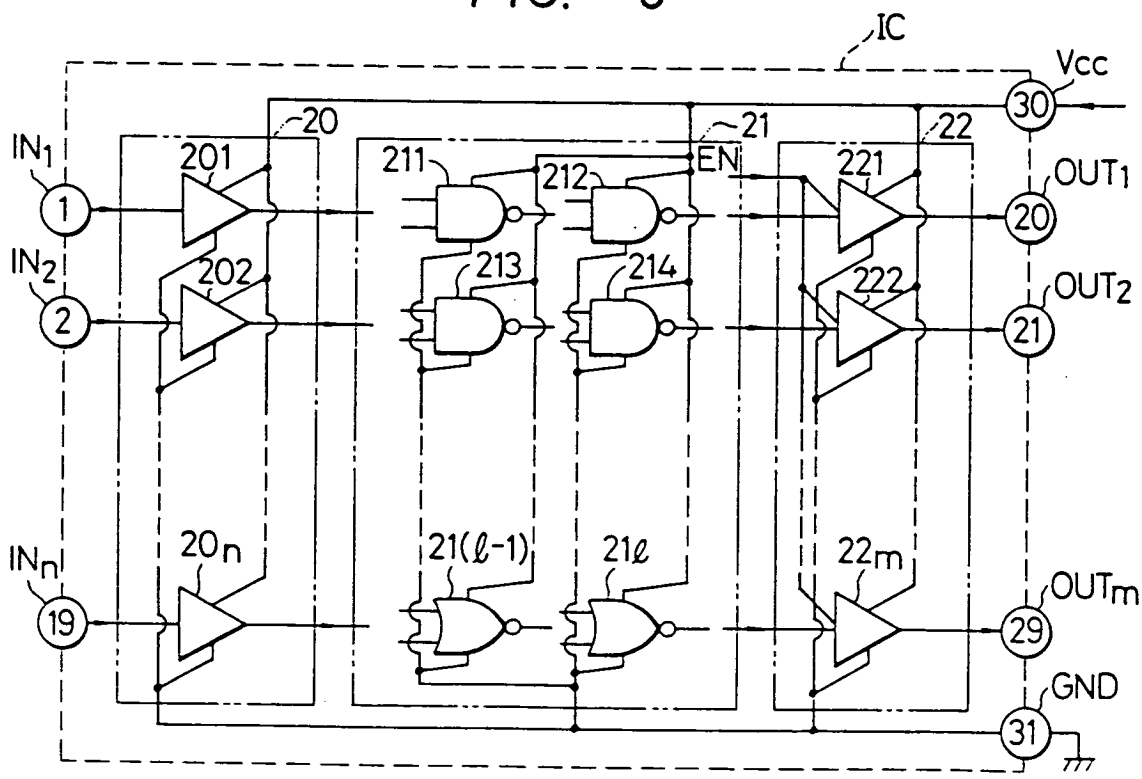

(nsec)
tPHL, tPLH
30
20
10
0
50
Cx(PF)
100
tPHL
tPHL34
tPLH
tPLH34

FIG. 6


IC
Vcc
30
20
21
22
EN
IN1
1
201
211
212
221
OUT1
20
IN2
2
202
213
214
222
OUT2
21
INn
19
20n
21(ℓ-1)
21ℓ
22m
OUTm
29
GND
31

DFA

4/12

FIG. 7

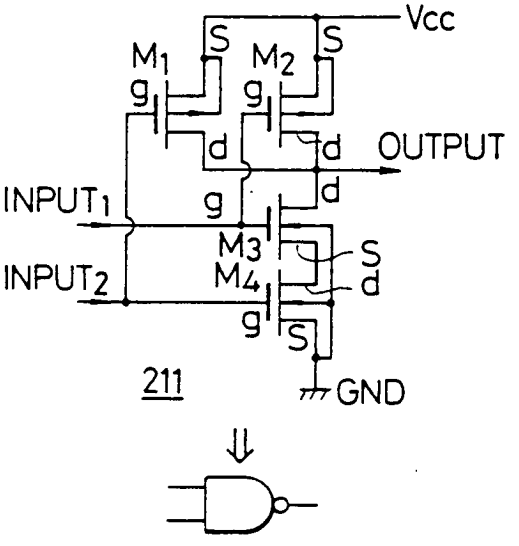


FIG. 8

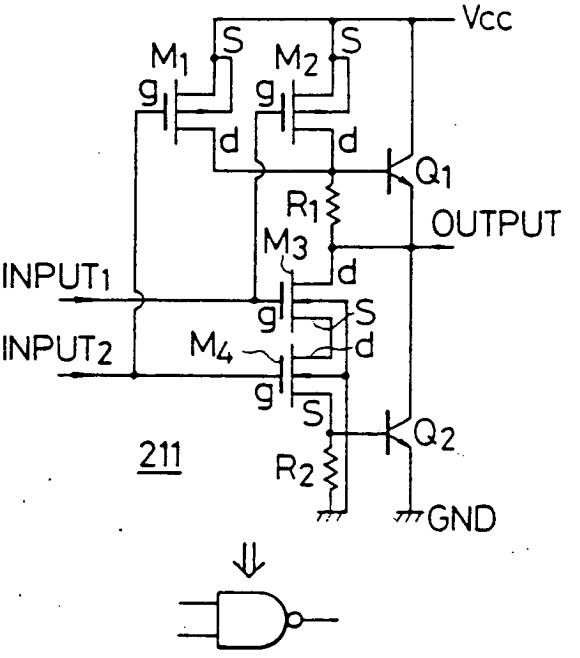


FIG. 9

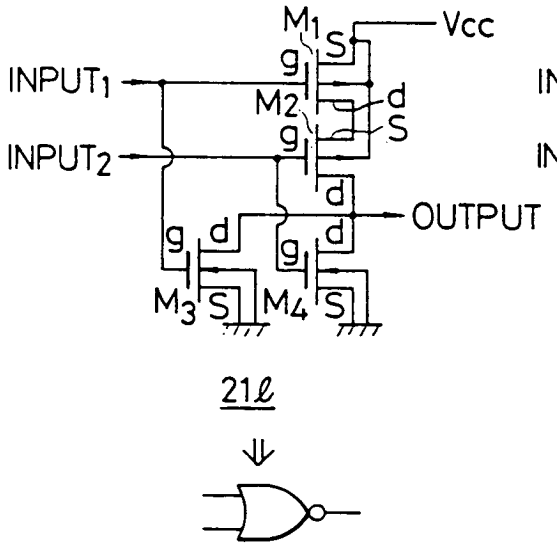


FIG. 10

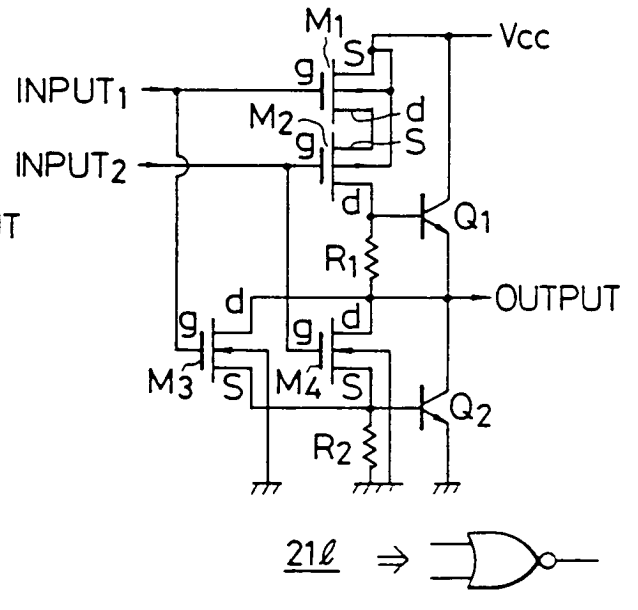


FIG. 11

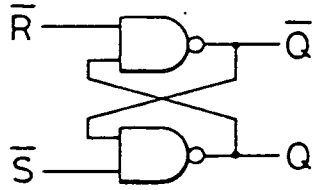


FIG. 12

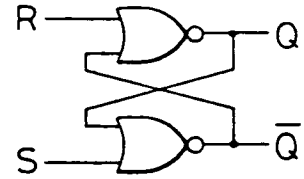


FIG. 13

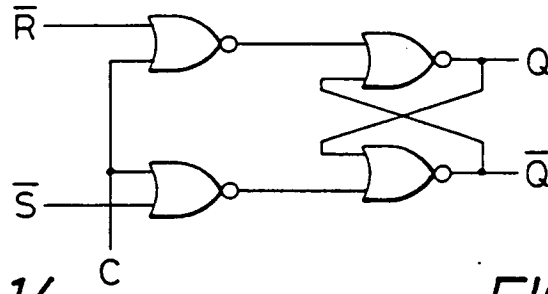


FIG. 14

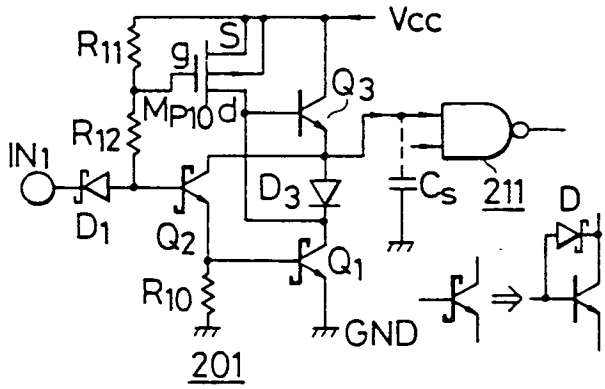


FIG. 15

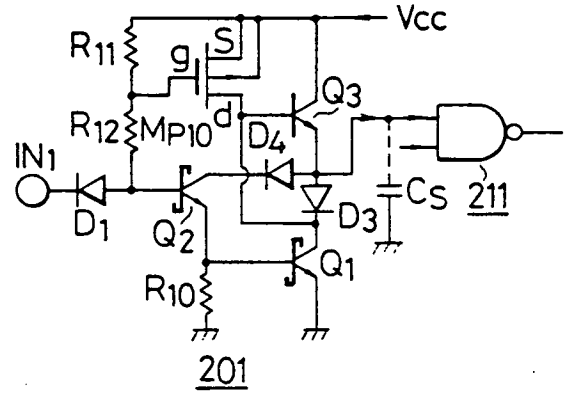


FIG. 16

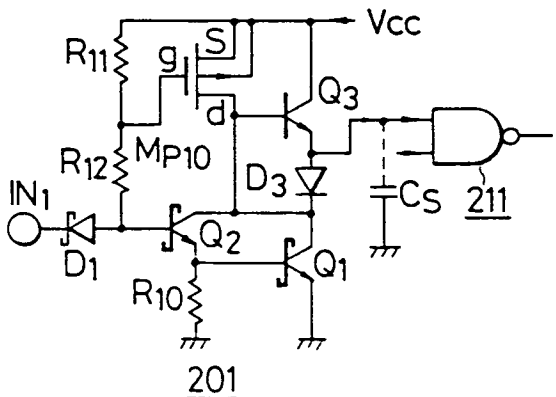


FIG. 17

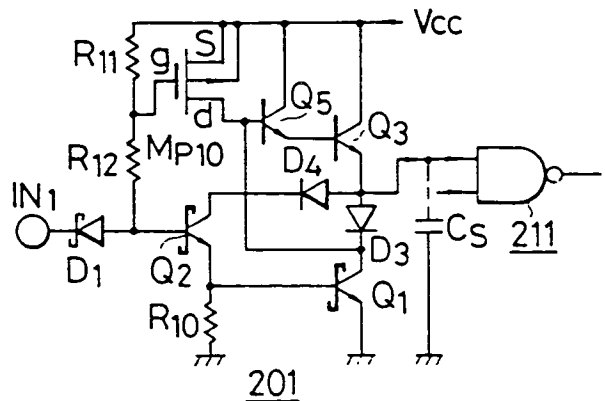


FIG. 18

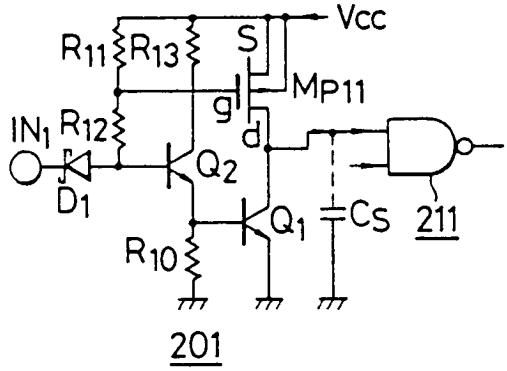


FIG. 19

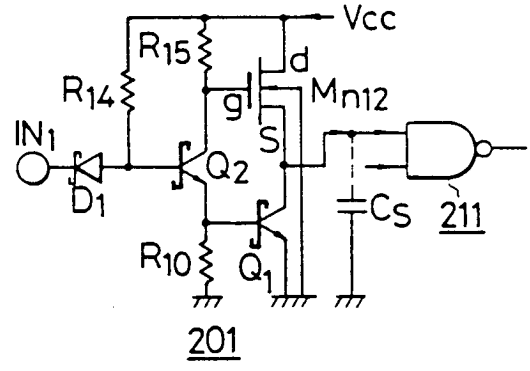


FIG. 20

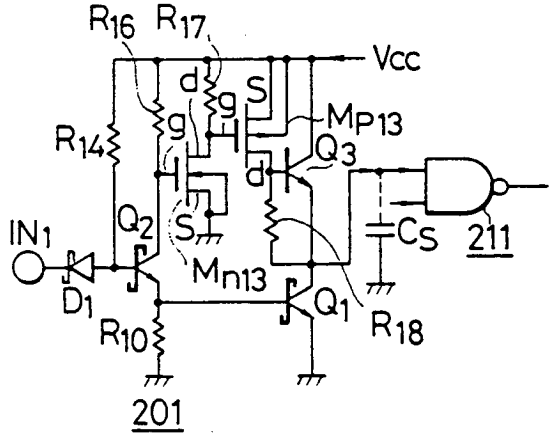


FIG. 21

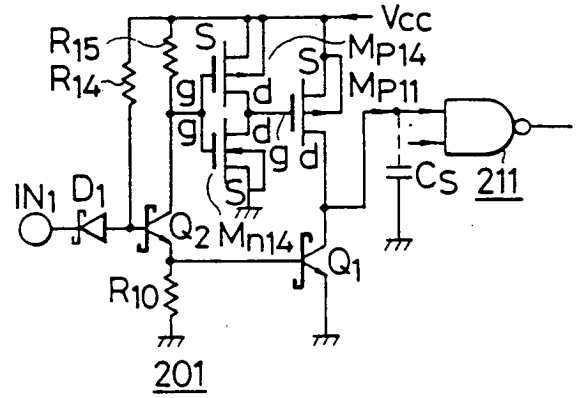


FIG. 22

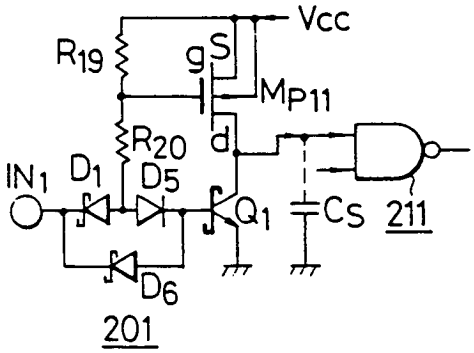


FIG. 23

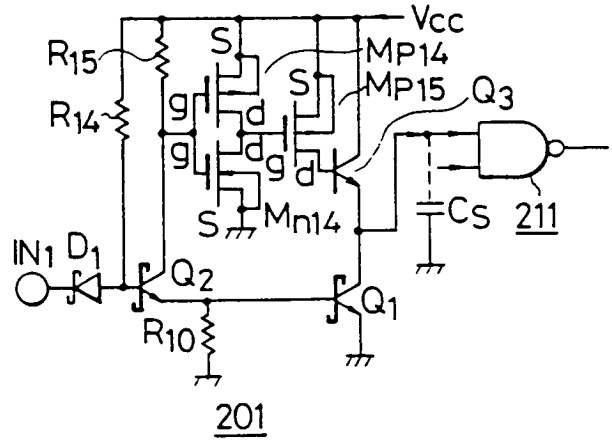


FIG. 24

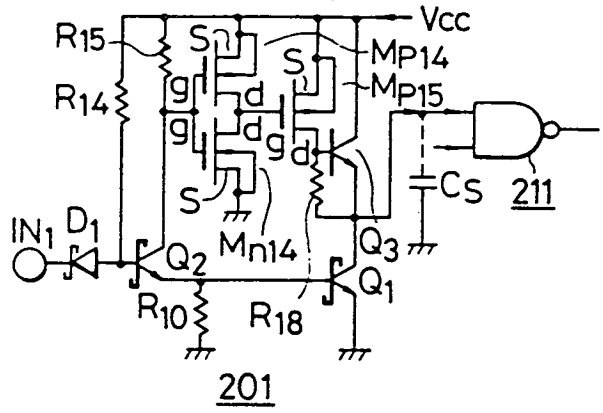


FIG. 25

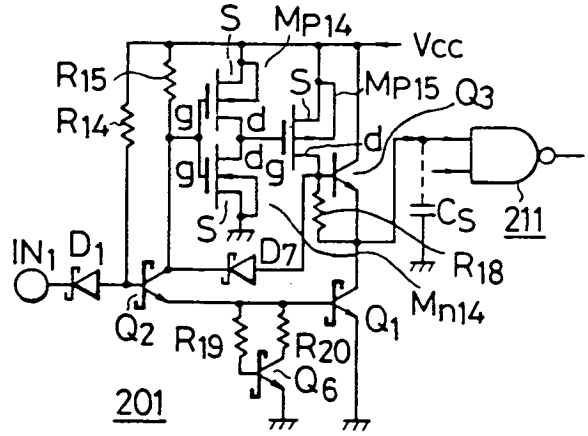


FIG. 26

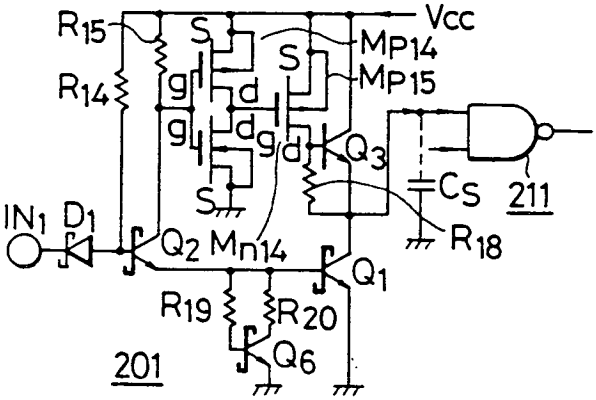


FIG. 27

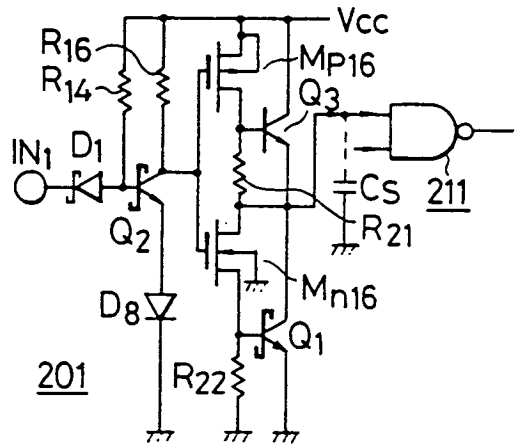


FIG. 28

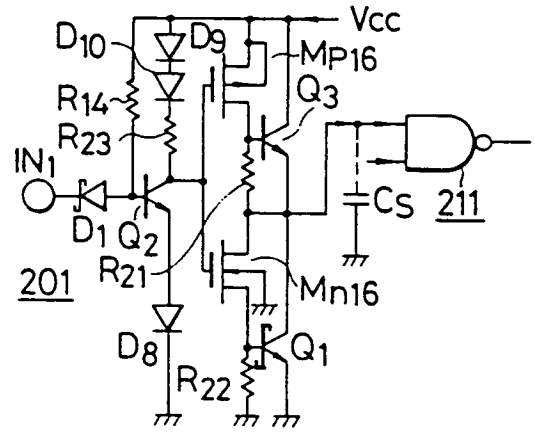


FIG. 29

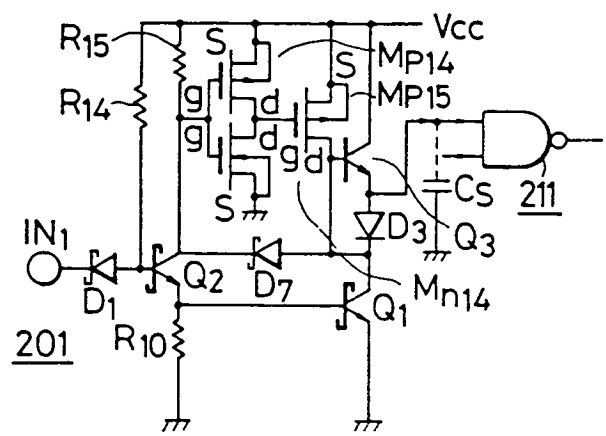


FIG. 30

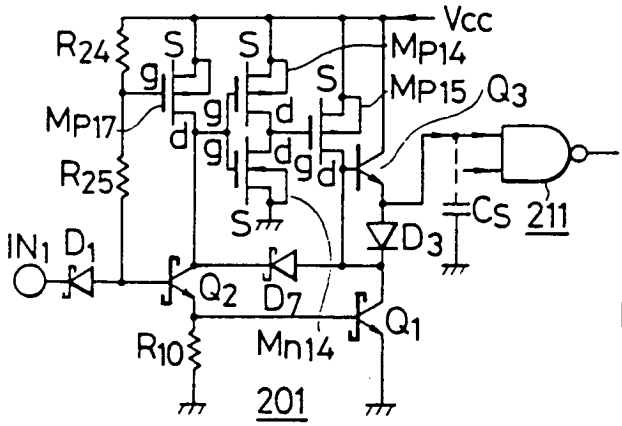


FIG. 31

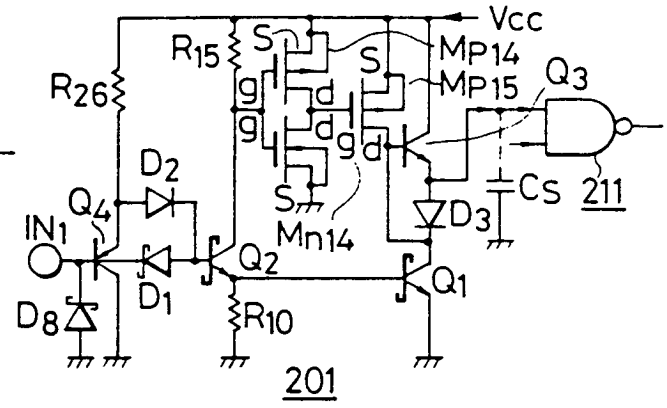


FIG. 32

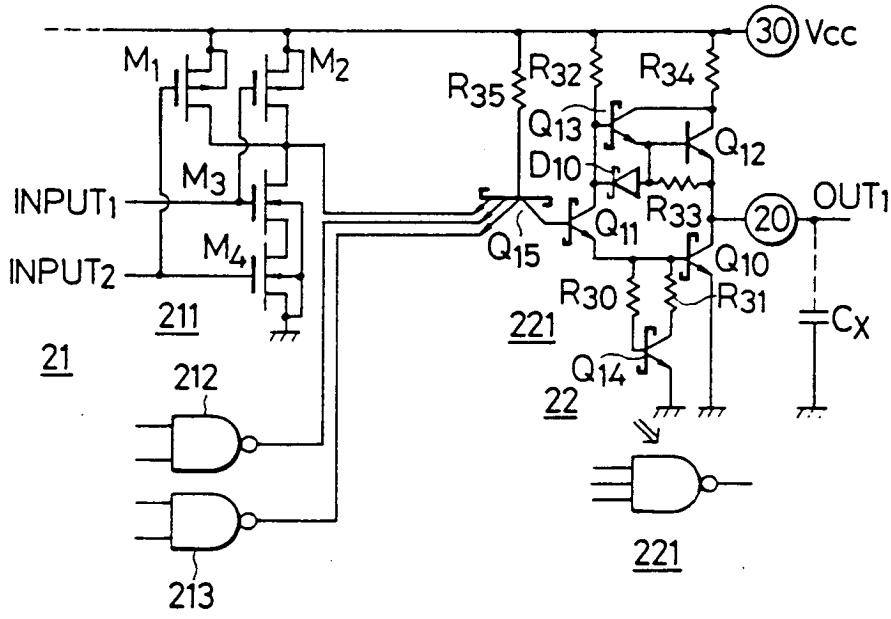


FIG. 35

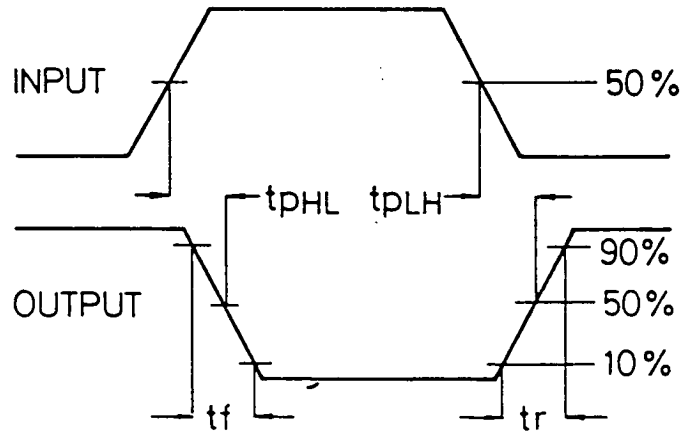


FIG. 33

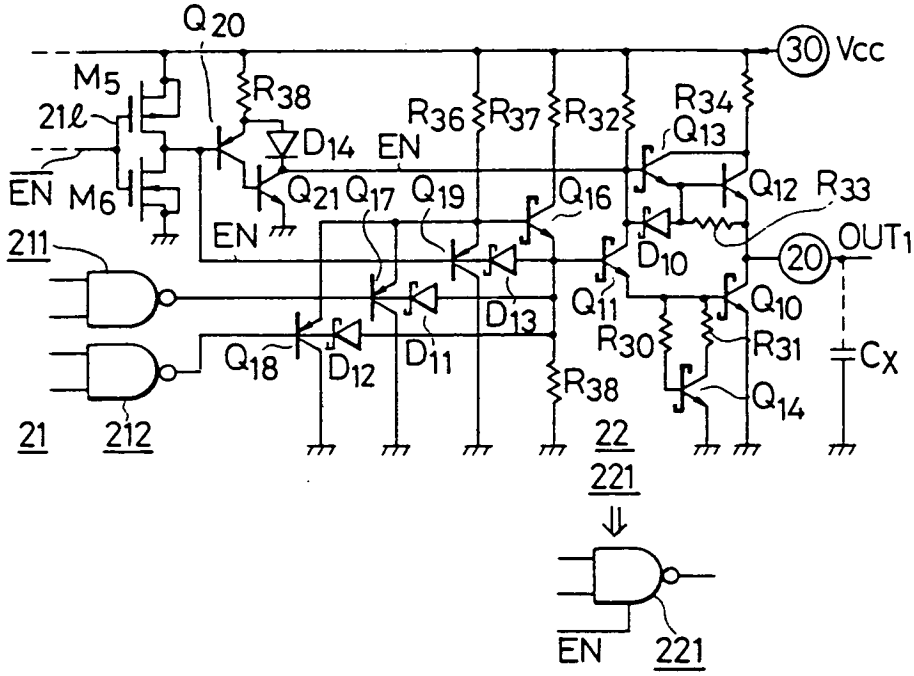

Q20
30
Vcc
M5
21ℓ
EN
M6
R38
D14
EN
R36
R37
R32
R34
Q13
Q21
Q17
Q19
Q16
Q12
R33
D10
20
OUT1
211
EN
D13
Q11
Q10
R30
R31
Cx
Q18
D12
D11
R38
Q14
21
212
22
221
EN
221

FIG. 34

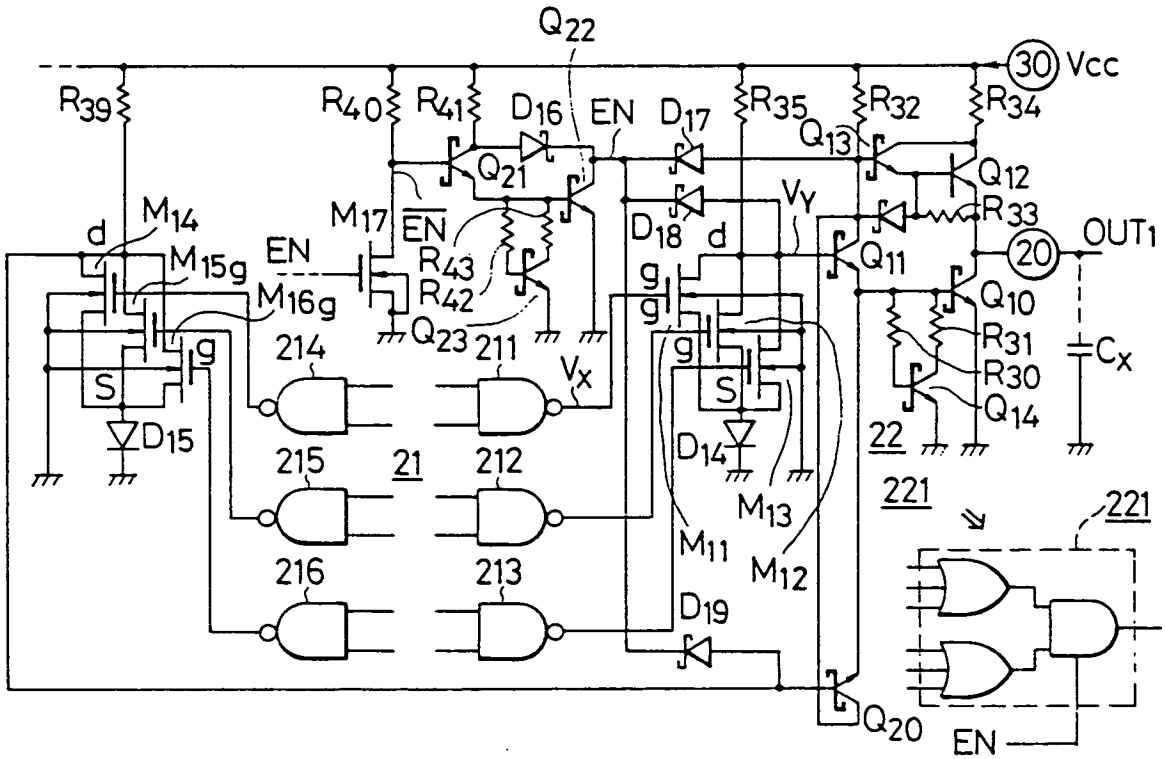

Q22
30
Vcc
R39
R40
R41
D16
EN
D17
R35
R32
R34
Q13
Q21
Q12
M14
M17
EN
D18
d
Vy
R33
OUT1
d
M15g
EN
R43
R42
Q11
20
M16g
g
g
Q10
Q23
211
214
Vx
g
g
R31
Cx
S
S
R30
Q14
D15
22
215
21
212
D14
M13
221
221
M11
M12
216
213
D19
Q20
EN

FIG. 36

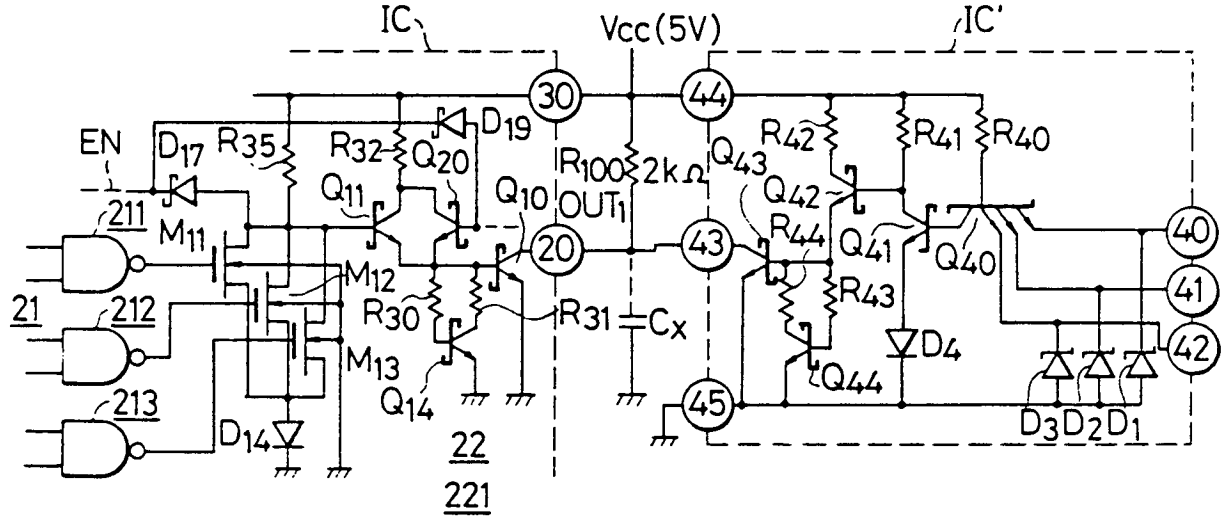

IC
Vcc(5V)
IC'
30
44
EN
D17
R35
R32
Q20
D19
R100
2kΩ
Q43
R42
R41
R40
211
M11
Q11
Q10
OUT1
20
43
R44
Q42
Q41
Q40
40
41
42
21
212
M12
R30
R31
Cx
R43
D4
213
M13
Q14
Q44
D14
22
45
D3
D2
D1
221

FIG. 37

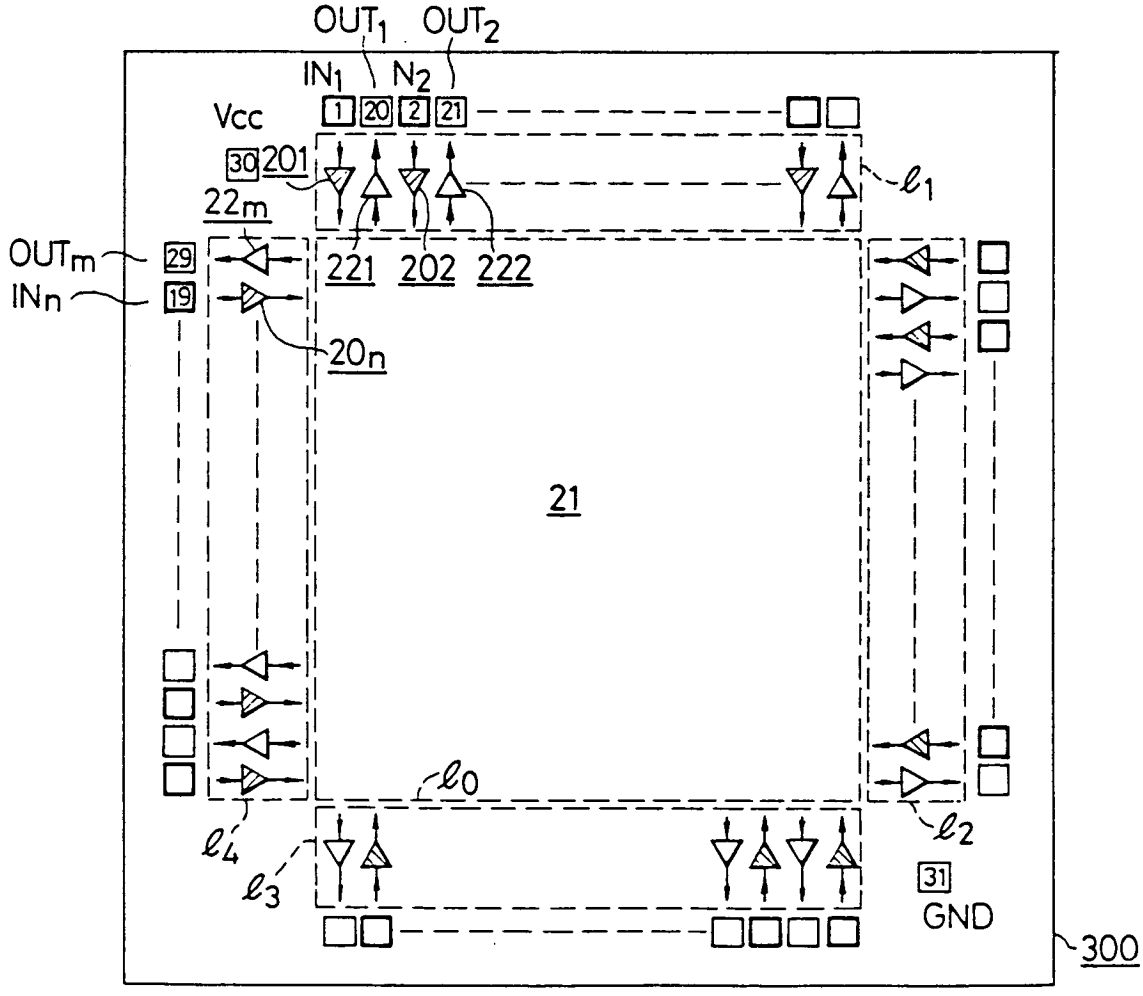

OUT1
OUT2
IN1
N2
Vcc
1
20
2
21
30
201
ℓ1
22m
OUTm
29
INn
19
221
202
222
20n
21
ℓ0
ℓ4
ℓ3
ℓ2
31
GND
300

FIG. 38

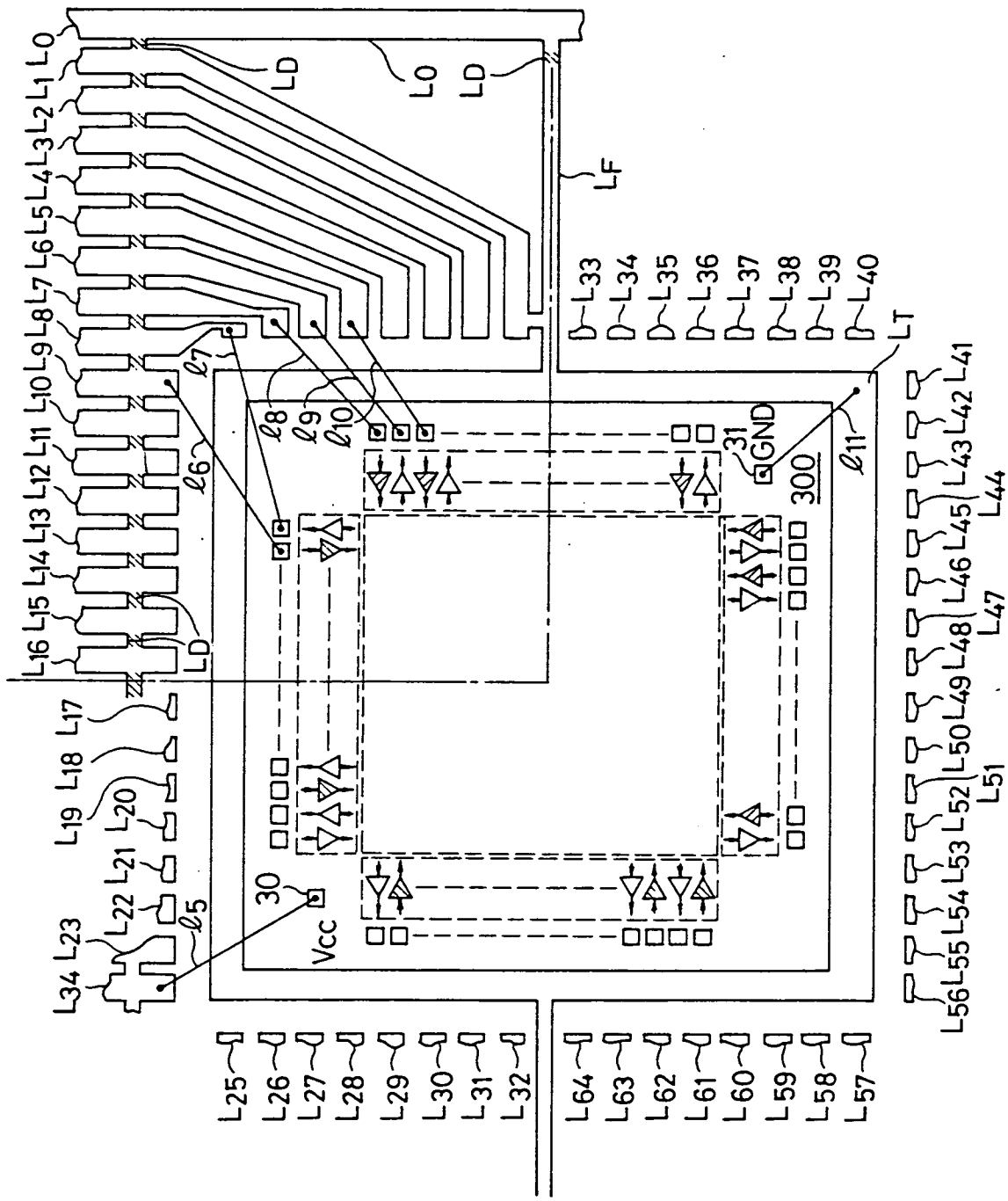

L0
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L25
L26
L27
L28
L29
L30
L31
L32
L33
L34
L35
L36
L37
L38
L39
L40
L41
L42
L43
L44
L45
L46
L47
L48
L49
L50
L51
L52
L53
L54
L55
L56
L57
L58
L59
L60
L61
L62
L63
L64
LD
LF
LT
ℓ5
ℓ6
ℓ7
ℓ8
ℓ9
ℓ10
ℓ11
30
Vcc
31
GND
300

FIG. 39

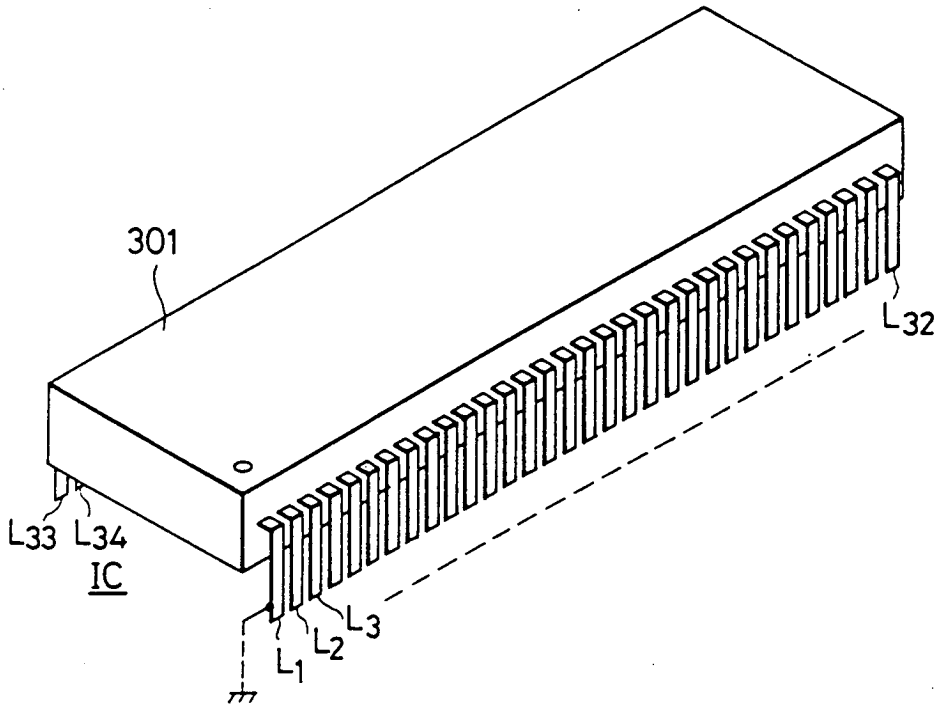
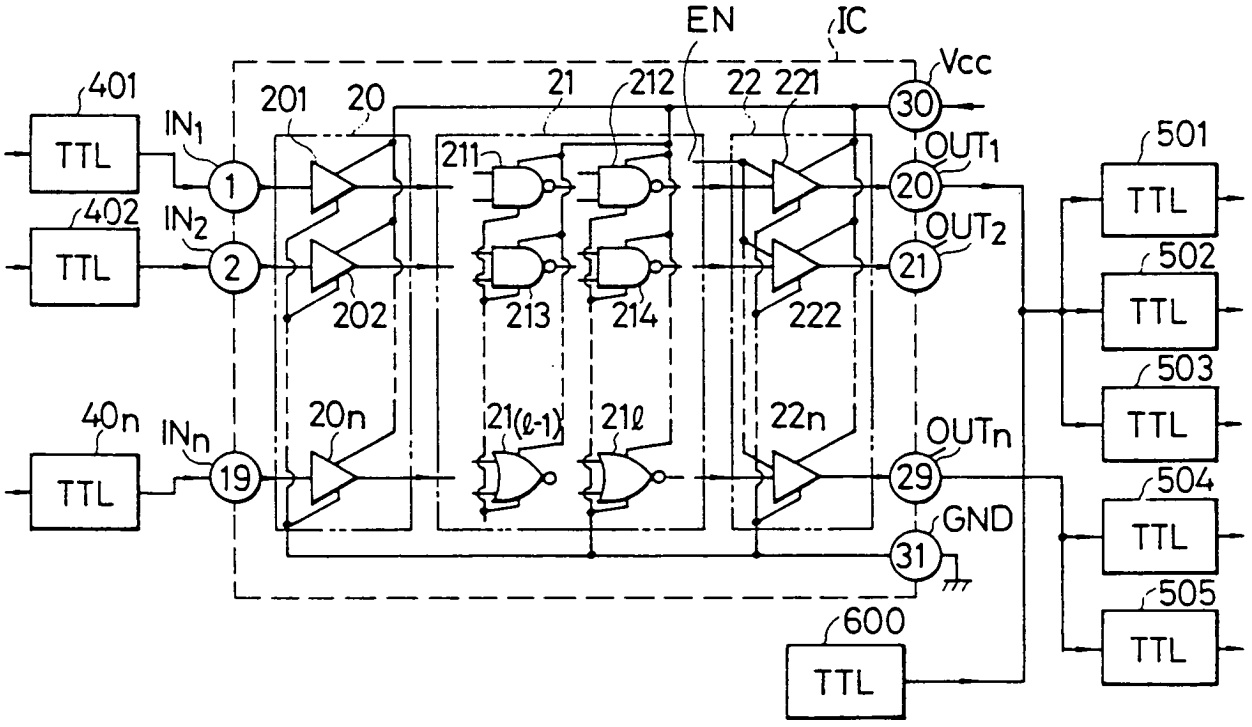

301
L32
L33
L34
IC
L1
L2
L3

FIG. 40


EN
IC
Vcc
401
TTL
IN1
1
201
20
21
212
22
221
30
OUT1
20
501
TTL
402
TTL
IN2
2
211
OUT2
21
502
TTL
202
213
214
222
503
TTL
40n
TTL
INn
19
20n
21(ℓ-1)
21ℓ
22n
OUTn
29
504
TTL
GND
31
505
TTL
600
TTL

"A semiconductor integrated circuit"

The present invention relates to a technique which is effective when applied to semiconductor integrated circuits, for example, a logic semiconductor integrated circuit whose input and output levels are TTL levels and whose internal logic levels are CMOS levels.

Figure 1 of the accompanying drawings is a block diagram of a known form of logic semiconductor integrated circuit IC having TTL levels as its input and output levels and CMOS levels as its internal logic levels.

The integrated circuit IC includes an input buffer 10 for level-converting input signals of TTL levels IN_1, IN_2, ... IN_n into signals of CMOS levels, an internal logic block 11 for executing logic operations with the CMOS levels, and an output buffer 12 for level-converting the CMOS level output signals of the internal logic block 11 into output signals of TTL levels OUT_1, OUT_2, ... OUT_m. The respective circuits 10, 11 and 12 are fed with a supply voltage V_{CC} of 5 volts, and are properly earthed.

A high level input voltage V_{iH10} to be supplied to the input terminals IN_1, IN_2, ... IN_n of the input buffer 10 is set at 2.0 volts or above, while a low level

input voltage V_{iL10} is set at 0.8 volt or below. Accordingly, an input threshold voltage V_{ith10} concerning the input terminals IN_1, IN_2, ... IN_n of the input buffer 10 is set at 1.3 - 1.5 volt which is between 0.8 volt and 2.0 volts.

On the other hand, a high level output voltage V_{0H10} to be derived from the output of the input buffer 10 is set to be equal to the high level input voltage V_{iH11} of the internal logic block 11, while a low level output voltage V_{oL10} to be derived from the output of the input buffer 10 is set to be equal to the low level input voltage V_{iL11} of the internal logic block 11. Accordingly, letting V_{TP} and V_{TN} denote the threshold voltages of a P-channel MOS FET and an N-channel MOS FET which constitute a CMOS inverter in the internal logic block 11, respectively, and V_{CC} denote the supply voltage, the above voltages V_{oH10}, V_{iH11}, V_{oL10} and V_{iL11} are respectively set as follows:

$$V_{oH10} = V_{iH11} > V_{CC} - |V_{TP}| \quad \text{..... (1)}$$

$$V_{oL10} = V_{iL11} < V_{TN} \quad \text{..... (2)}$$

When V_{CC} is set at 5 volts, $|V_{TP}|$ at 0.6 volt and V_{TN} at 0.6 volt, V_{oH10} and V_{iH11} are set at above 4.4 volts, and V_{oL10} and V_{iL11} at below 0.6 volt.

Accordingly, the input logic threshold voltage V_{ith11} of the CMOS inverter in the internal logic block 11 is set at approximately 2.5 volts which is between 0.6 volt

and 4.4 volts.

Likewise, the high level output voltage V_{oH11} of the internal logic block 11 and the high level input voltage V_{iH12} of the output buffer 12 are set at above 4.4 volts, the low level output voltage V_{oL11} of the internal logic block 11 and the low level input voltage V_{iL12} of the output buffer 12 are set at below 0.6 volt, and the input logic threshold voltage V_{ith12} of the output buffer 12 is set at approximately 2.5 volts which is between 0.6 volt and 4.4 volts.

In order to generate the output signals of TTL levels, the output buffer 12 has its high level output voltage V_{oH12} set at 2.7 volts or above and its low level output voltage V_{oL12} at 0.5 volt or below.

Fig. 2 of the accompanying drawings is a circuit diagram showing one known form of an input buffer 20 which is constructed of P-channel MOS FETs M_{p1}, M_{p2}, N-channel MOS FETs M_{n1}, M_{n2}, M_{n3} and a resistor R_p. The gates, sources and drains of the MOS FETs are respectively indicated by symbols g, s and d.

A first stage CMOS inverter composed of the FETs M_{p1} and M_{n1}, and a second stage CMOS inverter composed of the FETs M_{p2} and M_{n2} are connected in cascade. The components R_p and M_{n3} constitute a gate protection circuit for protecting the gate insulating films of the FETs

M_{p1} and M_{n1}. An output capacitance C_s connected to the drains of the FETs M_{p2} and M_{n2} of the second stage CMOS inverter has, in practice, its value determined by the drain capacitances of the FETs M_{p2} and M_{n2}, the wiring stray capacitance between the output of the input buffer 10 and the input of the internal logic block 11, and the input capacitance of the internal logic block 11.

The ratios W/L between the channel widths W and channel lengths L of the MOS FETs M_{p1}, M_{p2}, M_{n1}, M_{n2} and M_{n3} are respectively set at 27/3.5, 42/3, 126/3.5, 42/3 and 15/3. The resistor R_p is set at a resistance of 2 kiloohms.

Fig. 3 of the accompanying drawings is a graph illustrating the dependencies of the propogation delay times t_{pLH}, t_{pLH} of the input buffer 10 of Fig. 2 upon the output capacitances C_s. In the graph, the ordinate represents the propagation delay times while the abscissa represents the output capacitance C_s.

As illustrated in Fig. 35 of the accompanying drawings, the first propagation delay time t_{pHL} is defined as a period of time which is required since an input INPUT has changed with its 50% value as the boundary, until an output OUTPUT changing from a high level to a low level changes with its 50% value as the boundary. The second propagation delay time t_{pLH} is defined as a period of time which

is required since the input INPUT has changed with its 50% value as the boundary, until the output OUTPUT changing from the low level to the high level changes with its 50% value as the boundary. In Fig. 35, t_f is defined as a fall time, and t_r as a rise time.

Thus, as will be understood from Fig. 3 of the accompanying drawings, the output capacitance-dependency K_{HL} ($= \Delta t_{pHL}/\Delta C_s$) of the first propagation delay time t_{pHL} of the input buffer 10 in Fig. 2 is about 0.8 nsec/pF, and the output capacitance-dependency K_{LH} ($=\Delta t_{pLH}/\Delta C_s$) of the second propagation delay time t_{pLH} is about 1.4 nsec/pF. Both are great.

In the input threshold voltage V_{ith10} at approximately 1.3 - 1.5 volt, the ratios W/L between the channel widths and channel lengths of the FETs M_{p1} and M_{n1} of the first stage CMOS inverter are made greatly different, and in order to lessen the output capacitance-dependencies K_{HL} and K_{LH} of the respective propagation delay times t_{pHL} and t_{pLH}, both the ratios W/L of the FETs M_{p2} and M_{n2} of the second stage CMOS inverter are set at the large value of 42/3 so as to increase the channel conductances of these FETs M_{p2} and M_{n2}.

To the end of reducing both the output capacitance-dependencies K_{HL} and K_{LH}, the ratios W/L of the FETs M_{p2} and M_{n2} of the second stage CMOS inverter may be increased more and more. This, however, incurs

conspicuous increase in the occupation area of the input buffer 10 on the surface of an integrated circuit chip for the following reason, to form an obstacle to enhancement in the density of integration.

In the production technology of integrated circuits fining is being vigorously promoted at present. With the present-day photolithography based on exposure to ultraviolet radiation, however, the channel length L of a MOS FET is 3 μm as its lower limit value. In order to set the ratio W/L of the MOS FET at a very large value, therefore, the channel width W thereof must be set at an extraordinary large value. Eventually, the device area of the MOS FET increases conspicuously.

Fig. 4 of the accompanying drawings is a circuit diagram showing one output buffer 12 which we have investigated and which is constructed of a P-channel MOS FET M_{p4} and an N-channel MOS FET M_{n4}. The gates, sources and drains of the MOS FETs are respectively indicated by symbols g, s and d.

In the integrated circuit IC, the output signal of CMOS level from the internal logic block 11 is applied to the gates of the FETs M_{p4} and M_{n4} of the output buffer 12. Terminal No. 30 is fed with the supply voltage V_{CC} of 5 volts. In order to set the input logic threshold voltage V_{ith12} of the output buffer 12 at approximately 2.5 volts, accordingly,

the ratios W/L of the FETs M_{p4} and M_{n4} are set at values equal to each other.

Figure 4 also shows a TTL circuit 14, which is fed with the supply voltage V_{CC} of 5 volts through terminal No. 35. The output signal of TTL level from the output buffer 12 is derived from terminal No. 20, and is supplied to one emitter of the multi-emitter transistor Q_1 of the TTL circuit 14 through terminal No. 32.

Meanwhile, a standard TTL circuit, a Schottky TTL circuit, a low power Schottky TTL circuit and an advanced low power Schottky TTL circuit have been published as TTL circuits. Naturally, the characteristics of these circuits are somewhat different from one another.

The output of the output buffer 12 needs to drive a large number of inputs of the TTL circuit 14 at the same time and in parallel. A criterion for the drive ability is to be capable of driving 20 inputs of the low power Schottky TTL circuit in parallel.

When the output of the output buffer 12 is at its low level, a low level input current I_{IL} of 0.4 mA flows from one input of the low power Schottky TTL circuit into the drain-source path of the N-channel MOS FET M_{n4} of the output buffer 12. Accordingly, the FET M_{n4} needs to pass a total of 8 mA in order that the output buffer 12 may drive the aforementioned 20 inputs to the low level.

On the other hand, the low level output voltage V_{oL12} of the output buffer 12 must be 0.5 volt or below as already explained. Therefore, the ON-resistance R_{ON} of the N-channel MOS FET M_{n4} of the output buffer 12 must be set at a small value of 0.5 volt/8 milliampere = 62.5 ohms or so.

In order to make the ON-resistance R_{ON} of the FET M_{n4} such low resistance, the ratio W/L of the FET M_{n4} must be set at a very large value of 700/3 to 1000/3. Meanwhile, as stated above, both the ratios W/L of the FETs M_{p4} and M_{n4} need to be the equal values to the end of setting the input logic threshold voltage V_{ith12} of the output buffer 12 at approximately 2.5 volts. Therefore, also the ratio W/L of the P-channel MOS FET M_{p4} of the output buffer 12 must be set at the very large value of 700/3 to 1000/3.

This fact similarly brings about a substantial increase in the occupation area of the output buffer 12 on the surface of the integrated circuit chip, to hamper enhancement in the density of integration. Moreover, it incurs drastic lowering in the switching speed of the internal logic block 11 for the following reason.

When both the ratios W/L of the two MOS FETs M_{p4} and M_{n4} of the output buffer 12 are set at the large values, the gate capacitances of these MOS FETs become

large values proportionally. Since the gate capacitances of the FETs M_{p4} and M_{n4} constitute the output load capacitance of the internal logic block 11, these gate capacitances and the output resistance of the internal logic block 11 incur the lowering of the switching speed of the internal logic block 11.

Meanwhile, since the output of the output buffer 12 is not only derived from the external output terminal (terminal No. 20) of the integrated circuit IC, but also connected to the large number of input terminals of the TTL circuit 14 through external wiring, the output load capacitance C_x of the output buffer 12 often becomes a very large value.

Fig. 5 of the accompanying drawings is a graph illustrating the dependencies of the propagation delay times t_{pHL}, t_{pHL} upon the output load capacitance C_x of the output buffer 12 in Fig. 4. The ordinate represents the propagation delay times, while the abscissa represents the output load capacitance.

Thus, as understood from Figure 5, the capacitance-dependency K_{HL} $(=\Delta t_{pHL}/\Delta C_x)$ of the first propagation delay time t_{pHL} of the output buffer 12 in Figure 4 is about 0.3 nsec/pF, and the capacitance-dependency $K_{LH}(=\Delta t_{pLH}/\Delta C_x)$ of the second propagation delay time t_{pLH} is about 0.17 nsec/pF. Both are great.

Accordingly, the input buffer 10 of Figure 2 forming the background art of the present invention involves problems as summed up below.

(a) In order to lessen the output capacitance-dependencies of the propagation delay times of the input buffer 10, the ratios W/L of both the MOS FETs M_{p2} and M_{n2} of the second stage CMOS inverter of the input buffer 10 must be made large, which hampers enhancement in the density of integration. Particularly in a case where the integrated circuit IC is of the master slice type or the semi-custom gate array type, there is the possibility that a very large number of gate input terminals in the internal logic block 11 will be connected to the output of the input buffer 10. When the output capacitance C_s of the input buffer 10 accordingly becomes very great, the above problem is very serious.

(b) Further, the first stage of the input buffer 10 is formed of the CMOS inverter M_{p1}, M_{n1}. Therefore, even when the gate protection circuit composed of the elements R_p and M_{n3} is connected, the breakdown strengths of the gate insulating films of both the MOS FETs M_{p1}, M_{n1} against a surge voltage applied to the input terminal IN_1 are not satisfactory.

In addition, the output buffer 12 of Figure 4 forming the background art of the present invention involves

problems as summed up below.

(c) In order to set the input logic threshold voltage V_{ith12} of the output buffer 12 at approximately 2.5 volts and to enhance the current sink ability at the low level output of the output buffer 12, the ratios W/L of both the MOS FETs M_{p4} and M_{n4} must be set at large values equal to each other, which hampers enhancement in the density of integration.

(d) When the ratios W/L of both the MOS FETs M_{p4} and M_{n4} of the output buffer 12 are made large, also the gate capacitances of these MOS FETs increase. In consequence, these gate capacitances and the output resistance of the internal logic block 11 incur lowering in the switching speed of the internal logic block 11. Particularly in a case where the output stage of the internal logic block 11 is composed of MOS FETs of high output resistance, the lowering of the switching speed is conspicuously problematic.

(e) Since the output buffer 12 is composed of the MOS FETs M_{p4} and M_{n4}, the dependencies of the propagation delay times upon the output load capacitance C_x are great. Particularly in a case where a large number of input terminals of the TTL circuit 14 are connected to the output of the output buffer 12, this problem becomes important.

According to the present invention there is provided a semiconductor integrated circuit including:

(a) an internal logic block including a plurality of quasi-CMOS circuits, the input stage of each of said quasi-CMOS circuits including P-channel and N-channel MOSFETs, and the output stage of each of said quasi-CMOS circuits including bipolar transistors; said internal logic block performing logic operations on input signals and generating output signals based upon the logic operations; and

(b) an output level converter having an input terminal coupled to receive at least one of said output signals of said internal logic block, in order to thereby provide an output signal of predetermined levels different than that of CMOS levels at an output terminal of said output level converter;

wherein an output transistor of said output level converter for executing charge or discharge of an output load capacitance of said output level converter is formed as a first bipolar output transistor; and

wherein said output level converter further comprises a high input impedance circuit which is connected between a base of said first bipolar output transistor and said input terminal of said output level converter.

The semiconductor integrated circuit may further include:

(c) a driver transistor which drives said first bipolar output transistor for executing the discharge of the output load capacitance; and

(d) a second bipolar output transistor for executing the charge of said output load capacitance, in response to the input signal of said input terminal of said output level converter.

The high input impedance circuit may be constructed of MOSFETs, and may logically process a plurality of output signals of said internal logic block.

The semiconductor integrated circuit may further include:

(e) a control circuit which turns "off" the discharging first bipolar output transistor and the charging second bipolar output transistor of said output level converter simultaneously in response to a control signal, in order to thereby bring said output terminal of said output level converter into a float state.

The present invention will now be described in greater detail by way of examples with reference to the remaining figures of the accompanying drawings, wherein:-

Fig. 6 shows a block diagram of a preferred form of a logic semiconductor integrated circuit;

Figs. 8 and 10 respectively show circuit examples within the scope of the invention of a CMOS·NAND gate 211 and a CMOS·NOR gate 21ℓ in the circuit of Fig. 6;

Figs. 7 and 9 respectively show circuit examples outside the scope of the invention of a CMOS·NAND gate 211 and a CMOS·NOR gate 21ℓ in the circuit of Fig. 6; it being appreciated that these examples are outside the scope of the present invention because they show only pure CMOS circuit, whereas those examples shown in Figs. 8 and 10 as well as the following examples show quasi CMOS circuits;

Figs. 11 and 12 show circuit examples of CMOS R-S flip-flops within an internal logic block 21 in the circuit of Fig. 6;

Fig. 13 shows a circuit example of a CMOS gated R-S flip-flop within the internal logic block 21 in the circuit of Figure 6;

Figs. 14 to 31 show diagrams of various preferred forms of circuits of the level converter 201 of an input buffer 20;

Figs. 32 to 34 and Fig. 36 show diagrams of

various preferred forms of circuits of the level converter 221 of an output buffer 21;

Fig. 35 shows a diagram of input and output waveforms for defining first and second propagation delay times t_{pHL}, t_{pLH};

Fig. 37 shows the layout of various circuit blocks on a semiconductor chip surface in a logic semiconductor integrated circuit;

Fig. 38 shows a structural diagram illustrative of the state of connection of a semiconductor chip to the tab lead L_T of a lead frame L_F and connection of bonding wires in a logic semiconductor integrated circuit;

Fig. 39 shows a diagram of the completion of a circuit resin moulding; and

Fig. 40 shows a block diagram of an electronic system constructed in such a way that a preferred form of circuit according to the present invention and another circuit are packaged on a printed circuit board.

The logic integrated circuit shown in Fig. 6 includes a TTL - CMOS level conversion input buffer 20 which executes an operation similar to that of the input buffer 10 in Fig. 1, an internal logic block 21 which operates with CMOS levels similarly to the internal logic block 11 in Fig. 1, and a CMOS - TTL level conversion output buffer 22 which executes an operation similar to that of the output buffer 12 in Fig. 1. The respective circuits 20, 21 and 22 are fed with a supply voltage

V_{CC} of 5 volts through terminal No. 30, and are earthed through terminal No. 31.

The input buffer 20 has a plurality of TTL - CMOS level converters 201, 202, ... 20n, the respective inputs of which are connected to terminal No. 1, terminal No. 2, ... terminal No. 19 and the respective outputs of which are connected with the internal logic block 21 by aluminium wiring layers inside the circuit IC.

The internal logic block 21 includes CMOS·NAND gates 211, 212, 213, 214, CMOS·NOR gates 21 (ℓ - 1), 21ℓ, and if necessary, CMOS exclusive OR gates, CMOS transmission gates, CMOS inverters.

As shown in the example of Fig. 7, which as noted above is outside the scope of the present invention because it relates to a pure CMOS circuit, the CMOS·NAND gate 211 includes P-channel MOS FETs M_1, M_2 and N-channel MOS FETs M_3, M_4. Another example of the CMOS·NAND gate 211 within the scope of the invention can be constructed of a quasi-CMOS circuit which further includes N-P-N transistors Q_1, Q_2 and resistors R_1, R_2 as shown in Fig. 8. Since such quasi-CMOS circuit has its output stage composed of the bipolar transistors Q_1, Q_2, the output drive ability is enhanced, and the output load capacitance-dependency of the propagation delay time can be lessened.

As shown in the example of Fig. 9, which as noted above is outside the scope of the present invention because it relates to a pure CMOS circuit, the CMOS·NOR gate 21ℓ includes P-channel MOS FETs M_1, M_2 and N-channel MOS FETs M_3, M_4. Another example of the CMOS·NOR gate 21ℓ within the scope of the invention can be constructed of a quasi-CMOS circuit which further includes N-P-N transistors Q_1, Q_2 and resistors R_1, R_2 as shown in Fig. 10. Since such quasi-CMOS circuit has its output stage composed of the bipolar transistors Q_1, Q_2, the output drive ability is enhanced, and the output load capacitance-dependency of the propagation delay time can be lessened.

In the internal logic block 21, these CMOS·NAND gates and CMOS·NOR gates are connected in various forms in accordance with the master slice type or the semi-custom gate array type.

For example, an R-S flip-flop is constructed by combining two of the CMOS·NAND gates as shown in Fig. 11

or by combining two of the CMOS·NOR gates as shown in Figure 12. Further, a gated R-S flip-flop which is controlled by a clock signal C is constructed by combining four of the CMOS·NOR gates as shown in Figure 13.

In this manner, in the logic semiconductor integrated circuit IC of the master slice type or the gate array type conforming to the needs of users, the outputs of the level converters 201, 202, ····· 20n of the input buffer 20 and the inputs of the various gates or inverters of the internal logic block 21 are connected in various forms by altering only the wiring pattern thereof. Similarly, the outputs of the various gates or inverters of the internal logic block 21 and the inputs of the level converters 221, 222, ····· 22m of the output buffer 22 are connected in various forms.

The output buffer 22 has the plurality of CMOS - TTL level converters 221, 222, ····· 22m, the respective outputs of which are connected to terminal No. 20, terminal No. 21, ····· terminal No. 29.

The essential features of the level converters 201, 202, ····· 20n of the input buffer 20 are as stated below.

(a) The input threshold voltage V_{ith} of each of the level converters 201, 202, ····· 20n is set between a TTL low level input voltage of 0.8 volt and a TTL

high level input voltage of 2.0 volts.

(b) An output transistor, which executes the charge or discharge of the output capacitance C_s of each of the level converters 201, 202, ····· 20n in response to an input signal supplied to the input terminal thereof, is formed of a bipolar transistor.

Further, meritorious features in preferable aspects of performance of the level converters 201, 202, ····· 20n of the input buffer 20 are as stated below.

(c) A Schottky barrier diode is connected between the base and collector of the bipolar output transistor Q_1 which executes the discharge of the output capacitance C_s in the above item (b)

(d) A second Schottky barrier diode is connected between the base and collector of a driver transistor Q_2 which serves to drive the base of the bipolar output transistor Q_1 with its output in response to the input signal supplied to the input terminal of each of the level converters 201, 202, ····· 20n.

(e) The output transistor which executes the charge of the output capacitance C_s of each of the level converters 201, 202, ····· 20n is also formed of a bipolar transistor Q_3.

(f) The base signal or collector signal of the driver transistor Q_2 is transmitted to the base of the charging bipolar output transistor Q_3 through a MOS buffer which

has a high input impedance and an amplifying function.

(g) A Schottky barrier diode D_1 for level shift is connected between the input terminal of each of the level converters 201, 202, ····· 20n and the base of the driver transistor Q_2.

(h) A P-N-P emitter follower transistor Q_4 and a P-N junction diode for level shift D_2 are connected between the input terminal of each of the level converters 201, 202, ····· 20n and the base of the driver transistor Q_2.

Figures 14 to 31 show diagrams of various circuits of the level converter 201 of the input buffer 20 according to embodiments of the present invention. All these level converters have the essential features of the above items (a) and (b). Further, these level converters have at least one of the meritorious features of the above items (c) to (h).

In the level converter 201 of Figure 14, the input terminal IN_1 is connected to the cathode of the Schottky barrier diode for level shift D_1, the anode of which is connected to the base of the driver transistor Q_2. The kind of the barrier metal of this diode D_1 and the barrier area thereof are determined so as to set the forward voltage V_F thereof at 0.35 volt to 0.41 volt. The forward voltages V_F of the Schottky barrier diodes D_1 of the level converters in Figures 15 to 31 are similarly set at 0.35 volt to 0.41 volt.

Further, in the arrangement of Figure 14, each of the driver transistor Q_2 and the discharging output transistor Q_1 has a Schottky barrier diode D connected between the base and collector thereof as indicated by the hook-shaped base electrode symbol thereof. As is well known, the clamped transistor provided with the Schottky barrier diode in this manner has a very short storage time. In the ensuing embodiments, transistors having hook-shaped base electrode symbols are such clamped transistors. The base of the discharging output transistor Q_1 is connected to earth through a resistor of 5 kiloohms R_{10} for discharging the base charges thereof.

Besides, in the arrangement of Figure 14, a resistor of 18 kiloohms R_{11} and a resistor of 2 kiloohms R_{12} are connected in series between the supply voltage V_{CC} and the anode of the Schottky barrier diode D_1. The junction between the resistors R_{11} and R_{12} is connected to the gate of a P-channel MOS FET M_{p10} which serves as a phase inverter, and the drain of which is connected to the base of the charging output transistor Q_3.

Further, a diode D_3 is connected in order to reliably turn "off" the transistor Q_3 when the level converter 201 produces its low level output. The output of the level converter 201 at the emitter of the charging output

transistor Q_3 is connected to the output capacitance C_s, and is also connected to one input of the CMOS-NAND gate 211 of the internal logic block 21.

The emitter area of each of the bipolar transistors Q_1, Q_2 and Q_3 is set at 100 μm^2 to 144 μm^2, and can also be set at a still smaller area. Further, the ratio W/L of each MOS FET is set at a value of 32/3 to 64/3.

We have been able to demonstrate that the embodiment of Figure 14 having the above arrangement exhibits propagation delay times and the output capacitance-dependencies thereof listed below:

t_{pHL} (for C_s = 0 pF) ····· 1.6 nsec
t_{pLH} (for C_s = 0 pF) ····· 5.7 nsec
K_{HL} ····· 0.4 nsec/pF
K_{LH} ····· 0.4 nsec/pF

It can be appreciated that the aforementioned propagation delay times t_{pHL}, t_{pLH} and output capacitance-dependencies K_{HL}, K_{LH} are excellent as compared with the characteristics of the input buffer 10 in Figure 2.

Moreover, the level converter 201 in Figure 14 can attain desired characteristics for reasons stated below.

(a) The forward voltage V_F of the Schottky barrier diode D_1 is set at 0.35 to 0.41 volt, and the base-emitter voltages V_{BE1}, V_{BE2} of the transistors Q_1, Q_2 are approximately 0.75 volt. Therefore, the input threshold voltage V_{ith}

of the level converter 201 is set as follows:

$$V_{ith} = -V_F + V_{BE1} + V_{BE2}$$

$$= 1.09 \text{ to } 1.15 \text{ volt}$$

(b) The output transistors Q_1, Q_3 for executing the charge or discharge of the output capacitance C_s of the level converter 201 are formed of the bipolar transistors of low output resistances. Therefore, the switching operation speeds can be raised or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) The Schottky barrier diode is connected between the base and collector of each of the transistors Q_1, Q_2 which are driven into their saturation regions. Therefore, when both the transistors Q_1, Q_2 operate to switch from "on" into "off", the storage times can be shortened.

(d) When the potential of the node of the resistors R_{11} and R_{12} rises to turn "off" the phase inverting MOS FET M_{p10} and the charging output transistor Q_3, current to flow from the node into the gate of the MOS FET M_{p10} becomes very small because the input impedance of the gate of the MOS FET M_{p10} is very high. Accordingly, the embodiment enhances an operating speed for switching the charging output transistor Q_3 from "off" into "on" when compared with a case of forming the phase inverter by the use of a bipolar transistor, not the MOS FET M_{p10}.

The level converter 201 of Figure 15 differs from that of Figure 14 only in that another P-N junction diode D_4 is added. Such addition of the diode D_4 makes it possible to lower the low level output voltage of the level converter still more.

Regarding the level converter 201 of Figure 15, the propagation delay times and the output capacitance-dependencies thereof have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 1.89 nsec
t_{pLH} (for C_s = 0 pF) ····· 6.37 nsec
K_{HL} ····· 0.4 nsec/pF
K_{LH} ····· 0.4 nsec/pF

Further, also the level converter 201 of Figure 15 can attain desired characteristics for the same reasons as in the case of Figure 14.

The level converter 201 of Figure 16 differs from that of Figure 14 only in the collector connection of the driver transistor Q_2. The propagation delay times and their output capacitance-dependencies of such level converter in Figure 16 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 1.81 nsec
t_{pLH} (for C_s = 0 pF) ····· 5.08 nsec
K_{HL} ····· 0.4 nsec/pF
K_{LH} ····· 0.4 nsec/pF

Also the level converter 201 of Figure 16 can attain desired characteristics for the same reasons as in the case of Figure 14.

The level converter 201 of Figure 17 differs from that of Figure 15 only in that another N-P-N transistor Q_5 is connected between the drain of the phase inverting MOS FET M_{p10} and the base of the charging output transistor Q_3. The propagation delay times and their output capacitance-dependencies of such level converter in Figure 17 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 2.01 nsec
t_{pLH} (for C_s = 0 pF) ····· 7.30 nsec
K_{HL} ····· 0.4 nsec/pF
K_{LH} ····· 0.4 nsec/pF

In the level converter 201 of Figure 18, the transistors Q_1, Q_2 are clamped transistors with Schottky barrier diodes, and the base of the discharging output transistor Q_1 is connected to earth through the resistor of 5 kiloohms R_{10} for discharging base charges. In addition, a resistor of 20 kiloohms R_{13} for limiting a collector current is connected to the collector of the transistor Q_2.

The resistor of 18 kiloohms R_{11} and the resistor of 2 kiloohms R_{12} are connected in series between the supply voltage V_{CC} and the anode of the Schottky barrier diode D_1.

The junction between the resistors R_{11} and R_{12} is connected to the gate of a P-channel MOS FET M_{p11} serving as a charging output transistor. In addition, the ratio W/L of this FET M_{p11} is 64/3.

The propagation delay times and their output capacitance-dependencies of such level converter 201 in Figure 18 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 1.9 nsec

t_{pLH} (for C_s = 0 pF) ····· 2.9 nsec

K_{HL} ····· 0.4 nsec/pF

K_{LH} ····· 1.3 nsec/pF

Further, the level converter 201 in Figure 18 can attain desired characteristics for reasons stated below.

(a) Likewise to the case of Figure 14, the input threshold voltage V_{ith} of the level converter 201 can be set at 1.09 to 1.15 volt.

(b) The output transistor Q_1 for executing the discharge of the output capacitance C_s of the level converter 201 is formed of the bipolar transistor of low output resistance. Therefore, the speed of a switching operation at the discharge of the output capacitance can be enhanced or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) Likewise to the case of Figure 14, the storage times

of the transistors Q_1, Q_2 can be shortened.

In the level converter 201 of Figure 19, the transistors Q_1, Q_2 are the clamped transistors with the Schottky barrier diodes, and the base of the discharging output transistor Q_1 is connected to earth through the resistor of 5 kiloohms R_{10} for discharging base charges. A load resistor of 8 kiloohms R_{15} is connected to the collector of the transistor Q_2, and a resistor of 20 kiloohms R_{14} is incorporated between the supply voltage V_{CC} and the anode of the Schottky barrier diode D_1. The collector signal of the driver transistor Q_2 is applied to the gate of an N-channel MOS FET M_{n12} which serves as a charging output transistor. In addition, the ratio W/L of this FET M_{n12} is set at 64/3.

The propagation delay times and their output capacitance-dependencies of such level converter 201 in Figure 19 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 1.1 nsec
t_{pLH} (for C_s = 0 pF) ····· 8.6 nsec
K_{HL} ····· 0.3 nsec/pF
K_{LH} ····· 2.0 nsec/pF

Further, the level converter 201 of Figure 19 can attain desired characteristics for reasons similar to those in the case of Figure 18.

In the level converter 201 of Figure 20, the transistors

Q_1, Q_2 are similarly the clamped transistors, and the base of the discharging output transistor Q_1 is connected to earth through the resistor of 5 kiloohms R_{10} for discharging base charges. A load resistor of 10 kiloohms R_{16} is connected to the collector of the transistor Q_2, and the resistor of 20 kiloohms R_{14} is connected between the supply voltage V_{CC} and the anode of the Schottky barrier diode D_1. The collector signal of the driver transistor Q_2 is applied to the gate of an N-channel MOS FET M_{n13} serving as an amplifier transistor, the ratio W/L of the FET M_{n13} is set at 32/3, and a load resistor of 20 kiloohms R_{17} is connected to the drain of the FET M_{n13}. The drain signal of the FET M_{n13} is applied to the gate of a P-channel MOS FET M_{p13} serving as an amplifier transistor, the ratio W/L of the FET M_{p13} is set at 64/3, and a resistor of 10 kiloohms R_{18} which serves as a load resistor and also as a resistor for discharging the base charges of the charging bipolar output transistor Q_3 is connected to the drain of the FET M_{p13}.

The propagation delay times and their output capacitance-dependencies of such level converter 201 in Figure 20 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 2.2 nsec

t_{pLH} (for C_s = 0 pF) ····· 7.5 nsec

K_{HL} ····· 0.4 nsec/pF

K_{LH} ····· 0.4 nsec/pF

Further, the level converter 201 in Figure 20 can attain desired characteristics for reasons stated below.

(a) Likewise to the case of Figure 14, the input threshold voltage V_{ith} of the level converter 201 can be set at 1.09 to 1.15 volt.

(b) Likewise to the case of Figure 14, the speed of a switching operation for the charge or discharge of the output capacitance C_s can be enhanced or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) Likewise to the case of Figure 14, the storage times of the transistors Q_1, Q_2 can be shortened.

(d) When the collector potential of the driver transistor Q_2 rises to operate the charging output transistor Q_3 so as to switch from "off" into "on", the amplifier MOS FETs M_{n13} and M_{p13} amplify the change of the collector potential of the transistor Q_2 and transmit the amplified signal to the base of the transistor Q_3. Moreover, since the gate input impedance of the MOS FET M_{n13} is very high, a great base current is inhibited from directly flowing from the collector of the transistor Q_2 into the base of the transistor Q_3. Therefore, the switching speed of the output transistor Q_3 can be enhanced.

In the level converter 201 of Figure 21, Q_1 and Q_2 indicate the clamped transistors, and D_1 indicates the Schottky barrier diode for level shift. The resistors R_{10}, R_{14} and R_{15} are respectively set at 5 kiloohms, 20 kiloohms and 8 kiloohms. The collector signal of the driver transistor Q_2 is applied to both the gates of a P-channel MOS FET M_{p14} and an N-channel MOS FET M_{n14} which constitute a CMOS inverter serving as a voltage amplifier, and the drain signal of both the MOS FETs M_{p14}, M_{n14} is applied to the gate of the P-channel MOS FET M_{p11} which serves as the charging output transistor. The ratios W/L of the FETs M_{p14}, M_{n14} and M_{p11} are respectively set at 24/3, 22/3 and 64/3.

The propagation delay times and their output capacitance-dependencies of such level converter 201 in Figure 21 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 2.02 nsec
t_{pLH} (for C_s = 0 pF) ····· 4.27 nsec
K_{HL} ····· 0.42 nsec/pF
K_{LH} ····· 1.32 nsec/pF

Further, the level converter 201 in Figure 21 can attain desired characteristics for the following reasons:

(a) Likewise to the case of Figure 14, the input threshold voltage V_{ith} of the level converter 201 can be set at 1.09 to 1.15 volt.

(b) The output transistor Q_1 for executing the discharge of the output capacitance C_s of the level converter 201 is formed of the bipolar transistor of low output resistance. Therefore, the speed of a switching operation at the discharge of the output capacitance can be enhanced, or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) Likewise to the case of Figure 14, the storage times of the transistors Q_1, Q_2 can be shortened.

In the level converter 201 of Figure 22, Q_1 indicates the clamped transistor as the discharging output transistor, and the cathode of the level-shifting Schottky barrier diode D_1 is connected to the input terminal IN_1. A P-N junction diode D_5 for level shift is connected between the anode of the diode D_1 and the base of the transistor Q_1, resistors R_{19} and R_{20} which are set at equal resistance values of 10 kiloohms are connected in series between the supply voltage V_{CC} and both the anodes of the diodes D_1 and D_5, and a Schottky barrier diode D_6 for discharging base charges is connected between the input terminal IN_1 and the base of the transistor Q_1.

The junction between the resistors R_{19} and R_{20} is connected to the gate of the P-channel MOS FET M_{p11} serving as the charging output transistor, and the ratio W/L of

the FET M_{p11} is set at 64/3.

The propagation delay times and their output capacitance-dependencies of such level converter in Figure 22 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 2.44 nsec

t_{pLH} (for C_s = 0 pF) ····· 5.41 nsec

K_{HL} ····· 1.0 nsec/pF

K_{LH} ····· 5.3 nsec/pF

Further, the level converter 201 in Figure 22 can attain desired characteristics for the following reasons:

(a) The forward voltage V_{F1} of the Schottky barrier diode D_1 is set at 0.35 to 0.41 volt, the forward voltage V_{F5} of the P-N junction diode D_5 is set at 0.75 volt, and the base-emitter voltage V_{BE1} of the transistor Q_1 is 0.75 volt. Therefore, the input threshold voltage V_{ith} of the level converter 201 for turning "on" the transistor Q_1 is set as below:

$$V_{ith} = - V_{F1} + V_{F5} + V_{BE1}$$
$$= 1.09 \text{ to } 1.15 \text{ volt}$$

(b) The output transistor Q_1 for executing the discharge of the output capacitance C_s is formed of the bipolar transistor of low output resistance. Therefore, the switching times or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) Since the transistor Q_1 is the clamped transistor, its storage time can be shortened.

In the level converter 201 of Figure 23, Q_1 and Q_2 indicate the clamped transistors, and D_1 indicates the Schottky barrier diode for level shift. The resistors R_{10}, R_{14} and R_{15} are respectively set at 5 kiloohms, 20 kiloohms and 8 kiloohms. The collector signal of the driver transistor Q_2 is applied to both the gates of the P-channel MOS FET M_{p14} and N-channel MOS FET M_{n14} which constitute the CMOS inverter serving as the voltage amplifier, and the drain output of both the MOS FETs is applied to the gate of a switching P-channel MOS FET M_{p15}. The ratios W/L of the FETs M_{p14}, M_{n14} and M_{p15} are respectively set at 24/3, 32/3 and 64/3.

The drain output of the MOS FET M_{p15} is applied to the base of the bipolar transistor Q_3 which serves as the charging output transistor.

The propagation delay times and their output capacitance-dependencies of such level converter in Figure 23 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 5.07 nsec
t_{pLH} (for C_s = 0 pF) ····· 5.09 nsec
K_{HL} ····· 0.4 nsec/pF
K_{LH} ····· 0.4 nsec/pF

Further, the level converter 201 in Figure 23 can

attain desired characteristics for the following reasons:

(a) Likewise to the case of Figure 14, the input threshold voltage V_{ith} of the level converter 201 can be set at 1.09 to 1.15 volt.

(b) Likewise to the case of Figure 14, the switching times for the charge and discharge of the output capacitance C_s or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) Likewise to the case of Figure 14, the storage times of the transistors Q_1, Q_2 can be shortened.

(d) When the collector potential of the driver transistor Q_2 rises to operate the charging output transistor Q_3 so as to switch from "off" into "on", the CMOS inverter M_{p14}, M_{n14} amplifies the change of the collector potential of the transistor Q_2 and transmits the amplified signal to the base of the transistor Q_3. Moreover, since the gate input impedances of the MOSFETs M_{p14}, M_{n14} are very high, a great base current is inhibited from directly flowing from the collector of the transistor Q_2 into the base of the transistor Q_3. Therefore, the switching speed of the output transistor Q_3 can be enhanced.

The level converter 201 of Figure 24 differs from that of Figure 23 only in that the resistor of 10 kiloohms R_{18} for discharging the base charges of the charging

output transistor Q_3 is connected between the base and emitter of the transistor Q_3. Regarding such level converter 201 in Figure 24, the propagation delay times and their output capacitance-dependencies have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 6.2 nsec
t_{pLH} (for C_s = 0 pF) ····· 4.9 nsec
K_{HL} ····· 0.4 nsec/pF
K_{LH} ····· 0.4 nsec/pF

Further, the level converter 201 in Figure 24 can attain desired characteristics for reasons similar to those in the case of Figure 23.

The level converter 201 of Figure 25 differs from that of Figure 24 only in that the resistor R_{10} of the base charge discharging circuit of the discharging output transistor Q_1 is replaced with an active pull-down circuit which is constructed of a resistor of 1.5 kiloohm R_{19}, a resistor of 3 kiloohms R_{20} and a clamped transistor Q_6, and that a Schottky barrier diode D_7 for discharging the base charges of the charging output transistor Q_3 is connected between the base of the transistor Q_3 and the collector of the transistor Q_2. Regarding such arrangement of Figure 25, the propagation delay times and their output capacitance-dependencies have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 6.6 nsec

t_{pLH} (for C_s = 0 pF) ····· 5.3 nsec

K_{HL} ····· 0.4 nsec/pF

K_{LH} ····· 0.4 nsec/pF

Further, the level converter 201 in Figure 25 can attain desired characteristics for reasons similar to those in the case of Figure 23.

The level converter 201 of Figure 26 differs from that of Figure 24 only in that the discharging resistor R_{10} is replaced with the same active pull-down circuit as the active pull-down circuit R_{19}, R_{20}, Q_6 in Figure 25. Regarding such arrangement of Figure 26, the propagation delay times and their output capacitance-dependencies have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 8.62 nsec

t_{pLH} (for C_s = 0 pF) ····· 4.7 nsec

K_{HL} ····· 0.4 nsec/pF

K_{LH} ····· 0.4 nsec/pF

Further, the level converter 201 in Figure 26 can attain desired characteristics for reasons similar to those in the case of Figure 23.

The level converter 201 shown in Fig. 27, includes: bipolar transistors Q_1, Q_2 and Q_3 which are respectively the discharging output transistor, driver transistor and charging output transistor, a Schottky barrier

diode Dl for level shift; a P-N junction diode D8; resistors R_{14}, R_{16}, R_{21} and R_{22} having values of resistance of 20 kiloohms, 8 kiloohms, 10 kiloohms and 10 kiloohms respectively; a P-channel MOS FET M_{p16}; and an N-channel MOS FET M_{n16}. In this circuit both the ratios W/L of the two FETs M_{p16} and M_{n16} are set at equal values of 32/3.

In the circuit shown in Fig. 27, the transistors M_{p16}, M_{n16}, Q_1 and Q_3 constitute an amplifier of the quasi-CMOS inverter type of low output resistance.

The propagation delay times and their output capacitance-dependencies of such level converter 201 in Fig. 27 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ..... 5.48 nsec

t_{pLH} (for C_s = 0 pF) ..... 5.23 nsec

K_{HL} ..... 0.37 nsec/pF

K_{LH} ..... 0.38 nsec/pF

Further, the level converter 201 in Fig. 27 can attain desired characteristics for reasons stated below.

(a) the forward voltage V_F1 of the Schottky barrier diode D_1 is set at 0.35 to 0.41 volt, the base-emitter voltage V_{BE2} of the transistor Q_2 at 0.75 volt, and the forward voltage V_{F8} of the P-N junction diode D_8 at 0.75 volt. Therefore, the input threshold voltage V_{ith} of the level converter 201 concerning the on-off

operation of the transistor Q_2 is set as follows:

$$V_{ith} = -V_{F1} + V_{BE2} + V_{F8}$$
$$= 1.09 \text{ to } 1.15 \text{ volt}$$

(b) The output transistors Q_1, Q_3 for executing the charge or discharge of the output capacitance C_s are formed of the bipolar transistors of low output resistances. Therefore, the switching operation speeds can be enhanced or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) Since the transistors Q_1, Q_2 are the clamped transistors, their storage times can be shortened.

(d) Since the change of the collector potential of the driver transistor Q_2 is amplified and then transmitted to the output end by the quasi-CMOS inverter M_{p16}, M_{n16}, Q_3, Q_1, the changing speed of an output waveform can be enhanced.

The level converter 201 of Figure 28 differs from that of Figure 27 only in that the collector load of the transistor Q_2 is not formed of the resistor R_{16}, but is formed of P-N junction diodes D_9, D_{10} and a resistor of 5 kiloohms R_{23}. The propagation delay times and their output capacitance-dependencies of such level converter in Figure 28 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 6.66 nsec

t_{pLH} (for C_s = 0 pF) ····· 4.16 nsec

K_{HL} ····· 0.42 nsec/pF

K_{LH} ····· 0.37 nsec/pF

Further, the level converter 201 in Figure 28 can attain desired characteristics for reasons similar to those in the case of Figure 27.

The level converter 201 of Figure 29 differs from that of Figure 23 only in the point of connecting the P-N junction diode D_3 for reliably turning "off" the transistor Q_3 and in the point of connecting the Schottky barrier diode D_7 for discharging the base charges of the transistor Q_3. Regarding such level converter 201 in Figure 29, the propagation delay times and their output capacitance-dependencies have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 1.72 nsec

t_{pLH} (for C_s = 0 pF) ····· 5.44 nsec

K_{HL} ····· 0.32 nsec/pF

K_{LH} ····· 0.29 nsec/pF

Further, the level converter 201 in Figure 29 can attain desired characteristics for reasons similar to those in the case of Figure 23.

The level converter 201 of Figure 30 differs from that of Figure 29 only in that the resistor R_{14} in Figure 29 is substituted by a resistor of 25 kiloohms R_{24} and

a resistor of 5 kiloohms R_{25}, and that the resistor R_{15} is substituted by a P-channel MOS FET M_{p17} whose ratio W/L is set at 24/3. Since the FET M_{p17} operates as the active load element of the transistor Q_2, the voltage gain of the amplifier Q_2, M_{p17} becomes a very large value. Regarding such arrangement of Fig. 30, the propagation delay times and their output capacitance-dependencies have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ..... 2.2. nsec

t_{pLH} (for C_s = 0 pF) ..... 5.2 nsec

K_{HL} ..... 0.4 nsect/pF

K_{LH} ..... 0.3 nsect/pF

Further, the level converter 201 in Fig. 30 can attain desired characteristics for reasons similar to those in the case of Fig. 23.

The level converter 201 shown in Fig. 31, includes: transistors Q_1 and Q_2 which are clamped transistors; a transistor Q_3 which is the charging output transistor; a transistor Q_4 which is a P-N-P emitter follower transistor; a diode D_1 which is a Schottky barrier diode for level shift; a diode D_2 which is a P-N junction diode for level shift; a diode D_3 which is a P-N junction diode for reliably turning "off" the transistor Q_3; a diode D_8 which is a Schottky barrier diode for clamping minus noise at the input terminal; resistors R_{10}, R_{15} and R_{26} which resistance values are respectively set at 5 kiloohms,

8 kiloohms and 20 kiloohms. The collector signal of the driver transistor Q_2 is applied to both the gates of the P-channel MOS FET M_{p14} and N-channel MOS FET M_{n14} which constitute the CMOS inverter serving as the voltage amplifier, and the drain output of which is applied to the gate of the switching P-channel MOS FET M_{p15}. The ratios W/L of the FETs M_{p14}, M_{n14} and M_{p15} are respectively set at 24/3, 32/3 and 64/3. The drain output of the MOS FET M_{p15} is applied to the base of the bipolar transistor Q_3 serving as the charging output transistor.

The propagation delay times and their output capacitance-dependencies of such level converter 201 in Figure 31 have been confirmed as follows:

t_{pHL} (for C_s = 0 pF) ····· 1.94 - 3.84 nsec

t_{pLH} (for C_s = 0 pF) ····· 4.64 - 5.44 nsec

K_{HL} ····· 0.38 nsec/pF

K_{LH} ····· 0.30 nsec/pF

Further, the level converter 201 in Figure 31 can attain desired characteristics for reasons stated below.

(a) The forward voltage V_{F1} of the Schottky barrier diode D_1 is 0.35 to 0.41 volt, the forward voltage V_{F2} of the P-N junction diode D_2 is approximately 0.75 volt, and the base-emitter voltages V_{BE1}, V_{BE2} and V_{BE4} of the respective transistors Q_1, Q_2 and Q_4 are approximately

0.75 volt. Therefore, the input threshold voltage V_{ith} at which the transistors Q_1, Q_2 are turned "on" becomes as follows:

$$V_{ith} = - V_{BE4} + V_{F2} + V_{BE2} + V_{BE1}$$
$$= 1.5 \text{ volt}$$

(b) The output transistors Q_1, Q_3 for executing the discharge or charge of the output capacitance C_s are formed of the bipolar transistors of low output resistances. Therefore, the speeds of switching operations can be enhanced or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) Since the transistors Q_1, Q_2 are the clamped transistors, their storage times can be shortened.

(d) When the collector potential of the driver transistor Q_2 rises to operate the charging bipolar output transistor Q_3 to switch from "off" into "on", the CMOS inverter M_{p14}, M_{n14} amplifies the change of the collector potential of the transistor Q_2 and transmits the amplified signal to the base of the transistor Q_3. Moreover, the gate input impedances of the MOS FETs M_{p14}, M_{n14} are very high and inhibit the direct flow of a great base current from the collector of the transistor Q_2 into the base of the transistor Q_3, and a base current is supplied to the base of the transistor Q_3 through the low ON-resistance

of the FET M_{p15}. Therefore, the switching speed of the output transistor Q_3 can be enhanced. Figure 3 shows with dot-and-dash lines the output capacitance-dependencies of the propagation delay times of the level converters illustrated in Figures 14, 19, 22 and 31. It is understood that the output capacitance-dependency of either of the first and second propagation delay times is improved.

There will now be explained the plurality of CMOS - TTL level converters 221, 222, ····· 22m of the output buffer 22 in Figure 6. The essential features of these level converters 221, 222, ····· 22m are as stated below.

(a) The input threshold voltage V_{ith} of each of the level converters 221, 222, ····· 22m is set between a CMOS low level output voltage of 0.6 volt and high level output voltage of 4.4 volts.

(b) An output transistor, which executes the discharge of the output load capacitance C_x of each of the level converters 221, 222, ····· 22m in response to an input signal supplied to the input terminal thereof, is formed of a bipolar transistor.

Further, meritorious features in preferable aspects of performance of the level converters 221, 222, ····· 22m of the output buffer 22 are as stated below.

(c) A high input impedance circuit is connected between

the output of the internal logic block 21 and the base of a driver transistor Q_{11} for driving the base of a discharging output transistor Q_{10}.

(d) The high input impedance circuit in the above item (c) has the function of logically processing a plurality of output signals from the internal logic block 21.

(e) The discharging output transistor Q_{10} and the driver transistor Q_{11} are formed of clamped transistors provided with Schottky barrier diodes.

(f) An output transistor Q_{12} for charging the output load capacitance C_x is formed of a bipolar transistor.

(g) The level converter has the function of simultaneously turning "off" the discharging output transistor Q_{10} and the charging output transistor Q_{12} in response to a control signal, thereby to control the corresponding output terminal, e. g., OUT_1 into a floating state.

(h) The level converters 221, 222, ····· 22m are of the open collector output form.

Figures 32 to 34 and Figure 36 show various examples of circuits of the level converter 221 of the output buffer 22 according to embodiments of the present invention. All these level converters have the essential features of the above items (a) and (b). Further, these level converters have at least one of the meritorious features of the above items (c) to (h).

The level converter 221 shown in Fig. 32, includes; an output transistor Q_{10} for discharging the output load capacitance C_x; a driver transistor Q_{11} for driving the transistor Q_{10}; an output transistor Q_{12} for charging the output load capacitance C_x; and a current amplifying transistor Q_{13} for transmittig the collector signal change of the transistor Q_{11} to the base of the transistor Q_{12}. Resistors R_{30} and R_{31} together with the transistor Q_{14} constitute an active pull-down circuit for discharging the base charges of the transistor Q_{10}. The circuit also includes a multi-emitter transistor Q_{15}; a collector resistor R_{32} of the transistor Q_{11}; a resistor R_{33} for discharging the base charges of the transistor Q_{12}; a Schottky barrier diode D_{10} for discharging the base charges of the transistor Q_{12}; a resistor R_{34} for limiting the collector currents of the transistors Q_{12} and Q_{13}; and a base resistor R_{35} of the transistor Q_{15}.

Further, the output of the CMOS NAND gate 211 of the internal logic block 21, this gate being composed of P-channel MOS FETs M_1, M_2 and N-channel MOS FETs M_3, M_4, is applied to the first emitter of the multi-emitter transistor Q_{15}; the output of the CMOS NAND gate 212 is applied to the second emitter of the transistor Q_{15}; and the output of the CMOS NAND gate 213 is applied to the third emitter of the transistor Q_{15}. The level converter 221 accordingly has, not only a level converting

function, but also a logical processing function as a 3-input NAND gate.

Moreover, the level converter 221 in Figure 32 can attain desired characteristics for reasons stated below.

(a) The base-emitter voltage V_{BE15} of the transistor Q_{15} is approximately 0.75 volt, the base-collector voltage V_{BC15} of the transistor Q_{15} is approximately 0.55 volt, and the base-emitter voltages V_{BE10} and V_{BE11} of the respective transistors Q_{10} and Q_{11} are approximately 0.75 volt. Therefore, the input threshold voltage V_{ith} of the level converter 221 is set as follows:

$$\begin{aligned} V_{ith} &= -V_{BE15} + V_{BC15} + V_{BE11} + V_{BE10} \\ &= -0.75 + 0.55 + 0.75 + 0.75 \\ &= 1.3 \text{ volt} \end{aligned}$$

(b) The output transistors Q_{10}, Q_{12}, which execute the discharge or charge of the output load capacitance C_x of the level converter 221, are formed of the bipolar transistors of low output resistances. Therefore, the speeds of switching operations can be enhanced or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened.

(c) Since the transistors Q_{10}, Q_{11}, Q_{13}, Q_{14} and Q_{15} are the clamped transistors, their storage times can be shortened.

(d) Since the multi-emitter transistor Q_{15} has the logical processing function, the design versatility of the logic semiconductor integrated circuit IC of the master slice type or the gate array type is enhanced.

In such level converter 221 of Figure 32, however, when the output of the CMOS·NAND gate 211 is at its low level, a large current of 0.4 milliampere continues to flow from the supply voltage V_{CC} to the output end of the CMOS·NAND gate 211 through the resistor R_{35} as well as the base-emitter junction of the transistor Q_{15}. Therefore, the ratios W/L of the N-channel MOS FETs M_3, M_4 of the CMOS·NAND gate 211 must be set at large values of 100/3 so as to lower ON-resistances R_{ON}. This incurs lowering in the density of integration of the integrated circuit IC. Moreover, from investigations we have discovered that, since the gate capacitances of both the MOS FETs M_3 and M_4 increase, the switching speed of the CMOS·NAND gate 211 is reduced.

Figure 33 shows a circuit diagram of the level converter 221 which has been developed in order to solve the problems described above, and in which the multi-emitter transistor Q_{15} in Figure 32 is substituted by the high input impedance circuit to be explained below.

Referring to Figure 33, such high input impedance circuit is constructed of P-N-P input transistors Q_{17}, Q_{18},

an N-P-N emitter follower transistor Q_{16}, Schottky barrier diodes D_{11}, D_{12} and resistors R_{36}, R_{37}, R_{38}.

Further, the level converter 221 includes a control circuit which is constructed of a P-N-P transistor Q_{20}, an N-P-N transistor Q_{21}, a P-N junction diode D_{14} and a resistor R_{38}' and which serves to control the output terminal OUT_1 into the floating state.

The base of the P-N-P transistor Q_{20} of this control circuit is driven by the enable signal EN of the CMOS inverter 21ℓ in the internal logic block 21, this inverter being composed of a P-channel MOS FET M_5 and an N-channel MOS FET M_6. The input of such CMOS inverter 21ℓ is supplied with the inverted enable signal $\overline{EN}$.

Further, since this control circuit has been added to the level converter 221, a P-N-P input transistor Q_{19} and a Schottky barrier diode D_{13} are also added to the aforementioned high input impedance circuit.

Accordingly, when the enable signal EN becomes its low level, the transistors Q_{10}, Q_{11}, Q_{12} and Q_{13} of the level converter 221 turn "off" at the same time, so that the output terminal OUT_1 falls into the floating state.

On the other hand, when the enable signal EN becomes its high level, the level converter 221 similarly has a logical processing function as a 2-input NAND gate,

so that the design versatility of the integrated circuit IC is enhanced.

Further, the forward voltages V_{F11}, V_{F12}, V_{F13} of the respective Schottky barrier diodes D_{11}, D_{12}, D_{13} are 0.35 to 0.41 volt, the base-emitter voltages V_{BE17}, V_{BE18}, V_{BE19} of the respective P-N-P input transistors Q_{17}, Q_{18}, Q_{19} are approximately 0.75 volt, and the base-emitter voltages V_{BE10}, V_{BE11}, V_{BE16} of the respective N-P-N transistors Q_{10}, Q_{11}, Q_{16} are approximately 0.75 volt. Therefore, the input threshold voltage V_{ith} at which the transistors Q_{10} and Q_{11} turn "on" in relation to, e.g., the output voltage of the CMOS-NAND gate 211 applied to the base of the P-N-P transistor Q_{17} becomes as follows:

$$V_{ith} = -V_{BE17} + V_{BE16} + V_{BE11} + V_{BE10}$$
$$= 1.5 \text{ volt}$$

Moreover, the output transistors Q_{10}, Q_{12} for executing the discharge or charge of the output load capacitance C_x are formed of the bipolar transistors of low output resistances. Therefore, the switching speeds can be enhanced or the propagation delay times can be shortened, and the output capacitance-dependencies of the propagation delay times can be lessened. In addition, since the transistors Q_{10}, Q_{11}, Q_{13}, Q_{14} and Q_{16} are the clamped transistors, their delay times can be shortened.

From investigation, we have noted that,

even with the level converter 221 of Figure 33, an unnegligible current similarly flows from the base of the P-N-P input transistor Q_{17} to the output end of the CMOS·NAND gate 211 when the output of this gate 211 is at the low level, so the foregoing problems cannot be perfectly solved.

Figure 34 shows the level converter 221 which has been finally developed in order to solve such problems substantially perfectly. The multi-emitter transistor Q_{15} in Figure 32 is replaced with the high input impedance circuit which is constructed of MOS FETs as explained below.

Referring to Figure 34, such high input impedance circuit is constructed of N-channel MOS FETs M_{11}, M_{12}, M_{13} and a P-N junction diode D_{14}. The drain-source paths of the FETs M_{11}, M_{12}, M_{13} are connected in parallel, and the gates thereof are respectively connected to the CMOS·NAND gates 211, 212, 213 of the internal logic block 21. In addition, the P-N junction diode D_{14} is connected in series with the drain-source paths.

Resistors R_{30}, R_{31}, R_{32}, R_{33}, R_{34} and R_{35} are respectively set at 2 kiloohms, 4 kiloohms, 10 kiloohms, 4 kiloohms, 50 - 75 ohms and 16 kiloohms. The emitter areas of the transistors Q_{10}, Q_{11}, Q_{12}, Q_{13} and Q_{14} are respectively set at 672 μm^2, 132 μm^2, 363 μm^2, 187 μm^2 and 242 μm^2.

Further, in such level converter 221, in order to

enhance the logic processing function still more, a second driver transistor Q_{20} which has an emitter area equal to that of the driver transistor Q_{11} is connected in parallel with the transistor Q_{11}, and a second high input impedance circuit is provided which is constructed of N-channel MOS FETs M_{14}, M_{15}, M_{16}, a P-N junction diode D_{15} and a resistor R_{39} likewise to the foregoing high input impedance circuit. This level converter 221 has a logic processing function as a 6-input complex gate circuit.

Further, a control circuit is similarly added to this level converter 221, the control circuit serving to control the output terminal OUT_1 into the floating state when the level converter is supplied with the enable signal EN of low level from the internal logic block 21. This control circuit is constructed of an N-channel MOS FET M_{17}, transistors Q_{21}, Q_{22}, Q_{23}, resistors R_{40}, R_{41}, R_{42}, R_{43}, and Schottky barrier diodes D_{16}, D_{17}, D_{18}, D_{19}.

Further, in the level converter 221 of Figure 34, in order to set input threshold voltages at the respective gates of the six MOS FETs M_{11}, ····· M_{16} at the middle value of 2.5 volts between the CMOS low level output voltage of 0.6 volt and the CMOS high level output voltage of 4.4 volts, the ratios W/L of the FETs M_{11}, ····· M_{16}

are set as stated below. At this time, the threshold voltages V_{TH} of the FETs M_{11}, ... M_{16} are set at approximately 0.75 volt, the forward voltage V_{F14} of the P-N junction diode D_{14} is set at 0.75 volt, and the channel conductances β_0 of the FETs M_{11}, ... M_{16} are set at 60×10^{-6} [1/ohm].

A case where only the MOS FET M_{11} is "on" will be considered, and the gate voltage V_X, gate-source voltage V_{GS}, drain current I_D, drain voltage V_Y etc. thereof will be calculated. At this time, the FET M_1 is supposed to be biased in its saturation region.

$$V_X = V_{GS} + V_{F14} \quad \ldots (1)$$

$$I_D = \frac{\beta_0}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \quad \ldots (2)$$

$$V_Y = V_{CC} - R_{35} \cdot I_D \quad \ldots (3)$$

From Equations (1) and (2),

$$I_D = \frac{\beta_0}{2} \cdot \frac{W}{L} \cdot (V_X - V_{F14} - V_{TH})^2 \quad \ldots (4)$$

Considered as the input threshold voltage is the voltage V_X which corresponds to the fact that the voltage V_Y lowers due to rise in the voltage V_X, resulting in the turn-off of the transistors Q_{10}, Q_{11}.

The drain voltage V_Y at which the transistors Q_{10}, Q_{11} turn "off" is evaluated as follows:

$$V_Y = V_{BE11} + V_{BE10} \quad \ldots (5)$$

From Equations (3) and (5),

$$I_D = \frac{V_{CC} - V_{BE11} - V_{BE10}}{R_{35}} \qquad \cdots(6)$$

From equations (4) and (6),

$$\frac{W}{L} = \frac{V_{CC} - V_{BE11} - V_{BE10}}{R_{35}} \cdot \frac{2}{\beta_0 (V_X - V_{F14} - V_{TH})^2} \qquad \cdots(7).$$

Substituting into equation (7) the conditions of V_{CC} being 5 volts, V_{BE11} and V_{BE10} being 0.75 volt, R_{35} being 16 kiloohms, β_0 being 60×10^{-6} [1/ohm], V_X being 2.5 volts, V_{F14} being 0.75 volt and V_{TH} being 0.75 volt,

$$\frac{W}{L} = \frac{5 - 0.75 - 0.75}{16 \times 10^3} \cdot \frac{2 \times 10^6}{60} \cdot \frac{1}{(2.5 - 0.75 - 0.75)^2}$$

$$= \frac{3.5}{960} \cdot 2 \times 10^3 \cdot \frac{1}{1^2}$$

$$= \frac{7}{960} \times 10^3$$

$$= 7.29 \fallingdotseq \frac{22}{3}$$

Thus, the input threshold voltage of the level converter 221 can be set at 2.5 volts by setting the ratios W/L of the FETs M_{11}, ····· M_{16} at 22/3.

The embodiment of Figure 34 having the above arrangement has been confirmed to exhibit the propagation delay times and the output capacitance-dependencies thereof as listed below.

t_{pHL} (for C_s = 0 pF) ····· 8.8 nsec

t_{pLH} (for C_s = 0 pF) ····· 7.8 nsec

K_{HL} ····· 0.11 nsec/pF

K_{LH} ····· 0.01 nsec/pF

Figure 5 shows with dot-and-dash lines the output load capacitance-dependencies of the propagation delay times of the level converter 221 of the embodiment illustrated in Figure 34. It is understood that the respective output capacitance-dependencies K_{HL}, K_{LH} of the first and second propagation delay times t_{pHL}, t_{pLH} are improved.

The level converter 221 in Figure 34 can attain desired characteristics for reasons stated below.

(a) As described above, the ratios W/L of the MOS FETs M_{11}, ····· M_{16} are set in correspondence with the supply voltage V_{CC}, the resistance R_{35}, the channel conductances β_0 and threshold voltages V_{TH} of the MOS FETs M_{11}, ····· M_{16}, and the forward voltage V_{F14} of the diode D_{14} concerning the base-emitter voltages V_{BE10}, V_{BE11} of the transistors Q_{10}, Q_{11}, whereby the input threshold voltage of the level converter 221 can be set at 2.5 volts which is between 0.6 volt and 4.4 volts.

(b) The output transistors Q_{10}, Q_{11} which execute the discharge and charge of the output load capacitance C_X are formed of the bipolar transistors of low output resistances. Therefore, the switching operation speeds can be enhanced or the propagation delay times can be shortened, and the output capacitance-dependencies of

the propagation delay times can be reduced.

(c) The high input impedance circuit including the MOS FET M_{11} is connected between the base of the driver transistor Q_{11} and the output of the internal logic block 21. Therefore, current to flow from the gate of the MOS FET M_{11} to the output of the CMOS·NAND gate 211 of the internal logic block 21 can be reduced to a negligible level, and conspicuous increase in the ratio W/L of the N-channel MOS FETs of the CMOS·NAND gate 211 can be prevented.

(d) Since the MOS FETs M_{11}, M_{12}, M_{13} of the high input impedance circuit execute 3-input OR logic, the logical processing function of the level converter 221 is enhanced.

(e) Since also the two driver transistors Q_{11}, Q_{20} execute AND logic, the logical processing function of the level converter 221 is more enhanced.

(f) Since the transistors Q_{10}, Q_{11}, Q_{13}, Q_{14}, Q_{20} are the clamped transistors, their storage times can be shortened.

(g) By bringing the enable signal EN into the low level, the output transistors Q_{10}, Q_{12} of the level converter 221 are simultaneously turned "off", so that the output terminal OUT_1 falls into the floating state. Thus, in a parallel operation wherein this output terminal OUT_1 and the output terminal of another logic circuit, not shown, are connected, the signal level of the output

terminal OUT_1 can be made independent of the output of the internal logic block 21.

Figure 36 shows a circuit example of the level converter 221 according to another embodiment of the present invention. The output terminal OUT_1 of this level converter is connected in common with the output terminal of another TTL level logic semiconductor integrated circuit IC' of the open collector output type, and the common connection point is connected to the supply voltage V_{CC} of 5 volts through a load resistor of 2 kiloohms R_{100}.

Although not especially restricted, the open collector output type TTL level circuit IC' is constructed of Schottky barrier diodes D_1, D_2, D_3, a multi-emitter transistor Q_{40}, clamped transistors Q_{41} to Q_{44}, resistors R_{40} to R_{44}, and a P-N junction diode D_4. As an open collector output, the collector of the output transistor Q_{43} is connected to terminal No. 43 serving as an output terminal. Inside the circuit IC', however, no circuit element is connected between the supply voltage V_{CC} and the collector of the output transistor Q_{43}.

The level converter 221 of Figure 36 is formed quite similarly to the level converter 221 of Figure 34 except that, inside the circuit IC, no circuit element is connected between the supply voltage V_{CC} and the collector of the output transistor Q_{10}.

Thus, the output terminals of the circuit IC and those of the circuit IC' are connected in the form of the so-called wired OR circuit. In addition, the output transistor Q_{10} of the level converter 221 is forcibly turned "off" by bringing the enable signal EN into the low level, whereby the level of the output terminal OUT_1 can be made independent of the output of the internal logic block 21.

Figure 37 shows the layout of the various circuit blocks in the front surface of a semiconductor chip of the logic semiconductor integrated circuit IC embodying the present invention.

In the central part (an area enclosed with a broken line ℓ_0) of the semiconductor chip 300, the internal logic block 21 formed of the CMOS circuit (pure CMOS circuit or quasi-CMOS circuit) is arranged. In the upper edge part (an area enclosed with a broken line ℓ_1) of the semiconductor chip 300, the plurality of input level converters as shown in Figure 31 (indicated by triangles whose inner parts are hatched) and the plurality of output level converters as shown in Figure 34 (indicated by triangles whose inner parts are white) are arranged alternately. Likewise, in each of the right edge part (an area enclosed with a broken line ℓ_2), lower edge part (an area enclosed with a broken

line ℓ_3) and left edge part (an area enclosed with a broken line ℓ_4) of the semiconductor chip 300, the plurality of input level converters as shown in Figure 31 and the plurality of output level converters as shown in Figure 34 are arranged alternately.

Above the upper edge part ℓ_1, bonding pads for inputs (indicated by squares of thick solid lines) corresponding in number to the input level converters and bonding pads for outputs (indicated by squares of thin solid lines) corresponding in number to the output level converters are arranged. The input parts of the input level converters confront the corresponding input bonding pads, while the output parts thereof confront the internal logic block 21, and the input parts of the output level converters confront the internal logic block 21, while the output parts thereof confront the corresponding output bonding pads.

A plurality of input bonding pads and a plurality of output bonding pads on the right of the right edge part ℓ_2, a plurality of input bonding pads and a plurality of output bonding pads below the lower edge part ℓ_3, and a plurality of input bonding pads and a plurality of output bonding pads on the left of the left edge part ℓ_4 are arranged similarly to the case of the upper edge part ℓ_1.

The orientations of the input and output parts

of the input level converters and those of the input and output parts of the output level converters in the right edge part ℓ_2, lower edge part ℓ_3 and left edge part ℓ_4 are respectively the same as in the case of the upper edge part ℓ_1.

A power source bonding pad 30 for feeding the supply voltage V_{CC} is arranged in at least one of the four corners of the semiconductor chip 300, and an earthing bonding pad 31 for connection to an earth point is arranged in at least one of the four corners.

The rear surface of such semiconductor chip of the layout shown in Figure 37 is connected to the front surface of the tab lead L_T of a metal lead frame L_F in Figure 38 in physical and electrical close contact.

Referring to Figure 38, this lead frame L_F has lead portions L_1 - L_{16}, a frame portion L_0 and hatched dam portions L_D which correspond to the right upper part of the semiconductor chip 300. In practice, however, parts corresponding to the right lower part, left lower part and left upper part of the semiconductor chip are similar to the above. Therefore, the lead frame L_F is a worked metal sheet of a structure wherein the frame portion L_0, lead portions L_1 - L_{64} and tab lead L_T are interconnected by the hatched dam portions.

After the rear surface of the semiconductor chip 300

has been connected to the front surface of the tab lead L_T, bonding wires (for example, gold wires or aluminium wires) to be described below are wired.

Using a wire bonding equipment which is commercially available, the power source bonding pad 30 and the lead portion L_{34} are electrically connected by a wire ℓ_5. Further, the input pad and the lead portion L_9 are electrically connected by a wire ℓ_6, the output pad and the lead portion L_8 by a wire ℓ_7, the input pad and the lead portion L_7 by a wire ℓ_8, the output pad and the lead portion L_6 by a wire ℓ_9, the input pad and the lead portion L_5 by a wire ℓ_{10}, and the earth bonding pad 31 and the tab lead L_T by a wire ℓ_{11}, in succession.

The lead frame L_T and the semiconductor chip 300 after the completion of the above wiring are put in a metal mould for resin moulding whereupon a liquid resin is poured inside the dam portions L_D of the lead frame L_F. Such dam portions L_D hinder the resin from flowing out of them. After the resin has solidified, the lead frame L_F, semiconductor chip 300 and resin which form a unitary structure are taken out from the metal mould. Further, the dam portions L_D are removed by a press machine or the like, whereby the respective lead portions L_1 - L_{64} can be electrically isolated.

If necessary, the leads L_1 - L_{64} protruding outside

the solidified resin are bent downwards. Then, the logic semiconductor integrated circuit IC moulded with the resin 301 is finished up as shown in a completion diagram of Figure 39. As seen from the figure, such circuit IC is not provided with any special radiation fin for positively radiating heat produced from the semiconductor chip 300, out of the moulded structure. If such radiation fin is mounted, the cost of the circuit IC will increase undesirably.

As methods of sealing the semiconductor chip, a ceramic moulding method and a method employing a metal case are considered besides the resin moulding method stated above. From the viewpoint of the cost of the circuit IC, however, the resin moulding method is the most advantageous.

In the logic semiconductor integrated circuit IC according to the embodiment drawn in Figures 37 to 39, the total number of the input level converters 201, 202, ..., 20n constituting the input buffer 20 is 18 - 50, the total number of the CMOS gates 211, 212, ..., 21ℓ constituting the internal logic block 21 is 200 - 1530, and the total number of the output level converters 221, 222, ..., 22m constituting the output buffer 22 is 18 - 50, so that the semiconductor chip 300 forms a large-scale semiconductor integrated circuit device. Nevertheless, the circuit IC has been successfully put into the radiation fin-less

structure for reasons stated below.

Since the power consumption of each of the CMOS gates 211, 212, ..., 21ℓ constituting the internal logic block 21 is as small as 0.039 milliwatt, the power consumption of the whole internal logic block 21 having the 200 - 1530 gates is as very low as 7.8 - 59.67 milliwatts. Since the input level converters 201, 202, ..., 20n constituting the input buffer 20 according to the embodiment of Figure 31 include a large number of bipolar transistors, the power consumption per converter is as high as 2.6 milliwatts, and the power consumption of the whole input buffer 20 having the 18 - 50 converters is as high as 46.8 - 130 milliwatts. Since also the output level converters 221, 222, ..., 22m constituting the output buffer 22 according to the embodiment of Figure 34 include a large number of bipolar transistors, the power consumption per converter is as high as 3.8 milliwatts, and the power consumption of the whole output buffer 22 having the 18 - 50 converters is as high as 68.4 - 190 milliwatts.

On the basis of the above data, in the circuit IC which is constructed of the input buffer 20 having the 18 converters, the internal logic block 21 having the 200 gates and the output buffer 22 having the 18 converters, heat of 6.4 % with respect to the entire

amount of heat is generated in the central part ℓ_0 of the front surface of the semiconductor chip shown in Figure 37, whereas heat of 93.6% is generated in the edge parts ℓ_1, ℓ_2, ℓ_3 and ℓ_4 in total.

Besides, in the circuit IC which is constructed of the input buffer 20 having the 50 converters, the internal logic block 21 having the 1530 gates and the output buffer 22 having the 50 converters, heat of 15.8% with respect to the entire amount of heat is generated in the central part ℓ_0 of the front surface of the semiconductor chip shown in Figure 37, whereas heat of 84.2% is generated in the edge parts ℓ_1, ℓ_2, ℓ_3 and ℓ_4 in total.

As illustrated in Figure 37, the internal logic block 21 which generates the slight heat is arranged in the central part ℓ_0 of the chip, and the input buffer 20 and the output buffer 22 which generate the large quantities of heat are arranged in the edge parts ℓ_1, ℓ_2, ℓ_3 and ℓ_4 of the chip. As seen from Figure 38, therefore, the large quantitites of heat in the edge parts ℓ_1, ℓ_2, ℓ_3 and ℓ_4 are taken out of the circuit IC (particularly, taken out to the earth line of a printed circuit board when the circuit IC is installed on the printed circuit board) through the tab lead L_T and the lead portion L_1 as an earth lead. Moreover, they can be taken out of the circuit IC (particularly, taken out to the signal

lines and power source line of the printed circuit board when the circuit IC is installed on the printed circuit board) through the large number of bonding wires and the lead portions L_2, ·····, L_{64}.

It has been confirmed by our computation that, in a case where conversely to the above embodiment, the input buffer 20 and the output buffer 22 which generate large quantities of heat are arranged in the central part ℓ_0 of the chip and the internal logic block 21 is arranged around the central part ℓ_0, the large quantities of heat in the central part ℓ_0 cannot be readily taken out of the circuit IC.

For the reasons described above, it has been possible to put the circuit IC of the above embodiment into the radiation fin-less structure. In addition, since such circuit IC has been put into the resin-moulded structure, it has become possible to sharply reduce the cost of the circuit IC.

Figure 40 shows a block diagram of an electronic system which is constructed by installing on a printed circuit board the logic semiconductor integrated circuit IC according to the embodiment illustrated in Figures 37 to 39 and other logic semiconductor integrated circuit devices of TTL levels 401, 402 ····· 40n, 501 to 505 and 600.

Referring to the figure, the outputs of the devices 401, 402 ····· 40n having the TTL level outputs are respectively supplied to the inputs IN_1, IN_2 ····· IN_n of the circuit IC, the outputs of which are supplied to the inputs of the devices 501, ····· 505 of TTL input levels.

Further, the output OUT_2 of the circuit IC and the output of the device 600 are connected in common, whereby both the devices IC and 600 execute a parallel operation.

Heat generated in large quantities in the input buffer 20 and output buffer 22 of the circuit IC can be dissipated to the earth line, power source line, input signal line and output signal line of the printed circuit board.

In addition, when the enable signal EN to be fed to the output buffer 22 is set at the low level, the outputs OUT_1, OUT_2 ····· OUT_m fall into the floating states, and the input levels of the devices 501, 502, 503 are set by the output level of the device 600.

Besides, a high speed is attained at the interface between the input buffer 20 and the devices 401, 402 ····· 40n; at the interface between the internal logic block 21 and the input buffer 20; at the interface between the output buffer 22 and the internal logic block 21;

and at the interface between the devices 501 ····· 505 and the output buffer 20.

According to the foregoing embodiments, favorable effects can be achieved for reasons as stated below.

(a) Output transistors for executing the charge or discharge of the output capacitance C_s of an input level converter 201 are formed of bipolar transistors. Thus, the propagation delay times of the input level converter and the output capacitance-dependencies thereof can be lessened owing to the function that, even when smaller in device size than a MOS FET, the bipolar transistor exhibits a lower output resistance and a higher current gain, so it can produce a great charging current or discharging current.

(b) In the input level converter 201, a Schottky barrier diode for executing a majority carrier operation is connected between the base and collector of a bipolar transistor which is driven into its saturation region. Therefore, the injection of minority carriers from a collector layer into a base layer can be reduced, so that the storage time of the bipolar transistor can be shortened.

(c) In an input level converter 201 according to a preferred embodiment, the base signal or collector signal of a driver transistor Q_2 is transmitted to the base of a charging bipolar output transistor Q_3 through a MOS

buffer which has a high input impedance and a voltage amplifying function. Thus, the operating speed of the output transistor Q_3 is enhanced owing to the high input impedance and the voltage amplifying function of the MOS buffer.

(d) In the input level converter 201 according to a preferred embodiment, a P-N-P emitter follower transistor Q_4 and a P-N junction diode D_2 are connected between an input terminal IN_1 and the driver transistor Q_2. Thus, the input threshold voltage of the input level converter 201 can be properly set. Moreover, since the input impedance of the P-N-P transistor Q_4 at the base thereof is enhanced owing to the current amplifying function thereof, the influence of the output impedance of a TTL level signal source connected to the input terminal IN_1 can be reduced.

(e) Output transistors for executing the charge or discharge of the output load capacitance C_x of an output level converter 221 are formed of bipolar transistors. Thus, the propagation delay times of the output level converter and the output capacitance-dependencies thereof can be lessened owing to the function that, even when smaller in device size than a MOS FET, the bipolar transistor exhibits a lower output resistance and a higher current gain, so it can produce a great charging current or

discharging current.

(f) In the output level converter 221, a Schottky barrier diode for executing a majority carrier operation is connected between the base and collector of a bipolar transistor which is driven into its saturation region. Therefore, the injection of minority carriers from a collector layer into a base layer can be reduced, so that the storage time of the bipolar transistor can be shortened.

(g) In an output level converter 211 according to a preferred embodiment, a high input impedance MOS circuit is connected between the output of an internal logic block 21 and the base of a driver transistor Q_{11}. Thus, current to flow from the gate of the MOS FET of this MOS circuit to the output of the internal logic block 21 can be reduced down to a negligible level. Therefore, lowering in the integration density of the output circuit of the internal logic block 21 and lowering in the switching speed can be prevented.

(h) In the output level converter 221 according to a preferred embodiment, the high input impedance MOS circuit is endowed with the function of logically processing a plurality of output signals of the internal logic block 21. Thus, the design versatility of a logic semiconductor integrated circuit IC of the master slice type or the gate

array type can be enhanced.

(i) In the output level converter 221 according to a preferred embodiment, a control circuit for controlling an output terminal OUT_1 into a floating state on the basis of an enable signal EN is arranged. Therefore, in a case where this output terminal OUT_1 and the output terminal of another logic circuit are connected in common, the level of the common output terminal can be set in accordance with the output of the other logic circuit.

(j) In a preferred embodiment, the internal logic block 21 which is formed of a pure CMOS circuit or a quasi-CMOS circuit thereby to have its power consumption reduced is arranged in the central part of the front surface of a semiconductor chip, while the input level converters 201, ····· and the output level converters 221, ····· each of which includes a plurality of bipolar transistors and exhibits a high power consumption are arranged in the peripheral edge parts of the front surface of the semiconductor chip. Thus, heat dissipation is facilitated. It has therefore been possible to put the logic semiconductor integrated circuit device IC into a radiation fin-less structure and to curtail the cost thereof.

(k) According to a preferred embodiment, the logic semiconductor integrated circuit device IC is put into a resin-molded structure, and hence, the curtailment of

the cost thereof has become possible.

(1) Meanwhile, the input terminal IN_1 of the input level converter 201 is not connected to the gate of a MOS FET, but it is connected to the cathode of the Schottky barrier diode D_1 or the base of the P-N-P transistor Q_4. It has therefore been permitted to enhance the breakdown strength against a surge voltage applied to the input terminal IN_1.

The following modifications of the above described embodiments may be made.

(a) The circuit shown in Fig. 6, can be arranged such that the level converters 201, 202 .....20n of the input buffer 20 execute ECC - CMOS level conversion, while the level converters 221, 222 ..... 22m of the output buffer 22 execute CMOS - ECL level conversion. In accordance with this arrangement, the input buffer 20, internal logic block 21 and output buffer 22 may be operated with earth potential and a minus supply voltage $-V_{EE}$. Likewise, in Fig. 6, the arrangement can be such that the level converters 201,202 ... 20n of the input buffer 20 execute i^2L - CMOS level conversion, while the level converters 221, 222 .... 22m of the output buffer 22 execute CMOS - i^2L level conversion.

(b) In the embodiments of Figs. 14 to 21, Figs. 23 to 26 and Figs. 29 and 30, the P-N-P emitter follower transistors Q_4 and the P-N junction diode D_2 in Fig. 31 may well be added.

(c) In addition, the reason why the denominator L of the ratio W/L of the MOS FET is set at 3 is that the channel length of the MOS FET is assumed to be 3 μm. The channel length L is presently being reduced down to 2 μM, 1.5 μm and 1 μm or less owing to improvements in photolithography, and the denominator L of the ratio W/L will become smaller accordingly. As a result the device sizes of bipolar transistors will be reduced further, resulting in changes in the resistances of resistors within the circuit

(d) The method of taking the large number of leads L_1, ... L_{64} out of the moulding resin 301 is not restricted to the embodiment shown in Fig. 39, either. It is more appropriate for reducing the size of the lead frame L_T as well as the circuit device IC and attains a higher packaging density on the printed circuit board that the external shape of the moulding resin 301 is made a substantially square, not an oblong, so as to take out the large number of leads L_1, ... L_{64} from all the four sides.

(e) In addition to the input buffer 20, internal logic block 21 and output buffer 22, being arranged on the semiconductor chip, the bipolar analog circuit, MOS analog circuit, P-channel MOS logic or N-channel MOS logic i^2L circuit, and ECL circuit may all be arranged on the semiconductor chip as desired.

Attention is drawn to our Application No. 84.01959 (Serial No. 2,135,148) from which the present Application has been divided.

CLAIMS.

1. A semiconductor integrated circuit including:

(a) an internal logic block including a plurality of quasi-CMOS circuits, the input stage of each of said quasi-CMOS circuits including P-channel and N-channel MOSFETs, and the output stage of each of said quasi-CMOS circuits including bipolar transistors; said internal logic block performing logic operations on input signals and generating output signals based upon the logic operations; and

(b) an output level converter having an input terminal coupled to receive at least one of said output signals of said internal logic block, in order to thereby provide an output signal of predetermined levels different than that of CMOS levels at an output terminal of said output level converter;

wherein an output transistor of said output level converter for executing charge or discharge of an output load capacitance of said output level converter is formed as a first bipolar output transistor; and

wherein said output level converter further comprises a high input impedance circuit which is connected between a base of said first bipolar output transistor and said input terminal of said output level converter.

2. A semiconductor integrated circuit according to claim 1, further including:

(c) a driver transistor which drives said

first bipolar output transistor for executing the discharge of the output load capacitance; and

(d) a second bipolar output transistor for executing the charge of said output load capacitance, in response to the input signal of said input terminal of said output level converter.

3. A semiconductor integrated circuit according to claim 1, wherein said high input impedance circuit is constructed of MOSFETs.

4. A semiconductor integrated circuit according to claim 3, wherein said high input impedance circuit logically processes a plurality of output signals of said internal logic block.

5. A semiconductor integrated circuit according to claim 2, further including:

(e) a control circuit which turns "off" the discharging first bipolar output transistor and the charging second bipolar output transistor of said output level converter simultaneously in response to a control signal, in order to thereby bring said output terminal of said output level converter into a float state.

6. A semiconductor integrated circuit according to claim 5, wherein said output terminal of said output level converter is connected in common with an output terminal of another semiconductor integrated circuit.

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THE PATENT OFFICE

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Switchboard 01-831 2525

RENEWAL DETAILS

PATENT No 2177866

RENEWAL DATE 25-1-84

RENEWAL FEE PAID FOR 5th year YEAR ON 15-1-88

E Dobinson

FOR THE COMPTROLLER

NOTE RENEWALS FILED WITHIN THE LAST FEW DAYS MAY NOT APPEAR IN THE RECORDS