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(54) Title: III-NITRIDE METAL INSULATOR SEMICONDUCTOR FIELD EFFECT TRANSISTOR

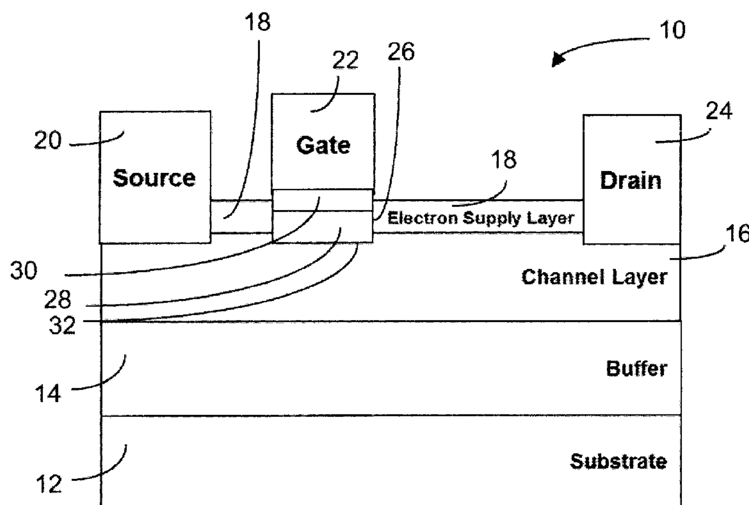

FIG. 1

(57) Abstract: A field effect transistor (FET) includes a Ill-Nitride channel layer, a III -Nitride barrier layer on the channel layer, wherein the barrier layer has an energy bandgap greater than the channel layer, a source electrode electrically coupled to one of the Ill-Nitride layers, a drain electrode electrically coupled to one of the Ill- Nitride layers, a gate insulator layer stack for electrically insulating a gate electrode from the barrier layer and the channel layer, the gate insulator layer stack including an insulator layer, such as SiN, and an AlN layer, the gate electrode in a region between the source electrode and the drain electrode and in contact with the insulator layer, and wherein the AlN layer is in contact with one of the III- Nitride layers.

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1. A field effect transistor (FET) comprising:

a III -Nitride channel layer;

a III -Nitride barrier layer on the channel layer, wherein the barrier layer has an energy bandgap greater than the channel layer;

a source electrode electrically coupled to one of the III-Nitride layers;

a drain electrode electrically coupled to one of the III -Nitride layers;

a gate trench between the source electrode and the drain electrode, the gate trench extending into the barrier layer or into the channel layer;

a gate insulator layer stack for electrically insulating a gate electrode from the barrier layer and the channel layer, the gate insulator layer stack comprising:

an AlN layer at a bottom of the gate trench; and

an insulator layer, such as SiN, over the AlN layer; and

the gate electrode in a region between the source electrode and the drain electrode and in contact with the insulator layer;

wherein the AlN layer is in contact with one of the III-Nitride layers;

wherein the field effect transistor is a normally-off field effect transistor.

2. The FET of claim 1 wherein:

the insulator layer is 1-50 nanometers thick; and

the AlN layer is 1-50 nanometers thick.

3. The FET of claim 1 wherein the bottom of the gate trench is in the barrier layer or in the channel layer.

4. The FET of claim 1 wherein:

the AlN layer is on the barrier layer; and

the insulator layer is above the AlN layer.

5. The FET of claim 1 further comprising;

a substrate comprising silicon (Si) , silicon carbide (SiC) , sapphire, gallium nitride (GaN) , or aluminum nitride (AlN) ; and

a buffer layer between the substrate and the channel layer .

6. The FET of claim 1 wherein:

the channel layer comprises GaN; and

the barrier layer comprises AlGaN.

7. The FET of claim 1 wherein the AlN layer comprises a single crystalline material, an amorphous material, or a poly-crystalline material.

8. The FET of claim 1 wherein a threshold voltage is greater than 1 volt (V).

9. The FET of claim 1 wherein a threshold voltage hysteresis is less than 0.5V.

10. The FET of claim 1 wherein a gate leakage current density is less than 10μA/mm within a gate bias range of -5V to +5V.

11. The FET of claim 1 wherein an off-state drain leakage current density is less than 10μA/mm at a gate bias of 0V.

12. The FET of claim 1 wherein a maximum drain current density is greater than 150mA/mm.

13. A method of fabricating a field effect transistor (FET) comprising:

forming a III -Nitride channel layer above a substrate;

forming a III -Nitride barrier layer on the channel layer, wherein the barrier layer has an energy bandgap greater than the channel layer;

forming a source electrode electrically coupled to one of the III-Nitride layers;

forming a drain electrode electrically coupled to one of the III -Nitride layers;

forming a gate trench between the source electrode and the drain electrode, the gate trench extending into the barrier layer or extending into the channel layer;

forming a gate insulator layer stack for electrically insulating a gate electrode from the barrier layer and the channel layer, the gate insulator layer stack comprising:

forming an AlN layer at a bottom of the gate trench; and

forming an insulator layer, such as SiN, over the AlN layer; and

forming the gate electrode on the insulator layer in a region between the source electrode and the drain electrode;

wherein the AlN layer is in contact with one of the III-Nitride layers .

14. The method of claim 13 wherein:

the insulator layer is 1-50 nanometers thick; and

the AlN layer is 1-50 nanometers thick.

15. The method of claim 13 wherein the bottom of the gate trench is in the barrier layer or in the channel layer.

16. The method of claim 15 wherein forming a gate trench comprises etching or plasma etching.

17. The method of claim 13 wherein:

the AlN layer is formed on the barrier layer; and

the insulator layer is formed above the AlN layer.

18. The method of claim 13 further comprising;

providing a substrate comprising silicon (Si) , silicon carbide (SiC) , sapphire, gallium nitride (GaN) , or aluminum nitride (AlN) ; and

forming a buffer layer between the substrate and the channel layer.

19. The method of claim 13 wherein the AlN layer is formed of a single crystalline material, an amorphous material, or a poly-crystalline material.

20. The method of claim 13 wherein forming the gate insulator layer stack comprises:

growing the AlN layer and the insulator layer using chemical vapor deposition (CVD) with a growth temperature higher than 300 degrees centigrade.

21. The method of claim 13 wherein forming the gate insulator layer stack comprises:

growing the AlN layer at a temperature less than 800 degrees centigrade by metal -organic chemical vapor deposition (CVD) ;

wherein the AlN layer is an amorphous material, or a poly-crystalline material.

22. The method of claim 13 wherein:

forming a III-Nitride channel layer comprises:

growing the channel layer using chemical vapor deposition or molecular beam epitaxy;

wherein the channel layer has a thickness of 5 nanometers to 3 micrometers; and

forming a III –Nitride barrier layer comprises:

growing the barrier layer using chemical vapor deposition or molecular beam epitaxy;

wherein the barrier layer has a thickness of 5 nanometers to 50 nanometers.