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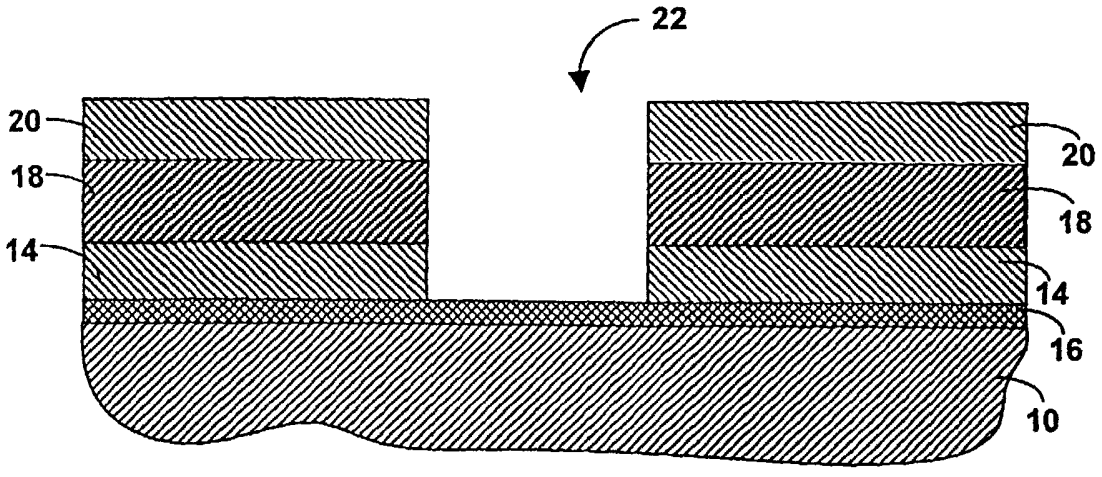
(54) Title: TECHNIQUES FOR FABRICATING A RESISTOR ON A FLEXIBLE BASE MATERIAL



(57) Abstract: A technique for fabricating a resistor on a flexible substrate (10) (28). Specifically, at least a portion of a polyimide substrate (10) (28) is activated by exposure to a ion sputter etch techniques. A metal layer (14) (36) is depositing over the activated portion (12) (34) of the substrate (10) (28), thereby resulting in the formation of a highly resistive metal-carbide region (16) (38). Interconnect layers (18, 20) (40, 42) are deposited over the metal-carbide region (16) (38) and patterned to form terminals (24, 26) (44, 46) at opposite ends of the metal carbide region (l6) (38). The metal-carbide region (16) (38) is patterned to form a resistor between the terminals. Alternatively, only a selected area of the polyimide substrate (10) (28) is activated. The selected area forms the area in which the metal-carbide region (16) (38) is formed. Interconnect layers (18, 20) (40, 42) are disposed over the metal-carbide region (16) (38) and patterned to form terminals (24, 26) (44, 46) at opposite ends of the metal-carbide region (16) (38).

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TECHNIQUES FOR FABRICATING A RESISTOR ON A FLEXIBLE BASE MATERIAL

BACKGROUND OF THE INVENTION

This invention relates generally to resistor fabrication and, more specifically, to highly resistive structures formed on a flexible base material and techniques for fabricating such a structure.

A number of commercial applications implement semiconductor devices which may be susceptible to electrostatic discharge. One such device is a semiconductor light emitting diode (LED). LEDs are semiconductor chips that are packaged to emit radiation in response to an applied voltage or current. These LEDs are used in a number of commercial applications such as automotive, display, safety/emergency and directed area lighting. LEDs may be fabricated using any materials which emit visible, ultra-violet or infrared radiation. Thus, LED devices may comprise materials having a p-n junction of semiconductor layers capable of emitting the desired radiation. For example, the LED devices may be fabricated using any desirable III-V semiconductor compound layer, such as GaAs, GaAlAs, GaN, InGaN, GaP, etc., II-VI semiconductor compound layers, such as ZnSe, ZnSSe, CdTe, etc., or IV-IV semiconductor compound layers, such as SiC, for example. Further, the LED devices may also include other layers such as cladding layers, wave guide layers and contact layers.

Currently semiconductor devices, such as LEDs, may be fabricated on a flexible base material such as polyimide to provide flexible device arrays that are conformal to a variety of different shapes for use in a variety of products. For instance, LED arrays may be fabricated on a flexible base material for use in lighting products such as round lamp bulbs, flood lights, cylindrical flashlights, etc. However, semiconductor devices such as GaN based LEDs, for example, are sensitive to electrostatic discharge, because they are fabricated on insulating sapphire substrates. As a result, there is no clear discharge path for electrostatic discharge other than through the LED. Electrostatic discharge through the LED may result in severe damage to the LED by degrading the p-

n junction characteristics of the device. It is therefore advantageous to create an alternative path for electrostatic discharge.

One mechanism for minimizing the likelihood of electrostatic damage to the semiconductor devices, such as LEDs, is to incorporate a high value bleed resistor to provide a discharge path for charge dissipation. However, for semiconductor devices fabricated on flexible base materials, the fabrication of resistors may offer certain challenges. It is often difficult to fabricate small high value thin film resistors in the range of 100 kohms - 1 Mohm on a flexible base material such as polyimide. Commonly used resistor films such as tantalum nitride (TaN_2), nickel chrome (NiCr), and chromium silicide (CrSi) have sheet resistance values in the range of 100-300 ohms/square. At these values, resistors in the range of 100 kohms - 1 Mohm are generally patterned in serpentine structures which may cover very large areas. For semiconductor devices fabricated on a flexible base material, the large serpentine structures used to fabricate the highly resistive thin film resistors may be unfeasible. Further, processing on flexible based materials, such as polyimide films, generally require relatively low temperatures (<200°C) such that the film maintains structural integrity. The lower temperatures required for processing on flexible base materials precludes the use of many of the materials that are typically used to fabricate high value resistors in semiconductor devices, since the materials require processing temperatures greater than 200°C.

BRIEF DESCRIPTION OF THE INVENTION

In accordance with one aspect of the present invention, there is provided a method of fabricating a resistor comprising the acts of activating a region on the surface of a flexible substrate, thereby forming an activated region, forming a resistive layer in the activated region, depositing one or more interconnect layers over at least a portion of the resistive layer, and patterning the one or more interconnect layers to form terminals of a resistor.

In accordance with another aspect of the present invention, there is provided a method of fabricating a resistor comprising the acts of activating the surface of a flexible substrate, thereby forming an activated layer, depositing a first metal layer over the surface of the activated layer, thereby causing a reaction in the activated layer that results in the formation of a resistive layer, depositing one or more interconnect layers over the first metal layer, etching each of the one or more interconnect layers and the first metal layer to the resistive layer, thereby forming terminals, and patterning the resistive layer to form a resistor coupled between the terminals.

In accordance with a further aspect of the present invention, there is provided a method of fabricating a resistor comprising the acts of depositing a masking layer over the surface of a flexible substrate, forming an opening in the masking layer, thereby exposing a portion of the flexible substrate through the opening, activating the exposed portion of the flexible substrate, thereby forming an activated region, removing the masking layer from the surface of the flexible substrate, depositing one or more interconnect layers over the surface of the flexible substrate, and patterning the one or more interconnect layers to form isolated terminals electrically coupled with respect to each other by the activated region.

In accordance with still another aspect of the present invention, there is provided a device comprising a flexible substrate, a resistive region formed on the flexible substrate and having a first end and a second end, and conductive terminals coupled to each of the first end and the second end.

In accordance with yet another aspect of the present invention, there is provided a device comprising a flexible substrate having a first side and a second side, a light emitting diode (LED) coupled to the first side of the flexible substrate and electrically coupled to contact regions on the second side of the flexible substrate, and a resistor formed on the second side of the flexible substrate, wherein the resistor is electrically coupled between each of the contact regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-6A illustrate a cross-sectional view of a first exemplary technique for fabricating a resistor in accordance with the present invention;

Figs. 7-12A illustrate a cross-sectional view of a second exemplary technique for fabricating a resistor in accordance with the present invention;

Fig. 13 illustrates a cross-sectional view of an exemplary light emitting diode (LED) die array; and

Fig. 14 illustrates a backside view of the LED die array illustrated in Fig. 14 incorporating the resistors fabricated in accordance with the present techniques.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

A first exemplary technique for fabricating high value resistors (in the range of 100 kohms - 1 Mohm) on a flexible base material will now be described with reference to Figs. 1-6A. Fig. 1 illustrates a flexible substrate material 10 on which the resistor will be fabricated. The flexible substrate 10 has a thickness of 0.5 mils – 3 mils and comprises a flexible plastic sheet that can be bent into a desired shape. A flexible substrate, capable of being bent or flexed, is defined as a film or composite with a

modulus of elasticity not exceeding 10,000 PSI at 23 degrees C, tested by the Standard Flexure Stiffness method. The flexible substrate material 10 is an electrically insulating material and preferably comprises a polymer film upon which an electrically conductive material can adhere. The flexible substrate material 10 includes an elastic modulus and coefficients of thermal and humidity expansion which provide minimal dimensional change during processing. To maintain flexibility, the thickness of the flexible substrate material 10 may be minimized. However the substrate material 10 also has enough rigidity (due to either thickness or material composition) to support layers of metallization and maintain dimensional stability through all subsequent processing steps. The flexible substrate 10 generally comprises any one of a number of polyimide-based materials. For example, the flexible substrate

10 may comprise a Kapton® polyimide sheet that is provided as a roll by E.I. DuPont De Nemours & Co., an Apical® polyimide sheet provided by Kanegafuchi Chem. Indus. Co., or an Upilex® polyimide sheet provided by UBE Indus. Inc. While the present techniques are generally directed to fabricating resistors on flexible base materials, such as polyimide, the exemplary techniques described herein may also be implemented on a more rigid substrate having a polyimide-based top layer.

Initially, the flexible substrate 10 is placed in a vacuum chamber wherein a physical vapor deposition (PVD) technique may be implemented to activate the flexible substrate 10. By activating the surface of the flexible substrate 10, the surface is rendered more reactive such that carbon bonds can be more easily formed, as described further below. To implement the PVD process, the flexible substrate 10 is placed in a substrate carrier in the chamber and gas, such as argon (Ar), is introduced into the chamber. To reduce contamination within the chamber and to provide a cleaning effect at the surface of the flexible substrate 10, a small negative bias (charge) may be applied to the substrate carrier. Radio frequency (RF) sputtering may be used in conjunction with electrical biasing to advantageously etch and clean the exposed surface of the flexible substrate 10. Etching and cleaning are achieved by biasing the substrate carrier at a different field potential than the argon (Ar) gas which is introduced into the vacuum chamber and ionized to a positive charge, causing the argon atoms to impinge directly on the exposed surface of the flexible substrate 10. Removal of contamination from the surface of the flexible substrate 10 improves electrical contact between the exposed flexible substrate 10 regions and the materials later disposed thereon and improves adhesion to the surface of the flexible substrate 10.

Aside from removing surface impurities, the ion bombardment of the argon (Ar) ions at the surface of the flexible substrate 10 also causes a preferential bond-breaking of imide carbonyl groups and results in the formation of graphite-like carbon, thus "activating" the surface of the flexible substrate 10 thereby making it receptive to the formation of carbide bonds with the introduction of an additional material. The bombardment of the Argon (Ar) ions onto the surface of the flexible substrate 10 is illustrated in Fig. 2. As previously described, the ion bombardment removes surface impurities and activates the

surface of the flexible substrate 10. By activating the surface of the flexible substrate 10, an activated region 12 is formed on the surface of the flexible substrate 10. As described below, the activated region 12 may be used to form high value resistor structures by providing an active area that easily combines with other materials to form a highly resistive region.

After the flexible substrate 10 is activated, a layer of titanium (Ti) 14 is deposited on the flexible substrate 10, as illustrated in Figure 3. The Ti layer 14 may be disposed using a second type of PVD technique such as planar magnetron sputtering. As can be appreciated by those skilled in the art, magnetron sputtering may be implemented using a low chamber pressure and a chamber temperature of less than 200°C which is advantageous for fabrication on polyimide-based materials, such as the flexible substrate 10. The Ti layer 14 may be disposed at a thickness of 300 angstroms – 1000 angstroms, for example. A system such as an MRC 603 may be used to implement the magnetron sputtering. In one embodiment, the chamber may be set to a pressure of 6μ and operated at a power level of 800W for 4 minutes to dispose the Ti layer 14.

As the Ti layer 14 is disposed onto the flexible substrate 10, the activated region 12 of the flexible substrate 10 reacts strongly with the titanium (Ti) and charge transfer occurs via the carbonyl groups of the activated region 12. As the Ti layer 14 coverage increases, a thin titanium carbide (Ti-C) layer 16 forms in the activated region 12 of the flexible substrate 10, as illustrated in Fig. 3. The Ti-C layer 16 is highly resistive (100 Kohms - 1 Mohm) and can therefore be used to fabricate high value (100 Kohms - 1 Mohm) resistors on the surface of the flexible substrate 10.

After the deposition of the Ti layer 14 and the formation of the Ti-C layer 16, interconnect materials may be deposited on the Ti layer 14 as illustrated in Fig. 4. A copper (Cu) seed layer 18 may be deposited on the Ti layer 14 by a physical vapor deposition (PVD) process, for example. The Cu seed layer 18 may be deposited at a thickness of 3000 angstroms, for example. Next, the Cu seed layer 18 may be electroplated. Finally, to complete the interconnect, a seed layer of titanium (Ti) 20 may

be deposited over the Cu seed layer 18 by a PVD process, for example. The Ti seed layer 20 is optional and may be deposited at a thickness of 1000 angstroms, for example.

Next, the Ti-C layer 16 is patterned into a resistor element having a highly resistive region coupled between two terminals. In one process, a photoresist patterning technique may be implemented. First, a photoresist (not shown) may be applied over the Ti seed layer 20 and patterned to provide an opening 22 which may be etched in the interconnect layers to expose a region of the underlying Ti-C layer 16, as illustrated with respect to Fig. 5. As can be appreciated, a photoresist may be patterned such that a wet or dry etch process may be implemented to remove each of the layers of the interconnect in a desirable pattern. For instance, a wet chemical etch process using a hydrofluoric acid (HF) solution for Ti and a ferric chloride ($FeCl_3$) for Cu may be used to selectively remove the areas patterned by the photoresist. While removing the lower Ti layer 14 using the HF solution, the Ti-C layer 16 remains unetched. It should be understood that those skilled in the art readily understand the deposition, masking and etching techniques needed to construct the structure illustrated in Fig. 5. The interconnect layers may be etched such that the opening 22 exposes a portion of the underlying Ti-C layer 16.

Fig. 5A illustrates a top view of the structure illustrated with respect to Fig. 5. As can be appreciated, the Ti-C layer 16 is exposed through the interconnect layers. The remainder of the surface remains covered with the interconnect layers. Accordingly, the top layer (Ti layer 20) is the only other material visible in the present view. The Ti-C layer 16 forms a resistor that may be coupled to an integrated circuit device by additional processing of the interconnect layers as further described with reference to Figs. 6 and 6A.

Fig. 6 illustrates the further fabrication of a resistor formed with the Ti-C layer 16. Fig. 6A illustrates a top view of the structure illustrated in Fig. 6. A photoresist may be used to further pattern the interconnect layers to provide isolated terminal regions 24 and 26. The terminal regions 24 and 26 are patterned to isolate the Ti-C layer 16 to form a high value resistor that may be electrically coupled to an integrated pattern

device, such as an LED, via the terminal regions 24 and 26. Accordingly, the structure of the terminal regions 24 and 26 will vary depending on the application. In the present exemplary embodiment, a simple linear resistor has been patterned, as best illustrated in Fig. 6A.

A two-step etch process may be implemented to form the structure illustrated with reference to Figs. 6 and 6A. First, a photoresist is patterned to form the desired structure of the terminal regions 24 and 26. As with the etch process described with reference to Figs. 5 and 5A, the interconnect layers are etched to the surface of the Ti-C layer 16 by a chemical etchant, for example. It should be understood that those skilled in the art readily understand the deposition, masking and etching techniques needed to construct the structure illustrated in Figs. 6 and 6A. While the present exemplary embodiment implements a first etch to pattern the structure illustrated with respect to Figs. 5 and 5A, and a second etch to further pattern the structure as illustrated in Figs. 6 and 6A, a single etch step may be implemented to etch the interconnect layers such that the underlying Ti-C layer 16 is exposed.

After the interconnect layers are removed, via a wet etch process, for example, the underlying Ti-C layer 16 may be etched using a dry etch process, such as a plasma etch. The dry plasma etch may be implemented using a CF_4 gas mixed with O_2, for example. The plasma etch will remove any areas of the resistive Ti-C layer 16 that are exposed to the gas/plasma. Accordingly, a photoresist mask may be applied over the exposed areas of the Ti-C layer 16 that are to be retained to form the resistor. In the present embodiment illustrated in Figs. 6 and 6A, a thin strip of photoresist may be applied in the opening 22 and patterned to cover the narrow region of the Ti-C layer 16 illustrated in Fig. 6A. The plasma etch removes any exposed areas of the Ti-C layer 16. Areas of Ti-C not covered by the protective photoresist or the interconnect layers will be removed during the plasma etch. Accordingly, the areas around the terminal regions 24 and 26 are etched to expose the underlying flexible substrate 10. As illustrated in Figs. 6 and 6A, the remaining structure forms a resistive region (the strip of Ti-C material 16) coupled between the terminal regions 24 and 26. Fig. 6A provides a top view of the final structure wherein the Ti seed layer 20 is viewable as

the top layer of the interconnect and the remainder of the Ti-C layer 16 is coupled between the terminal regions 24 and 26 such that a resistor is formed on the surface of the flexible substrate 10. As previously described, the resistor may be patterned to form any desired shape.

Figs. 7-12A illustrate an alternate exemplary technique for fabricating high value resistors (in the range of 100 kohms – 1 Mohm). As will become evident, many of the fabrication steps and materials are the same as the steps and materials described above with reference to Figs. 1-6A. To avoid repetition, some of the specific details have been omitted in the discussion below. However, the discussion of the exemplary technique described with reference to Figs. 7-12A should be read in view of the more complete processing and material descriptions discussed above with reference to Figs. 1-6A.

Referring initially to Fig. 7, a flexible substrate 28 is illustrated. As previously discussed, the flexible substrate 28 generally comprises a polyimide-based material. Initially, a masking layer, such as a layer of titanium (Ti) 30, is deposited over the flexible substrate 28 by a physical vapor deposition (PVD) process, for example. In the present exemplary embodiment, the Ti layer 30 may be deposited at a thickness of 300 angstroms – 1000 angstroms, for example. In the present exemplary embodiment, the Ti layer 30 will be used as an activation mask to control the area of the flexible substrate 28 that will be activated, as described further below.

Referring to Fig. 8, an opening 32 is etched in the Ti layer 30. The Ti layer 30 may be patterned using a photoresist and photomask and then etched implementing a wet chemical etch process using a hydrofluoric acid (HF) solution, for example. The opening 32 is patterned to the desirable dimensions of the region that will be activated. Thus, the opening 32 provides a window to expose a portion of the flexible substrate 28. Fig. 8A is a top view of the structure illustrated in Fig. 8. As illustrated with reference to Fig. 8A, the surface of the flexible substrate 28 is completely covered by the Ti layer 30, with the exception of the area etched through the opening 32 (Fig. 8) to expose the underlying flexible substrate 28.

Next, the area of the flexible substrate 28 that is exposed through the opening 32 is subjected to high energy argon (Ar) ion bombardment to activate the exposed area of the flexible substrate 28, as illustrated in Fig. 9. As previously described, the argon (Ar) ion bombardment at the surface of the flexible substrate 28 causes a preferential bond-breaking of imide carbonyl groups and the formation of graphite-like carbon, thereby forming an activated region 34 of the flexible substrate 28 receptive to the formation of carbide bonds with the introduction of an additional material. The activated region 34 may be used to form high value resistor structures by providing an active area that easily combines with other materials to form a highly resistive region. As can be appreciated, the Ti layer 30 provides a mask for the planar magnetron sputtering (ion bombardment) process such that the only area of the flexible substrate 28 that is activated is the area not covered by the Ti layer 30 (i.e. the area exposed through the opening 32). By patterning the Ti layer 30 to provide a selective opening, the shape of the resistive area is already established, thereby eliminating the later step of forming the resistive geometry through plasma etching as described in the previous embodiment with respect to Figs. 6 and 6A. Further, in the present exemplary embodiment, the Ti layer 30 is implemented to provide a masking layer. Titatium is used to avoid contamination in the magnetron sputtering chamber. However, other materials may be used to provide a masking layer.

After formation of the activated region 34, the masking layer (Ti layer 30) is completely removed, as illustrated in Fig. 10. The Ti layer 30 may be etched implementing a wet chemical etch process using a hydrofluoric acid (HF) solution, for example. Thus, the remaining structure includes the flexible substrate 28 having a patterned activated region 34.

Next, interconnect layers are disposed on the surface of the flexible substrate 28, as illustrated in Fig. 11. First, a layer of titanium (Ti) 36 is deposited using a PVD technique, such as planar magnetron sputtering. The Ti layer 36 may be disposed at a thickness of 300 angstroms – 1000 angstroms, for example. As the Ti layer 36 is disposed onto the flexible substrate 28, the activated region 34 reacts strongly with the titanium (Ti) and charge transfer occurs via the carbonyl groups of the activated region

34. As the Ti layer 36 coverage increases, a thin titanium carbide (Ti-C) layer 38 forms in the activated region 34, as illustrated in Fig. 3. As previously described, the Ti-C layer 38 is highly resistive and can therefore be used to fabricate high value (100 Kohms - 1 Mohm) resistors on the surface of the flexible substrate 38.

After the deposition of the Ti layer 36 and the formation of the Ti-C layer 38, additional interconnect materials may be disposed over the Ti layer 36, as further illustrated in Fig. 11. A copper (Cu) seed layer 40 may be deposited on the Ti layer 36 using physical vapor deposition (PVD), for example. The Cu seed layer 40 may be disposed at a thickness of 3000 angstroms, for example. Next, the Cu seed layer 40 may be electroplated. Finally, to complete the interconnect, a seed layer of titanium (Ti) 42 may be disposed over the Cu seed layer 40 by a PVD process, for example. The Ti seed layer 42 is optional and may be disposed at a thickness of 1000 angstroms, for example.

Because the Ti-C layer 38 is already patterned into a useful resistor, the only remaining step is to form the terminal regions by patterning the interconnect layers into a desirable pattern. Fig. 12 illustrates the formation of the terminal regions 44 and 46. Fig. 12A illustrates a top view of the structure illustrated in Fig. 12. A photoresist may be used to pattern the interconnect layers to provide isolated terminal regions 44 and 46. After the photoresist is patterned, the interconnect layers are etched to the surface of the flexible substrate 28 by a chemical etchant, for example. As previously described, the terminal regions 44 and 46 are patterned to isolate the Ti-C layer 38 to form a high value resistor that may be electrically coupled to an integrated circuit device, such as an LED, via the terminal regions 44 and 46. Accordingly, the structure of the terminal regions 44 and 46 will vary depending on the application. In the present exemplary embodiment, a simple linear resistor has been patterned, as best illustrated in Fig. 12A. It should be understood that those skilled in the art readily understand the deposition, masking and etching techniques needed to construct the structure illustrated in Figs. 12 and 12A.

As previously described, the exemplary high value resistors fabricated on the flexible substrates in accordance with the present techniques may be used in a number of

applications. For instance, the resistors may be formed on the backside of a flexible substrate to provide high value bleed resistors to prevent damage to light emitting diodes (LEDs) from electrostatic discharge. Accordingly, Figs. 13 and 14 illustrate an exemplary implementation of the present techniques.

Referring initially to Fig. 13, a cross section of an exemplary LED array 48 formed on a flexible substrate 50 is illustrated. The specific embodiment of the LED array 48 and method for fabricating the array is not critical to the present application, other than the fact that the array is fabricated on a flexible substrate 50. Accordingly, the following description of the LED array 48 is not believed to limit the presently disclosed structures in any way and is only meant to provide an exemplary use of the resistive structures described herein.

As previously described, the flexible substrate 50 generally comprises a polyimide-based material such as Kapton®. Rigid carriers 52 may be attached to the flexible substrate 50 using an adhesive layer 54. The rigid carriers 52 may comprise a ceramic material, a moldable plastic or a polymer material, for example. The adhesive layer 54 may comprise an anisotropic conductive adhesive, for example. Each rigid carrier 52 includes a LED chip 56. The LED chip 56 may be surrounded with an encapsulating material 58, such as an epoxy, glass-filled epoxy or a polymer material, such as silicone, for example. Each LED structure further includes a lens structure 60 which may comprise any suitable material that is transparent to LED radiation, such as a polycarbonate layer. The lens structure 60 improves the light output of the LED chips 56.

Each rigid carrier 52 also includes a plurality of feed-through conductive elements, such as electrodes 62 that are used to electrically couple the LED chips 56 to the underside of the rigid carriers 52. The electrodes 62 are coupled to the anisotropic conductive adhesive layer 54. Conductive interconnect paths 64 provide an electrically conductive path through the flexible substrate 50. As can be appreciated, the conductive interconnect paths 64 may comprise vias filled with a conductive material. The interconnect paths 64 are electrically coupled to interconnect layers 66 on the underside

of the flexible substrate 50. Thus, a conductive path exists from the LED chip 56 to the electrodes 62, through the anisotropic conductive adhesive layer 54, through the interconnect paths 64 and to the interconnect layers 66 on the underside of the flexible substrate 50. These interconnect layers 66 may form the terminals of a resistor structure fabricated in accordance with the techniques described herein.

Fig. 14 illustrates a backside view of the flexible substrate 50 with bleed resistors 68 fabricated thereon, in accordance with the techniques described herein. As can be appreciated, the resistor 68 advantageously provides an electrical path for the discharge of electricity. The resistors 68 and terminal regions may be fabricated into the exemplary pattern illustrated in Fig. 14. After the resistors 68 are patterned and fabricated onto the flexible substrate 50, the LED array 48 may be formed and electrically coupled to the resistors 68 to provide protection of the LED chips 56 from damage due to electrostatic discharge, as previously described.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims. For example, while reference is made herein to resistors formed in conjunction with semiconductor LEDs, the present techniques are equally applicable for use with other LED types, such as organic LEDs. Similarly, the resistors offered by the present advancement may find uses in any number of electrical and electronic circuitry within and beyond the lighting field.

CLAIMS:

1. A method of fabricating a resistor comprising the acts of:

activating a region on the surface of a flexible substrate (10) (28), thereby forming an activated region (12) (34);

forming a resistive layer (16) (38) in the activated region (12) (34);

depositing one or more interconnect layers (18, 20) (40, 42) over at least a portion of the resistive layer (16) (38); and

patterning the one or more interconnect layers (18, 20) (40, 42) to form terminals (24, 26) (44, 46) of a resistor.

2. The method, as set forth in claim 1, wherein act (a) comprises the act of ion etching the surface of a flexible substrate (10) (28).

3. The method, as set forth in claim 1, wherein act (a) comprises the act of activating a region on the surface of a polyimide substrate (10) (28).

4. The method, as set forth in claim 1, wherein act (b) comprises the act of depositing a metal layer (14) (36) over the activated region (12) (34), thereby causing a reaction in the activated region (12) (34) that results in the formation of the resistive layer (16) (38).

5. The method, as set forth in claim 4, wherein the act of depositing a metal layer (14) (36) comprises the act of depositing a titanium layer (14) (36) over the activated region (12) (34), thereby causing a reaction in the activated region (12) (34), that results in the formation of a titanium-carbide layer (16) (38).

6. The method, as set forth in claim 4, wherein act (c) comprises the act of depositing a copper layer (18) (40) over at least a portion of the metal layer (14) (36).

7. The method, as set forth in claim 6, wherein act (c) comprises the act of depositing a titanium layer (20) (42) over the copper layer (18) (40).

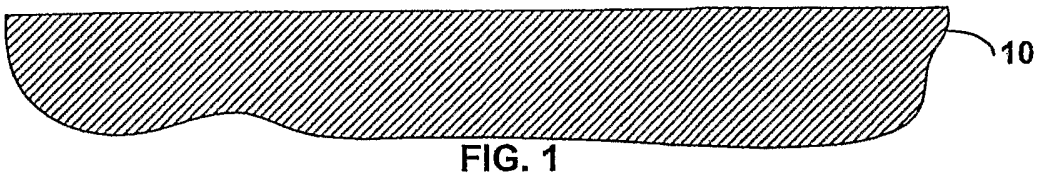

FIG. 1

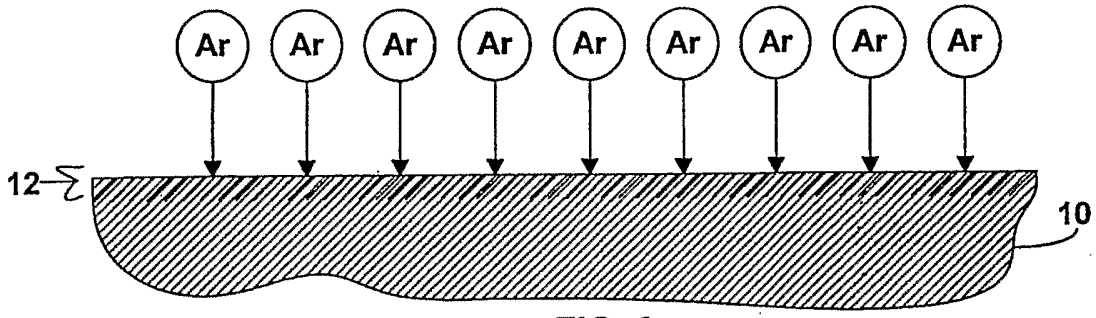

FIG. 2

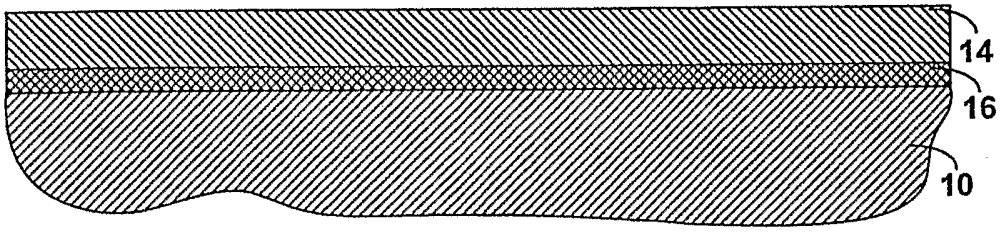

FIG. 3

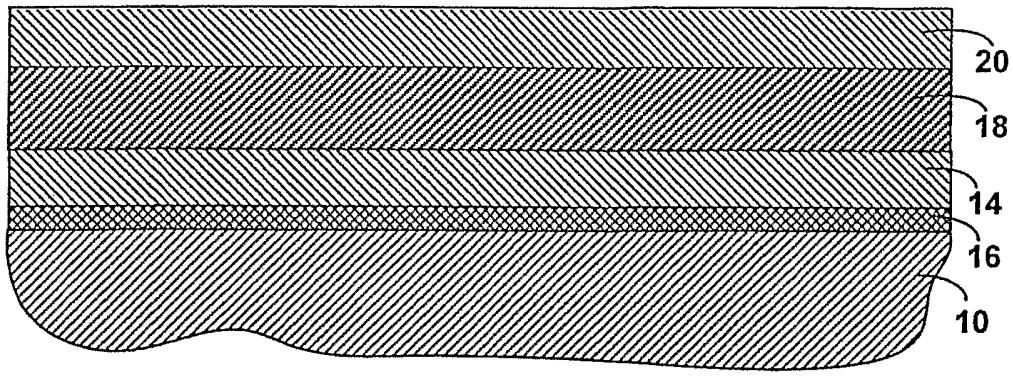

FIG. 4

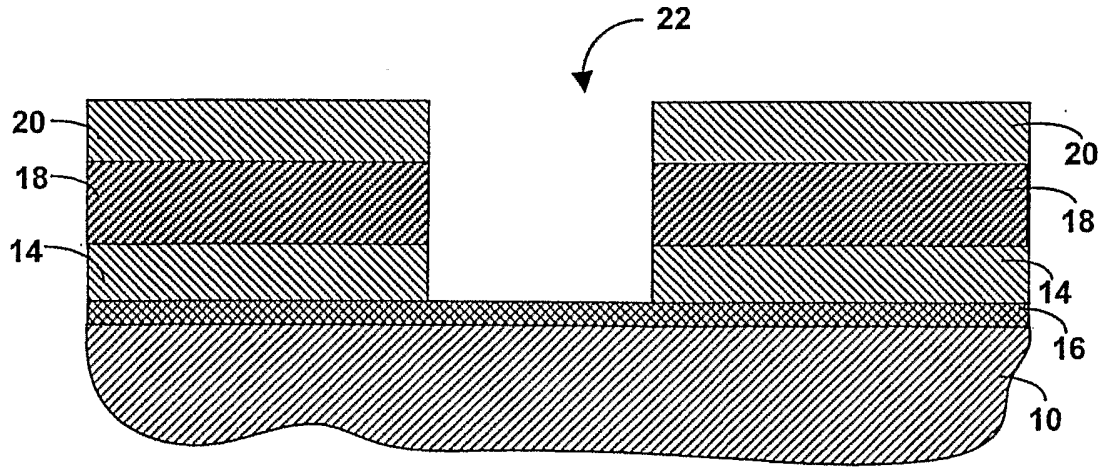

FIG. 5

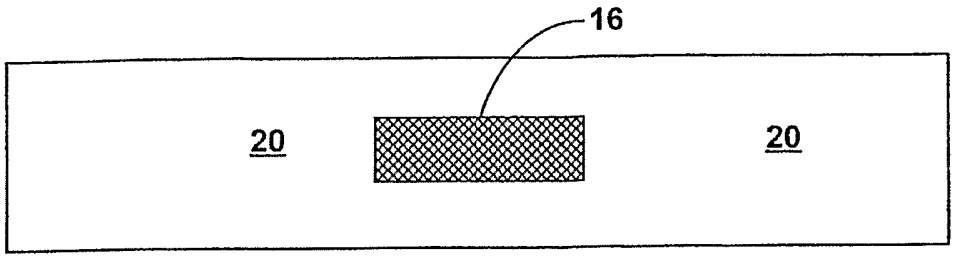

FIG. 5A

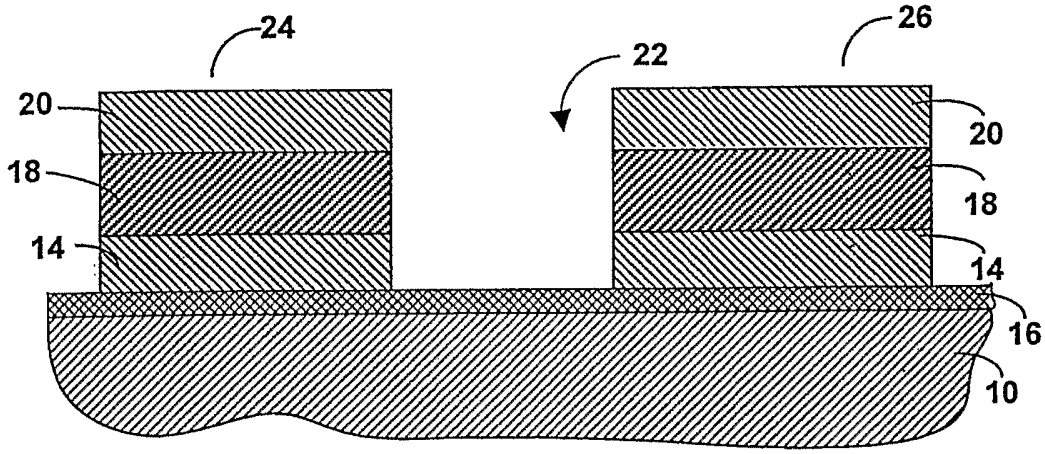

FIG. 6

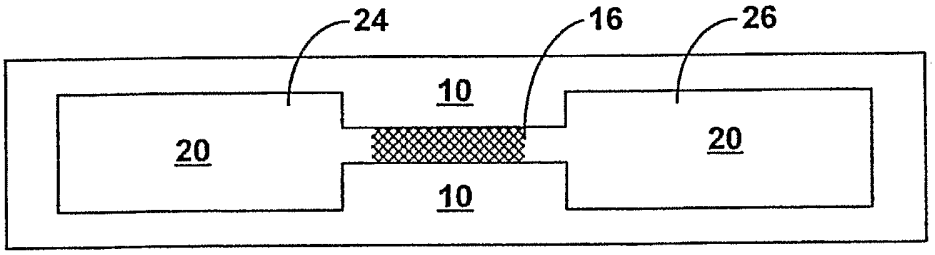

FIG. 6A

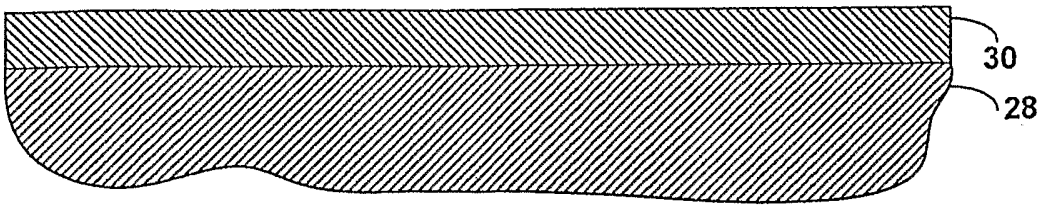

FIG. 7

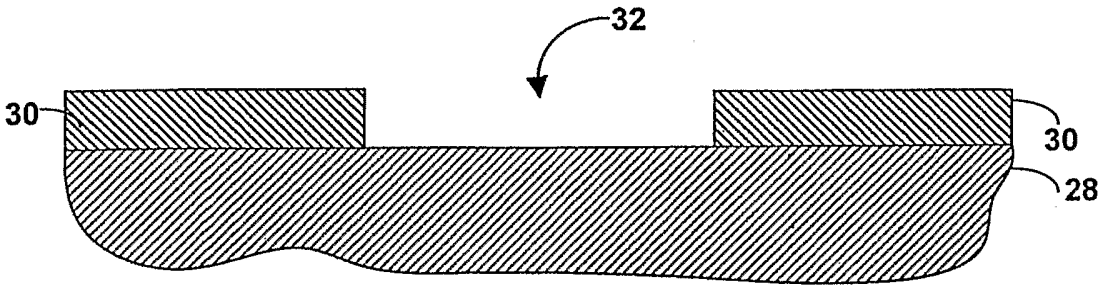

FIG. 8

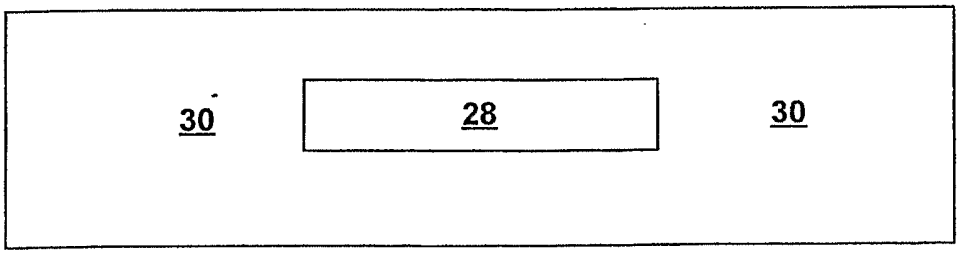

FIG. 8A

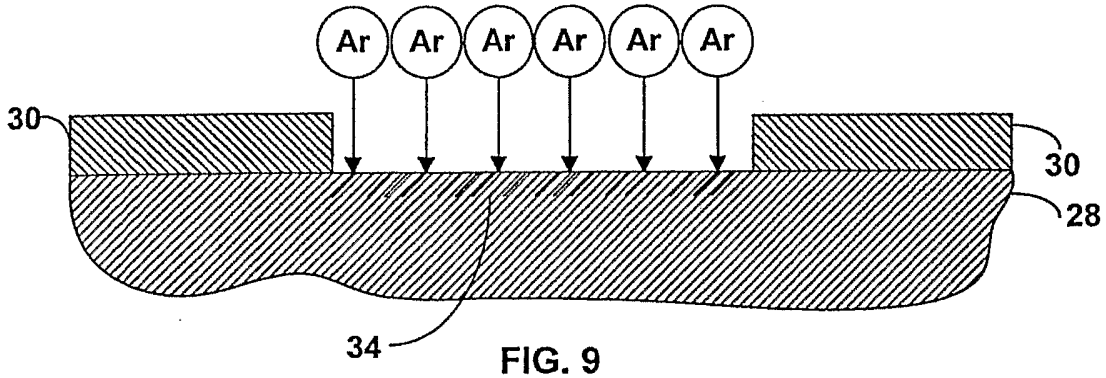

FIG. 9

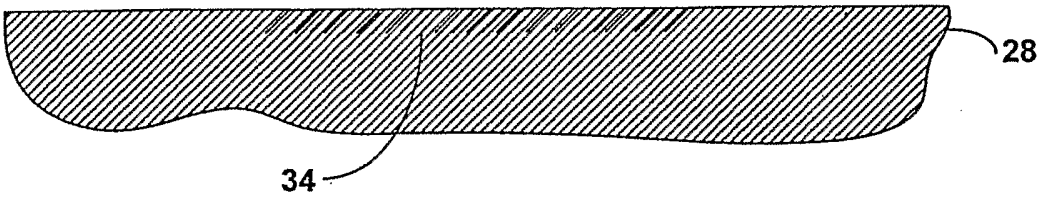

FIG. 10

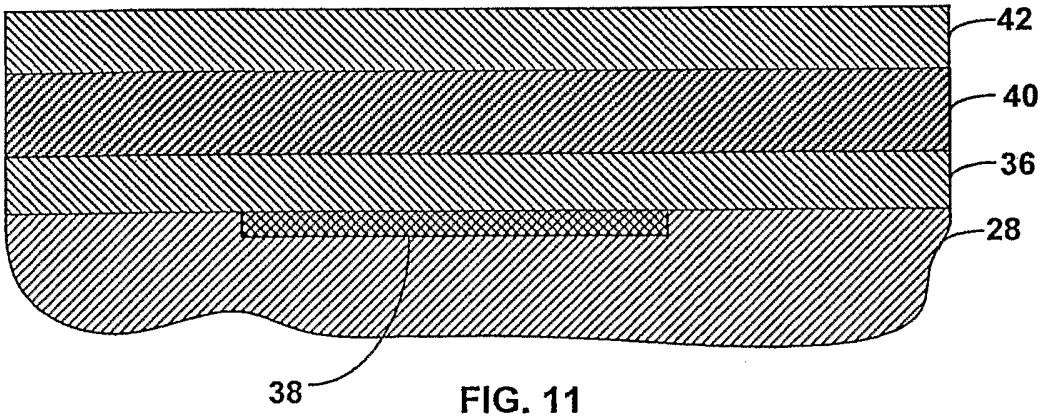

FIG. 11

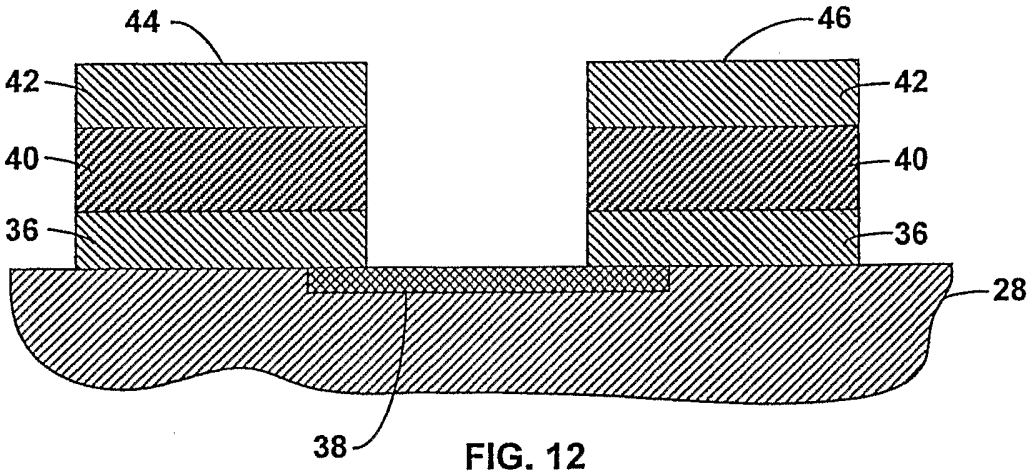

FIG. 12

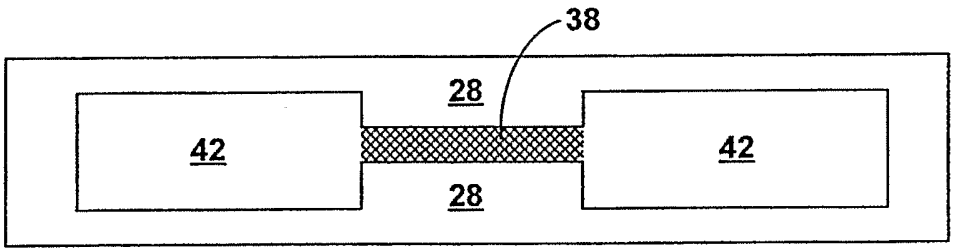

FIG. 12A

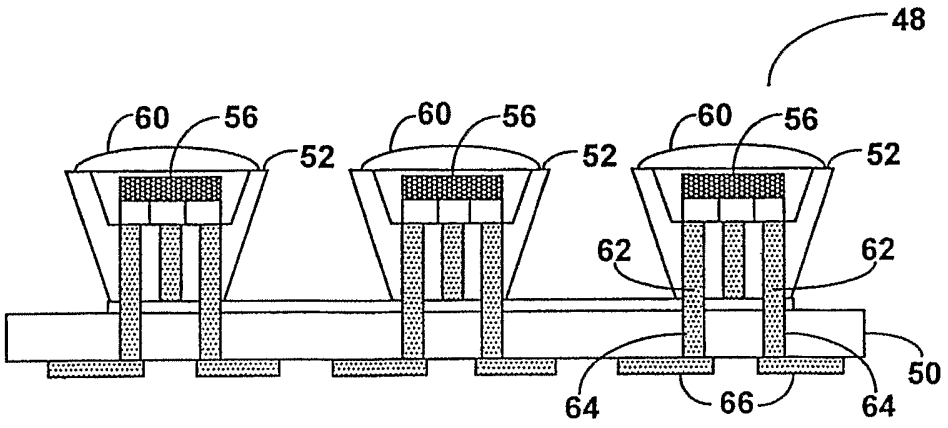

FIG. 13

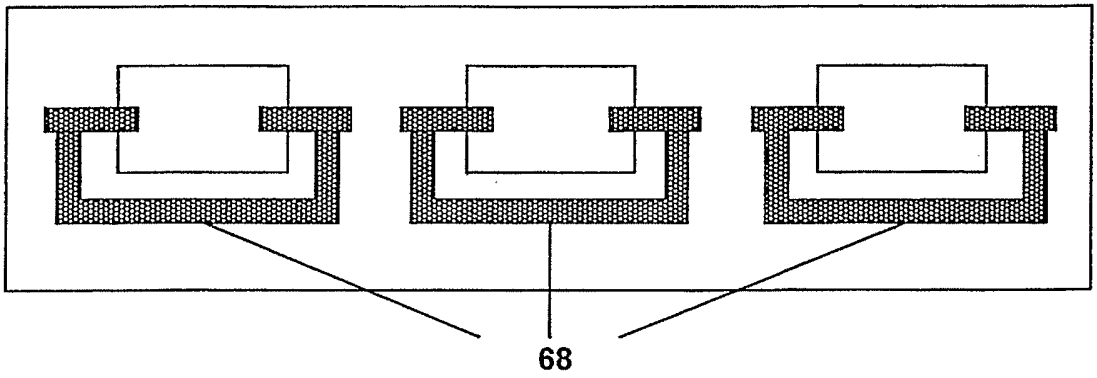

FIG. 14

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/27112

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01C7/00 H01C17/12 H05K1/16 B29C59/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01C H05K H01L B29C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 3 966 578 A (SOMMER ALFRED) 29 June 1976 (1976-06-29) column 2, line 19 -column 3, line 15; figures 1,2	1 2-4 5-7
Y A	EP 0 388 888 A (HITACHI CHEMICAL CO LTD ;HITACHI LTD (JP)) 26 September 1990 (1990-09-26) column 1, line 19 -column 11, line 1; figure 1	2-4 1,5-7
A	GB 1 319 765 A (ATOMIC ENERGY AUTHORITY UK) 6 June 1973 (1973-06-06) the whole document	1-7

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 January 2004	27/01/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Frias Rebelo, A

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INTERNATIONAL SEARCH REPORT

Informat patent family members

International A[redacted]ation No
PCT/US 03/27112

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 3966578 A	29-06-1976	US 3851291 A	26-11-1974
EP 0388888 A	26-09-1990	CA 2012579 A1	20-09-1990
		EP 0388888 A2	26-09-1990
		JP 2664265 B2	15-10-1997
		JP 3028365 A	06-02-1991
		US 5178962 A	12-01-1993
GB 1319765 A	06-06-1973	NONE	