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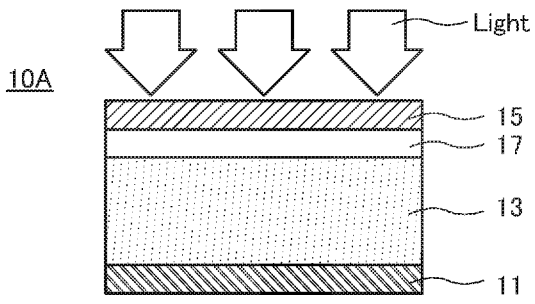
(54) Title: PHOTOELECTRIC CONVERSION ELEMENT AND MANUFACTURING METHOD THEREOF

FIG. 1A



(57) Abstract: An imaging device with high photosensitivity and high resolution is provided. A photoelectric conversion element includes a first electrode, a photoelectric conversion layer over the first electrode, a hole injection blocking layer over the photoelectric conversion layer, and a second electrode over the hole injection blocking layer. The photoelectric conversion layer contains selenium and an element X. The element X is one or more of silver, bismuth, indium, tin, and tellurium. The hole injection blocking layer contains tin, gallium, and oxygen. The hole injection blocking layer includes a region where the ratio of the number of tin atoms to the number of gallium atoms (Sn/Ga) is greater than or equal to 0.0010 and less than or equal to 0.050.

WO 2018/172880 A1

DESCRIPTION

PHOTOELECTRIC CONVERSION ELEMENT AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

[0001]

One embodiment of the present invention relates to an imaging device.

[0002]

Note that one embodiment of the present invention is not limited to the above technical field. The technical field of one embodiment of the invention disclosed in this specification and the like relates to an object, a method, or a manufacturing method. Furthermore, one embodiment of the present invention relates to a process, a machine, manufacture, or a composition of matter. Specifically, examples of the technical field of one embodiment of the present invention disclosed in this specification include a semiconductor device, a display device, a liquid crystal display device, a light-emitting device, a lighting device, a power storage device, a memory device, an imaging device, a method for operating any of them, and a method for manufacturing any of them.

[0003]

In this specification and the like, a semiconductor device generally means a device that can function by utilizing semiconductor characteristics. A transistor and a semiconductor circuit are embodiments of semiconductor devices. In some cases, a memory device, a display device, an imaging device, or an electronic device includes a semiconductor device.

BACKGROUND ART

[0004]

Imaging devices are incorporated in a variety of electronic devices, and imaging devices capable of higher-resolution imaging are required. A photoelectric conversion element in which silicon is used for a photoelectric conversion layer has been used for an imaging device; while an imaging device in which crystalline selenium, which is a material with a higher light-absorption coefficient, is used for a photoelectric conversion element has been proposed (see Patent Document 1).

[0005]

Moreover, a technique by which transistors are formed using oxide semiconductor thin films formed over a substrate has been attracting attention. For example, Patent Document 2

discloses an imaging device in which a transistor including an oxide semiconductor and having an extremely low off-state current is used in a pixel circuit.

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2014-17440

[Patent Document 2] Japanese Published Patent Application No. 2011-119711

DISCLOSURE OF INVENTION

[0007]

To make an image sensor have high resolution, the area of one pixel needs to be reduced. When the pixel area is reduced, the light-receiving area of a photoelectric conversion element is also reduced; as a result, the photosensitivity is lowered. In particular, in imaging under a low illuminance condition, the S/N ratio of imaging data largely decreases in some cases. That is, in the image sensor having the conventional structure, there is a trade-off between resolution and photosensitivity.

[0008]

A solution to the above problem is to use a photoelectric conversion element utilizing avalanche multiplication effect, which has high photosensitivity.

[0009]

Therefore, an object of one embodiment of the present invention is to provide a photoelectric conversion element with high photosensitivity. Another object is to provide an imaging device that easily performs imaging under a low illuminance condition. Another object is to provide an imaging device with low power consumption. Another object is to provide an imaging device with high resolution. Another object is to provide an imaging device with high reliability. Another object is to provide a novel imaging device or the like. Another object is to provide a novel semiconductor device or the like.

[0010]

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0011]

One embodiment of the present invention is a photoelectric conversion element including a first electrode, a photoelectric conversion layer over the first electrode, a hole injection blocking layer over the photoelectric conversion layer, and a second electrode over the

hole injection blocking layer. The photoelectric conversion layer contains selenium and an element *X*. The element *X* is one or more of silver, bismuth, indium, tin, and tellurium. The hole injection blocking layer contains tin, gallium, and oxygen.

[0012]

In the photoelectric conversion element, the hole injection blocking layer preferably includes a region where the ratio Sn/Ga is greater than or equal to 0.0010 and less than or equal to 0.050. The ratio Sn/Ga is a ratio of the number of tin atoms to the number of gallium atoms.

[0013]

In the photoelectric conversion element, the thickness of the hole injection blocking layer is preferably greater than or equal to 5 nm and less than or equal to 50 nm.

[0014]

In the photoelectric conversion element, the photoelectric conversion layer preferably contains crystalline selenium and the crystal grain size of the crystalline selenium is preferably greater than or equal to 0.010 μm and less than or equal to 1.10 μm.

[0015]

One embodiment of the present invention is a method for manufacturing a photoelectric conversion element including the steps of providing a base layer containing an element *X* over a first electrode, providing a layer containing selenium over the base layer, performing heat treatment, providing a hole injection blocking layer containing tin, gallium and oxygen over the layer containing selenium, and providing a second electrode over the hole injection blocking layer. The element *X* is one or more of silver, bismuth, indium, and tellurium.

[0016]

One embodiment of the present invention is a method for manufacturing a photoelectric conversion element including the steps of providing a layer containing selenium over a first electrode, providing a base layer containing an element *X* over the layer containing selenium, performing heat treatment, providing a hole injection blocking layer containing tin, gallium and oxygen over the layer containing selenium, and providing a second electrode over the hole injection blocking layer. The element *X* is one or more of silver, bismuth, indium, tin, and tellurium.

[0017]

In the method for manufacturing a photoelectric conversion element, the heat treatment preferably contains a first process, a second process, and a third process. The first process is preferably performed at a temperature higher than or equal to 50 °C and lower than or equal to 90 °C. After the first process, the second process is preferably performed at a temperature higher than the temperature of the first process and higher than or equal to 70 °C and lower than

or equal to 170 °C. After the second process, the third process is preferably performed at a temperature higher than the temperature of the second process and higher than or equal to 110 °C and lower than or equal to 220 °C.

[0018]

In the method for manufacturing a photoelectric conversion element, the hole injection blocking layer is preferably formed in vacuum through the first and second processes successively. The first process is preferably performed before the second process. The proportion of oxygen in the whole deposition gas is preferably higher in the second process than in the first process.

[0019]

One embodiment of the present invention can provide a photoelectric conversion element with high photosensitivity. Another embodiment can provide an imaging device that easily performs imaging under a low illuminance condition. Another embodiment can provide an imaging device with low power consumption. Another embodiment can provide an imaging device with high resolution. Another embodiment can provide an imaging device with high reliability. Another embodiment can provide a novel imaging device or the like. Another embodiment can provide a novel semiconductor device or the like.

[0020]

Note that one embodiment of the present invention is not limited to these effects. For example, one embodiment of the present invention might produce another effect depending on circumstances or conditions. Furthermore, for example, one embodiment of the present invention might not produce any of the above effects depending on circumstances or conditions.

BRIEF DESCRIPTION OF DRAWINGS

[0021]

In the accompanying drawings:

FIGS. 1A to 1C are cross-sectional views illustrating structures of photoelectric conversion elements;

FIGS. 2A and 2B are diagrams showing band structures of a photoelectric conversion element;

FIG. 3 is a diagram showing a band structure of a photoelectric conversion element;

FIG. 4 is a flow chart showing a method for manufacturing a photoelectric conversion element;

FIGS. 5A to 5E are cross-sectional views illustrating a method for manufacturing a photoelectric conversion element;

FIGS. 6A to 6D are cross-sectional views illustrating a method for manufacturing a photoelectric conversion element;

FIGS. 7A to 7D are schematic cross-sectional views illustrating solid phase crystallization;

FIGS. 8A to 8C are schematic cross-sectional views illustrating solid phase crystallization;

FIG. 9 is a diagram showing a thermal profile of heat treatment;

FIGS. 10A and 10B are a diagram illustrating a pixel circuit and a timing chart showing imaging operation;

FIGS. 11A and 11B are a diagram illustrating a structure of a pixel of an imaging device and a block diagram of the imaging device;

FIGS. 12A to 12C are cross-sectional views illustrating a structure of an imaging device;

FIGS. 13A to 13C are cross-sectional views illustrating structures of an imaging device;

FIGS. 14A to 14C are cross-sectional views illustrating structures of an imaging device;

FIGS. 15A1 to 15A3 and 15B1 to 15B3 are perspective views of a package including an imaging device;

FIGS. 16A to 16F illustrate electronic devices;

FIGS. 17A and 17B are cross-sectional views illustrating a sample in Example 1;

FIGS. 18A and 18B are plan SEM images according to Example 1;

FIGS. 19A and 19B are plan SEM images according to Example 1;

FIGS. 20A and 20B are plan SEM images according to Example 1;

FIGS. 21A and 21B are plan SEM images according to Example 1;

FIGS. 22A and 22B are plan SEM images according to Example 1;

FIGS. 23A and 23B are plan SEM images according to Example 1;

FIGS. 24A to 24D are diagrams illustrating a method for calculating a crystal grain size according to Example 1;

FIGS. 25A and 25B are histograms of a crystal grain size according to Example 1;

FIGS. 26A and 26B are histograms of a crystal grain size according to Example 1;

FIGS. 27A and 27B are diagrams showing current-voltage characteristics according to Example 2;

FIGS. 28A and 28B are diagrams showing current-voltage characteristics according to Example 2;

FIG. 29 is a diagram showing current-voltage characteristics according to Example 2;

FIG. 30 is a diagram showing wavelength dependence of a current amplification factor according to Example 2;

FIGS. 31A and 31B are cross-sectional STEM images according to Example 2;

FIG. 32 is a cross-sectional STEM image according to Example 2;

FIGS. 33A and 33B are cross-sectional STEM images according to Example 2;

FIGS. 34A and 34B are cross-sectional STEM images according to Example 2;

FIGS. 35A and 35B are diagrams showing current-voltage characteristics according to Example 3;

FIG. 36 is a diagram showing wavelength dependence of current-voltage characteristics according to Example 3;

FIGS. 37A and 37B are diagrams showing measurement temperature dependence of a dark current according to Example 3;

FIGS. 38A and 38B are diagrams showing XPS spectra around a valence band according to Example 4;

FIG. 39 is a diagram showing XPS spectra according to Example 5;

FIGS. 40A to 40D are diagrams showing XPS spectra according to Example 5;

FIG. 41 is a diagram showing UPS spectra according to Example 5;

FIGS. 42A to 42C are diagrams showing transmittance and reflectance according to Example 5;

FIGS. 43A to 43C are Tauc plots according to Example 5;

FIGS. 44A and 44B are diagrams showing current-voltage characteristics according to Example 6;

FIGS. 45A and 45B are diagrams showing current-voltage characteristics according to Example 6;

FIG. 46 is a diagram showing wavelength dependence of a current amplification factor according to Example 6;

FIGS. 47A and 47B are diagrams showing current-electric field strength characteristics according to Example 7;

FIGS. 48A and 48B are diagrams showing current-electric field strength characteristics according to Example 7; and

FIG. 49 is a diagram showing wavelength dependence of a current amplification factor according to Example 7.

BEST MODE FOR CARRYING OUT THE INVENTION

[0022]

Embodiments will be described in detail with reference to drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be interpreted as being limited to the description of embodiments below. Note that in structures of the present invention described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and description thereof is not repeated in some cases. It is also to be noted that the same components are denoted by different hatching patterns in different drawings, or the hatching patterns are omitted in some cases.

[0023]

Note that the ordinal numbers such as "first" and "second" in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. Thus, for example, the term "first" can be replaced with the term "second," "third," or the like as appropriate. In addition, the ordinal numbers in this specification and the like do not correspond to the ordinal numbers, which specify one embodiment of the present invention in some cases.

[0024]

Note that the terms "film" and "layer" can be interchanged with each other depending on the case or circumstances. For example, the term "conductive layer" can be changed into the term "conductive film" in some cases, and the term "insulating film" can be changed into the term "insulating layer" in some cases.

[0025]

(Embodiment 1)

In this embodiment, a photoelectric conversion element of one embodiment of the present invention will be described with reference to drawings.

[0026]

<Structure example of photoelectric conversion element>

A schematic view of a cross-sectional structure of a photoelectric conversion element 10A of one embodiment of the present invention is illustrated in FIG. 1A. The photoelectric conversion element 10A includes a first electrode 11, a photoelectric conversion layer 13 over the first electrode 11, a hole injection blocking layer 17 over the photoelectric conversion layer 13, and a second electrode 15 over the hole injection blocking layer 17.

[0027]

One embodiment of the present invention is a photoelectric conversion element in which selenium is used for the photoelectric conversion layer 13, which is capable of imaging utilizing avalanche multiplication effect at relatively low voltage. When crystalline selenium is used for the photoelectric conversion layer, photosensitivity can be improved in almost the entire visible light region. As a result, a photoelectric conversion element having such a structure can have higher photosensitivity than a conventional photoelectric conversion element in which silicon is used for a photoelectric conversion layer; thus, imaging under a low illuminance condition can be easily performed. Furthermore, an imaging device capable of high-resolution imaging can be provided.

[0028]

An n-type semiconductor having an ionization potential of greater than or equal to 7.0 eV and a band gap of greater than or equal to 4.0 eV and containing an element that forms a donor level is preferably used for the hole injection blocking layer 17. Tin-containing gallium oxide can be favorably used for the hole injection blocking layer 17, for example.

[0029]

It can be said that a pn junction is formed in the photoelectric conversion element of one embodiment of the present invention in which selenium, which is a p-type semiconductor, is used for the photoelectric conversion layer 13 and an n-type semiconductor is used for the hole injection blocking layer 17. The hole injection blocking layer 17 that is an n-type semiconductor layer with a wide band gap and appropriate carrier density can decrease a dark current and increase a photocurrent.

[0030]

As a photoelectric conversion element 10B illustrated in FIG. 1B, the hole injection blocking layer 17 preferably has a stacked structure of a first hole injection blocking layer 17a and a second hole injection blocking layer 17b over the first hole injection blocking layer 17a. Tin-containing gallium oxide can be used for each of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b.

[0031]

Alternatively, as a photoelectric conversion element 10C illustrated in FIG. 1C, the photoelectric conversion element of one embodiment of the present invention may include an electron injection blocking layer 19 between the photoelectric conversion layer 13 and the first electrode 11.

[0032]

The photoelectric conversion element may be formed over a substrate or over a driver transistor formed in or over a substrate.

[0033]

The second electrode 15 side is a light-receiving surface of each of the photoelectric conversion elements 10A to 10C. In FIGS. 1A to 1C, light (Light) entering each of the photoelectric conversion elements 10A to 10C is indicated by arrows.

[0034]

<Components of photoelectric conversion element>

Components of the photoelectric conversion element of one embodiment of the present invention will be described in below.

[0035]

[Photoelectric conversion layer 13]

The photoelectric conversion layer 13 will be described. A selenium-based material can be used for the photoelectric conversion layer 13. A photoelectric conversion element including a selenium-based material has high internal quantum efficiency with respect to visible light. In such a photoelectric conversion element, carriers generated by incident light are amplified due to the effect of charge amplification by an avalanche phenomenon; thus, the photoelectric conversion efficiency can be improved. A photodiode utilizing avalanche multiplication effect is referred to as an avalanche photodiode (APD) in some cases.

[0036]

Crystalline selenium is preferably used for the photoelectric conversion layer 13. Selenium can be classified into single crystal selenium, polycrystalline selenium, microcrystalline selenium, amorphous selenium, and the like according to its crystallinity. In this specification and the like, "crystalline selenium" means selenium having crystallinity such as single crystal selenium, polycrystalline selenium, or microcrystalline selenium. Alternatively, mixed selenium including crystalline selenium and amorphous selenium may be used. In this specification and the like, "having crystallinity" may be referred to as "being crystalline."

[0037]

Since crystalline selenium has a higher absorption coefficient in the entire wavelength region of visible light than silicon and amorphous selenium, the crystalline selenium can be thinner than the silicon and the amorphous selenium. Thin film thickness enables high electric field application. Moreover, avalanche multiplication effect occurs in the crystalline selenium at low voltage and the crystalline selenium has high photosensitivity. Therefore, a photoelectric conversion element containing crystalline selenium in the photoelectric conversion layer 13 has high photosensitivity and is suitable for imaging even in a low-illuminance environment. Furthermore, such a photoelectric conversion element is preferable because it can be operated at low voltage.

[0038]

Since selenium has a melting point of as low as approximately 221 °C, amorphous selenium may be crystallized when exposed to a high temperature in manufacturing process or a usage environment. Thus, amorphous selenium has low thermal stability. In contrast, the photoelectric conversion layer 13 of the photoelectric conversion element of one embodiment of the present invention has high thermal stability because of containing uniform crystalline selenium.

[0039]

The crystallinity of the selenium contained in the photoelectric conversion layer 13 can be evaluated using X-ray diffraction (XRD), electron diffraction (ED), an image obtained with a transmission electron microscope (TEM), an image obtained with scanning transmission electron microscopy (STEM), or the like.

[0040]

A known method for obtaining crystalline selenium is to form amorphous selenium and then perform heat treatment. However, crystallization of amorphous selenium by heat treatment could cause aggregation of selenium; thus, there may be a region not containing selenium. In this specification and the like, such a region is referred to as a film separation region. The film separation region in a photoelectric conversion layer may vary the characteristics of photoelectric conversion elements, which may reduce the imaging performance of an imaging device. Moreover, when unevenness of the photoelectric conversion layer 13 is increased along with aggregation of the selenium or generation of the film separation region, coverage and adhesion of the second electrode 15 over the photoelectric conversion layer 13 become poor in some cases. The poor coverage and adhesion of the second electrode 15 can cause a short circuit between the first electrode 11 and the second electrode 15. Since a surface of the photoelectric conversion layer 13 is to be a pn-junction surface, an uneven shape, for example, causes degradation in interface properties. Thus, a photoelectric conversion layer is preferably a uniform crystalline selenium that includes few film separation regions and has little unevenness.

[0041]

The photoelectric conversion layer 13 of one embodiment of the present invention contains selenium and an element *X*. The element *X* is one or more of silver, bismuth, indium, tin, and tellurium. The element *X* together with selenium forms a compound (hereinafter, the compound is referred to as a selenium compound). The photoelectric conversion layer 13 of one embodiment of the present invention contains crystalline selenium formed by solid phase crystallization (SPC) using the selenium compound as a crystal nucleus. In the solid phase

crystallization, the surface of the photoelectric conversion layer 13 may become uneven along with the growth of crystal grains. Moreover, in the case where the crystal grains are large, the surface unevenness of the photoelectric conversion layer 13 may be large. Thus, the surface unevenness of the photoelectric conversion layer 13 can be decreased by making the crystal grains small. Note that the photoelectric conversion layer 13 of one embodiment of the present invention may include an element other than selenium and the element *X*. Examples of the element other than the element *X* include silicon and germanium.

[0042]

The crystal grain size (major diameter) of the photoelectric conversion layer 13 is preferably less than or equal to 1.10 μm, further preferably less than or equal to 1.00 μm, still further preferably less than or equal to 0.90 μm. With the above crystal grain size (major diameter), the surface unevenness of the photoelectric conversion layer 13 can be small. As a result, the coverage and adhesion of the second electrode 15 over the photoelectric conversion layer 13 having small surface unevenness become high, whereby a short circuit between the first electrode 11 and the second electrode 15 can be prevented. Moreover, when the surface unevenness of the photoelectric conversion layer 13 is small, the pn-junction surface has excellent interface properties. Accordingly, a photoelectric conversion element having favorable characteristics can be manufactured. Note that the minimum value of the crystal grain size (major diameter) is preferably greater than or equal to 0.010 μm although there is no particular limitation. With the crystal grain size (major diameter) of greater than or equal to 0.010 μm, a trap level due to a grain boundary can be reduced, which enables manufacture of a photoelectric conversion element having favorable characteristics.

[0043]

Note that in this specification and the like, the length of the longest line connecting two points on an outline of the crystal grain is regarded as the crystal grain size (major diameter).

[0044]

The crystal grain size (major diameter) of the selenium contained in the photoelectric conversion layer 13 can be measured using an image obtained with scanning electron microscopy (SEM), an image obtained with a transmission electron microscope (TEM), an image obtained with scanning transmission electron microscopy (STEM), an electron backscatter diffraction (EBSD) pattern, or the like.

[0045]

The photoelectric conversion layer 13 preferably includes a region where the ratio of the atomic concentration of the element *X* to the atomic concentration of selenium (*X*/Se) is greater than or equal to 0.0010 and less than or equal to 0.70, preferably greater than or equal to 0.0030

and less than or equal to 0.50, further preferably greater than or equal to 0.0050 and less than or equal to 0.30. If *X*/Se is in the above range, the photoelectric conversion layer 13 that contains uniform crystalline selenium and includes few film separation regions can be formed. Note that segregation of the element *X* at a grain boundary or a surface of the crystalline selenium may increase a dark current. If *X*/Se is in the above range, a photoelectric conversion element and an imaging device can have a small dark current.

[0046]

The element *X* preferably has a high diffusion coefficient in selenium and forms a compound with the selenium. The selenium compound preferably has crystallinity. The degree of mismatch between the lattice constant of single crystal selenium and the lattice constant of the selenium compound is preferably small. It is further preferable that the selenium compound has the same crystal structure as the single crystal selenium; however, when the degree of mismatch between the lattice constants is small, the selenium compound may have a crystal structure different from that of the single crystal selenium. Note that the photoelectric conversion layer 13 of one embodiment of the present invention includes the selenium compound in some cases. In the case of using two or more elements as the element *X*, the total atomic concentration of those elements may be used as the value *X* of *X*/Se.

[0047]

The atomic concentrations of the selenium and the element *X* of the photoelectric conversion layer 13 can be measured using energy dispersive X-ray spectroscopy (EDX), secondary ion mass spectrometry (SIMS), time-of-flight secondary ion mass spectrometry (ToF-SIMS), X-ray photoelectron spectroscopy (XPS), auger electron spectroscopy (AES), electron energy-loss spectroscopy (EELS), or the like.

[0048]

In this specification and the like, the "ratio of the atomic concentration" is the same as the "ratio of the number of atoms," so that the "ratio of the atomic concentration" can be replaced with the "ratio of the number of atoms." That is, the value of *X*/Se can be regarded as the ratio of the atomic concentration of the element *X* to the atomic concentration of selenium, and the ratio of the number of atoms of the element *X* to the number of selenium atoms.

[0049]

[Hole injection blocking layer 17]

The photoelectric conversion element of one embodiment of the present invention includes the hole injection blocking layer 17 between the photoelectric conversion layer 13 and the second electrode 15 as illustrated in FIGS. 1A to 1C. The hole injection blocking layer 17 suppresses hole injection from the second electrode 15 into the photoelectric conversion layer 13.

Since the hole injection blocking layer 17 suppresses charge injection into the photoelectric conversion layer 13, the hole injection blocking layer 17 is referred to as a charge injection blocking layer in some cases.

[0050]

The hole injection blocking layer 17 preferably has a light-transmitting property with respect to visible light. When the hole injection blocking layer 17 has the light-transmitting property, the photoelectric conversion element can have high photosensitivity in the entire visible light region. The hole injection blocking layer 17 preferably has a wide band gap. The hole injection blocking layer 17 with a wide band gap can suppress hole injection from the electrode to the photoelectric conversion layer, so that the photoelectric conversion element can have a small dark current. In addition, the hole injection blocking layer 17 preferably has a low barrier to electrons. If the barrier to electrons is high, electrons may be trapped by the barrier and problems such as an image lag or image persistence may occur in imaging. When a photoelectric conversion element has a low barrier to electrons, an image lag or image persistence hardly occurs. Moreover, the hole injection blocking layer 17 preferably has few defect states. If the number of defect states is large, an effective energy barrier with respect to holes is lowered and a dark current is increased in some cases. Since the hole injection blocking layer 17 has few defect states, a photoelectric conversion element can have a low dark current. Tin-containing gallium oxide can be favorably used for the hole injection blocking layer 17, for example.

[0051]

The hole injection blocking layer 17 of one embodiment of the present invention contains tin, gallium, and oxygen. The hole injection blocking layer 17 preferably includes a region where the atomic concentration of tin is greater than or equal to 0.020 atomic% and less than or equal to 2.0 atomic%, further preferably greater than or equal to 0.10 atomic% and less than or equal to 1.2 atomic%, still further preferably greater than or equal to 0.20 atomic% and less than or equal to 1.0 atomic%. If the tin concentration is in the above range, the photoelectric conversion element can have a large current amplification factor.

[0052]

The hole injection blocking layer 17 preferably includes a region where the ratio of the atomic concentration of tin to the atomic concentration of gallium (Sn/Ga) is greater than or equal to 0.0010 and less than or equal to 0.050, preferably greater than or equal to 0.0030 and less than or equal to 0.030, further preferably greater than or equal to 0.0050 and less than or equal to 0.020. If Sn/Ga is in the above range, the photoelectric conversion element can have a large current amplification factor.

[0053]

In addition, a tunnel current flowing through the hole injection blocking layer 17 needs to be prevented so that the hole injection blocking layer 17 is efficiently utilized; therefore, the layer needs to be greater than or equal to a certain thickness. The thickness is preferably set to be greater than or equal to 5 nm and less than or equal to 50 nm, further preferably greater than or equal to 10 nm and less than or equal to 40 nm, for example. If the thickness is in the above range, a photoelectric conversion element can have a small dark current.

[0054]

The energy difference between the Fermi level and the valence band (E_f–E_v) of crystalline selenium is smaller than that of amorphous selenium, so that the crystalline selenium may have higher carrier density than the amorphous selenium. When the photoelectric conversion layer 13 has high carrier density, a photoelectric conversion element may have a high dark current (I_{dark}) and a small current amplification factor (I_{photo}/I_{dark}).

[0055]

In this specification and the like, the current amplification factor (I_{photo}/I_{dark}) refers to the ratio of a photocurrent (I_{photo}) to a dark current (I_{dark}), that is, the value of a photocurrent (I_{photo}) / a dark current (I_{dark}).

[0056]

In order to obtain a large current amplification factor, a low dark current or a high photocurrent is needed. The high photocurrent is effectively obtained by increasing a depletion layer width *Wp* in the photoelectric conversion layer 13 when voltage is applied to a photoelectric conversion element. The depletion layer width *Wp* in the photoelectric conversion layer 13 when voltage is applied to the photoelectric conversion element can be expressed by Formula 1.

[0057]

[Formula 1]
$$Wp = \sqrt{\frac{2 \times \varepsilon \times Nd}{q \times Na \times (Nd + Na)} \times (Vbi - V)} \quad \text{(Formula 1)}$$

[0058]

Here, *Wp* is the depletion layer width in the photoelectric conversion layer 13, *Nd* is the carrier density of the hole injection blocking layer 17, *Na* is the carrier density of the photoelectric conversion layer 13, ε is a dielectric constant, *q* is elementary charge, *Vbi* is internal potential, and *V* is an applied voltage.

[0059]

As expressed by Formula 1, the depletion layer width *Wp* in the photoelectric conversion layer 13 is greatly affected by the ratio of the carrier density of the hole injection blocking layer 17 and the carrier density of the photoelectric conversion layer 13. A high photocurrent is effectively obtained by using the hole injection blocking layer 17 having the carrier density appropriate for the carrier density of the photoelectric conversion layer 13.

[0060]

As described above, crystalline selenium may have higher carrier density than amorphous selenium. In the case where crystalline selenium is used for a photoelectric conversion layer, a photocurrent and a current amplification factor can be increased by using the hole injection blocking layer 17 having high carrier density.

[0061]

FIG. 2A is a band diagram of a stacked structure of the second electrode 15, the hole injection blocking layer 17, and the photoelectric conversion layer 13. In this example, amorphous selenium and indium gallium oxide are respectively used for the photoelectric conversion layer 13 and the hole injection blocking layer 17. The band gap of the amorphous selenium is approximately 2.3 eV and an energy difference between the Fermi level and the valence band (Ef–Ev) of the amorphous selenium is approximately 0.2 eV. The band gap of the indium gallium oxide is approximately 4.6 eV. Note that the atomic ratio of the indium gallium oxide is In:Ga = 5:95.

[0062]

FIG. 2B is a band diagram in the case where crystalline selenium and indium gallium oxide are respectively used for the photoelectric conversion layer 13 and the hole injection blocking layer 17. The band gap of the crystalline selenium is approximately 1.8 eV and an energy difference between the Fermi level and the valence band (E_f–E_v) of the crystalline selenium is approximately 0.1 eV. The energy difference between the Fermi level and the valence band of the crystalline selenium is smaller than that of the amorphous selenium, so that the crystalline selenium may have higher carrier density than the amorphous selenium. Therefore, the depletion layer width *Wp* in the structure illustrated in FIG. 2B in which crystalline selenium is used is smaller than that in the structure illustrated in FIG. 2A in which amorphous selenium is used. When the depletion layer width *Wp* is small, incident light is not fully absorbed in the depletion layer; thus, the incident light is absorbed also in a region other than the depletion layer. Photocarriers generated in the depletion layer can be efficiently extracted outside by an internal electric field; however, photocarriers generated in a region other than the depletion layer are deactivated.

[0063]

Thus, in order to efficiently extract the photocarriers outside, that is, in order to increase a photocurrent (I_{photo}), the depletion layer width *Wp* formed in the photoelectric conversion layer 13 is preferably increased. The depletion layer width *Wp* can be increased by heightening the carrier concentration of the hole injection blocking layer 17. However, in the case of using a material having extremely high carrier concentration, holes may be injected from the second electrode 15 into the photoelectric conversion layer 13 through a deep level. Therefore, the hole injection blocking layer 17 is preferably formed using a material having a slightly higher carrier concentration than that of indium gallium oxide. Examples of such a material include tin-containing gallium oxide.

[0064]

FIG. 3 is a band diagram in the case where crystalline selenium and tin-containing gallium oxide are respectively used for the photoelectric conversion layer 13 and the hole injection blocking layer 17. The structure illustrated in FIG. 3 is one embodiment of the present invention. The band gap of the tin-containing gallium oxide is approximately 4.6 eV and the carrier density of the tin-containing gallium oxide is higher than that of the indium gallium oxide. Therefore, the depletion layer width *Wp* in the structure illustrated in FIG. 3 is larger than that in the structure illustrated in FIG. 2B, so that a photocurrent is estimated to be increased.

[0065]

The carrier density of the hole injection blocking layer 17 can be increased by, for example, increasing oxygen vacancies (Vo) in an oxide used for the hole injection blocking layer 17. However, increased oxygen vacancies may increase deep levels and lower an effective energy barrier to holes. The low effective energy barrier with respect to holes is not preferable because it may increase a dark current. Accordingly, the hole injection blocking layer 17 preferably contains few oxygen vacancies.

[0066]

In addition to increasing oxygen vacancies (Vo), the carrier density of the hole injection blocking layer 17 can be increased by, for example, adding an element to be a donor source. Tin-containing gallium oxide is particularly preferably used for the hole injection blocking layer 17.

[0067]

In the photoelectric conversion element of one embodiment of the present invention, crystalline selenium and tin-containing gallium oxide are respectively used for the photoelectric conversion layer 13 and the hole injection blocking layer 17. The photoelectric conversion

element having the above structure can have a large current amplification factor and high thermal stability.

[0068]

As illustrated in FIG. 1B, the hole injection blocking layer 17 preferably has a stacked structure of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b over the first hole injection blocking layer 17a. A material that can be used for the hole injection blocking layer 17 can be used for each of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b.

[0069]

Tin-containing gallium oxide can be used for each of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b, for example. When the compositions of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b are substantially the same, they can be formed using the same sputtering target and the manufacturing cost can thus be reduced.

[0070]

The first hole injection blocking layer 17a and the second hole injection blocking layer 17b each preferably include a region where the atomic concentration of tin is greater than or equal to 0.020 atomic% and less than or equal to 2.0 atomic%, further preferably greater than or equal to 0.10 atomic% and less than or equal to 1.2 atomic%, still further preferably greater than or equal to 0.20 atomic% and less than or equal to 1.0 atomic%. If the tin concentration is in the above range, the photoelectric conversion element can have a large current amplification factor.

[0071]

The first hole injection blocking layer 17a and the second hole injection blocking layer 17b each preferably include a region where the ratio of the atomic concentration of tin to the atomic concentration of gallium (Sn/Ga) is greater than or equal to 0.0010 and less than or equal to 0.050, preferably greater than or equal to 0.0030 and less than or equal to 0.030, further preferably greater than or equal to 0.0050 and less than or equal to 0.020. If Sn/Ga is in the above range, the photoelectric conversion element can have a large current amplification factor.

[0072]

For the first hole injection blocking layer 17a and the second hole injection blocking layer 17b, it is particularly preferable to use stacked films deposited successively in vacuum without exposure to the air using targets with the same composition, although it is also possible to use films deposited using targets with different compositions. When the layers are deposited successively, one deposition apparatus can be shared between a plurality of deposition steps,

remaining of impurities such as atmospheric components between the first hole injection blocking layer 17a and the second hole injection blocking layer 17b can be suppressed. Impurities in the hole injection blocking layer are not preferable because the impurities form defect states serving as carrier traps and degrade the frequency characteristics of a photodiode in some cases. When the first hole injection blocking layer 17a and the second hole injection blocking layer 17b are successively formed in vacuum, an increase in defect states can be suppressed and favorable characteristics can be obtained.

[0073]

The first hole injection blocking layer 17a and the second hole injection blocking layer 17b can be formed separately in different conditions, for example. For example, the flow rates of oxygen gas in the deposition gases can be different between the first hole injection blocking layer 17a and the second hole injection blocking layer 17b.

[0074]

As the deposition condition of the first hole injection blocking layer 17a, the proportion of oxygen gas flow rate (also referred to as oxygen gas flow rate ratio or oxygen partial pressure) in a whole deposition gas is higher than or equal to 0 % and lower than or equal to 30 %, preferably higher than or equal to 5 % and lower than or equal to 15 %. With the above oxygen flow rate ratio, oxidation of the surface of the photoelectric conversion layer 13 over which the first hole injection blocking layer 17a is to be formed and the vicinity thereof can be suppressed.

[0075]

In the case where the first hole injection blocking layer 17a is formed by a sputtering method, for example, a substrate temperature is increased by collision of sputtered particles in some cases. When the substrate temperature is increased, the selenium contained in the photoelectric conversion layer 13 may be evaporated. The deposition rate of the first hole injection blocking layer 17a can be increased with the above oxygen flow rate ratio. In other words, the time during which the surface of the photoelectric conversion layer 13 is exposed to sputtered particles in the formation of the first hole injection blocking layer 17a can be shortened; thus, evaporation of the selenium can be suppressed.

[0076]

As the deposition condition of the second hole injection blocking layer 17b, the oxygen flow rate ratio is higher than 30 % and lower than or equal to 100 %, preferably higher than or equal to 35 % and lower than or equal to 100 %, further preferably higher than or equal to 40 % and lower than or equal to 70 %. With the above oxygen flow rate ratio, the second hole injection blocking layer 17b having few oxygen vacancies can be formed.

[0077]

In the case where the oxygen flow rate ratio is high, the second hole injection blocking layer 17b having crystallinity may be formed. The second hole injection blocking layer 17b having crystallinity is not preferable because it increases the resistance of the second hole injection blocking layer 17b and decreases a photocurrent in some cases. With the above oxygen flow rate ratio, the crystallinity of the second hole injection blocking layer 17b can be low and a photoelectric conversion element can have a large photocurrent.

[0078]

The thickness of the first hole injection blocking layer 17a is greater than or equal to 1 nm and less than or equal to 10 nm, preferably greater than or equal to 2 nm and less than or equal to 8 nm. The thickness of the second hole injection blocking layer 17b is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 5 nm and less than or equal to 40 nm.

[0079]

Note that there is a case where a boundary (interface) between the first hole injection blocking layer 17a and the second hole injection blocking layer 17b is not clearly observed. Then, in the drawings illustrating one embodiment of the present invention, the boundary is denoted by a dashed line.

[0080]

The hole injection blocking layer 17 may have a single layer structure. The same structure as the first hole injection blocking layer 17a or the second hole injection blocking layer 17b can be applied to the hole injection blocking layer 17. The hole injection blocking layer 17 has a single layer structure, whereby the productivity can be improved.

[0081]

[Electron injection blocking layer 19]

The photoelectric conversion element of one embodiment of the present invention may further include the electron injection blocking layer 19 between the first electrode 11 and the photoelectric conversion layer 13 as illustrated in FIG. 1C. The electron injection blocking layer 19 suppresses electron injection from the first electrode 11 into the photoelectric conversion layer 13. Since the electron injection blocking layer 19 suppresses charge injection into the photoelectric conversion layer 13, the electron injection blocking layer 19 is referred to as a charge injection blocking layer in some cases.

[0082]

The electron injection blocking layer can contain nickel oxide, antimony sulfide, or the like.

[0083]

[First electrode 11]

The first electrode 11 will be described. The first electrode 11 can be formed using gold, titanium nitride, molybdenum, tungsten, aluminum, titanium, or the like. In addition, for example, a stack of titanium, aluminum, and titanium that are stacked in this order can be used. The first electrode 11 can be formed by a sputtering method or a plasma CVD method. The first electrode 11 may be formed over a substrate or over a driver transistor formed in or over a substrate.

[0084]

The first electrode 11 illustrated in FIGS. 1A to 1C preferably has small surface unevenness in order to prevent a short circuit with the second electrode 15 caused by, for example, poor coverage with the photoelectric conversion layer 13. The first electrode 11 having small surface unevenness contributes to less unevenness of the top surface of the photoelectric conversion layer 13.

[0085]

An example of a conductive film having small surface unevenness is an indium tin oxide film containing silicon oxide at 1 wt% to 20 wt%.

[0086]

The surface unevenness can be observed using an atomic force microscope (AFM), a scanning electron microscope (SEM), or the like.

[0087]

Since the indium tin oxide film is crystallized at a relatively low temperature even when it is amorphous at the time of its deposition, surface roughness due to the growth of crystal grains is easily caused. In contrast, when analyzed by an X-ray diffraction (XRD), the indium tin oxide film containing silicon does not exhibits crystallinity even in the case where the film is subjected to heat treatment at a temperature higher than 400 °C. In other words, the indium tin oxide film containing silicon keeps its amorphous state even after heat treatment at a relatively high temperature. Therefore, the surface roughness of the indium tin oxide film containing silicon is less likely to occur.

[0088]

[Second electrode 15]

Then, the second electrode 15 will be described. The following can be used for the second electrode 15: indium tin oxide (ITO); indium tin oxide containing silicon; indium oxide containing zinc; zinc oxide; zinc oxide containing gallium; zinc oxide containing aluminum; tin oxide; tin oxide containing fluorine; tin oxide containing antimony; graphene; or the like, for example. In particular, indium tin oxide or indium tin oxide containing silicon is preferably

used. The second electrode 15 is not limited to a single layer, and may be a stacked layer of different films. Note that indium tin oxide contains In, Sn, and O.

[0089]

The second electrode 15 preferably has a high light-transmitting property so that light reaches the photoelectric conversion layer 13. When the second electrode 15 has a high light-transmitting property, an imaging device with high resolution can be provided. Specifically, in order to provide an imaging device with high resolution, it is preferable to provide many pixels. For example, to take a 2K image, 1920 × 1080 or more pixels are preferably provided; to take a 4K image, 3840 × 2160 or more pixels are preferably provided; and to take an 8K image, 7680 × 4320 or more pixels are preferably provided. The light-transmitting property is further important especially for an 8K imaging device because an area occupied by one pixel is extremely small and an area which can be used for receiving light is extremely small. The second electrode 15 can be formed over the photoelectric conversion layer 13 by a sputtering method, a plasma CVD method, or the like.

[0090]

<Method 1 for manufacturing photoelectric conversion element>

A method for manufacturing the photoelectric conversion element 10B of one embodiment of the present invention will be described.

[0091]

The method for manufacturing the photoelectric conversion element 10B containing crystalline selenium in the photoelectric conversion layer 13 will be described with reference to drawings. FIG. 4 is a flow chart showing the method for manufacturing the photoelectric conversion element 10B. FIGS. 5A to 5E are cross-sectional views illustrating the method for manufacturing the photoelectric conversion element 10B.

[0092]

First, as Step S401, the first electrode 11 is formed over a layer 41 (FIG. 5A). Note that in FIG. 5A, a layer over which the first electrode 11 is formed is illustrated as the layer 41 for convenience. The layer 41 may be a substrate or a layer including a driver transistor formed in or over a substrate.

[0093]

Next, as Step S402, a base layer 43 and an amorphous selenium layer 45 over the base layer 43 are formed over the first electrode 11 (FIG. 5B).

[0094]

The base layer 43 contains one or more elements selected from the elements that can be used for the element *X*. As the element *X*, the above-described elements can be used. One or

more of silver, bismuth, indium, indium oxide, tin, tin oxide, tellurium, In-Sn oxide (indium tin oxide or ITO), and In-Sn-Si oxide (ITSO) can be used for the base layer 43, for example. The base layer 43 may be a single layer or a stacked layer.

[0095]

The base layer 43 preferably has high wettability with respect to selenium. In addition, a selenium compound preferably has high wettability with respect to selenium. High wettability with respect to selenium can suppress aggregation, re-evaporation, or the like of selenium in crystallization of the selenium. Accordingly, generation of a film separation region in formation of crystalline selenium can be reduced. Specifically, a material containing silver is preferably used for the base layer 43. Silver diffuses in selenium rapidly. Moreover, a compound of selenium and silver (Ag_2Se) has high wettability. Similarly, a material containing bismuth is preferably used for the base layer 43.

[0096]

The thickness of the base layer 43 is preferably greater than or equal to 0.20 nm and less than or equal to 140 nm, further preferably greater than or equal to 0.60 nm and less than or equal to 100 nm, still further preferably greater than or equal to 1.0 nm and less than or equal to 60 nm. If the thickness is in the above range, a photoelectric conversion element that contains uniform crystalline selenium including few film separation regions can be formed. Moreover, an imaging device with less variation in characteristics can be manufactured with use of the crystalline selenium including few film separation regions. Furthermore, a photoelectric conversion element and an imaging device that have a small dark current can be manufactured.

[0097]

The base layer 43 can be formed by a sputtering method, an evaporation method, a pulse laser deposition (PLD) method, a plasma enhanced chemical vapor deposition (PECVD) method, a thermal chemical vapor deposition (CVD) method, an atomic layer deposition (ALD) method, a vacuum evaporation method, or the like. As an example of the thermal CVD method, a metal organic chemical vapor deposition (MOCVD) method can be given.

[0098]

Although FIG. 5B illustrates an example in which the shape of the base layer 43 is not processed, one embodiment of the present invention is not limited to this example. The base layer 43 may have an island shape as illustrated in FIG. 6A. The base layer 43 may have a stripe shape, a net-like shape, a shape in which an opening is provided, or the like. For example, the base layer 43 can be partly formed over the first electrode 11 using a metal mask. The base layer 43 formed over the first electrode 11 may be processed into a predetermined shape by dry etching or wet etching. When the base layer 43 has an island shape, the amount of the element

X contained in the base layer 43 to the amount of selenium contained in the selenium layer can be adjusted in some cases. The base layer 43 can be provided in a desired region.

[0099]

The amorphous selenium layer 45 can be formed by a sputtering method, an evaporation method, a pulsed laser deposition (PLD) method, a plasma-enhanced chemical vapor deposition (PECVD) method, a thermal CVD method, an ALD method, a vacuum evaporation method, or the like. As an example of the thermal CVD method, an MOCVD method can be given.

[0100]

The substrate temperature in the formation of the amorphous selenium layer 45 is preferably a temperature at which the temperature of the layer 41 is higher than or equal to room temperature (20 °C) and lower than 50 °C. If the substrate temperature is in the above range, generation of a film separation region in the amorphous selenium layer 45 can be reduced. Note that the amorphous selenium layer 45 may be partly crystallized.

[0101]

The amorphous selenium layer 45 is preferably formed immediately after the formation of the base layer 43. Further preferably, the amorphous selenium layer 45 is formed after the formation of the base layer 43 without a surface of the base layer 43 being exposed to an air atmosphere. Still further preferably, the base layer 43 and the amorphous selenium layer 45 are successively formed in vacuum. When the base layer 43 and the amorphous selenium layer 45 are successively formed, attachment of impurities such as atmospheric components to the surface of the base layer 43 can be suppressed; therefore, the photoelectric conversion layer 13 including few impurities can be formed. Moreover, generation of a film separation region in the photoelectric conversion layer 13 can be reduced. Furthermore, the photoelectric conversion layer 13 with high crystallinity can be formed.

[0102]

In this specification and the like, the case where a process substrate is not exposed to an air atmosphere between the formation of the base layer and the formation of the amorphous selenium layer but kept under a vacuum atmosphere, a nitrogen atmosphere, or a rare gas atmosphere may be referred to as "successive film formation" or "films are formed in succession." The case where the process substrate is exposed to an air atmosphere after the formation of the base layer and then the amorphous selenium layer is formed may be referred to as "non-successive film formation" or "films are not formed in succession."

[0103]

The amorphous selenium layer can be formed in, for example, a multi-chamber sputtering apparatus equipped with a plurality of film formation chambers and provided with a

plurality of targets, in which various kinds of films are successively formed in vacuum. A multi-chamber evaporation device provided with a plurality of evaporation sources, in which various kinds of films are successively formed in vacuum, can be used. A composite apparatus equipped with a sputtering chamber and an evaporation chamber, in which various kinds of films are successively formed in vacuum, can be used.

[0104]

In the case where the base layer 43 and the amorphous selenium layer 45 are formed by an evaporation method, the substrate illustrated in FIG. 5B is placed upside down. In the case of performing evaporation, a substrate is sandwiched between a substrate holder and an evaporation mask; a permanent magnet provided in the substrate holder attracts the evaporation mask made of metal and fixes the substrate; and evaporation is performed with an evaporation source located below the base layer 43 that is exposed. Note that the pressure during the evaporation is preferably less than or equal to 1.0×10^{-3} Pa, further preferably less than or equal to 1.0×10^{-4} Pa, still further preferably about 1.0×10^{-5} Pa.

[0105]

Then, as Step S403, the photoelectric conversion layer 13 is formed by heat treatment (FIG. 5C).

[0106]

The heat treatment is preferably divided into first to third processes that are sequentially performed at different temperatures. It is preferable that the first process at a first temperature (T1), the second process at a second temperature (T2), and the third process at a third temperature (T3) are performed in this order.

[0107]

The first temperature (T1) is preferably higher than or equal to 50 °C and lower than or equal to 90 °C, further preferably higher than or equal to 60 °C and lower than or equal to 80 °C. The first temperature (T1) is preferably a temperature at which the element *X* contained in the base layer 43 diffuses into the amorphous selenium layer 45 and a selenium compound containing selenium and the element *X* is formed.

[0108]

The second temperature (T2) is preferably higher than the first temperature (T1). In addition, the second temperature (T2) is preferably higher than or equal to 70 °C and lower than or equal to 170 °C, further preferably higher than or equal to 90 °C and lower than or equal to 160 °C, still further preferably higher than or equal to 100 °C and lower than or equal to 150 °C. The second temperature (T2) is preferably a temperature at which solid phase crystallization of

amorphous selenium progresses using the selenium compound formed in the process performed at the first temperature (T1) as a crystal nucleus.

[0109]

The third temperature (T3) is preferably higher than the second temperature (T2). In addition, the third temperature (T3) is preferably higher than or equal to 110 °C and lower than or equal to 220 °C, further preferably higher than or equal to 130 °C and lower than or equal to 220 °C, still further preferably higher than or equal to 150 °C and lower than or equal to 210 °C. The third temperature (T3) is preferably a temperature at which solid phase crystallization of the amorphous selenium progresses.

[0110]

If the heat treatment is divided into the first to third processes performed at different temperatures and the first temperature (T1), the second temperature (T2), and the third temperature (T3) are in the above ranges, uniform crystalline selenium having small surface unevenness can be formed.

[0111]

Schematic views of solid phase crystallization by which the crystalline selenium of one embodiment of the present invention is formed are illustrated in FIGS. 7A to 7D. FIGS. 7A to 7D are cross-sectional views illustrating the formation of a crystalline selenium layer by solid phase crystallization of an amorphous selenium layer.

[0112]

When heat treatment is performed at 70 °C as the first temperature (T1), for example, the element *X* is diffused from the base layer into an amorphous selenium layer 1001, whereby a selenium compound 1003 containing selenium and the element *X* is formed (FIG. 7A).

[0113]

Heat treatment is performed at 110 °C as the second temperature (T2), for example, whereby a crystal grain 1005, which is selenium crystallized by solid phase crystallization using the selenium compound 1003 as a crystal nucleus, is formed (FIG. 7B). Since the second temperature (T2) is relatively low, the growth rate of the crystal grains is low, and the crystal grains 1005 grow at approximately the same growth rate. In the solid phase crystallization, the crystal grain grows until the crystal grain meets adjacent crystal grains. That is, the growth of the crystal grain terminates when the crystal grain meets adjacent crystal grain. In the case where the second temperature (T2) is low and the growth rate of the crystal grains is low, a large number of crystal grains 1005 can grow as illustrated in FIG. 7B before the crystal grains 1005 meet adjacent crystal grains.

[0114]

Then, heat treatment is performed at 200 °C as the third temperature (T3), for example, whereby the crystal grains 1005 further grow (FIG. 7C).

[0115]

As a result of the further growth of the crystal grains, the entire amorphous selenium layer is crystallized, whereby a crystalline selenium layer 1007 is formed (FIG. 7D). As described above, since the large number of crystal grains 1005 grow, the crystal grains 1005 have substantially uniform small crystal grain sizes at the termination of the solid phase crystallization. In addition, since the crystal grain 1005 has a small crystal grain size, the surface unevenness of the crystalline selenium layer 1007 is small; that is, the surface unevenness of a photoelectric conversion layer can be small. Such a structure is preferable because a favorable pn-junction surface can be formed. At the lower second temperature (T2), a larger number of crystal grains 1005 can grow. Accordingly, each crystal grain 1005 has a smaller crystal grain size, which reduces the surface unevenness of the crystalline selenium layer 1007.

[0116]

Since the growth of the crystal grain terminates when the crystal grain meets an adjacent crystal grain, the crystal grain after the entire amorphous selenium layer is crystallized may have a polygonal shape as illustrated in FIG. 7D or a polygonal shape having round corners.

[0117]

For comparison, schematic views of solid phase crystallization in the case where heat treatment at the second temperature (T2) is not performed but heat treatment at the first temperature (T1) and heat treatment at the third temperature (T3) are performed in this order are illustrated in FIGS. 8A to 8C.

[0118]

When heat treatment is performed at 70 °C as the first temperature (T1), for example, the element *X* is diffused from the base layer into the amorphous selenium layer 1001, whereby the selenium compound 1003 containing selenium and the element *X* is formed (FIG. 8A).

[0119]

Heat treatment is performed at 200 °C as the third temperature (T3), for example, whereby the crystal grain 1005, which is selenium crystallized by solid phase crystallization using the selenium compound 1003 as a crystal nucleus, is formed. Here, the third temperature (T3) is relatively high and the growth rate of the crystal grains is sufficiently high, so that some crystal grains 1005a grow faster than the others (FIG. 8B).

[0120]

The entire amorphous selenium layer is crystallized, so that the crystalline selenium layer 1007 is formed (FIG. 8C). As described above, some crystal grains grow faster than the

others; thus, the crystal grain size of such a fast-growing crystal grain increases. Consequently, the surface unevenness of the crystalline selenium layer 1007 increases. The large surface unevenness of the photoelectric conversion layer, which may degrade the interface properties of a pn-junction surface, is not preferable. In the case where heat treatment is not performed at the second temperature (T2), both large crystal grains and small crystal grains may be formed, whereby variation in the sizes of the crystal grains of the crystalline selenium layer 1007 may be increased as illustrated in FIG. 8C.

[0121]

FIG. 9 shows a thermal profile of the heat treatment of one embodiment of the present invention. In FIG. 9, the horizontal axis represents time (Time) and the vertical axis represents temperature (Temperature).

[0122]

A zeroth temperature (T0) is a temperature at the beginning of the heat treatment. The zeroth temperature (T0) is preferably lower than or equal to the first temperature (T1), and higher than or equal to room temperature (20 °C) and lower than or equal to 70 °C. A first period (P1) is a period in which the zeroth temperature (T0) is kept. Note that the first period (P1) may not be provided in the thermal profile.

[0123]

A second period (P2) is a period in which the temperature is increased from the zeroth temperature (T0) to the first temperature (T1). The length of the second period (P2) is not particularly limited.

[0124]

A third period (P3) is a period in which the first temperature (T1) is kept. The length of the third period (P3) can be longer than or equal to 10 seconds and shorter than or equal to 60 minutes.

[0125]

A fourth period (P4) is a period in which the temperature is increased from the first temperature (T1) to the second temperature (T2). The length of the fourth period (P4) is not particularly limited.

[0126]

A fifth period (P5) is a period in which the second temperature (T2) is kept. The length of the fifth period (P5) can be longer than or equal to 10 seconds and shorter than or equal to 60 minutes.

[0127]

A sixth period (P6) is a period in which the temperature is increased from the second temperature (T2) to the third temperature (T3). The length of the sixth period (P6) is not particularly limited.

[0128]

A seventh period (P7) is a period in which the third temperature (T3) is kept. The length of the seventh period (P7) can be longer than or equal to 10 seconds and shorter than or equal to 60 minutes.

[0129]

An eighth period (P8) is a period in which the temperature is decreased from the third temperature (T3). The length of the eighth period (P8) is not particularly limited.

[0130]

A thermal profile in which heat treatment is performed from the first period (P1) to the eighth period (P8) successively is preferably used. A photoelectric conversion element can be manufactured with high productivity by performing the successive heat treatment. Note that the successive heat treatment from P1 to P8 is not necessarily performed.

[0131]

An electric furnace, a laser annealing apparatus, a lamp annealing apparatus, or the like can be used for the heat treatment. An apparatus for heating an object to be processed by heat conduction or heat radiation from a heater such as a resistance heater may be used. Alternatively, a hot plate may be used. In addition, a rapid thermal annealing (RTA) apparatus can be used. Examples of RTA apparatuses include a gas rapid thermal anneal (GRTA) apparatus and a lamp rapid thermal anneal (LRTA) apparatus. A GRTA apparatus is an apparatus for performing heat treatment using a high-temperature gas. As the high-temperature gas, an inert gas which does not react by a heat treatment with an object to be processed, such as nitrogen or a rare gas like argon, is used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp.

[0132]

A rare gas such as argon (Ar), an air atmosphere, nitrogen, oxygen, dry air, or the like can be used as an atmosphere of the heat treatment. Moreover, a mixed atmosphere of a rare gas and oxygen and a mixed atmosphere of a rare gas and nitrogen can be used.

[0133]

After the formation of the photoelectric conversion layer 13, the base layer 43 is not clearly observed in some cases. Although FIG. 5C illustrates an example in which the base

layer 43 is not clearly observed after the formation of the photoelectric conversion layer 13 and the photoelectric conversion layer 13 is formed over the first electrode 11, one embodiment of the present invention is not limited to this example. As illustrated in FIG. 6B, the photoelectric conversion layer 13 may be formed over a base layer 43a which is thinner than the initial base layer 43. The thickness of the base layer 43a may be the same as or larger than that of the initial base layer 43. As illustrated in FIG. 6C, the base layer 43 may be an island-shaped base layer 43b and the photoelectric conversion layer 13 may be formed over the first electrode 11 and the base layer 43b. Boundaries between the photoelectric conversion layer 13 and the base layer 43a and between the photoelectric conversion layer 13 and the base layer 43b are not necessarily clear.

[0134]

The base layers 43a and 43b may each contain selenium in addition to components of the base layer 43.

[0135]

Subsequently, as Step S404, the hole injection blocking layer 17 is formed over the photoelectric conversion layer 13 (FIG. 5D).

[0136]

The hole injection blocking layer 17 can be formed by a sputtering method, an evaporation method, a pulsed laser deposition (PLD) method, a plasma-enhanced chemical vapor deposition (PECVD) method, a thermal CVD method, an ALD method, a vacuum evaporation method, or the like. As an example of the thermal CVD method, an MOCVD method can be given.

[0137]

As illustrated in FIG. 1B, the hole injection blocking layer 17 preferably has a stacked structure of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b over the first hole injection blocking layer 17a. For each of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b, the above-described material can be used.

[0138]

The first hole injection blocking layer 17a and the second hole injection blocking layer 17b can be formed separately in different conditions, for example. For example, the flow rates of oxygen gas in the deposition gases can be different between the first hole injection blocking layer 17a and the second hole injection blocking layer 17b.

[0139]

When the first hole injection blocking layer 17a is formed, plasma discharge is performed in an atmosphere containing an oxygen gas. At this time, oxygen is added to the photoelectric conversion layer 13 over which the first hole injection blocking layer 17a is to be formed, whereby the photoelectric conversion layer might be oxidized. Thus, for the formation conditions of the first hole injection blocking layer 17a, the proportion of oxygen gas flow rate (also referred to as oxygen flow rate ratio or oxygen partial pressure) in a whole deposition gas is preferably low.

[0140]

As the deposition condition of the first hole injection blocking layer 17a, the proportion of oxygen gas flow rate (also referred to as oxygen gas flow rate ratio or oxygen partial pressure) in a whole deposition gas is higher than or equal to 0 % and lower than or equal to 30 %, preferably higher than or equal to 5 % and lower than or equal to 15 %. With the above oxygen flow rate ratio, oxidation of the surface of the photoelectric conversion layer 13 over which the first hole injection blocking layer 17a is to be formed and the vicinity thereof can be suppressed.

[0141]

In the case where the first hole injection blocking layer 17a is formed by a sputtering method, for example, a substrate temperature is increased by collision of sputtered particles in some cases. When the substrate temperature is increased, the selenium contained in the photoelectric conversion layer 13 may be evaporated. The deposition rate of the first hole injection blocking layer 17a can be increased with the above oxygen flow rate ratio. In other words, the time during which the surface of the photoelectric conversion layer 13 is exposed to sputtered particles in the formation of the first hole injection blocking layer 17a can be shortened; thus, evaporation of the selenium can be suppressed.

[0142]

As the deposition condition of the second hole injection blocking layer 17b, the oxygen flow rate ratio is higher than 30 % and lower than or equal to 100 %, preferably higher than or equal to 35 % and lower than or equal to 100 %, further preferably higher than or equal to 40 % and lower than or equal to 70 %. With the above oxygen flow rate ratio, the second hole injection blocking layer 17b having few oxygen vacancies can be formed.

[0143]

In the case where the oxygen flow rate ratio is high, the second hole injection blocking layer 17b having crystallinity may be formed. The second hole injection blocking layer 17b having crystallinity is not preferable because it increases the resistance of the second hole injection blocking layer 17b and decreases a photocurrent in some cases. With the above

oxygen flow rate ratio, the crystallinity of the second hole injection blocking layer 17b can be low and a photoelectric conversion element can have a large photocurrent.

[0144]

The substrate temperature at which the first hole injection blocking layer 17a and the second hole injection blocking layer 17b are formed is preferably higher than or equal to room temperature (20 °C) and lower than or equal to 60 °C, further preferably higher than or equal to room temperature and lower than or equal to 50 °C. If the substrate temperature is in the above range, evaporation of selenium contained in the photoelectric conversion layer 13 over which the hole injection blocking layer 17 is to be formed can be suppressed. In the case where the first hole injection blocking layer 17a and the second hole injection blocking layer 17b are formed with the same substrate temperature, the productivity can be increased.

[0145]

For the formation of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b, Ga_2O_3 containing SnO_2 at greater than or equal to 0.2 mol% and less than or equal to 15 mol% can be used as a sputtering target.

[0146]

Next, as Step S405, the second electrode 15 is formed over the hole injection blocking layer 17 (FIG. 5E). Through the above process, the photoelectric conversion element 10B of one embodiment of the present invention can be manufactured.

[0147]

Another heat treatment may be performed after the second electrode 15 is formed. In this case, the crystallinity of crystalline selenium contained in the photoelectric conversion layer 13 may be further increased. Note that this heat treatment is not necessarily performed.

[0148]

<Method 2 for manufacturing photoelectric conversion element>

Another method for manufacturing the photoelectric conversion element 10B of one embodiment of the present invention will be described with reference to drawings. This method is different from Method 1 for manufacturing photoelectric conversion element described above in Step S402.

[0149]

First, as Step S401, the first electrode 11 is formed over the layer 41 (FIG. 5A). For formation of the first electrode 11, the description in Method 1 for manufacturing photoelectric conversion element described above can be referred to, and thus the detailed description is omitted.

[0150]

Next, as Step S402, the amorphous selenium layer 45 and the base layer 43 over the amorphous selenium layer 45 are formed over the first electrode 11 (FIG. 6D). For formation of the amorphous selenium layer 45 and the base layer 43, the description in Method 1 for manufacturing photoelectric conversion element described above can be referred to, and thus the detailed description is omitted.

[0151]

Then, as Step S403, the photoelectric conversion layer 13 is formed by heat treatment (FIG. 5C). For the heat treatment, the description in Method 1 for manufacturing photoelectric conversion element described above can be referred to, and thus the detailed description is omitted.

[0152]

Subsequently, as Step S404, the hole injection blocking layer 17 is formed over the photoelectric conversion layer 13 (FIG. 5D). For formation of the hole injection blocking layer 17, the description in Method 1 for manufacturing photoelectric conversion element described above can be referred to, and thus the detailed description is omitted.

[0153]

Next, as Step S405, the second electrode 15 is formed over the hole injection blocking layer 17 (FIG. 5E). Through the above process, the photoelectric conversion element 10B of one embodiment of the present invention can be manufactured.

[0154]

Another heat treatment may be performed after the second electrode 15 is formed. In this case, the crystallinity of the crystalline selenium contained in the photoelectric conversion layer 13 may be further increased. Note that this heat treatment is not necessarily performed.

[0155]

(Embodiment 2)

In this embodiment, an example of an imaging device for which one embodiment of the present invention can be used will be described with reference to drawings.

[0156]

FIG. 10A illustrates a pixel circuit of the imaging device. The pixel circuit includes a photoelectric conversion element 50, a transistor 51, a transistor 52, a transistor 53, and a transistor 54.

[0157]

As the photoelectric conversion element 50, any one of the photoelectric conversion elements 10A to 10C described in Embodiment 1 can be used.

[0158]

One electrode (anode) of the photoelectric conversion element 50 is electrically connected to one of a source and a drain of the transistor 51 and one of a source and a drain of the transistor 52. The other of the source and the drain of the transistor 51 is electrically connected to a gate of the transistor 53. One of a source and a drain of the transistor 53 is electrically connected to one of a source and a drain of the transistor 54. Note that a capacitor electrically connected to the gate of the transistor 53 may be provided.

[0159]

The other electrode (cathode) of the photoelectric conversion element 50 is electrically connected to a wiring 72. A gate of the transistor 51 is electrically connected to a wiring 75. The other of the source and the drain of the transistor 53 is electrically connected to a wiring 79. A gate of the transistor 52 is electrically connected to a wiring 76. The other of the source and the drain of the transistor 52 is electrically connected to a wiring 73. The other of the source and the drain of the transistor 54 is electrically connected to a wiring 71. A gate of the transistor 54 is electrically connected to a wiring 78. The wiring 72 is electrically connected to one terminal of a power source 56. The other terminal of the power source 56 is electrically connected to a wiring 77.

[0160]

Here, the wiring 71 can function as an output line that outputs a signal from a pixel. The wiring 73, the wiring 77, and the wiring 79 can function as power supply lines. For example, the wiring 73 and the wiring 77 can function as low potential power supply lines, and the wiring 79 can function as a high potential power supply line. The wiring 75, the wiring 76, and the wiring 78 can function as signal lines that control the on/off states of the transistors.

[0161]

To increase light detection sensitivity under a low illuminance condition, it is preferable to use a photoelectric conversion element that causes avalanche multiplication effect as the photoelectric conversion element 50. To cause avalanche multiplication effect, comparatively high potential HVDD is needed. Thus, the power source 56 is capable of supplying the potential HVDD, and the potential HVDD is supplied to the other electrode of the photoelectric conversion element 50 through the wiring 72. Note that the photoelectric conversion element 50 is available even when a potential that does not cause avalanche multiplication effect is applied thereto.

[0162]

The transistor 51 can have a function of transferring the potential of a charge accumulation portion (NR) that changes in response to output of the photoelectric conversion element 50 to a charge detection portion (ND). The transistor 52 can have a function of

initializing the potentials of the charge accumulation portion (NR) and the charge detection portion (ND). The transistor 53 can have a function of outputting a signal based on the potential of the charge detection portion (ND). The transistor 54 can have a function of selecting a pixel from which a signal is read.

[0163]

In the case where high voltage is applied to the photoelectric conversion element 50, a transistor to be connected to the photoelectric conversion element 50 needs to withstand the high voltage. As the high withstand voltage transistor, for example, an OS transistor can be used. Specifically, OS transistors are preferably used as the transistors 51 and 52.

[0164]

Although the transistors 51 and 52 are desired to have excellent switching characteristics, the transistor 53 is desired to have excellent amplifying characteristics; thus, a transistor with high on-state current is preferably used. Therefore, a transistor including silicon in an active layer or an active region (hereinafter referred to as a Si transistor) is preferably used as each of the transistors 53 and 54.

[0165]

When the transistors 51 to 54 have the above structures, it is possible to manufacture an imaging device that has high light detection sensitivity under a low illuminance condition and can output a signal with little noise. Since the imaging device has high light detection sensitivity, light capturing time can be shortened and imaging can be performed at high speed.

[0166]

The structure is not limited to the structure described above, and the transistors 53 and 54 may be OS transistors. Alternatively, the transistors 51 and 52 may be Si transistors. In either case, the pixel circuit can perform imaging.

[0167]

Next, operation of the pixel is described with reference to a timing chart in FIG. 10B. Note that in the following description of an operation example, HVDD and GND are supplied to the wiring 76 connected to the gate of the transistor 52 as an "H" potential and an "L" potential, respectively. In addition, VDD and GND are supplied to the wiring 75 connected to the gate of the transistor 51 and the wiring 78 connected to the gate of the transistor 54 as an "H" potential and an "L" potential, respectively. Furthermore, a potential VDD is supplied to the wiring 79 connected to the source of the transistor 53. Other potentials also can be supplied to the wirings.

[0168]

At Time T1, the wiring 76 is set at "H" and the wiring 75 is set at "H," and the potentials of the charge accumulation portion (NR) and the charge detection portion (ND) are each set to a reset potential (GND) (that is, reset operation). Note that in reset operation, the potential VDD may be supplied to the wiring 76 as an "H" potential.

[0169]

At Time T2, the wiring 76 is set at "L" and the wiring 75 is set at "L," whereby the potential of the charge accumulation portion (NR) changes (that is, accumulation operation). The potential of the charge accumulation portion (NR) is changed from GND to HVDD at the maximum depending on the intensity of light that enters the photoelectric conversion element 50.

[0170]

At Time T3, the wiring 75 is set at "H," and charge in the charge accumulation portion (NR) is transferred to the charge detection portion (ND) (that is, transfer operation).

[0171]

At Time T4, the wiring 76 is set at "L" and the wiring 75 is set at "L," whereby the transfer operation terminates. At this time, the potential of the charge detection portion (ND) is determined.

[0172]

In a period from Time T5 to Time T6, the wiring 76 is set at "L," the wiring 75 is set at "L," and the wiring 78 is set at "H," and a signal based on the potential of the charge detection portion (ND) is output to the wiring 71. In other words, an output signal based on the intensity of light that enters the photoelectric conversion element 50 in the accumulation operation can be obtained.

[0173]

FIG. 11A illustrates a structure example of a pixel of an imaging device including the above-described pixel circuit. The imaging device includes a layer 61, a layer 62, and a layer 63, which partly overlap with each other.

[0174]

The layer 61 has the same structure as that of the photoelectric conversion element 50. The photoelectric conversion element 50 includes an electrode 65 corresponding to a pixel electrode, a photoelectric conversion portion 66, and an electrode 67 corresponding to a common electrode.

[0175]

A low-resistance metal layer or the like is preferably used for the electrode 65. For example, aluminum, titanium, tungsten, tantalum, silver, or a stacked layer thereof can be used.

[0176]

A conductive layer having a high light-transmitting property with respect to visible light is preferably used for the electrode 67. For example, indium oxide, tin oxide, zinc oxide, indium tin oxide, gallium zinc oxide, indium gallium zinc oxide, graphene, or the like can be used. Note that the electrode 67 can be omitted.

[0177]

For example, a pn-junction photodiode including a selenium-based material in a photoelectric conversion layer can be used for the photoelectric conversion portion 66. The selenium-based material described in Embodiment 1 is preferably used for a photoelectric conversion layer 66a, and the material with a wide band gap described in Embodiment 1 is preferably used for a hole injection blocking layer 66b.

[0178]

A photoelectric conversion element including a selenium-based material has high external quantum efficiency with respect to visible light. Such a photoelectric conversion element can be a sensor in which the amount of amplification of electrons with respect to the amount of incident light is large because of avalanche multiplication effect, that is, a sensor with high photosensitivity. A selenium-based material has a high light-absorption coefficient, and thus enables, for example, formation of a thin photoelectric conversion layer; accordingly, the use of a selenium-based material has advantages in production. A thin film of a selenium-based material can be formed using a vacuum evaporation method, a sputtering method, or the like.

[0179]

As a selenium-based material, crystalline selenium such as single crystal selenium or polycrystalline selenium, amorphous selenium, a compound of copper, indium, and selenium (CIS), a compound of copper, indium, gallium, and selenium (CIGS), or the like can be used.

[0180]

An n-type semiconductor is preferably formed using a material with a wide band gap and a light-transmitting property with respect to visible light. For example, zinc oxide, gallium oxide, indium oxide, tin oxide, or mixed oxide thereof can be used. In addition, these materials also have a function as a hole injection blocking layer, so that a dark current can be decreased.

[0181]

The structure of the layer 61 is not limited to the above structure, and the layer 61 may be a pn-junction photodiode using silicon or a pin-junction photodiode using silicon.

[0182]

The layer 62 can include, for example, OS transistors (the transistors 51 and 52). In the circuit structure of the pixel illustrated in FIG. 10A, a decrease in the intensity of light entering the photoelectric conversion element 50 reduces the potential of the charge detection

portion (ND). Since the OS transistor has extremely low off-state current, current based on a gate potential can be accurately output even when the gate potential is extremely low. Thus, it is possible to widen the detection range of illuminance, i.e., the dynamic range.

[0183]

A period during which charge can be held in the charge detection portion (ND) and the charge accumulation portion (NR) can be extremely long owing to the low off-state current of the transistors 51 and 52. Therefore, a global shutter system in which accumulation operation is performed in all the pixels at the same time can be used without a complicated circuit structure and operation method.

[0184]

The layer 63 can be a support substrate or a layer including Si transistors (the transistors 53 and 54). The Si transistor can include an active region in a single-crystal silicon substrate or include a crystalline silicon active layer over an insulating surface. In the case where the layer 63 contains a single-crystal silicon substrate, a pn-junction photodiode using silicon or a pin-junction diode using silicon may be formed in the single-crystal silicon substrate. In this case, the layer 61 can be omitted.

[0185]

FIG. 11B is a block diagram illustrating a circuit configuration of an imaging device of one embodiment of the present invention. The imaging device includes a pixel array 81 including pixels 80 arranged in a matrix, a circuit 82 (row driver) having a function of selecting a row of the pixel array 81, a circuit 83 (CDS circuit) for performing correlated double sampling on an output signal of the pixel 80, a circuit 84 (A/D converter circuit or the like) having a function of converting analog data output from the circuit 83 to digital data, and a circuit 85 (column driver) having a function of selecting and reading data converted in the circuit 84. Note that a structure without the circuit 83 can be employed.

[0186]

For example, components of the pixel array 81 except the photoelectric conversion element can be provided in the layer 62 illustrated in FIG. 11A. The circuits 82 to 85 can be provided in the layer 63. Those circuits can be formed of CMOS circuits using silicon transistors.

[0187]

With this structure, transistors suitable for respective circuits can be used, and an area of the imaging device can be made small.

[0188]

FIGS. 12A to 12C illustrate a specific structure of the imaging device illustrated in FIG. 11A. FIG. 12A is a cross-sectional view in the channel length direction of the transistors 51, 52, 53, and 54. FIG. 12B is a cross-sectional view in the channel width direction of the transistor 52 taken along dashed-dotted line A1-A2 in FIG. 12A. FIG. 12C is a cross-sectional view in the channel width direction of the transistor 53 taken along dashed-dotted line B1-B2 in FIG. 12A.

[0189]

The layer 61 can include a partition wall 92 in addition to the photoelectric conversion element 50 including a selenium layer. The partition wall 92 is provided so as to cover a step of the electrode 65. The selenium layer used for the photoelectric conversion element 50 has high resistance and the selenium layer is not divided between pixels.

[0190]

The transistors 51 and 52, which are OS transistors, are provided in the layer 62. Although both the transistors 51 and 52 include back gates 91, either of the transistors may include the back gate. As illustrated in FIG. 12B, the back gate 91 might be electrically connected to a front gate of the transistor, which is provided to face the back gate. Alternatively, different fixed potentials may be supplied to the back gate 91 and the front gate.

[0191]

Although FIG. 12A illustrates an example in which an OS transistor is a top-gate transistor having a self-aligned structure, a transistor having a non-self-aligned structure may be used as illustrated in FIG. 13A.

[0192]

The transistors 53 and 54, which are Si transistors, are provided in the layer 63. Although FIG. 12A illustrates an example in which the Si transistor is a fin transistor including a semiconductor layer in a silicon substrate 200, a planar transistor including an active region in a silicon substrate 201 may be used as illustrated in FIG. 13B. Alternatively, as illustrated in FIG. 13C, transistors each including a semiconductor layer 210 of a silicon thin film may be used. The semiconductor layer 210 can be SOI (silicon on insulator); specifically, the semiconductor layer 210 can be single crystal silicon formed over an insulating layer 220 over a silicon substrate 202, for example. Alternatively, the semiconductor layer 210 may be polycrystalline silicon formed over an insulating surface of a glass substrate or the like. In addition, a circuit for driving a pixel can be provided in the layer 63.

[0193]

An insulating layer 93 that has a function of inhibiting diffusion of hydrogen is provided between a region including OS transistors and a region including Si transistors. Dangling

bonds of silicon are terminated with hydrogen in insulating layers provided in the vicinities of the active regions of the transistors 53 and 54. Meanwhile, hydrogen in insulating layers which are provided in the vicinity of the oxide semiconductor layer that is the active layer of the transistors 51 and 52 causes generation of carriers in the oxide semiconductor layer.

[0194]

Hydrogen is confined in the one layer by the insulating layer 93, so that the reliability of the transistors 53 and 54 can be improved. Furthermore, diffusion of hydrogen from the one layer to the other layer is inhibited, so that the reliability of the transistors 51 and 52 can also be improved.

[0195]

The insulating layer 93 can be, for example, formed using aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, hafnium oxynitride, or yttria-stabilized zirconia (YSZ).

[0196]

FIG. 14A is a cross-sectional view illustrating an example in which a color filter and the like are added to the imaging device of one embodiment of the present invention. The cross-sectional view illustrates part of a region including pixel circuits for three pixels. An insulating layer 300 is formed over the layer 61 where the photoelectric conversion element 50 is formed. As the insulating layer 300, for example, a silicon oxide film with a high visible-light transmitting property can be used. In addition, a silicon nitride film may be stacked as a passivation film. Furthermore, a dielectric film of hafnium oxide or the like may be stacked as an anti-reflection film.

[0197]

A light-blocking layer 310 may be formed over the insulating layer 300. The light-blocking layer 310 has a function of inhibiting color mixing of light passing through the upper color filter. The light-blocking layer 310 can be formed using a metal layer of aluminum, tungsten, or the like, or a stack including the metal layer and a dielectric film functioning as an anti-reflection film.

[0198]

An organic resin layer 320 can be formed as a planarization film over the insulating layer 300 and the light-blocking layer 310. A color filter 330 (a color filter 330a, a color filter 330b, or a color filter 330c) is formed in each pixel. For example, the color filter 330a, the color filter 330b, and the color filter 330c each have a color of red (R), green (G), blue (B), yellow (Y), cyan (C), magenta (M), or the like, so that a color image can be obtained.

[0199]

For example, an insulating layer 360 having a light-transmitting property with respect to visible light can be provided over the color filter 330.

[0200]

As illustrated in FIG. 14B, an optical conversion layer 350 may be used instead of the color filter 330. Such a structure enables the imaging device to capture images in various wavelength regions.

[0201]

For example, when a filter that blocks light having a wavelength shorter than or equal to that of visible light is used as the optical conversion layer 350, an infrared imaging device can be obtained. When a filter that blocks light having a wavelength shorter than or equal to that of near infrared light is used as the optical conversion layer 350, a far infrared imaging device can be obtained. When a filter that blocks light having a wavelength longer than or equal to that of visible light is used as the optical conversion layer 350, an ultraviolet imaging device can be obtained.

[0202]

Furthermore, when a scintillator is used as the optical conversion layer 350, an imaging device that captures an image visualizing the intensity of radiation and is used for an X-ray imaging device, for example, can be obtained. Radiation such as X-rays passes through an object to enter a scintillator, and then is converted into light (fluorescence) such as visible light or ultraviolet light owing to a photoluminescence phenomenon. Then, the photoelectric conversion element 50 detects the light to obtain image data. Furthermore, the imaging device having the structure may be used in a radiation detector or the like.

[0203]

A scintillator contains a substance that, when irradiated with radiation such as X-rays or gamma-rays, absorbs energy of the radiation to emit visible light or ultraviolet light. For example, a resin or ceramics in which any of Gd_2O_2S:Tb, Gd_2O_2S:Pr, Gd_2O_2S:Eu, BaFCl:Eu, NaI, CsI, CaF_2, BaF_2, CeF_3, LiF, LiI, and ZnO is dispersed can be used.

[0204]

In the photoelectric conversion element 50 including a selenium-based material, radiation such as X-rays can be directly converted into charge; thus, the scintillator is not necessarily used.

[0205]

As illustrated in FIG. 14C, a microlens array 340 may be provided over the color filters 330a, 330b, and 330c. Light penetrating lenses included in the microlens array 340 goes through the color filters positioned thereunder to reach the photoelectric conversion element 50.

The microlens array 340 may be provided over the optical conversion layer 350 illustrated in FIG. 14B.

[0206]

Hereinafter, examples of a package and a camera module each including an image sensor chip are described. For the image sensor chip, the structure of the above imaging device can be used.

[0207]

FIG. 15A1 is an external perspective view showing the top surface side of a package including an image sensor chip. The package includes a package substrate 410 to which an image sensor chip 450 is fixed, a cover glass 420, an adhesive 430 for bonding the package substrate 410 and the cover glass 420 to each other, and the like.

[0208]

FIG. 15A2 is an external perspective view showing the bottom surface side of the package. On the bottom surface of the package, a ball grid array (BGA) including solder balls as bumps 440 is formed. Although the BGA is employed here, a land grid array (LGA), a pin grid array (PGA), or the like may be alternatively employed.

[0209]

FIG. 15A3 is a perspective view of the package, in which the cover glass 420 and the adhesive 430 are partly illustrated. Electrode pads 460 are formed over the package substrate 410, and electrically connected to the bumps 440 through through-holes. The electrode pads 460 are electrically connected to the image sensor chip 450 through wires 470.

[0210]

FIG. 15B1 is an external perspective view showing the top surface side of a camera module in which an image sensor chip is mounted on a package with a built-in lens. The camera module includes a package substrate 411 to which an image sensor chip 451 is fixed, a lens cover 421, a lens 435, and the like. Furthermore, an IC chip 490 having functions of a driver circuit, a signal conversion circuit, and the like of an imaging device is provided between the package substrate 411 and the image sensor chip 451. Thus, a system in package (SiP) is formed.

[0211]

FIG. 15B2 is an external perspective view showing the bottom surface side of the camera module. On the bottom surface and side surfaces of the package substrate 411, mounting lands 441 are provided; this structure can be called a quad flat no-lead package (QFN). Although QFN is employed here, a quad flat package (QFP), the above BGA, or the like may be alternatively employed.

[0212]

FIG. 15B3 is a perspective view of the module, in which the lens cover 421 and the lens 435 are partly illustrated. The lands 441 are electrically connected to electrode pads 461. The electrode pads 461 are electrically connected to the image sensor chip 451 or the IC chip 490 through wires 471.

[0213]

The image sensor chip placed in the package having the above structure can be easily mounted on a printed circuit board or the like and incorporated into a variety of semiconductor devices and electronic devices.

[0214]

This embodiment can be combined with any of the other embodiments as appropriate.

[0215]

(Embodiment 3)

Examples of an electronic device that can use the imaging device of one embodiment of the present invention include display devices, personal computers, image memory devices or image reproducing devices provided with storage media, mobile phones, game machines (including portable game machines), portable data terminals, e-book readers, cameras such as video cameras and digital still cameras, goggle-type displays (head mounted displays), navigation systems, audio reproducing devices (e.g., car audio players and digital audio players), copiers, facsimiles, printers, multifunction printers, automated teller machines (ATM), and vending machines. FIGS. 16A to 16F illustrate specific examples of these electronic devices.

[0216]

FIG. 16A illustrates a monitoring camera, which includes a housing 951, a lens 952, a support portion 953, and the like. The imaging device of one embodiment of the present invention can be included as a component for obtaining an image in the monitoring camera. Note that a "monitoring camera" is a common name and does not limit the uses. For example, a device that has a function of a monitoring camera can also be called a camera or a video camera.

[0217]

FIG. 16B illustrates a video camera, which includes a first housing 971, a second housing 972, a display portion 973, operation keys 974, a lens 975, a joint 976, and the like. The operation keys 974 and the lens 975 are provided for the first housing 971, and the display portion 973 is provided for the second housing 972. The imaging device of one embodiment of the present invention can be included as a component for obtaining an image in the video camera.

[0218]

FIG. 16C illustrates a digital camera, which includes a housing 961, a shutter button 962, a microphone 963, a light-emitting portion 967, a lens 965, and the like. The imaging device of one embodiment of the present invention can be included as a component for obtaining an image in the digital camera.

[0219]

FIG. 16D illustrates a wrist-watch-type information terminal, which includes a housing 931, a display portion 932, a wristband 933, operation buttons 935, a winder 936, a camera 939, and the like. The display portion 932 may be a touch panel. The imaging device of one embodiment of the present invention can be included as a component for obtaining an image in the information terminal.

[0220]

FIG. 16E shows an example of a mobile phone which includes a housing 981, a display portion 982, an operation button 983, an external connection port 984, a speaker 985, a microphone 986, a camera 987, and the like. The mobile phone includes a touch sensor in the display portion 982. Operations such as making a call and inputting a character can be performed by touch on the display portion 982 with a finger, a stylus, or the like. The imaging device of one embodiment of the present invention can be included as one component for obtaining an image in the mobile phone.

[0221]

FIG. 16F illustrates a portable data terminal, which includes a housing 911, a display portion 912, a camera 919, and the like. A touch panel function of the display portion 912 enables input and output of information. The imaging device of one embodiment of the present invention can be included as one component for obtaining an image in the portable data terminal.

[0222]

This embodiment can be combined with any of the other embodiments in this specification as appropriate.

[Example 1]

[0223]

In this example, crystalline selenium of one embodiment of the present invention was fabricated and the crystal grain size of a crystal grain and unevenness of a crystal selenium layer were evaluated.

[0224]

Samples were six in total: Samples A1 to A6 of one embodiment of the present invention. Samples A1 to A6 were different from each other in conditions of heat treatment after formation of an amorphous selenium layer.

[0225]

<Fabrication method of Samples A1 to A6>

The structure and the fabrication method of each sample will be described with reference to FIGS. 17A and 17B. FIGS. 17A and 17B are cross-sectional views illustrating the fabrication method of the sample.

[0226]

First, a base layer 1063 and an amorphous selenium layer 1067 over the base layer 1063 were formed over a substrate 1061 (see FIG. 17A).

[0227]

As the substrate 1061 of each of Samples A1 to A6, a p-type silicon wafer with a plane orientation (100) was used.

[0228]

For each of Samples A1 to A6, a 2-nm-thick silver film was formed as the base layer 1063, and then the 700-nm-thick amorphous selenium layer 1067 was formed. The base layer 1063 and the amorphous selenium layer 1067 were formed successively in vacuum.

[0229]

The base layer 1063 of each of Samples A1 to A6 was formed in an evaporation chamber of an evaporation/sputtering composite apparatus (VD15-065, manufactured by Shinko Seiki Co., Ltd.). The base layer was formed using silver as an evaporation source and resistive heating (a Ta board) at an evaporation rate of 0.05 nm/sec. The substrate temperature during the evaporation was room temperature. The pressure during the evaporation was about 1.5×10^{-5} Pa.

[0230]

The amorphous selenium layer 1067 of each of Samples A1 to A6 was formed in an evaporation chamber of an evaporation/sputtering composite apparatus (VD15-065, manufactured by Shinko Seiki Co., Ltd.). The amorphous selenium layer 1067 was formed using selenium as an evaporation source and resistive heating (a Ta board) at an evaporation rate of 0.20 nm/sec. The substrate temperature during the evaporation was room temperature. The pressure during the evaporation was about 1.5×10^{-5} Pa.

[0231]

Next, heat treatment was performed to form a crystalline selenium layer 1065 (see FIG. 17B).

[0232]

The heat treatment on Sample A1 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, and then raised to 110 °C and kept for 1 minute.

[0233]

The heat treatment on Sample A2 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 110 °C and kept for 1 minute, and then raised to 200 °C and kept for 1 minute.

[0234]

The heat treatment on Sample A3 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, and then raised to 150 °C and kept for 1 minute.

[0235]

The heat treatment on Sample A4 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 150 °C and kept for 1 minute, and then raised to 200 °C and kept for 1 minute.

[0236]

The heat treatment on Sample A5 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, and then raised to 200 °C and kept for 1 minute.

[0237]

The heat treatment on Sample A6 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 110 °C and kept for 1 minute, raised to 150 °C and kept for 1 minute, and then raised to 200 °C and kept for 1 minute.

[0238]

The heat treatment on Samples A1 to A6 was performed in a draft chamber using a hot plate (EC-1200N, manufactured by AS ONE Corporation) in an air atmosphere.

[0239]

Through the above process, Samples A1 to A6 were fabricated.

[0240]

<SEM observation>

Next, SEM observations of Samples A1 to A6 were performed to evaluate the presence or absence of a film separation region in the selenium layer. The SEM observation was performed at an acceleration voltage of 1.0 kV using a scanning electron microscope (SU8030, manufactured by Hitachi High-Technologies Corporation).

[0241]

FIGS. 18A and 18B are plane SEM images of Sample A1, FIGS. 19A and 19B are those of Sample A2, FIGS. 20A and 20B are those of Sample A3, FIGS. 21A and 21B are those of Sample A4, FIGS. 22A and 22B are those of Sample A5, and FIGS. 23A and 23B are those of Sample A6. FIG. 18A, FIG. 19A, FIG. 20A, FIG. 21A, FIG. 22A, and FIG. 23A are SEM images at a magnification of 10000 times. FIG. 18B, FIG. 19B, FIG. 20B, FIG. 21B, FIG. 22B, and FIG. 23B are SEM images at a magnification of 30000 times.

[0242]

As shown in FIGS. 18A and 18B, FIGS. 19A and 19B, FIGS. 20A and 20B, FIGS. 21A and 21B, FIGS. 22A and 22B, and FIGS. 23A and 23B, no film separation region was observed in Samples A1 to A6 of one embodiment of the present invention. It was found that Samples A1 to A6 containing crystalline selenium having few film separation regions can be fabricated by using silver for the base layer 1063 and performing heat treatment after the formation of the amorphous selenium layer 1067 over the base layer 1063. In addition, the crystal grain of each sample had a substantially polygonal shape.

[0243]

The crystalline selenium layers of Samples A1 and A3, which were not subjected to the heat treatment at 200 °C, had large surface unevenness. Among the crystalline selenium layers of Samples A2, A4, A5, and A6, which were subjected to the heat treatment at 200 °C, the crystalline selenium layer of Sample A5 had the largest surface unevenness.

[0244]

The crystal grain sizes of the crystal grains of Samples A2, A4, A5, and A6, which were subjected to the heat treatment at 200 °C, were calculated. In this example, the crystal grain sizes (major diameters) were calculated. The crystal grain sizes (major diameters) were calculated using SEM images at a magnification of 30000 times shown in FIG. 19B, FIG. 21B, FIG. 22B, and FIG. 23B.

[0245]

FIG. 24A shows portions where the crystal grain sizes (major diameters) of Sample A2 were measured. FIG. 24A shows the same image as the SEM image at a magnification of 30000 times shown in FIG. 18B, and crystal grain sizes (major diameters) of the portions denoted by arrows were measured.

[0246]

As illustrated in each of FIGS. 24B to 24D, the length of the longest line connecting two points on an outline of a crystal grain 1009 was calculated as a crystal grain size 1011. When the crystal grain 1009 has a polygonal shape as illustrated in FIG. 24D, the length of the longest diagonal line is measured as the crystal grain size 1011. Note that in the case of a triangular crystal grain, the length of the longest side of a triangle was regarded as the crystal grain size.

[0247]

Table 1 shows the number *n* of measured crystal grains and the calculated maximum, minimum, average, and median values of the crystal grain sizes (major diameters) of the crystal grains of Samples A2, A4, A5, and A6.

[0248]

[Table 1]

	number of measurement points	crystal grain size (diameter) [μm]			
	n [number]	maximum value	minimum value	average value	median value
Sample A2	169	0.73	0.09	0.34	0.33
Sample A4	112	0.89	0.09	0.37	0.37
Sample A5	125	1.20	0.10	0.35	0.32
Sample A6	158	0.71	0.14	0.36	0.35

[0249]

FIG. 25A, FIG. 25B, FIG. 26A, and FIG. 26B show a histogram of the crystal grain sizes (major diameters) of the crystal grains of Sample A2, that of Sample A4, that of Sample A5, and that of Sample A6, respectively. In each of FIG. 25A, FIG. 25B, FIG. 26A, and FIG. 26B, the horizontal axis represents a crystal grain size (major diameter) [μm]. A bar labeled "0.1 μm" represents the number of crystal grains having a crystal grain size (major diameter) of greater than or equal to 0.00 μm and less than or equal to 0.10 μm, and a bar labeled "0.2 μm" represents the number of crystal grains having a crystal grain size (major diameter) of greater than 0.10 μm and less than or equal to 0.20 μm. The left vertical axis represents a frequency of the crystal grains [number], and the right vertical axis represents a cumulative relative frequency of the crystal grains [%].

[0250]

In Samples A2, A4, and A6, a crystal grain having a crystal grain size (major diameter) of greater than 1.0 μm was not observed and the maximum value of the crystal grain size (major diameter) was less than or equal to 1.10 μm. On the contrary, in Sample A5, a plurality of crystal grains having a crystal grain size (major diameter) of greater than 1.0 μm were observed

and the maximum value of the crystal grain size (major diameter) was 1.20 μm. The crystal grain size (major diameter) of Sample A5 was larger than that of the crystal grain of each of Samples A2, A4, and A6.

[0251]

Crystal grains with large crystal grain sizes (major diameters) were observed in Sample A5; on the other hand, Sample A5 also contained many small-sized crystal grains as compared to Samples A2, A4, and A6. That is, variation in the crystal grain sizes of the crystal grains was large in Sample A5.

[0252]

The crystal grain size (major diameter) of Sample A4 was larger than that of each of Samples A2 and A6. Note that there was no particular difference in the minimum value of the crystal grain size (major diameter) between the samples.

[0253]

There was a correlation between the degree of the surface unevenness of the crystalline selenium layer and the crystal grain size (major diameter). The sample having the crystalline selenium layer having large surface unevenness tended to have a crystal grain having a large crystal grain size (major diameter), and the sample having the crystalline selenium layer having small surface unevenness tended to have a small crystal grain size (major diameter). That is, when the second temperature (T2) was approximately 110 °C with the first temperature (T1) being 70 °C and the third temperature (T3) being 200 °C, the crystal grain size (major diameter) was less than or equal to 1.10 μm. Accordingly, the surface unevenness of the crystalline selenium layer was decreased. The low second temperature T2 may have contributed to growth of many crystal grains in solid phase crystallization and reduction in size of crystal grains, which may have been responsible for a decrease in unevenness of the crystal selenium layer.

[Example 2]

[0254]

In this example, the photoelectric conversion element of one embodiment of the present invention was fabricated and the current-voltage characteristics thereof were evaluated.

[0255]

Samples were five in total: Samples B1 to B5 of one embodiment of the present invention. Samples B1 to B5 were different from each other in conditions of heat treatment after formation of an amorphous selenium layer.

[0256]

<Fabrication method of Samples B1 to B5>

The structure and the fabrication method of each sample will be described using reference numerals used for the photoelectric conversion element 10B illustrated in FIGS. 5A to 5E.

[0257]

First, the first electrode 11 was formed over the layer 41 (see FIG. 5A). For the first electrode 11, a 50-nm-thick first titanium film, a 200-nm-thick aluminum film, and a 50-nm-thick second titanium film were formed in this order with a sputtering apparatus.

[0258]

As the layer 41 of each of Samples B1 to B5, a glass substrate (AN100, manufactured by Asahi Glass Co., Ltd.) was used.

[0259]

The first titanium film was formed by a sputtering method using a titanium target. Argon was used as a deposition gas and the pressure in deposition was adjusted to 0.1 Pa. The deposition power was set to 12 kW with use of a DC power source. The substrate temperature in deposition was room temperature.

[0260]

The aluminum film was formed by a sputtering method using an aluminum target. Argon was used as a deposition gas and the pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 1 kW with use of a DC power source. The substrate temperature in deposition was room temperature.

[0261]

The second titanium film was formed by a sputtering method using a titanium target. Argon was used as a deposition gas and the pressure in deposition was adjusted to 0.1 Pa. The deposition power was set to 12 kW with use of a DC power source. The substrate temperature in deposition was room temperature.

[0262]

Next, the base layer 43 and the amorphous selenium layer 45 were formed in this order (see FIG. 5B).

[0263]

For each of Samples B1 to B5, a 2-nm-thick silver film was formed as the base layer 43, and then the 500-nm-thick amorphous selenium layer 45 was formed. The base layer 43 and the selenium layer 45 were formed successively in vacuum.

[0264]

The description in Example 1 can be referred to for the description of a method for forming the base layer 43 and the amorphous selenium layer 45; thus, the detailed description is omitted.

[0265]

Subsequently, heat treatment was performed, so that the photoelectric conversion layer 13 was formed (see FIG. 5C).

[0266]

The heat treatment on Sample B1 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, and then raised to 200 °C and kept for 1 minute.

[0267]

The heat treatment on Sample B2 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 90 °C and kept for 2 minute, and then raised to 200 °C and kept for 1 minute.

[0268]

The heat treatment on Sample B3 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 110 °C and kept for 1 minute, and then raised to 200 °C and kept for 1 minute.

[0269]

The heat treatment on Sample B4 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 120 °C and kept for 1 minute, and then raised to 200 °C and kept for 1 minute.

[0270]

The heat treatment on Sample B5 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 150 °C and kept for 1 minute, and then raised to 200 °C and kept for 1 minute.

[0271]

The heat treatments on Samples B1 to B5 were performed in a draft chamber using the hot plate (EC-1200N, manufactured by AS ONE Corporation) in an air atmosphere.

[0272]

Next, the first hole injection blocking layer 17a and the second hole injection blocking layer 17b were formed in this order with a sputtering apparatus (see FIG. 5D). A 5-nm-thick first tin-containing gallium oxide film and a 10-nm-thick second tin-containing gallium oxide film were formed for the first hole injection blocking layer 17a and the second hole injection blocking layer 17b, respectively.

[0273]

The first tin-containing gallium oxide film was formed by a sputtering method using tin-containing gallium oxide (Ga_2O_3:SnO_2 = 95:5 [molar ratio]) as a sputtering target. Argon at a flow rate of 45 sccm and oxygen at a flow rate of 5 sccm (an oxygen flow rate ratio of 10 %) were used as deposition gases and the pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source. The substrate temperature in deposition was room temperature.

[0274]

The second tin-containing gallium oxide film was formed by a sputtering method using tin-containing gallium oxide (Ga_2O_3:SnO_2 = 95:5 [molar ratio]) as a sputtering target. Argon at a flow rate of 25 sccm and oxygen at a flow rate of 25 sccm (an oxygen flow rate ratio of 50 %) were used as deposition gases and the pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source. The substrate temperature in deposition was room temperature.

[0275]

The first tin-containing gallium oxide film and the second tin-containing gallium oxide film were formed successively in vacuum.

[0276]

Subsequently, the second electrode 15 was formed. For the second electrode 15, a 110-nm-thick ITSO film was formed with a sputtering apparatus (see FIG. 5E).

[0277]

The ITSO film was formed by a sputtering method using a target with a composition of In_2O_3:SnO_2:SiO_2 = 85:10:5 [weight ratio] as a sputtering target. Argon at a flow rate of 50 sccm and oxygen at a flow rate of 2 sccm were used as deposition gases and the pressure in deposition was adjusted to 0.32 Pa. The deposition power was set to 200 W with use of a DC power source. The substrate temperature in deposition was room temperature.

[0278]

Through the above-described steps, Samples B1 to B5 were fabricated.

[0279]

<Current-voltage characteristics>

Next, the current-voltage characteristics of Samples B1 to B5 were measured. FIG. 27A, FIG. 27B, FIG. 28A, FIG. 28B, and FIG. 29 show the current-voltage characteristics of Sample B1, those of Sample B2, those of Sample B3, those of Sample B4, and those of Sample B5, respectively. In each of FIG. 27A, FIG. 27B, FIG. 28A, FIG. 28B, and FIG. 29, the horizontal axis represents voltage (Voltage) [V] between electrodes facing each other, and the vertical axis represents a current value (Current) [A].

[0280]

In each of FIG. 27A, FIG. 27B, FIG. 28A, FIG. 28B, and FIG. 29, a dark current (I_{dark}) is shown by a solid line, and a photocurrent (I_{photo}) measured while the sample was irradiated with light with a wavelength of 450 nm and an intensity of 20 $\mu W/cm^2$ is shown by a dashed line. The size of a light-receiving surface of each sample was 2mm × 2mm.

[0281]

As shown in FIGS. 27A and 27B, FIGS. 28A and 28B, and FIG. 29, Samples B1 and B5 each tended to have a high dark current. The surface unevenness of the photoelectric conversion layer of each of Samples B1 and B5 are supposed to have been larger than that of Samples B2 to B4 (see Example 1). Such large unevenness might have degraded interface properties between the photoelectric conversion layer and the hole injection blocking layer, leading to an increase in a dark current. Sample B3 tended to have a higher photocurrent than Samples B1, B2, B4, and B5.

[0282]

FIG. 30 shows the wavelength dependence of current amplification factors of Samples B1 to B5. In FIG. 30, the horizontal axis represents the irradiation light wavelength λ [nm], and the vertical axis represents the current amplification factor (I_{photo}/I_{dark}). A photocurrent used for calculation of the current amplification factor was measured while the sample was irradiated with light with an intensity of 20 $\mu W/cm^2$ and a voltage of −15 V (reverse bias: V_R) was applied between electrodes of the sample. A dark current used for calculation of the current amplification factor was measured while a voltage of −15 V (reverse bias: V_R) was applied between the electrodes of the sample.

[0283]

As shown in FIG. 30, Sample B3 tended to have a large current amplification factor. As described in Example 1, the heat treatment condition used for Sample B3 was a condition under which the crystalline selenium with a small crystal grain size (major diameter) contained in the photoelectric conversion layer 13 and the photoelectric conversion layer 13 with small unevenness are obtained. The small surface unevenness of the photoelectric conversion layer 13 probably improved the interface properties between the photoelectric conversion layer and the

hole injection blocking layer, so that a photoelectric conversion element having a high current amplification factor was obtained.

[0284]

<TEM observation>

Next, Sample B3 was thinned by a focused ion beam (FIB), and a cross section of Sample B3 was observed with a STEM. The FIB processing was performed at an acceleration voltage of 30 kV using gallium (Ga) as an irradiation ion with an FIB-SEM double beam apparatus (XVision210DB, manufactured by SII Nano Technology Inc.). The STEM observation was performed at an acceleration voltage of 200 kV using a scanning transmission electron microscope (HD-2700, manufactured by Hitachi High-Technologies Corporation).

[0285]

FIGS. 31A and 31B are STEM images of a cross section of Sample B3. FIG. 31A is a transmission electron image (TE image) at a magnification of 100000 times. FIG. 31B is a Z contrast image (ZC image) of the same portion as FIG. 31A at a magnification of 100000 times. A substance having a larger atomic number is seen brighter in a Z contrast image. As shown in FIGS. 31A and 31B, the concentration (luminance) inside the selenium layer in the STEM images is substantially uniform; thus, the film quality of the inside of the selenium layer of Sample B3 was substantially uniform. In addition, the surface unevenness of the selenium layer was small, so that the ITSO film, which was the second electrode, was formed with good coverage.

[0286]

The thickness of the selenium layer was measured using the cross-sectional STEM image shown in FIG. 31A. FIG. 32 shows a point A and a point B, which were measured portions. The point A and the point B were respectively the thinnest portion and the thickest portion of the selenium layer shown in the cross-sectional STEM image shown in FIG. 32. Note that FIG. 31A and FIG. 32 show the same STEM image. According to the results of the measurements, the thickness of the point A was 592 nm and the thickness of the point B was 661 nm. The height difference between the projection and the depression (the highest portion and the lowest portion) of the selenium layer was approximately 70 nm.

[0287]

Moreover, many crystal grains each having a crystal grain size (major diameter) of approximately 0.3 μm were observed in FIG. 31A.

[0288]

FIGS. 33A and 33B and FIGS. 34A and 34B are transmission electron images (TE images) at a magnification of 3000000 times. FIG. 33A is a cross-sectional STEM image

showing the selenium layer in the vicinity of the second electrode. FIG. 33B is a cross-sectional STEM image showing the selenium layer around the center in the thickness direction. FIG. 34A is a cross-sectional STEM image showing a first electrode side of the point B. FIG. 34B is a cross-sectional STEM image showing the selenium layer in the vicinity of the first electrode. Sample B3 contained crystalline selenium because crystal lattice patterns were observed.

[Example 3]

[0289]

In this example, a photoelectric conversion element was fabricated and the current-voltage characteristics thereof were evaluated.

[0290]

Samples C1, C2, and B3 will be described in this example. Sample B3 in this example is the same as that in Example 2. Samples C1, C2, and B3 were different from each other in the structures of a photoelectric conversion layer and a hole injection blocking layer.

[0291]

Crystalline selenium and indium gallium oxide were respectively used for the photoelectric conversion layer 13 and the hole injection blocking layer 17 of Sample C1.

[0292]

A stacked structure in which a 60-nm-thick crystalline selenium layer and a 440-nm-thick amorphous selenium layer are stacked in this order was used for the photoelectric conversion layer 13 of Sample C2, and indium gallium oxide was used for the hole injection blocking layer 17 of Sample C2.

[0293]

As described in Example 2, crystal selenium was used for the photoelectric conversion layer 13 of Sample B3 and tin-containing gallium oxide was used for the hole injection blocking layer 17 of Sample B3.

[0294]

<Fabrication method of Sample C1>

The structure and the fabrication method of Sample C1 will be described using reference numerals used for the photoelectric conversion element 10B illustrated in FIGS. 5A to 5E.

[0295]

First, the first electrode 11 was formed over the layer 41 (see FIG. 5A). As the layer 41, the glass substrate (AN100, manufactured by Asahi Glass Co., Ltd.) was used. For the first electrode 11, a 50-nm-thick first titanium film, a 200-nm-thick aluminum film, and a

50-nm-thick second titanium film were formed in this order with a sputtering apparatus. The description in Example 2 can be referred to for the description of the first electrode 11; thus, the detailed description is omitted.

[0296]

Next, the base layer 43 and the amorphous selenium layer 45 were formed in this order (see FIG. 5B). First, a 2-nm-thick silver film was formed as the base layer 43, and then the 500-nm-thick amorphous selenium layer 45 was formed. The description in Example 1 can be referred to for the description of the base layer 43 and the amorphous selenium layer 45; thus, the detailed description is omitted.

[0297]

Subsequently, heat treatment was performed, so that the photoelectric conversion layer 13 was formed (see FIG. 5C). The heat treatment on Sample C1 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 110 °C and kept for 1 minute, and then raised to 200 °C and kept for 1 minute. The heat treatment was performed in a draft chamber using the hot plate (EC-1200N, manufactured by As One Corporation) in an air atmosphere.

[0298]

Next, the hole injection blocking layer 17 was formed with a sputtering apparatus (see FIG. 5D). A 10-nm-thick indium gallium oxide film was formed as the hole injection blocking layer 17 of Sample C1.

[0299]

The indium gallium oxide film was formed by a sputtering method using indium gallium oxide (In:Ga = 5:95 [atomic ratio]) as a sputtering target. Argon at a flow rate of 45 sccm and oxygen at a flow rate of 5 sccm were used as deposition gases and the pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source. The substrate temperature in deposition was room temperature.

[0300]

Subsequently, the second electrode 15 was formed. For the second electrode 15, a 110-nm-thick ITSO film was formed with a sputtering apparatus (see FIG. 5E). The description in Example 2 can be referred to for the description of the second electrode 15; thus, the detailed description is omitted.

[0301]

Through the above process, Sample C1 was fabricated.

[0302]

<Fabrication method of Sample C2>

The structure and the fabrication method of Sample C2 will be described. Sample C2 is different from Sample C1 described above in the structure of the photoelectric conversion layer 13. The other steps were the same as the steps for Sample C1.

[0303]

For Sample C2, a 10-nm-thick first amorphous selenium layer, a 2-nm-thick silver film, and a 50-nm-thick second amorphous selenium layer were formed in this order. The description in Example 1 can be referred to for the description of the silver film and the amorphous selenium layer; thus, the detailed description is omitted.

[0304]

Next, heat treatment was performed, so that the first and second amorphous selenium layers were crystallized. The heat treatment on Sample C2 was started at room temperature. The treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, and then raised to 110 °C and kept for 10 seconds. The heat treatment was performed in a draft chamber using the hot plate (EC-1200N, manufactured by As One Corporation) in an air atmosphere.

[0305]

Subsequently, a 440-nm-thick third amorphous selenium layer was formed. The description in Example 2 can be referred to for the description of the amorphous selenium layer; thus, the detailed description is omitted.

[0306]

Through the above process, Sample C2 was fabricated.

[0307]

<Current-voltage characteristics>

Next, the current-voltage characteristics of Samples C1 and C2 were measured. FIGS. 35A and 35B show the current-voltage characteristics of Sample C1 and those of Sample C2, respectively. In each of FIGS. 35A and 35B, the horizontal axis represents voltage (Voltage) [V] between electrodes facing each other, and the vertical axis represents a current value (Current) [A].

[0308]

In each of FIGS. 35A and 35B, a dark current (I_{dark}) is shown by a solid line, and a photocurrent (I_{photo}) measured while the sample was irradiated with light with a wavelength of 450 nm and an intensity of 20 $\mu W/cm^2$ is shown by a dashed line. The size of a light-receiving surface of each sample was 2mm × 2mm.

[0309]

Samples B3 and C1 each contained crystalline selenium in the photoelectric conversion layer. Sample B3 in which tin-containing gallium oxide was used for the hole injection blocking layer had a higher photocurrent than Sample C1 in which indium gallium oxide was used for the hole injection blocking layer when voltage applied between electrodes was −10 V to −20 V. Sample B3 had a high photocurrent probably because the width of a depletion layer was increased by tin-containing gallium oxide with high carrier density that was used for the hole injection blocking layer.

[0310]

Sample C2 tended to have a lower dark current than Samples B3 and C1. Samples B3 and C1 each contained crystalline selenium in the photoelectric conversion layer. The photoelectric conversion layer of Sample C2 had a stacked structure of crystalline selenium and amorphous selenium over the crystalline selenium. Sample C2 had a low dark current probably because the surface unevenness of the photoelectric conversion layer of Sample C2 smaller than that of Samples B3 and C1 improves the interface properties between the photoelectric conversion layer and the hole injection blocking layer.

[0311]

FIG. 36 shows wavelength dependence of current amplification factors of Samples C1, C2, and B3. In FIG. 36, the horizontal axis represents the irradiation light wavelength λ [nm], and the vertical axis represents a current amplification factor (I_{photo}/I_{dark}). A photocurrent used for calculation of the current amplification factor was measured while the sample was irradiated with light with an intensity of 20 μW/cm^2 and a voltage of −15 V (reverse bias: V_R) was applied between electrodes of the sample. A dark current used for calculation of the current amplification factor was measured while a voltage of −15 V (reverse bias: V_R) was applied between the electrodes of the sample.

[0312]

Sample B3 had a higher current amplification factor than Samples C1 and C2 in the entire wavelength region of greater than or equal to 400 nm and less than or equal to 700 nm. That is, Sample B3 had a large current amplification factor in almost the entire visible light region.

[0313]

<Measurement temperature dependence of current-voltage characteristics>

Then, measurement temperature dependence of the current-voltage characteristics of Samples B3 and C2 was evaluated. Sample B3 was a photoelectric conversion element containing crystalline selenium in the photoelectric conversion layer. Sample C2 was a

photoelectric conversion element whose photoelectric conversion layer had a stacked structure of crystalline selenium and amorphous selenium over the crystalline selenium.

[0314]

The measurement of the current-voltage characteristics of Sample B3 was performed as follows: first measurement was performed at a substrate temperature of room temperature (20 °C); second measurement was performed at an increased substrate temperature of 40 °C; third measurement was performed at an increased substrate temperature of 60 °C; fourth measurement was performed at an increased substrate temperature of 80 °C; fifth measurement was performed at an increased substrate temperature of 100 °C; sixth measurement was performed at an increased substrate temperature of 120 °C; seventh measurement was performed at a decreased substrate temperature of 100 °C; eighth measurement was performed at a decreased substrate temperature of 80 °C; ninth measurement was performed at a decreased substrate temperature of 60 °C; tenth measurement was performed at a decreased substrate temperature of 40 °C; and eleventh measurement was performed at a decreased substrate temperature of room temperature (20 °C). Note that current-voltage characteristics were measured after the set temperature was kept for 5 minutes in any measurement.

[0315]

FIG. 37A shows the measurement temperature dependence of the current-voltage characteristics of Sample B3. In FIG. 37A, the horizontal axis represents substrate temperature in the measurement (Temperature) [°C], and the vertical axis represents a dark current I_{dark} [A]. In FIG. 37A, dark currents I_{dark} of the first to sixth measurement are represented as triangles, and dark currents I_{dark} of the seventh to eleventh measurement are represented as white circles.

[0316]

As shown in FIG. 37A, the dark currents of Sample B3 of the first measurement and the eleventh measurement, which were performed at room temperature (20 °C), were almost the same. Therefore, Sample B3 including the crystalline selenium layer in the photoelectric conversion layer was a thermally stable photoelectric conversion element having a small change in current-voltage characteristics even in a high-temperature environment.

[0317]

The measurement of the current-voltage characteristics of Sample C2 was performed as follows: first measurement was performed at a substrate temperature of room temperature (20 °C); second measurement was performed at an increased substrate temperature of 80 °C; third measurement was performed at an increased substrate temperature of 120 °C; fourth measurement was performed at a decreased substrate temperature of 80 °C; and fifth

measurement was performed at a decreased substrate temperature of room temperature (20 °C). Note that current-voltage characteristics were measured after the set temperature was kept for 5 minutes in any measurement.

[0318]

FIG. 37B shows the measurement temperature dependence of the current-voltage characteristics of Sample C2. In FIG. 37B, the horizontal axis represents substrate temperature in the measurement (Temperature) [°C], and the vertical axis represents a dark current [A]. In FIG. 37B, dark currents of the first to third measurement are represented as triangles, and dark currents of the fourth and fifth measurements are represented as white circles.

[0319]

As shown in FIG. 37B, the value of the dark current of Sample C2 in the fifth measurement performed at room temperature (20 °C) was about one digit higher than that of the first measurement performed at room temperature (20 °C). Since Sample C2 included the amorphous selenium layer in the photoelectric conversion layer, the amorphous selenium layer was probably partly or entirely crystallized in the measurement at a high temperature (e.g., 120 °C), so that the dark current increased in the fifth measurement performed at room temperature (20 °C). Therefore, Sample C2 including the amorphous selenium layer in the photoelectric conversion layer was a photoelectric conversion element that was less thermally stable than Sample B3 because the current-voltage characteristics of Sample C2 were changed in a high-temperature environment.

[Example 4]

[0320]

In this example, an energy difference between the Fermi level (E_f) and the valence band (E_v) of each of crystalline selenium and amorphous selenium was evaluated.

[0321]

Samples D1 and D2 will be described in this example. A 500-nm-thick crystalline selenium layer and a 500-nm-thick amorphous selenium layer were formed over glass substrates for Samples D1 and D2, respectively.

[0322]

<Fabrication method of Sample D1>

For Sample D1, a 2-nm-thick silver film was formed as a base layer over a substrate, and then the 500-nm-thick amorphous selenium layer was formed. The base layer and the amorphous selenium layer were formed successively in vacuum.

[0323]

As the substrate, the glass substrate (AN100, manufactured by Asahi Glass Co., Ltd.) was used. The description in Example 1 can be referred to for the description of the base layer and the amorphous selenium layer; thus, the detailed description is omitted.

[0324]

Subsequently, heat treatment was performed, so that a crystalline selenium layer was formed. The heat treatment was performed during a period in which the temperature was raised from room temperature to 70 °C and kept for 3 minutes, raised to 110 °C and kept for 1 minute, and then raised to 200 °C and kept for 1 minute. The heat treatment was performed in a draft chamber using the hot plate (EC-1200N, manufactured by As One Corporation) in an air atmosphere.

[0325]

Through the above process, Sample D1 was fabricated.

[0326]

<Fabrication method of Sample D2>

For Sample D2, the 500-nm-thick amorphous selenium layer was formed over the glass substrate.

[0327]

As a substrate, the glass substrate (AN100, manufactured by Asahi Glass Co., Ltd.) was used. The description in Example 1 can be referred to for the description of the amorphous selenium layer; thus, the detailed description is omitted.

[0328]

Through the above process, Sample D2 was fabricated.

[0329]

<X-ray photoelectron spectroscopy measurement>

Samples D1 and D2 were measured by X-ray photoelectron spectroscopy (XPS).

[0330]

For the XPS measurement, Quantera SXM manufactured by PHI, Inc. was used. Monochromatic Al Kα ray (1486.6 eV) was used for an X-ray source. A detection area was set to 100 μmϕ. An extraction angle was set to 45°. Thus, the detection depth might be approximately 4 to 5 nm.

[0331]

FIGS. 38A and 38B show an XPS spectrum around the Fermi level of Sample D1 and that of Sample D2, respectively. In each of FIGS. 38A and 38B, the horizontal axis represents the binding energy (Binding Energy) [eV], and the vertical axis represents the intensity of photoelectron (Intensity) [arbitrary unit (arb. u)]. In each of FIGS. 38A and 38B, measurement

values are shown by a solid line, and an approximate line obtained by linear approximation using a least-square method in a range of 0.4 eV to 0.9 eV is shown by a dashed-dotted line.

[0332]

As shown in FIG. 38A, the energy difference between the Fermi level and the valence band (E_f–E_v) of Sample D1, which contained crystalline selenium, was estimated to be approximately 0.1 eV from the extrapolated approximate line. As shown in FIG. 38B, the energy difference between the Fermi level and the valence band (E_f–E_v) of Sample D2 containing amorphous selenium was estimated to be approximately 0.2 eV from the extrapolated approximate line.

[0333]

The energy difference between the Fermi level and the valence band (E_f–E_v) of crystalline selenium is smaller than that of amorphous selenium, so that the crystalline selenium presumably has high carrier density.

[0334]

As described above, crystal selenium has high carrier density; thus, in the case where crystal selenium is used for a photoelectric conversion layer, a photocurrent can be increased by (e.g., tin-containing gallium oxide) having increased carrier density using an n-type semiconductor for a hole injection blocking layer.

[Example 5]

[0335]

In this example, the compositions and the like of tin-containing gallium oxide and indium gallium oxide were evaluated.

[0336]

Samples E1 to E4 will be described in this example. For Sample E1, a 30-nm-thick tin-containing gallium oxide film was formed over a silicon wafer. For each of Samples E2 and E3, a 100-nm-thick tin-containing gallium oxide film was formed over a glass substrate. For Sample E4, a 100-nm-thick indium gallium oxide (IGO) film was formed over a glass substrate. The deposition conditions of the tin-containing gallium oxide films of Samples E1 and E2 were the same. The deposition conditions of the tin-containing gallium oxide films of Samples E2 and E3 were different.

[0337]

<Fabrication method of Samples E1 to E4>

As the silicon wafer of Sample E1, a p-type silicon wafer with a plane orientation (100) was used. As the glass substrate of each of Samples E2 to E4, the glass substrate (AN100, manufactured by Asahi Glass Co., Ltd.) was used.

[0338]

For each of Samples E1 and E2, a tin-containing gallium oxide target (Ga_2O_3:SnO_2 = 95:5 [molar ratio]) was used and an argon gas at a flow rate of 45 sccm and oxygen at a flow rate of 5 sccm (an oxygen flow rate ratio of 10 %) were used as deposition gases. The substrate temperature in deposition was room temperature. The pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source.

[0339]

For Sample E3, a tin-containing gallium oxide target (Ga_2O_3:SnO_2 = 95:5 [molar ratio]) was used and an argon gas at a flow rate of 25 sccm and oxygen at a flow rate of 25 sccm (an oxygen flow rate ratio of 50 %) were used as deposition gases. The substrate temperature in deposition was room temperature. The pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source.

[0340]

For Sample E4, an indium gallium oxide target (In:Ga = 5:95 [atomic ratio]) was used and an argon gas at a flow rate of 45 sccm and oxygen at a flow rate of 5 sccm were used as deposition gases. The substrate temperature in deposition was room temperature. The pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source.

[0341]

Through the above process, Samples E1 to E4 were fabricated.

[0342]

<X-ray photoelectron spectroscopy measurement>

Sample E1 was measured by X-ray photoelectron spectroscopy (XPS).

[0343]

For the XPS measurement, Quantera SXM manufactured by PHI, Inc. was used. Monochromatic Al Kα ray (1486.6 eV) was used for an X-ray source. A detection area was set to 100 μmϕ. An extraction angle was set to 45°. Thus, the detection depth might be approximately 4 to 5 nm.

[0344]

First, the XPS measurement was performed in a wide energy range of 0 eV to 1350 eV (hereinafter referred to as wide scanning). FIG. 39 shows a spectrum obtained by the wide scanning. In FIG. 39, the horizontal axis represents the binding energy (Binding Energy) [eV], and the vertical axis represents the intensity of photoelectron (Intensity) [arbitrary unit (arb. u)]. As shown in FIG. 39, peaks derived from Ga, O, Sn, and C were observed in Sample E1.

[0345]

Next, the XPS measurement was performed in an energy range where each of the peaks of Ga, O, Sn, and C is obtained (hereinafter referred to as narrow scanning). FIG. 40A, FIG. 40B, FIG. 40C, and FIG. 40D respectively show the spectrum of Ga3d, that of O1s, that of $Sn3d_{5/2}$, and that of C1s, which were obtained by the narrow scanning. In each of FIG. 40A, FIG. 40B, FIG. 40C, and FIG. 40D, the horizontal axis represents the binding energy (Binding Energy) [eV], and the vertical axis represents the intensity of photoelectron (Intensity) [arbitrary unit (arb. u)].

[0346]

As shown in FIGS. 40A to 40C, Ga and Sn of tin-containing gallium oxide of Sample E1 were in an oxidation state.

[0347]

Table 2 shows quantitative values of the elements obtained from the XPS spectra. Note that the quantitative accuracy is about ±1 atomic%. Although the lower limit of detection is about 1 atomic%, it is different from the elements. As shown in Table 2, the Sn concentration was 0.5 atomic% (lower than 1 atomic%); however, since a peak derived from tin oxide was observed slightly but clearly as shown in FIG. 40C, the value can be considered to be significant.

[0348]

[Table 2]

	atomic concentration [atomic%]			
	Ga	O	Sn	C
Sample E1	31.4	47.7	0.5	20.4

[0349]

Note that C was present mainly in a state of C-C, C-H, and the like, and it may be derived from organic contamination on the surface of the sample. Table 3 shows quantitative values of the elements shown in Table 2 except C. As shown in Table 3, Sample E1 contained Ga at 39.4 atomic%, O at 59.9 atomic%, and Sn at 0.6 atomic%. The ratio of the atomic concentration of tin to the atomic concentration of gallium (Sn/Ga) was 0.016. Note that in Table 3, since the value of each element is rounded off to one decimal place, the total is not 100 %.

[0350]

[Table 3]

	atomic concentration [atomic%]			atomic concentration ratio
	Ga	O	Sn	Sn/Ga
Sample E1	39.4	59.9	0.6	0.016

[0351]

The sputtering target used for the formation of the tin-containing gallium oxide in Sample E1 had a composition of Ga_2O_3:SnO_2 = 95:5 [molar ratio] (Ga:O:Sn = 38.8:60.2:1.0 [atomic ratio]). The tin-containing gallium oxide film formed by a sputtering method had a lower content of Sn than the sputtering target.

[0352]

<X-ray photoelectron spectroscopy measurement>

Sample E1 was measured by ultraviolet photoelectron spectroscopy (UPS).

[0353]

For the UPS measurement, VersaProbe manufactured by PHI, Inc. was used. For an ultraviolet light source, He I ray (21.22 eV) was used. A detection region was set to less than or equal to 8 mm square. An extraction angle was set to 90°. The bias voltage was set to −10 V. Before the measurement, the surface of the sample was cleaned by a sputtering with use of argon ions.

[0354]

FIG. 41 shows a UPS spectrum. In FIG. 41, the horizontal axis represents the binding energy (Binding Energy) [eV], and the vertical axis represents the intensity of photoelectron (Intensity) [arbitrary unit (arb. u)].

[0355]

As shown in FIG. 41, kinetic energy of an electron emitted from the Fermi level (E_{Fermi}) and zero kinetic energy of the electron (E_{cutoff}) were calculated to be approximately −5.0 eV and approximately 7.6 eV, respectively. Accordingly, an ionization potential of Sample E1 was estimated to be approximately 8.6 eV. Note that E_{Fermi} was calculated without including a tail of the spectrum. Specifically, E_{Fermi} was calculated from an intersection of the background and a straight line, extrapolated from the spectrum in the vicinity of the top of the valence band.

[0356]

<Band gap>

Then, transmittance and reflectance of Samples E2 to E4 were measured, and a band gap (Eg) thereof was calculated. FIG. 42A, FIG. 42B, and FIG. 42C show the transmittance and reflectance of Sample E2, those of Sample E3, and those of Sample E4, respectively. In each of FIG. 42A, FIG. 42B, and FIG. 42C, the horizontal axis represents a wavelength of light

(Wavelength) [nm], and the vertical axis represents transmittance (Transmittance) [%] and reflectance (Reflectance) [%]. The transmittance is shown by a solid line, and the reflectance is shown by a dashed-dotted line.

[0357]

Samples E2 to E4 each had high transmittance at the wavelengths of 300 nm to 1200 nm.

[0358]

FIG. 43A, FIG. 43B, and FIG. 43C respectively show Tauc plots of Sample E2, those of Sample E3, and those of Sample E4 calculated from the transmittance and reflectance. In each of FIG. 43A, FIG. 43B, and FIG. 43C, the horizontal axis represents energy hν (Energy) [eV], and the vertical axis represents $(\alpha h\nu)^2$. Here, α represents an absorption coefficient, h represents a Planck constant, and ν represents the number of vibrations. The Tauc plot is assumed to be the band structure of an indirect transition semiconductor.

[0359]

In each of FIG. 43A, FIG. 43B, and FIG. 43C, $(\alpha h\nu)^2$ calculated from the transmittance and reflectance is shown by a dashed line, and an approximate line obtained by linear approximation using a least-square method in a range of 4.8 eV to 5.1 eV is shown by a dashed line. As shown in FIGS. 43A to 43C, the band gap (Eg) of each of Samples E2 to E4 was estimated to be approximately 4.6 eV from the extrapolated approximate line.

[Example 6]

[0360]

In this example, photoelectric conversion element was fabricated and the current-voltage characteristics thereof were evaluated.

[0361]

Samples F1 to F4 and B3 will be described in this example. Sample B3 in this example is the same as that in Example 2. Samples F1 to F4 and B3 each contained crystalline selenium in a photoelectric conversion layer and were different from each other in the structure of the hole injection blocking layer 17.

[0362]

A 15-nm-thick Sn-GaOx film formed at 10 % of the oxygen flow rate was used for the hole injection blocking layer 17 of Sample F1.

[0363]

A 15-nm-thick Sn-GaOx film formed at 50 % of the oxygen flow rate was used for the hole injection blocking layer 17 of Sample F2.

[0364]

The hole injection blocking layer 17 of Sample F3 had a stacked structure of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b over the first hole injection blocking layer 17a. A 5-nm-thick tin-containing gallium oxide film formed at 10 % of the oxygen flow rate and a 5-nm-thick tin-containing gallium oxide film formed at 50 % of the oxygen flow rate were used for the first hole injection blocking layer 17a and the second hole injection blocking layer 17b, respectively.

[0365]

The hole injection blocking layer 17 of Sample F4 had a stacked structure of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b over the first hole injection blocking layer 17a. A 10-nm-thick tin-containing gallium oxide film formed at 10 % of the oxygen flow rate and a 20-nm-thick tin-containing gallium oxide film formed at 50 % of the oxygen flow rate were used for the first hole injection blocking layer 17a and the second hole injection blocking layer 17b, respectively.

[0366]

The hole injection blocking layer 17 of Sample B3 had a stacked structure of the first hole injection blocking layer 17a and the second hole injection blocking layer 17b over the first hole injection blocking layer 17a. A 5-nm-thick tin-containing gallium oxide film formed at 10 % of the oxygen flow rate and a 10-nm-thick tin-containing gallium oxide film formed at 50 % of the oxygen flow rate were used for the first hole injection blocking layer 17a and the second hole injection blocking layer 17b, respectively.

[0367]

<Fabrication method of Samples F1 to F4>

The structure and the fabrication method of each of Samples F1 to F4 will be described. Samples F1 to F4 are different from Sample B3 described above in the structure of the hole injection blocking layer 17. The other steps were the same as the steps for Sample B3.

[0368]

A tin-containing gallium oxide film was used for the hole injection blocking layer 17 of Sample F1. The tin-containing gallium oxide film was formed by a sputtering method using tin-containing gallium oxide (Ga_2O_3:SnO_2 = 95:5 [molar ratio]) as a sputtering target. Argon at a flow rate of 45 sccm and oxygen at a flow rate of 5 sccm (an oxygen flow rate ratio of 10 %) were used as deposition gases and the pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source. The substrate temperature in deposition was room temperature.

[0369]

A tin-containing gallium oxide film was used for the hole injection blocking layer 17 of Sample F2. The tin-containing gallium oxide film was formed by a sputtering method using tin-containing gallium oxide (Ga_2O_3:SnO_2 = 95:5 [molar ratio]) as a sputtering target. Argon at a flow rate of 25 sccm and oxygen at a flow rate of 25 sccm (an oxygen flow rate ratio of 50 %) were used as deposition gases and the pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source. The substrate temperature in deposition was room temperature.

[0370]

For each of Samples F3 and F4, the first hole injection blocking layer 17a and the second hole injection blocking layer 17b were sequentially formed with a sputtering apparatus.

[0371]

The first tin-containing gallium oxide film was formed by a sputtering method using tin-containing gallium oxide (Ga_2O_3:SnO_2 = 95:5 [molar ratio]) as a sputtering target. Argon at a flow rate of 45 sccm and oxygen at a flow rate of 5 sccm (an oxygen flow rate ratio of 10 %) were used as deposition gases and the pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source. The substrate temperature in deposition was room temperature.

[0372]

The second tin-containing gallium oxide film was formed by a sputtering method using tin-containing gallium oxide (Ga_2O_3:SnO_2 = 95:5 [molar ratio]) as a sputtering target. Argon at a flow rate of 25 sccm and oxygen at a flow rate of 25 sccm (an oxygen flow rate ratio of 50 %) were used as deposition gases and the pressure in deposition was adjusted to 0.4 Pa. The deposition power was set to 400 W with use of an RF power source. The substrate temperature in deposition was room temperature.

[0373]

Through the above process, Samples F1 to F4 were fabricated.

[0374]

<Current-voltage characteristics>

Next, the current-voltage characteristics of Samples F1 to F4 were measured. FIG. 44A, FIG. 44B, FIG. 45A, and FIG. 45B show the current-voltage characteristics of Sample F1, those of Sample F2, those of Sample F3, and those of Sample F4, respectively. In each of FIG. 44A, FIG. 44B, FIG. 45A, and FIG. 45B, the horizontal axis represents voltage (Voltage) [V] between electrodes facing each other, and the vertical axis represents a current value (Current) [A].

[0375]

In each of FIG. 44A, FIG. 44B, FIG. 45A, and FIG. 45B, a dark current (I_{dark}) is shown by a solid line, and a photocurrent (I_{photo}) with a wavelength of 450 nm and irradiance of 20 $\mu W/cm^2$ is shown by a dashed line. The size of a light-receiving surface of each sample was 2mm × 2mm.

[0376]

As shown in FIGS. 44A and 44B and FIGS. 45A and 45B, as the thickness of the hole injection blocking layer decreased, the dark current tended to become higher; in contrast, as the thickness of the hole injection blocking layer increased, the photocurrent tended to become lower. The total thickness of the hole injection blocking layer was preferably about 15 nm.

[0377]

Sample F1 tended to have a higher dark current than Samples B3 and F2. The dark current was increased probably because the hole injection blocking layer of Sample F1 was formed with tin-containing gallium oxide at 10 % of the oxygen flow rate and thus included many oxygen vacancies. In addition, Sample F2 tended to have a lower photocurrent than Samples B3 and F1. The photocurrent was decreased probably because the hole injection blocking layer of Sample F2 was formed with tin-containing gallium oxide at 50 % of the oxygen flow rate and thus the surface of the photoelectric conversion layer and the vicinity thereof were oxidized, for example, in the formation of the hole injection blocking layer. In contrast, the hole injection blocking layer of Sample B3 had a stacked structure of tin-containing gallium oxide formed at 10 % of the oxygen flow rate and tin-containing gallium oxide formed at 50 % of the oxygen flow rate; therefore, both a low dark current and a high photocurrent were achieved.

[0378]

FIG. 46 shows the wavelength dependence of current amplification factors of Samples F1 to F4 and B3. In FIG. 46, the horizontal axis represents the irradiation light wavelength λ [nm], and the vertical axis represents the current amplification factor (I_{photo}/I_{dark}). A photocurrent used for calculation of the current amplification factor was measured while the sample was irradiated with light with an intensity of 20 $\mu W/cm^2$ and a voltage of −15 V (reverse bias: V_R) was applied between electrodes of the sample. A dark current used for calculation of the current amplification factor was measured while a voltage of −15 V (reverse bias: V_R) was applied between the electrodes of the sample.

[0379]

Sample B3 had a higher current amplification factor than Samples F1 to F4 in the entire wavelength region of greater than or equal to 400 nm and less than or equal to 700 nm. That is, Sample B3 had a large current amplification factor in almost the entire visible light region.

[Example 7]

[0380]

In this example, photoelectric conversion element was fabricated and the current-voltage characteristics thereof were evaluated.

[0381]

Samples G1 to G3 and B3 will be described in this example. Sample B3 in this example is the same as that in Example 2. Samples G1 to G3 and B3 were different from each other in the thickness of a photoelectric conversion layer. The other steps were the same as the steps for Sample B3.

[0382]

A 300-nm-thick crystalline selenium layer, a 750-nm-thick crystalline selenium layer, a 1000-nm-thick crystalline selenium layer, and a 500-nm-thick crystalline selenium layer were used for the photoelectric conversion layers 13 of Samples G1, G2, G3, and B3, respectively.

[0383]

<Fabrication method of Samples G1 to G3>

For Sample G1, a 2-nm-thick silver film was formed as the base layer 43, and then the 300-nm-thick amorphous selenium layer 45 was formed. The base layer 43 and the selenium layer 45 were formed successively in vacuum. The description in Example 1 can be referred to for the description of a method for forming the base layer 43 and the amorphous selenium layer 45; thus, the detailed description is omitted.

[0384]

For Sample G2, a 2-nm-thick silver film was formed as the base layer 43, and then the 750-nm-thick amorphous selenium layer 45 was formed. The base layer 43 and the selenium layer 45 were formed successively in vacuum. The description in Example 1 can be referred to for the description of a method for forming the base layer 43 and the amorphous selenium layer 45; thus, the detailed description is omitted.

[0385]

For Sample G3, a 2-nm-thick silver film was formed as the base layer 43, and then the 1000-nm-thick amorphous selenium layer 45 was formed. The base layer 43 and the selenium layer 45 were formed successively in vacuum. The description in Example 1 can be referred to for the description of a method for forming the base layer 43 and the amorphous selenium layer 45; thus, the detailed description is omitted.

[0386]

Through the above process, Samples G1 to G3 were fabricated.

[0387]

<Current-electric field strength characteristics>

Next, the current-voltage characteristics of Samples G1 to G3 and B3 were measured. FIG. 47A, FIG. 47B, FIG. 48A, and FIG. 48B show the current-electric field strength characteristics of Sample G1, those of Sample G2, those of Sample G3, and those of Sample B3, respectively. In each of FIG. 47A, FIG. 47B, FIG. 48A, and FIG. 48B, the horizontal axis represents electric field strength [MV/cm], and the vertical axis represents a current value (Current) [A]. Since the photoelectric conversion layers of Samples G1 to G3 and B3 had different thicknesses, the value of the voltage between electrodes facing each other divided by the value of the thickness of the photoelectric conversion layer (electric field strength) is shown in each of FIG. 47A, FIG. 47B, FIG. 48A, and FIG. 48B.

[0388]

In each of FIG. 47A, FIG. 47B, FIG. 48A, and FIG. 48B, a dark current (I_{dark}) is shown by a solid line, and a photocurrent (I_{photo}) measured while the sample was irradiated with light with a wavelength of 450 nm and an intensity of 20 $\mu W/cm^2$ is shown by a dashed line. The size of a light-receiving surface of each sample was 2mm × 2mm.

[0389]

As shown in FIGS. 47A and 47B and FIGS. 48A and 48B, as the thickness of the photoelectric conversion layer increased, a photocurrent tended to increase.

[0390]

FIG. 49 shows the wavelength dependence of current amplification factors of Samples G1 to G3 and B3. In FIG. 49, the horizontal axis represents the irradiation light wavelength λ [nm], and the vertical axis represents the current amplification factor (I_{photo}/I_{dark}). A photocurrent used for calculation of the current amplification factor was measured while the sample was irradiated with light with an intensity of 20 $\mu W/cm^2$ and a voltage of −15 V (reverse bias: V_R) was applied between electrodes of the sample. A dark current used for calculation of the current amplification factor was measured while a voltage of −15 V (reverse bias: V_R) was applied between the electrodes of the sample.

[0391]

As shown in FIG. 49, as the thickness of the photoelectric conversion layer increased, the current amplification factor tended to increase.

[0392]

The thickness of a photoelectric conversion layer may be determined in accordance with the use application. In the case where an imaging device including the photoelectric conversion element is intended to perform imaging utilizing avalanche multiplication effect at lower voltage, for example, the photoelectric conversion layer may be relatively thin. In the case where imaging with higher photosensitivity is intended to be performed regardless of voltage, for example, the photoelectric conversion layer may be relatively thick.

REFERENCE NUMERALS

[0393]

10A: photoelectric conversion element, 10B: photoelectric conversion element, 10C: photoelectric conversion element, 11: first electrode, 13: photoelectric conversion layer, 15: second electrode, 17: hole injection blocking layer, 17a: hole injection blocking layer, 17b: hole injection blocking layer, 19: electron injection blocking layer, 41: layer, 43: base layer, 43a: base layer, 43b: base layer, 45: amorphous selenium layer, 50: photoelectric conversion element, 51: transistor, 52: transistor, 53: transistor, 54: transistor, 56: power source, 61: layer, 62: layer, 63: layer, 65: electrode, 66: photoelectric conversion portion, 66a: photoelectric conversion layer, 66b: hole injection blocking layer, 67: electrode, 71: wiring, 72: wiring, 73: wiring, 75: wiring, 76: wiring, 77: wiring, 78: wiring, 79: wiring, 80: pixel, 81: pixel array, 82: circuit, 83: circuit, 84: circuit, 85: circuit, 91: back gate, 92: partition wall, 93: insulating layer, 200: silicon substrate, 201: silicon substrate, 202: silicon substrate, 210: semiconductor layer, 220: insulating layer, 300: insulating layer, 310: light-blocking layer, 320: organic resin layer, 330: color filter, 330a: color filter, 330b: color filter, 330c: color filter, 340: microlens array, 350: photoelectric conversion layer, 360: insulating layer, 410: package substrate, 411: package substrate, 420: cover glass, 421: lens cover, 430: adhesive, 435: lens, 440: bump, 441: land, 450: image sensor chip, 451: image sensor chip, 460: electrode pad, 461: electrode pad, 470: wire, 471: wire, 490: IC chip, 911: housing, 912: display portion, 919: camera, 931: housing, 932: display portion, 933: wristband, 935: button, 936: winder, 939: camera, 951: housing, 952: lens, 953: support portion, 961: housing, 962: shutter button, 963: microphone, 965: lens, 967: light-emitting portion, 971: housing, 972: housing, 973: display portion, 974: operation key, 975: lens, 976: joint, 981: housing, 982: display portion, 983: operation button, 984: external connection port, 985: speaker, 986: microphone, 987: camera, 1001: amorphous selenium layer, 1003: selenium compound, 1005: crystal grain, 1005a: crystal grain, 1007: crystalline selenium layer, 1009: crystal grain, 1011: crystal grain size, 1061: substrate, 1063: base layer, 1065: crystalline selenium layer, and 1067: amorphous selenium layer.

This application is based on Japanese Patent Application Serial No. 2017-059878 filed with Japan Patent Office on March 24, 2017, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A photoelectric conversion element comprising:

a first electrode;

a photoelectric conversion layer over the first electrode;

a hole injection blocking layer over the photoelectric conversion layer; and

a second electrode over the hole injection blocking layer;

wherein the photoelectric conversion layer contains selenium and an element *X*,

wherein the element *X* is one or more of silver, bismuth, indium, tin, and tellurium, and

wherein the hole injection blocking layer contains tin, gallium, and oxygen.

2. The photoelectric conversion element according to claim 1,

wherein the hole injection blocking layer comprises a region where a ratio Sn/Ga is greater than or equal to 0.0010 and less than or equal to 0.050, and

wherein the ratio Sn/Ga is a ratio of a number of tin atoms to a number of gallium atoms.

3. The photoelectric conversion element according to claim 1,

wherein a thickness of the hole injection blocking layer is greater than or equal to 5 nm and less than or equal to 50 nm.

4. The photoelectric conversion element according to claim 1,

wherein the photoelectric conversion layer contains crystalline selenium, and

wherein a crystal grain size of the crystalline selenium is greater than or equal to 0.010 μm and less than or equal to 1.10 μm.

5. The photoelectric conversion element according to claim 1,

wherein the hole injection blocking layer comprises a first hole injection blocking layer and a second hole injection blocking layer.

6. A method for manufacturing a photoelectric conversion element, comprising:

providing a base layer containing an element *X* over a first electrode;

providing a layer containing selenium over the base layer;

performing heat treatment;

providing a hole injection blocking layer containing tin, gallium, and oxygen over the layer containing selenium; and

providing a second electrode over the hole injection blocking layer,

wherein the element *X* is one or more of silver, bismuth, indium, tin, and tellurium.

7. The method for manufacturing a photoelectric conversion element, according to claim 6,

wherein the heat treatment contains a first process, a second process, and a third process,

wherein the first process is performed at a temperature higher than or equal to 50 °C and lower than or equal to 90 °C,

wherein after the first process, the second process is performed at a temperature higher than the temperature of the first process and higher than or equal to 70 °C and lower than or equal to 170 °C, and

wherein after the second process, the third process is performed at a temperature higher than the temperature of the second process and higher than or equal to 110 °C and lower than or equal to 220 °C.

8. The method for manufacturing a photoelectric conversion element, according to claim 6,

wherein the hole injection blocking layer is formed in vacuum through the first and second processes successively,

wherein the first process is performed before the second process, and

wherein proportion of oxygen in a whole deposition gas is higher in the second process than in the first process.

9. A method for manufacturing a photoelectric conversion element, comprising:

providing a layer containing selenium over a first electrode;

providing a base layer containing an element *X* over the layer containing selenium;

performing heat treatment;

providing a hole injection blocking layer containing tin, gallium, and oxygen over the layer containing selenium; and

providing a second electrode over the hole injection blocking layer,

wherein the element *X* is one or more of silver, bismuth, indium, tin, and tellurium.

10. The method for manufacturing a photoelectric conversion element, according to claim 9,

wherein the heat treatment contains a first process, a second process, and a third process,

wherein the first process is performed at a temperature higher than or equal to 50 °C and lower than or equal to 90 °C,

wherein after the first process, the second process is performed at a temperature higher than the temperature of the first process and higher than or equal to 70 °C and lower than or equal to 170 °C, and

wherein after the second process, the third process is performed at a temperature higher than the temperature of the second process and higher than or equal to 110 °C and lower than or equal to 220 °C.

11. The method for manufacturing a photoelectric conversion element, according to claim 9,

wherein the hole injection blocking layer is formed in vacuum through the first and second processes successively,

wherein the first process is performed before the second process, and

wherein proportion of oxygen in a whole deposition gas is higher in the second process than in the first process.

FIG. 1A

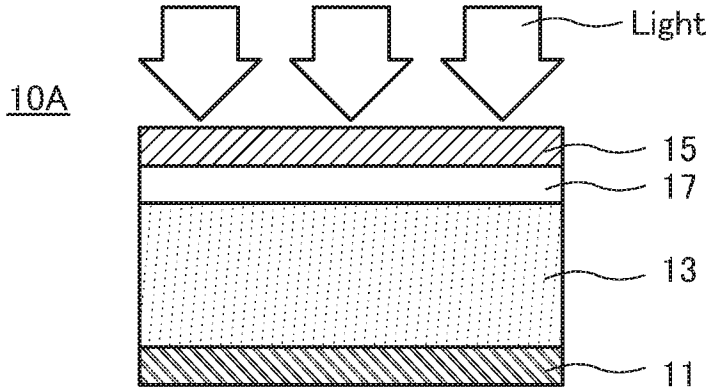


FIG. 1B

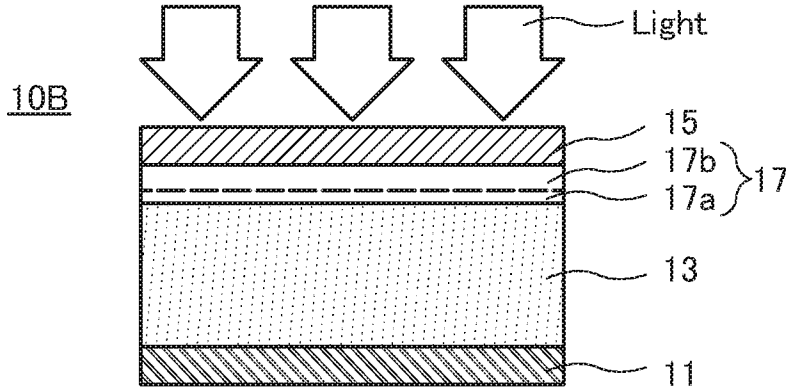


FIG. 1C

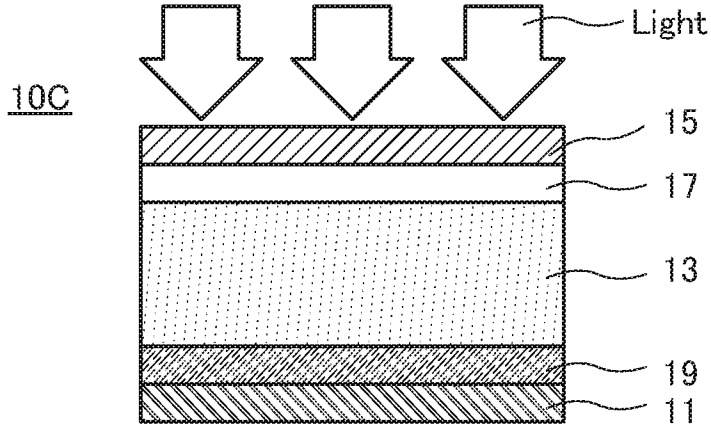


FIG. 2A

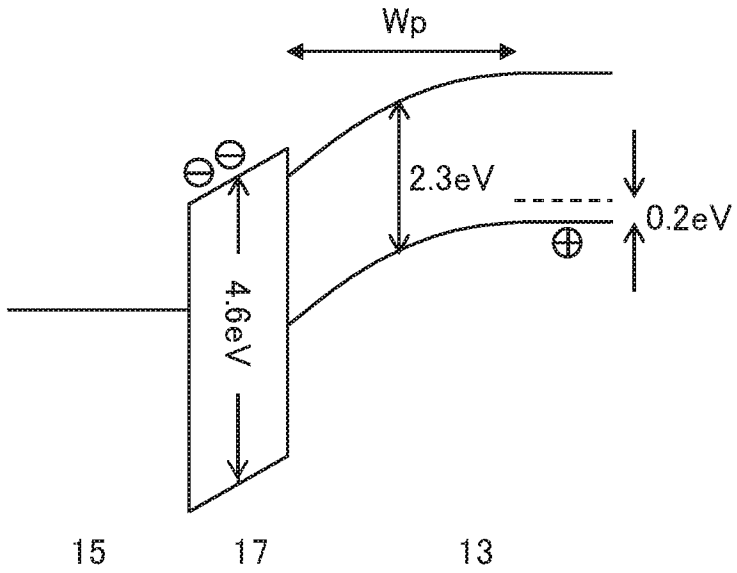


FIG. 2B

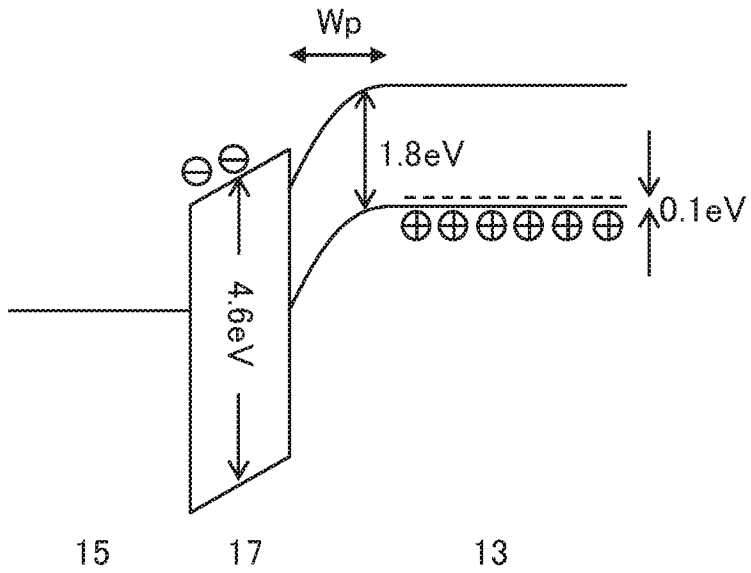


FIG. 3

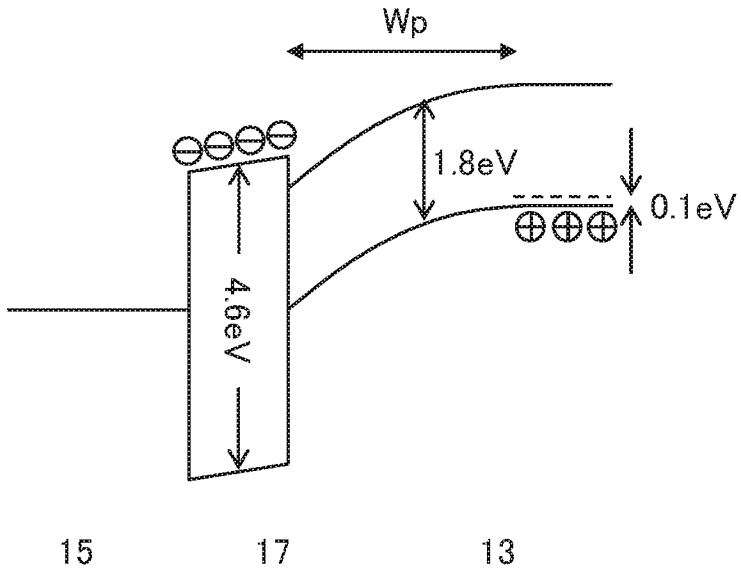


FIG. 4

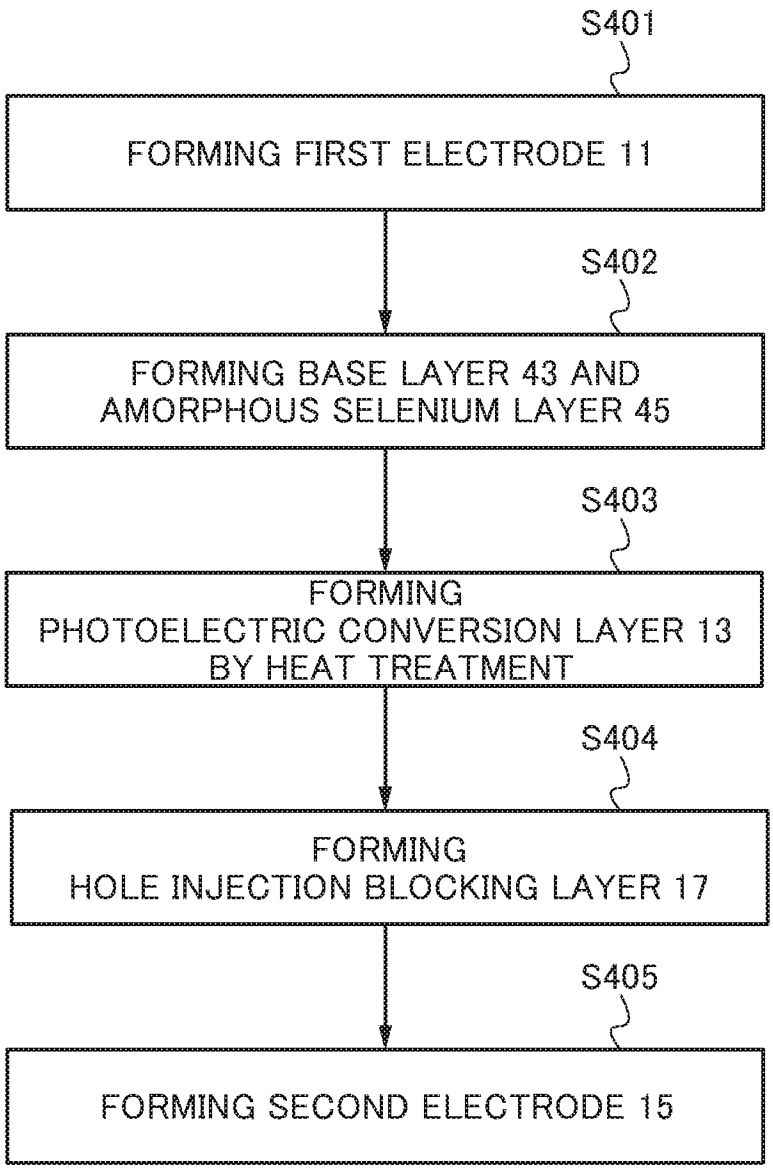

S401
FORMING FIRST ELECTRODE 11
S402
FORMING BASE LAYER 43 AND AMORPHOUS SELENIUM LAYER 45
S403
FORMING PHOTOELECTRIC CONVERSION LAYER 13 BY HEAT TREATMENT
S404
FORMING HOLE INJECTION BLOCKING LAYER 17
S405
FORMING SECOND ELECTRODE 15

FIG. 5A

FIG. 5B

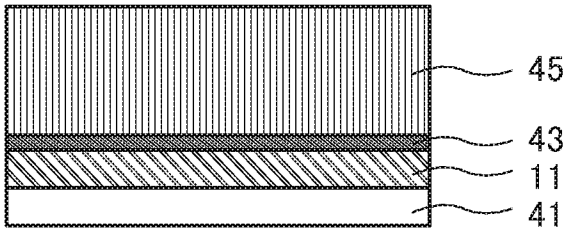


FIG. 5C

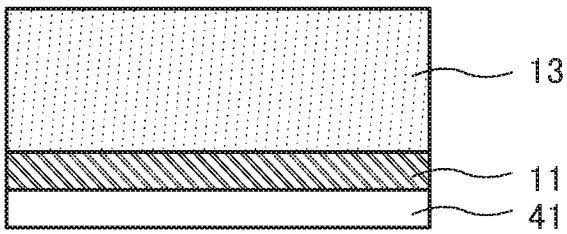


FIG. 5D

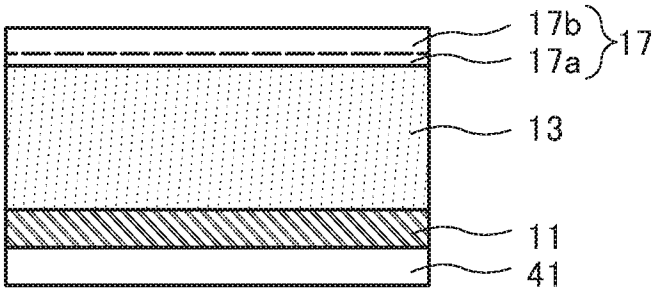


FIG. 5E

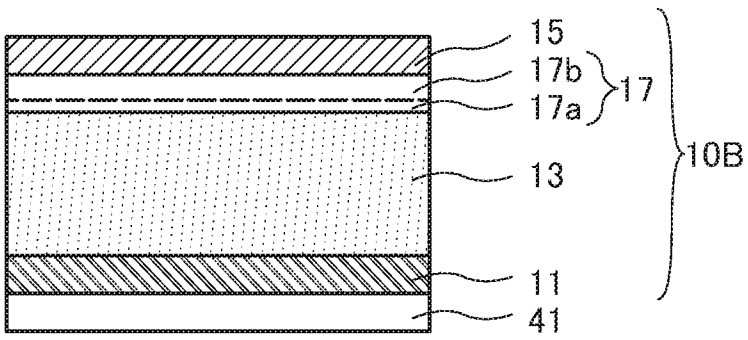


FIG. 6A

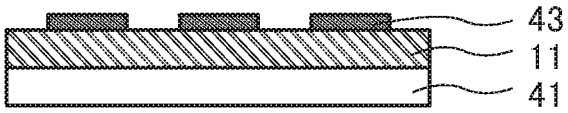


FIG. 6B

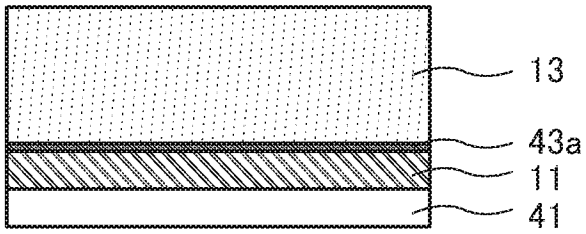


FIG. 6C

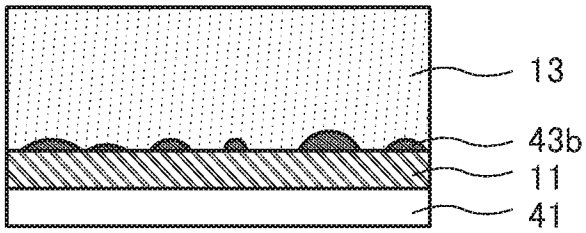


FIG. 6D

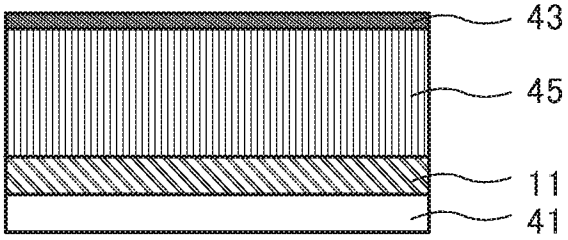


FIG. 7A

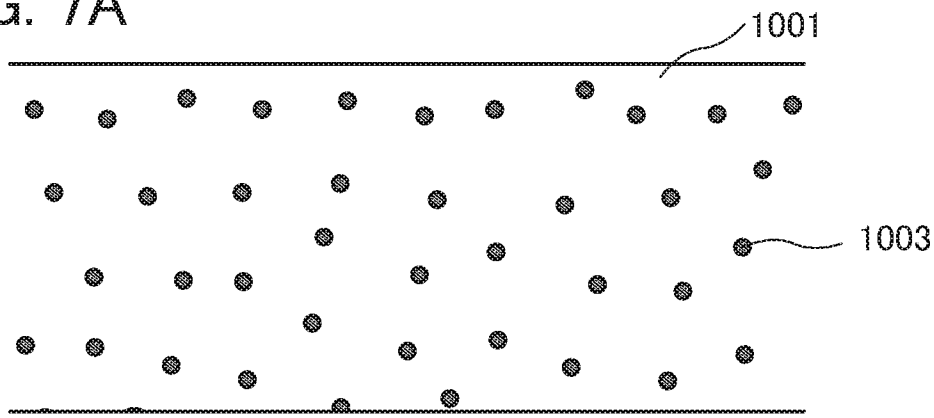


FIG. 7B

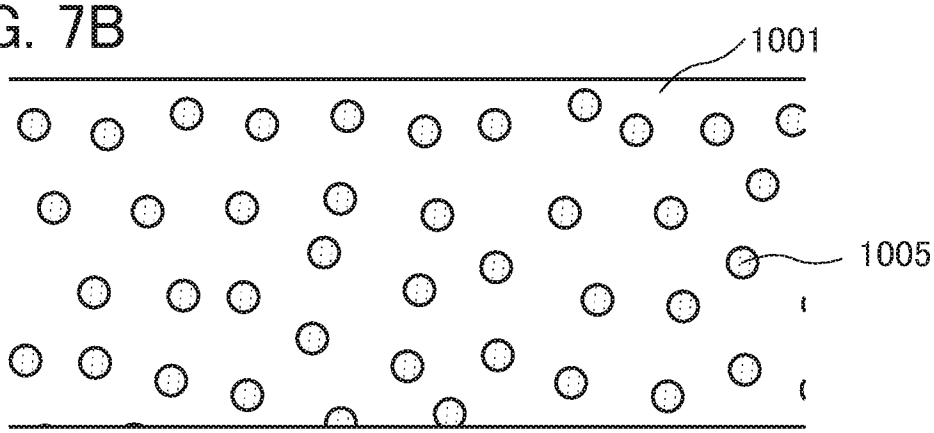


FIG. 7C

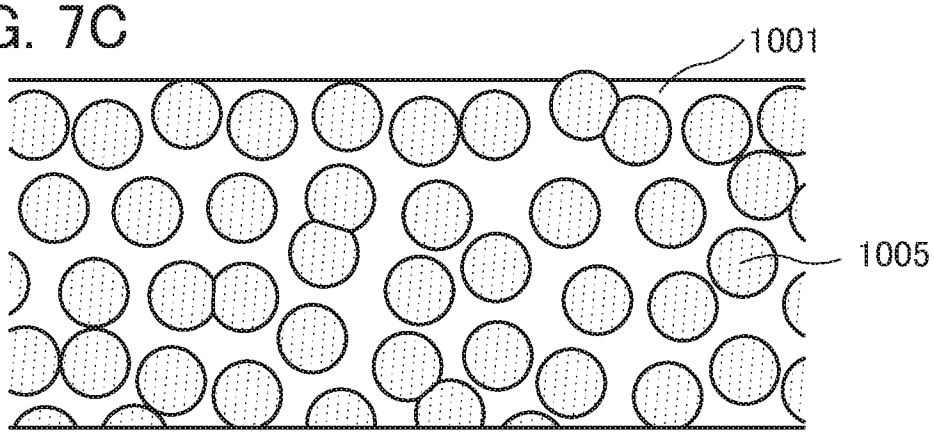


FIG. 7D

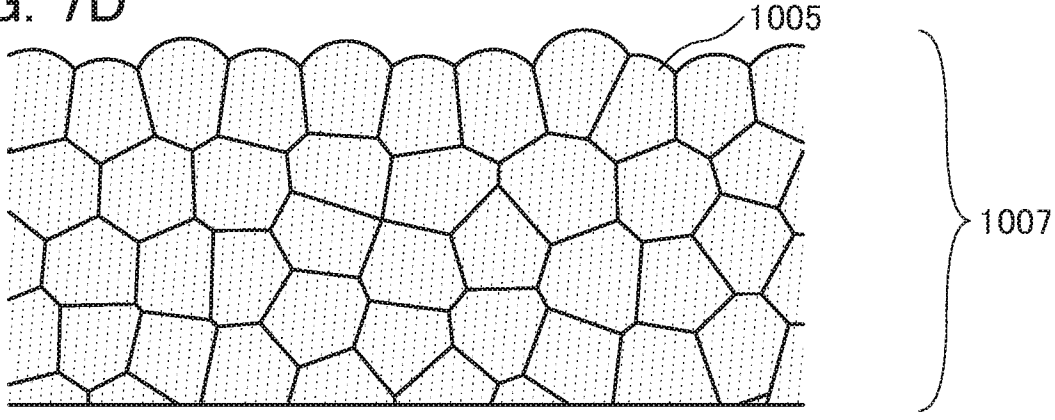


FIG. 8A

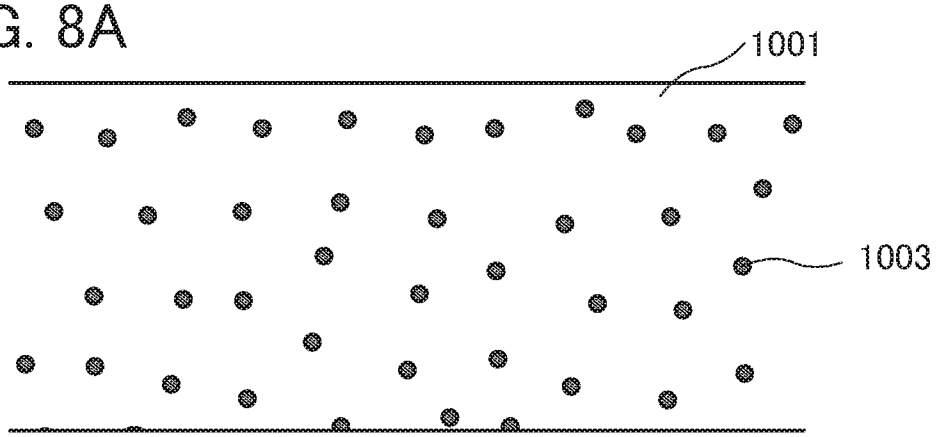


FIG. 8B

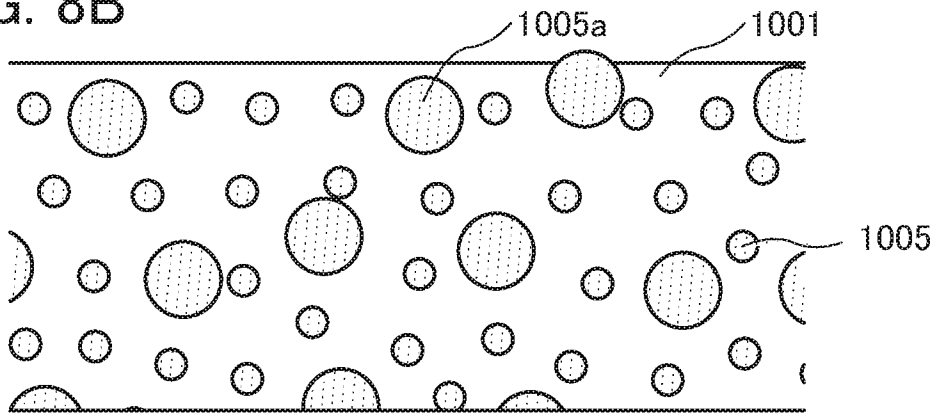


FIG. 8C

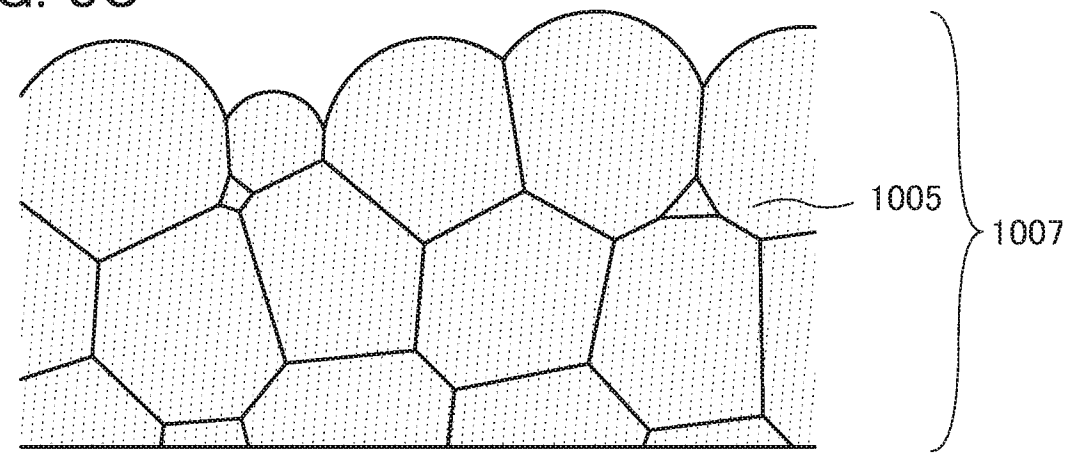


FIG. 9

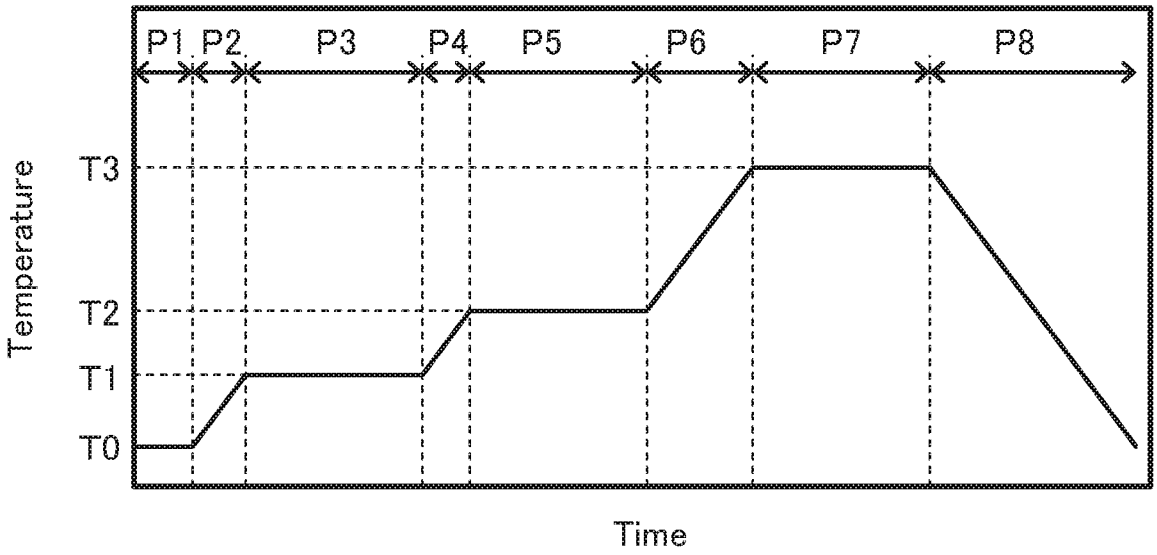


FIG. 10A

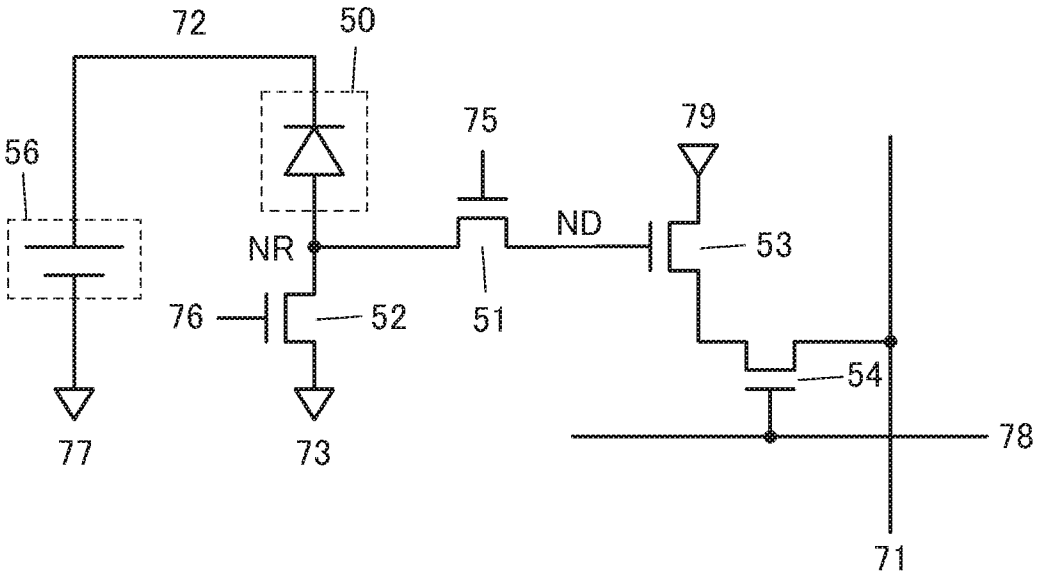


FIG. 10B

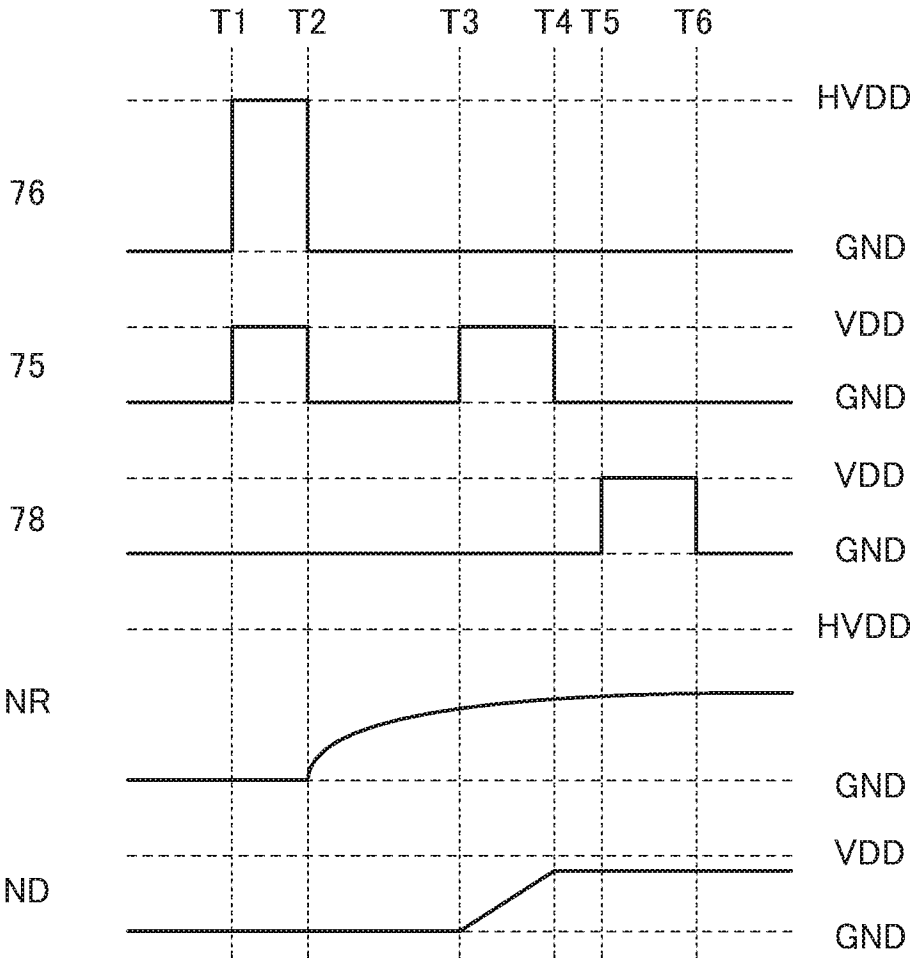


FIG. 11A

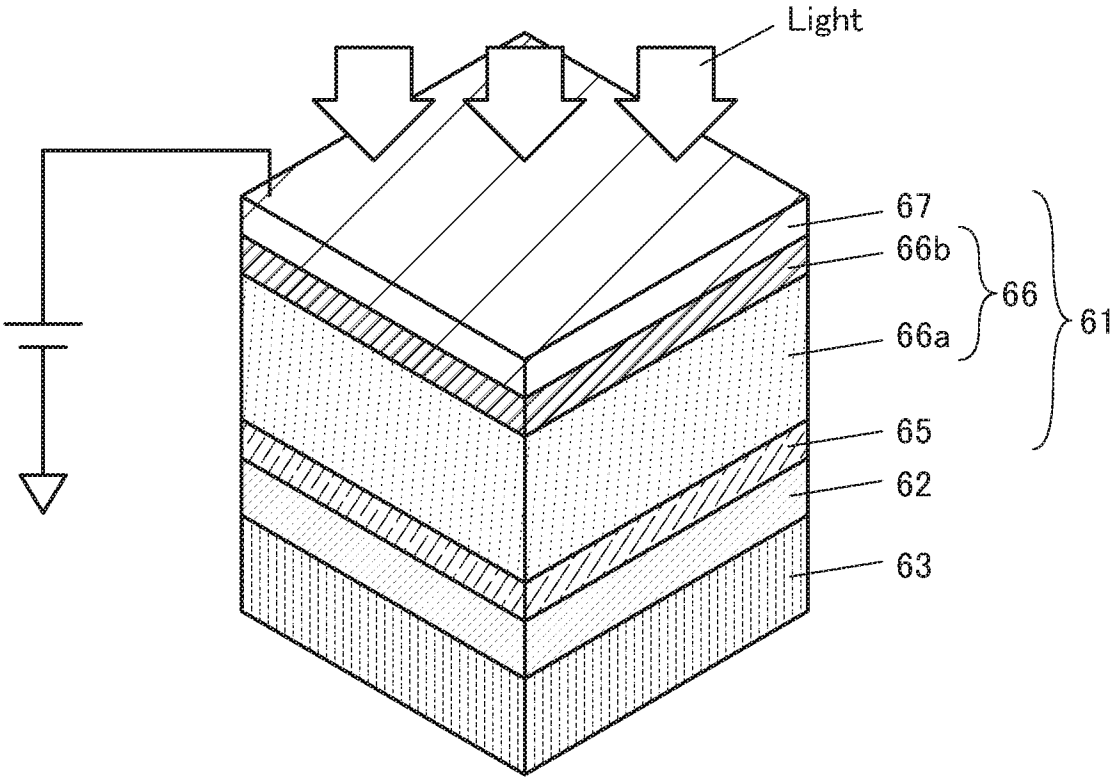


FIG. 11B

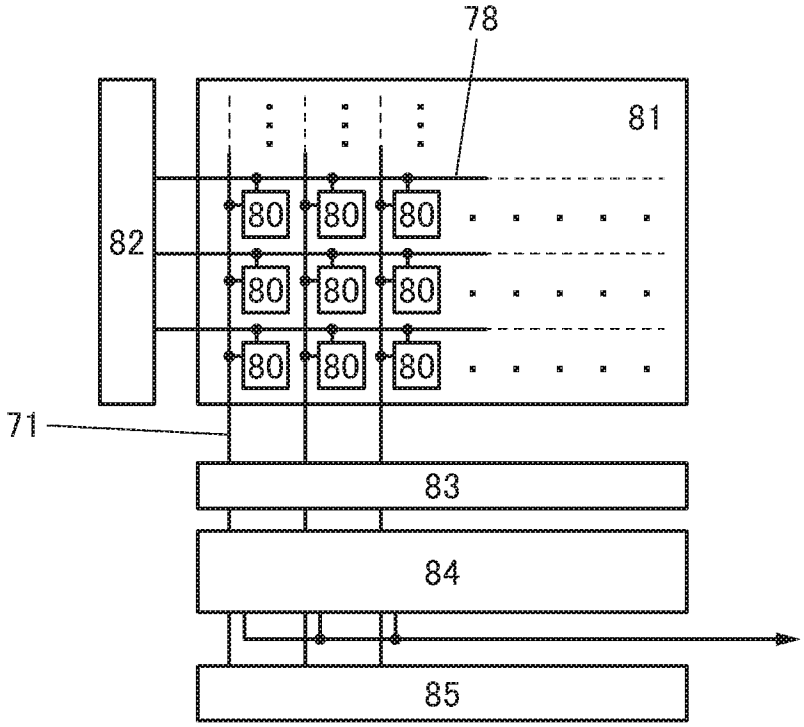


FIG. 12A

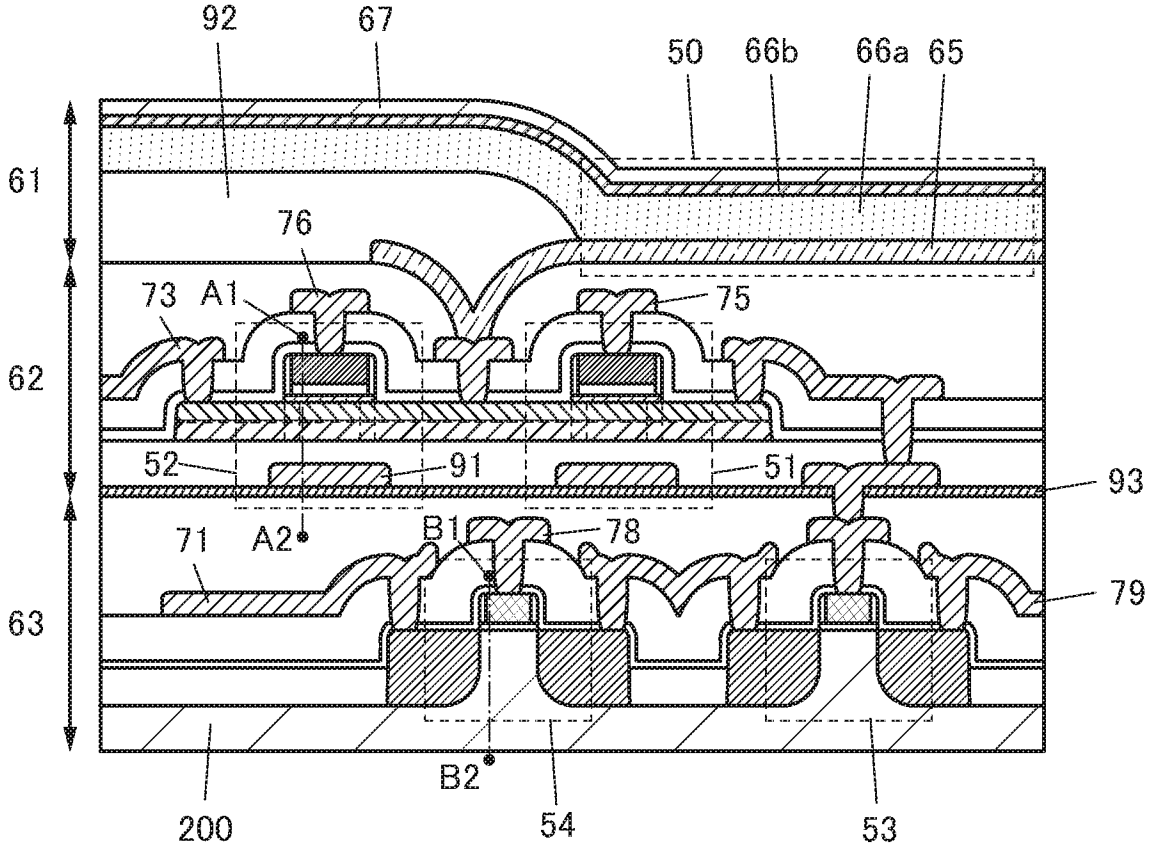


FIG. 12B

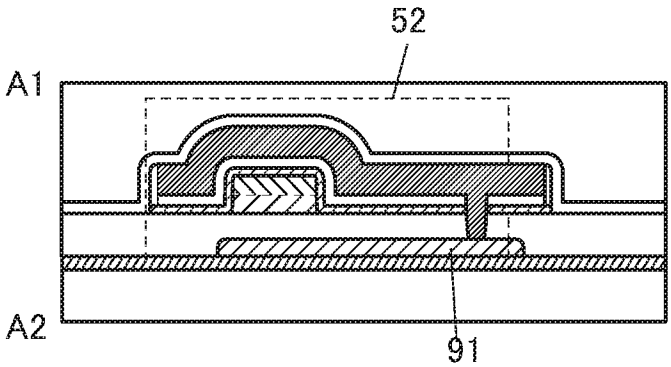


FIG. 12C

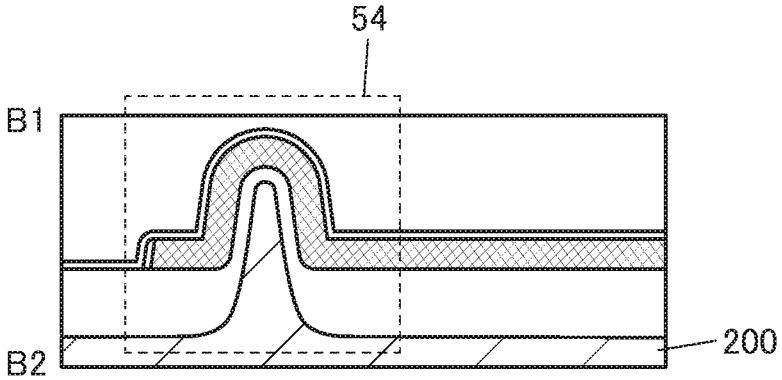


FIG. 13A

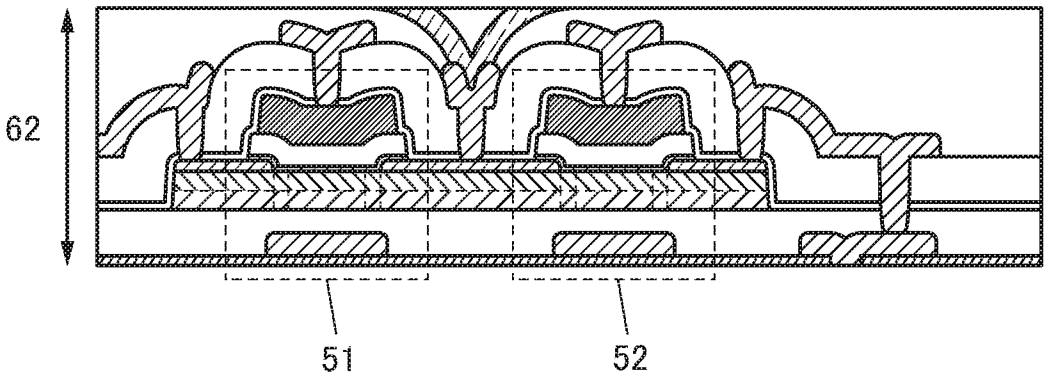


FIG. 13B

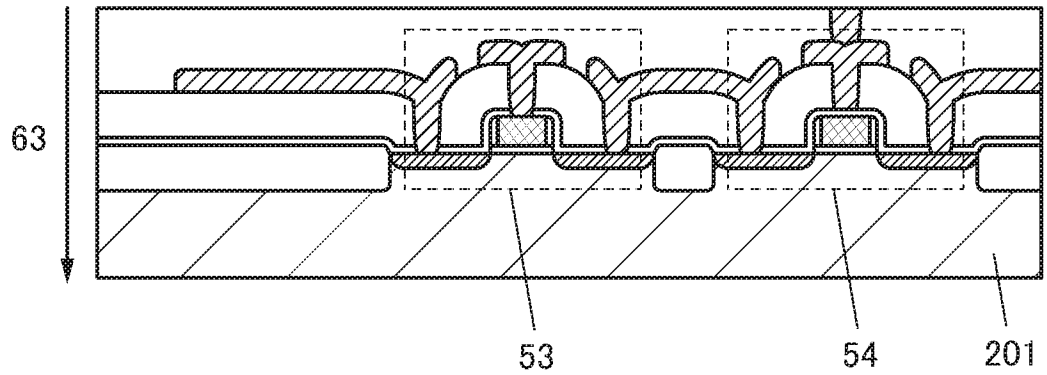


FIG. 13C

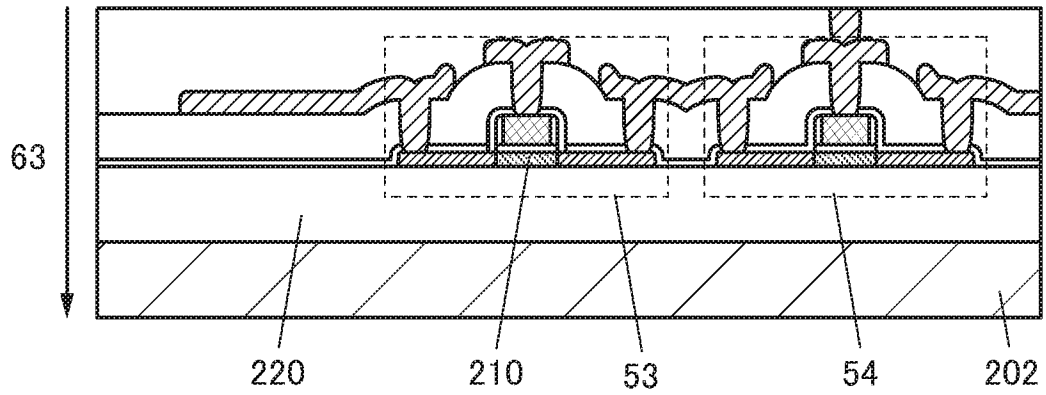


FIG. 14A

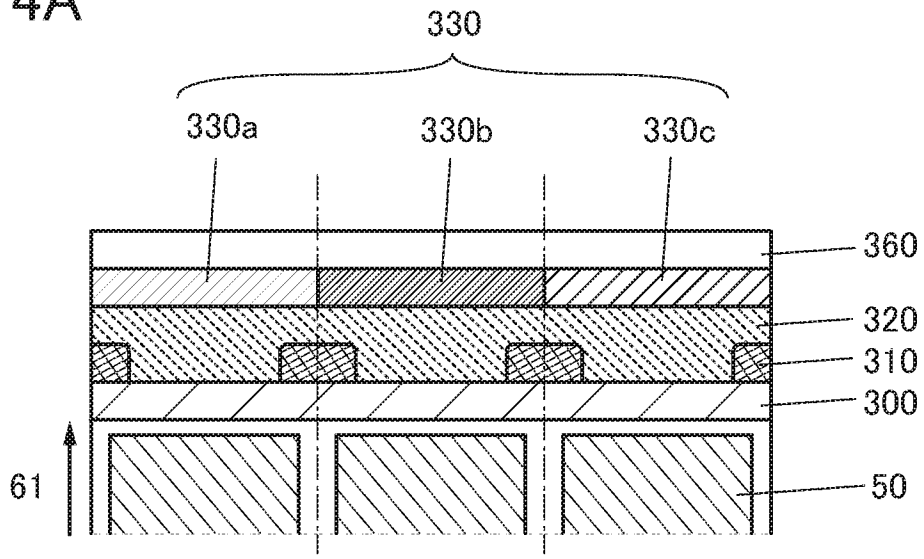


FIG. 14B

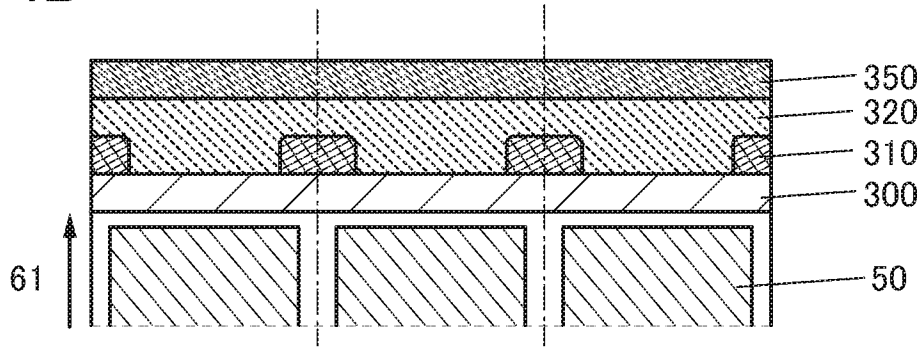


FIG. 14C

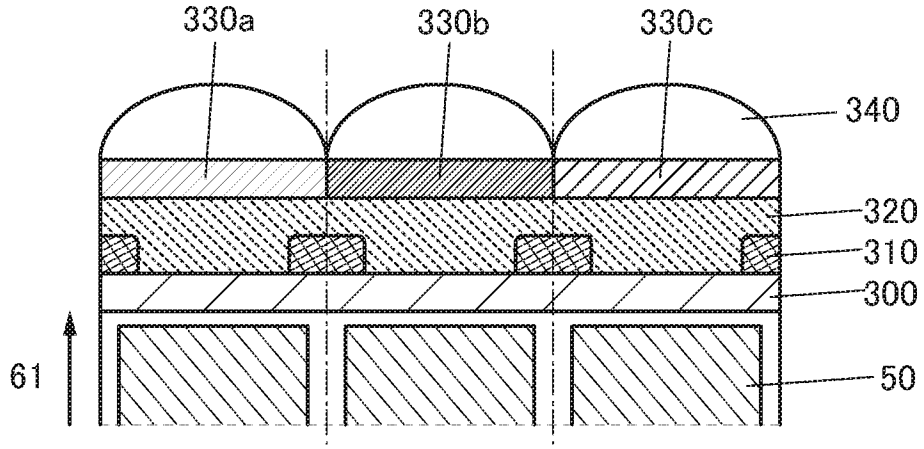


FIG. 15A1

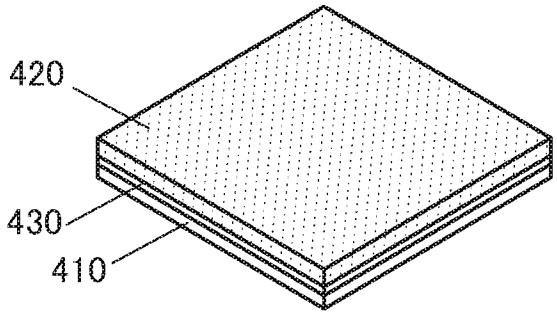


FIG. 15B1

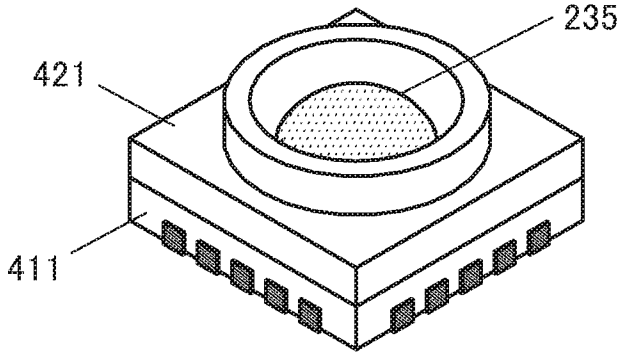


FIG. 15A2

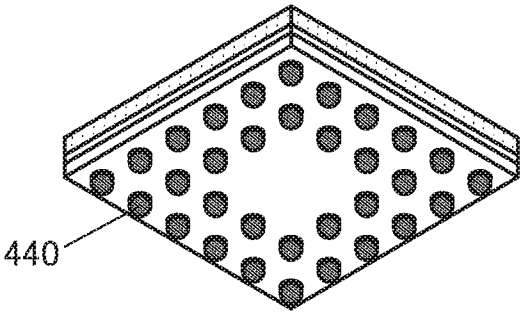


FIG. 15B2

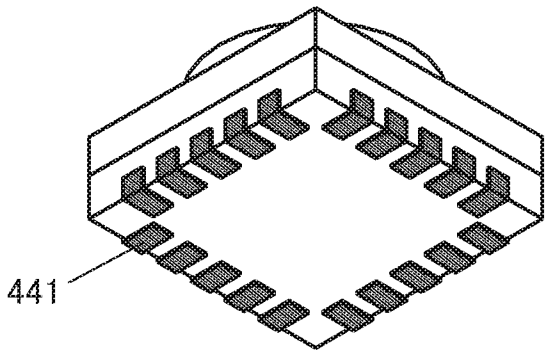


FIG. 15A3

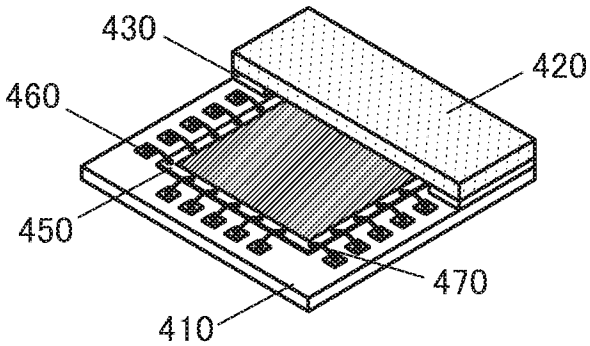


FIG. 15B3

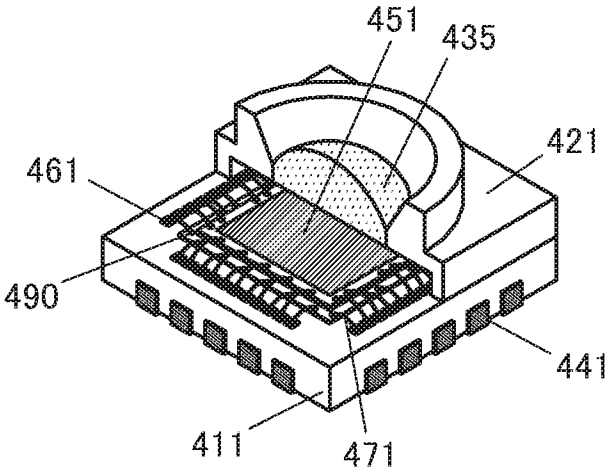


FIG. 16A

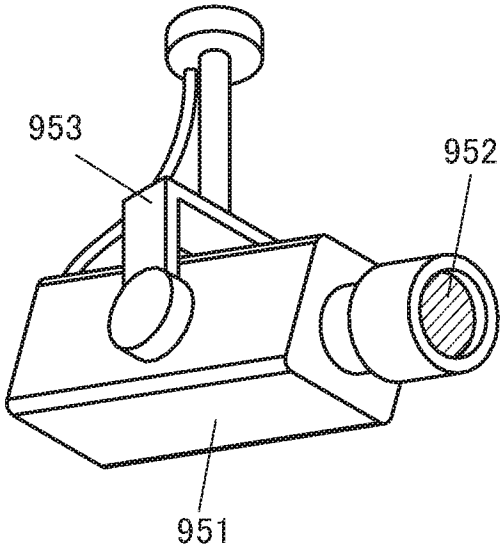


FIG. 16B

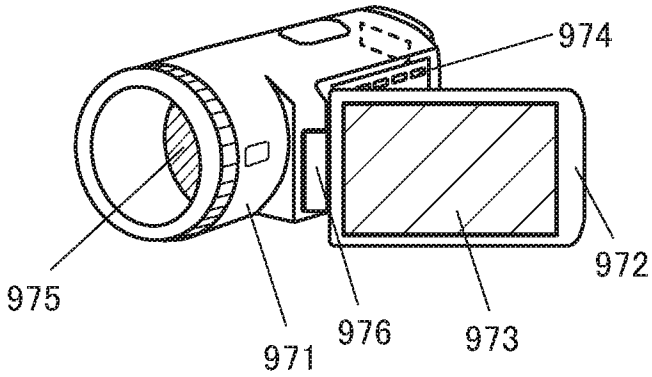


FIG. 16C

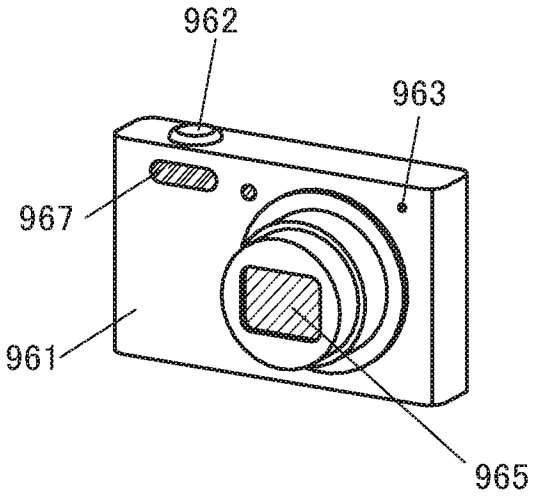


FIG. 16D

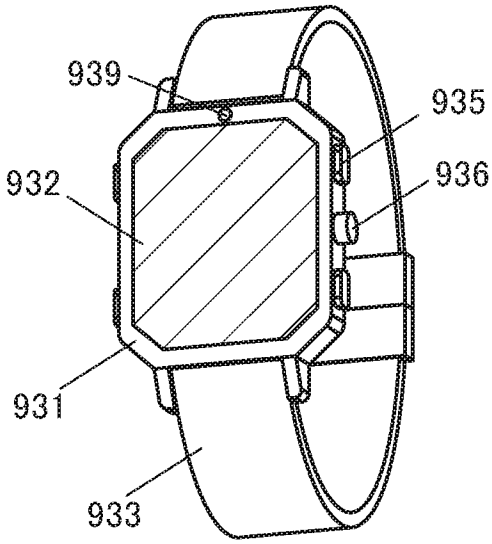


FIG. 16E

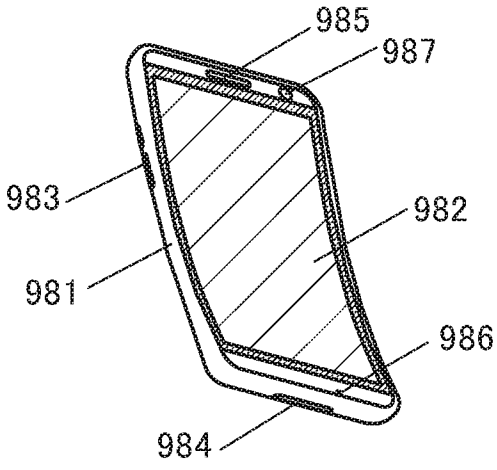


FIG. 16F

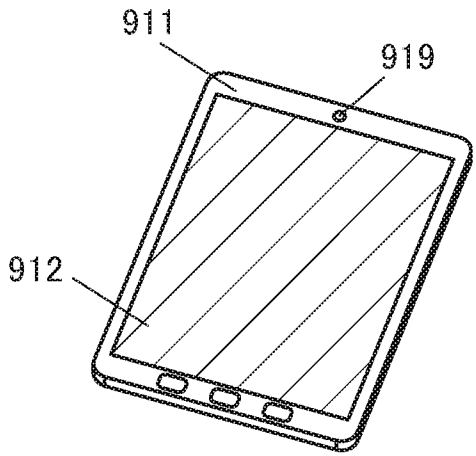


FIG. 17A

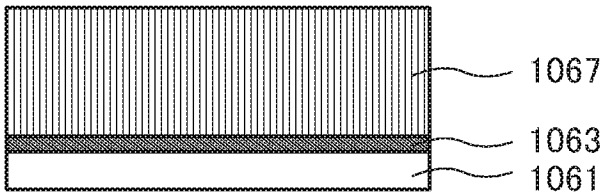


FIG. 17B

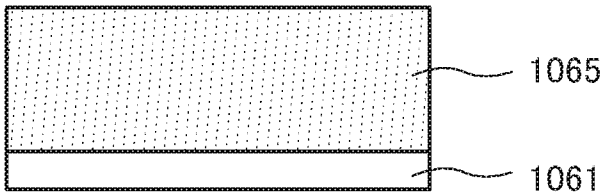
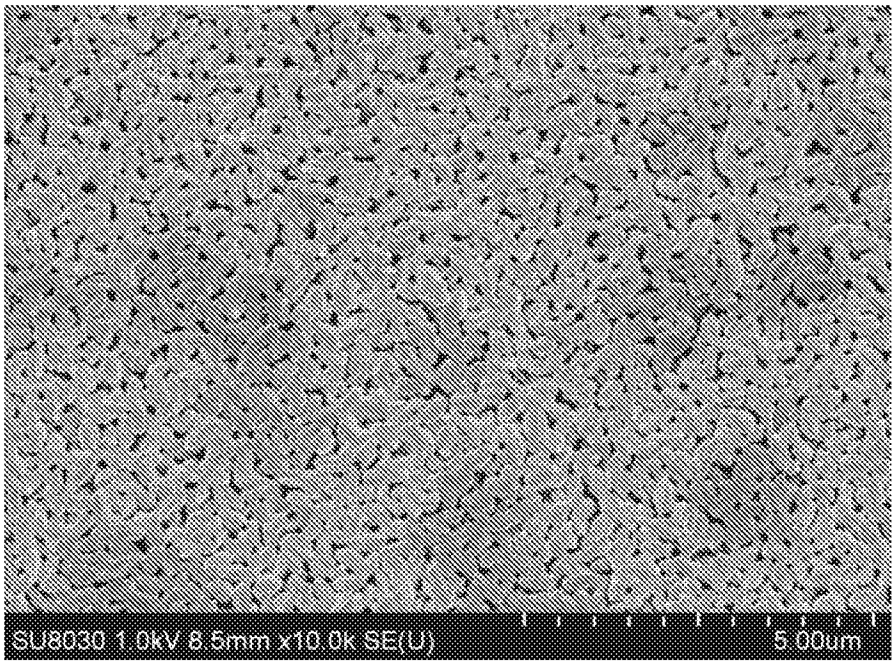
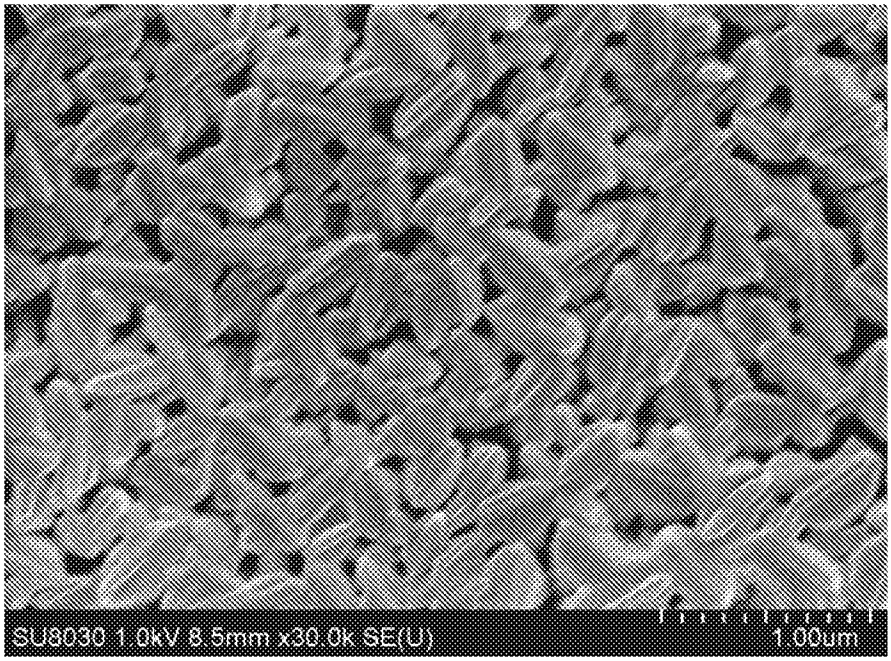


FIG. 18A



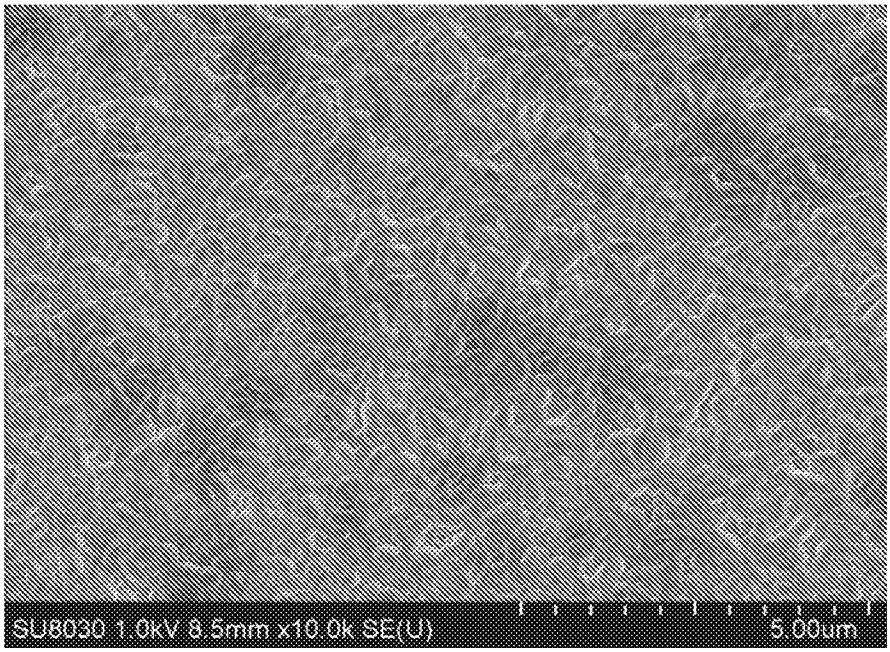
5.00 μm

FIG. 18B



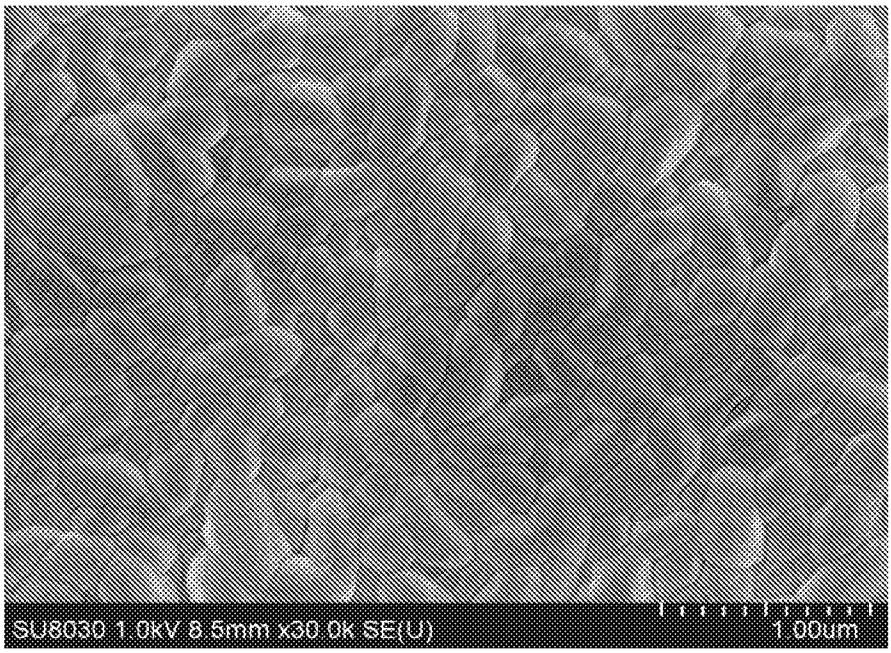
1.00 μm

FIG. 19A



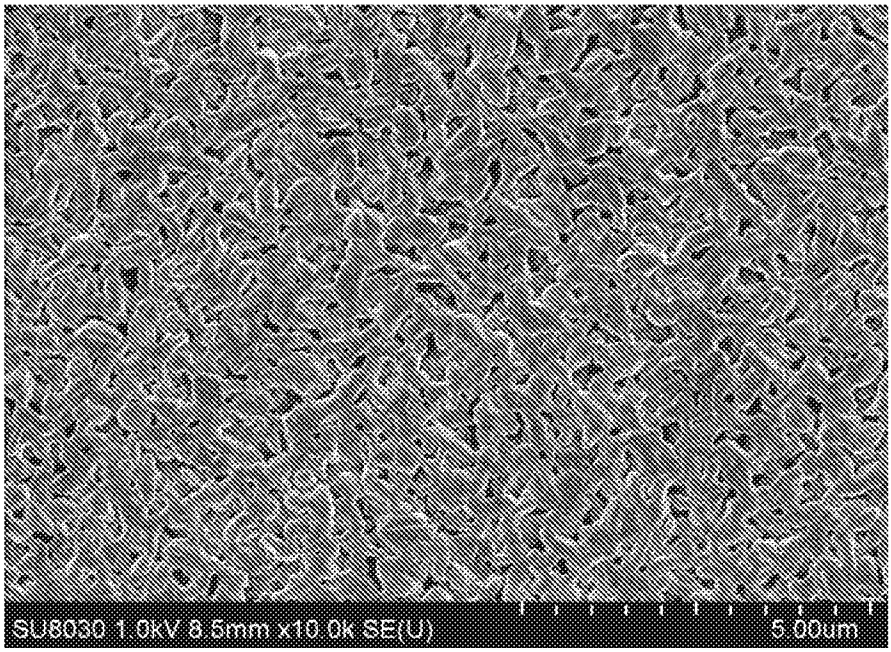
5.00 μm

FIG. 19B



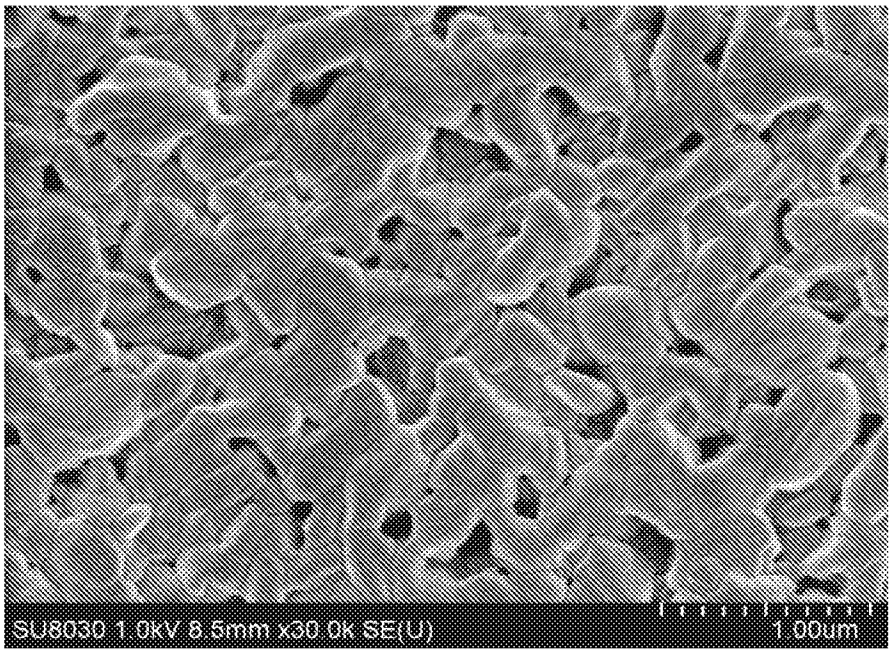
1.00 μm

FIG. 20A



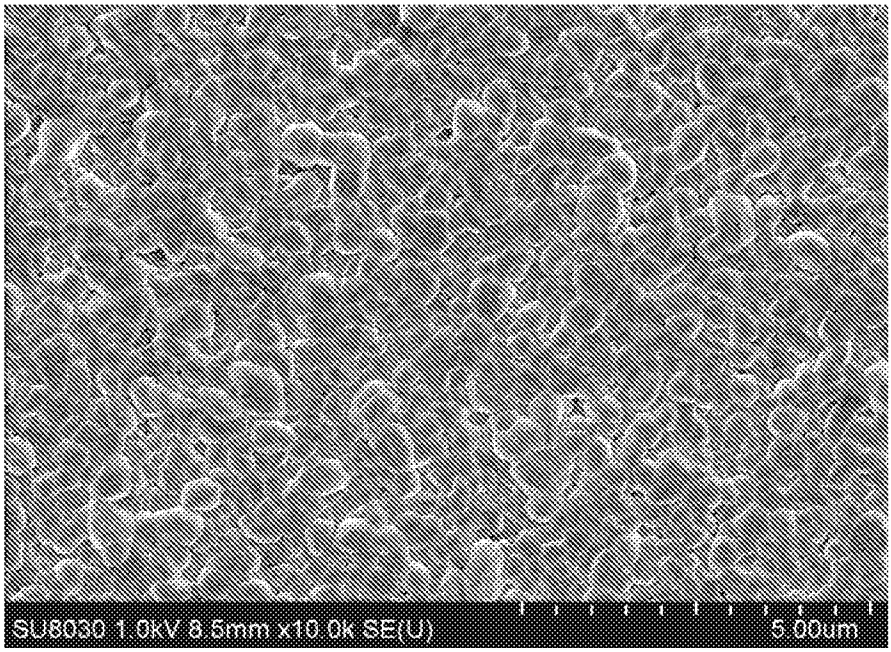
5.00 μm

FIG. 20B



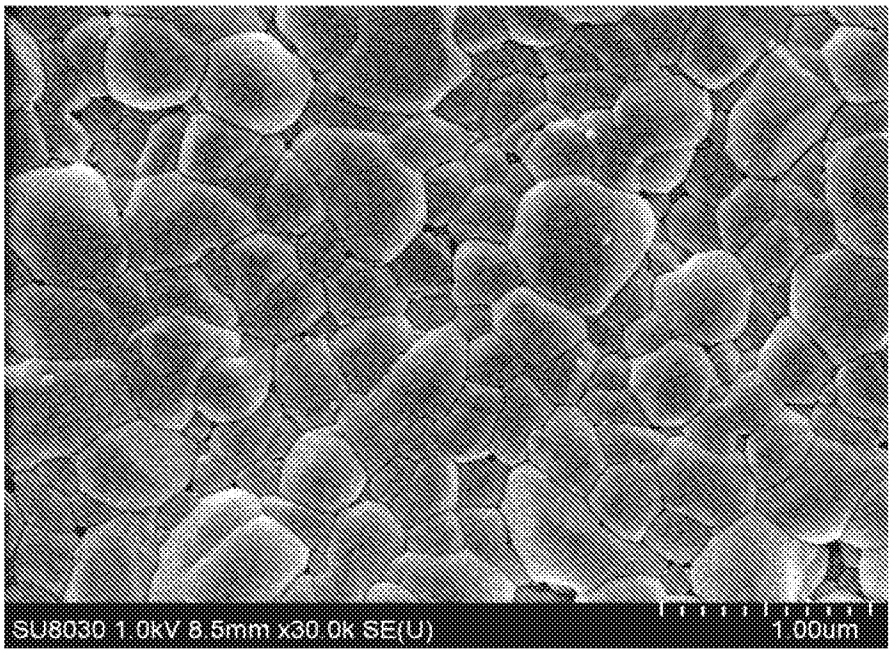
1.00 μm

FIG. 21A



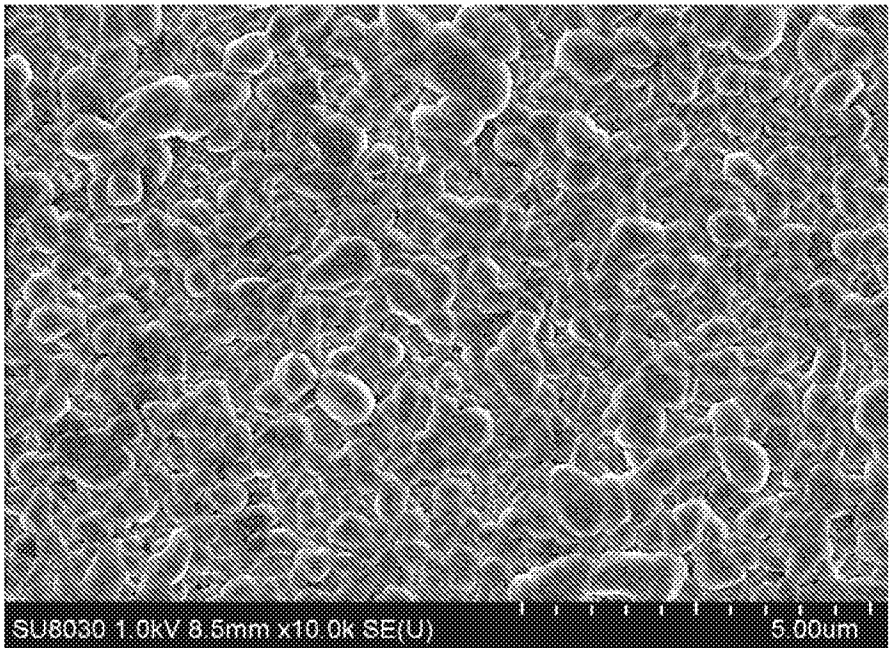
5.00 μm

FIG. 21B



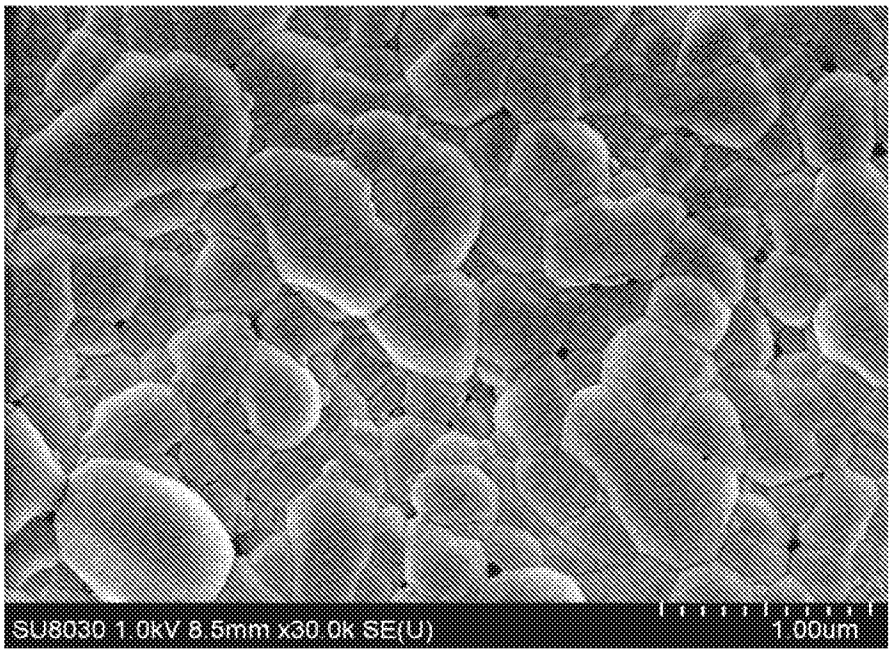
1.00 μm

FIG. 22A



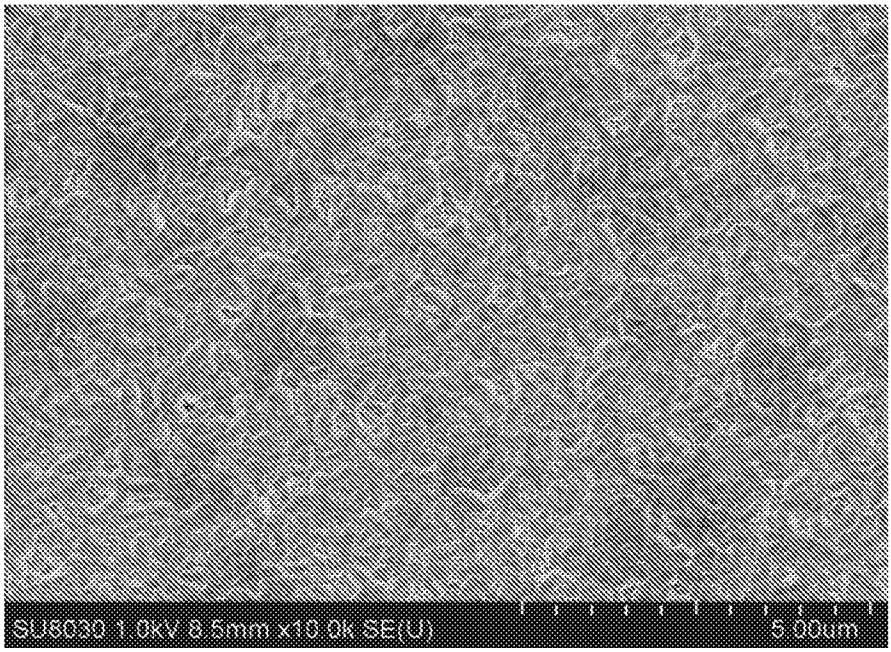
5.00 μ m

FIG. 22B



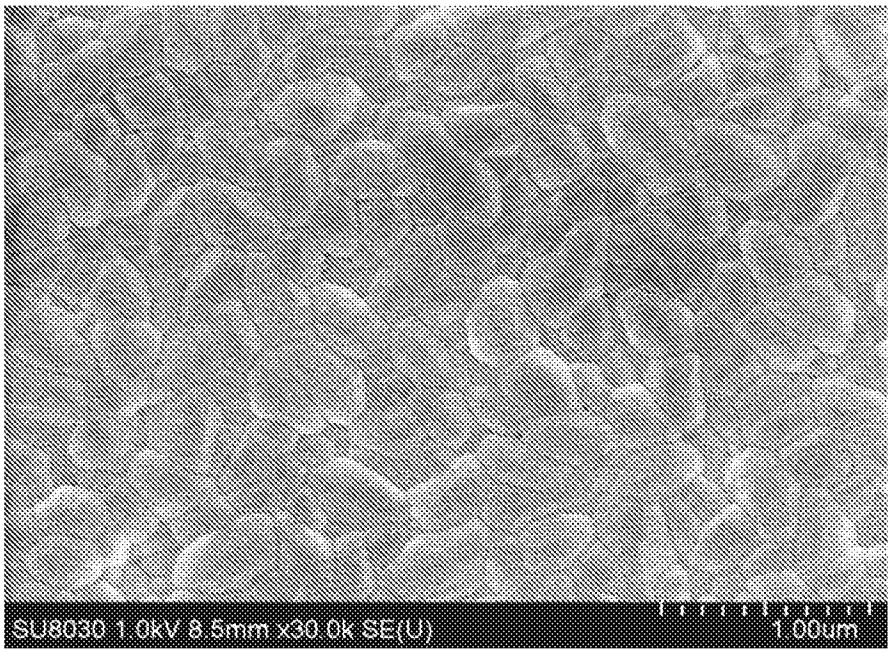
1.00 μ m

FIG. 23A



5.00 μ m

FIG. 23B



1.00 μ m

FIG. 24A

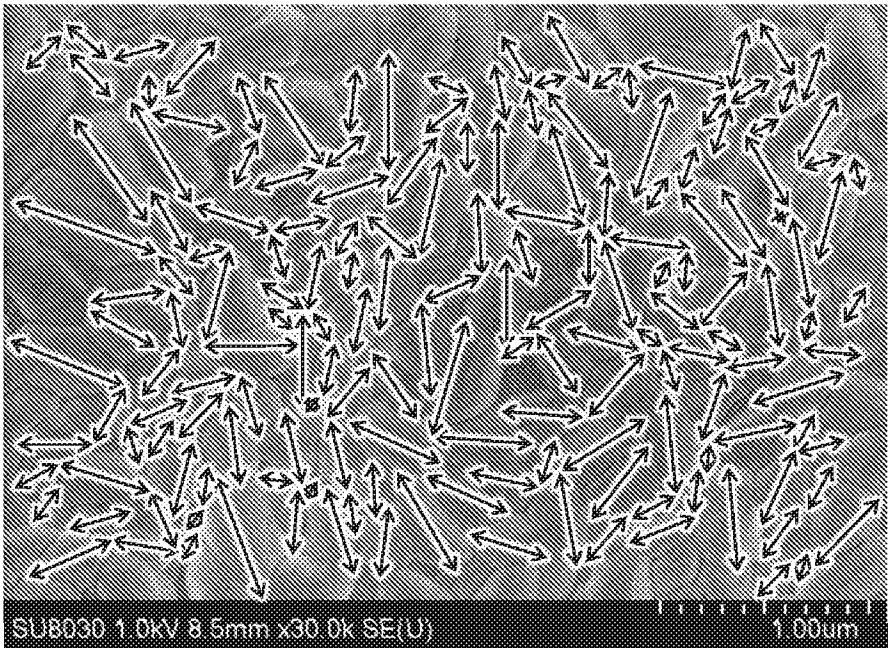


FIG. 24B

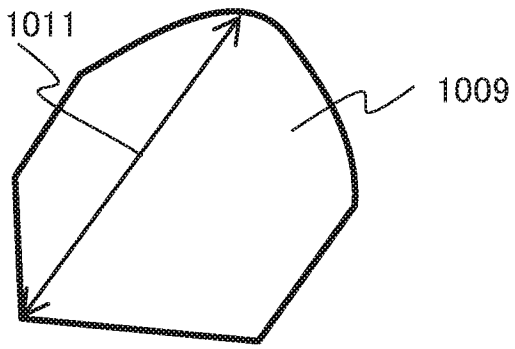


FIG. 24C

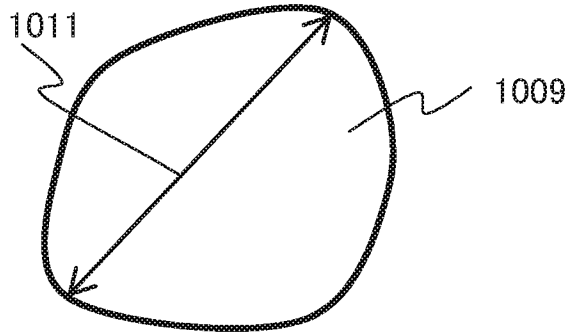


FIG. 24D

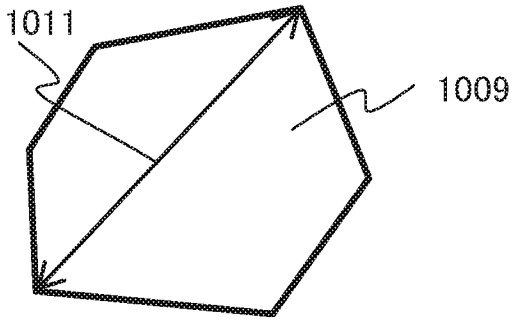


FIG. 25A

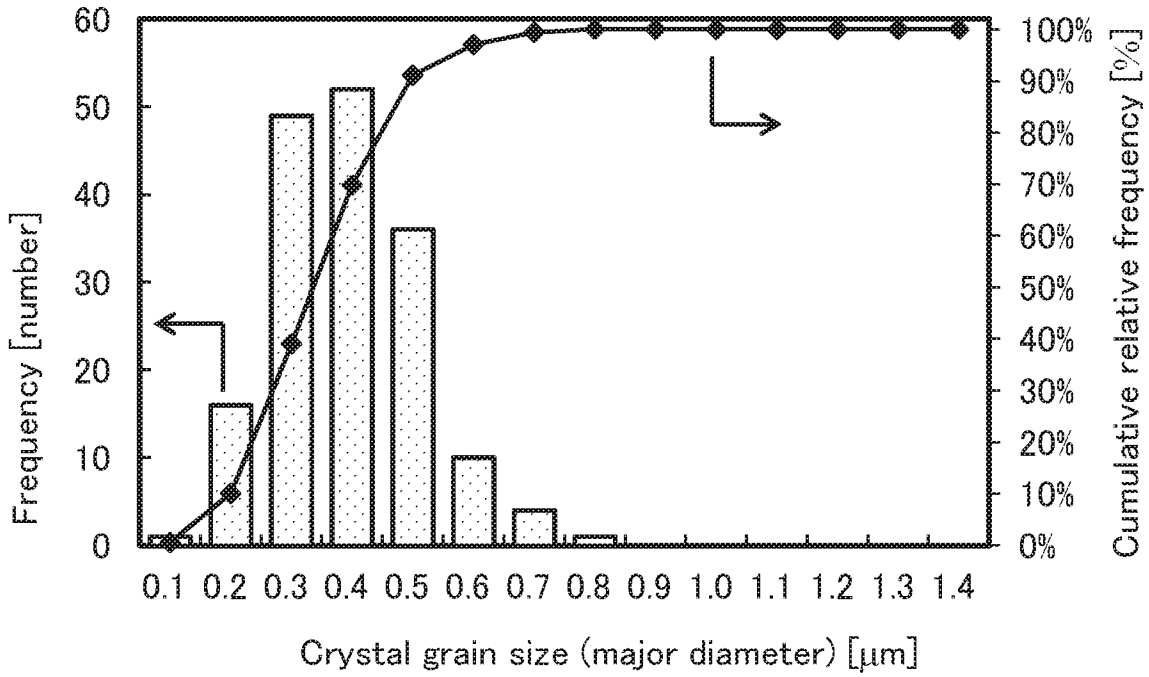


FIG. 25B

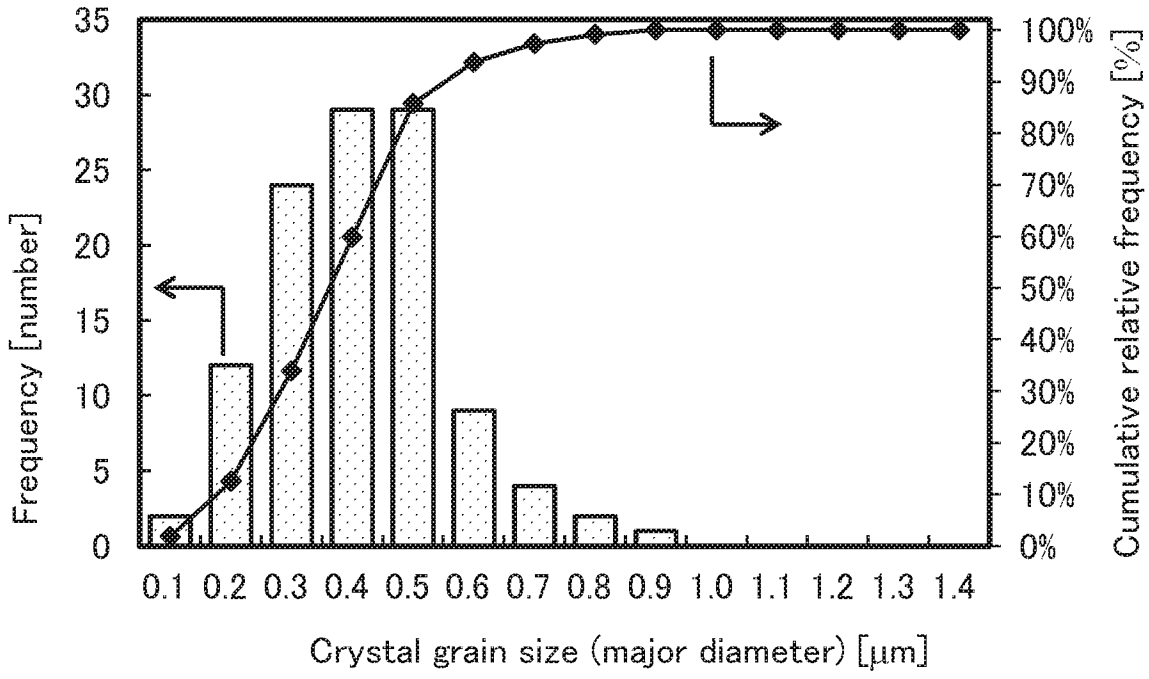


FIG. 26A

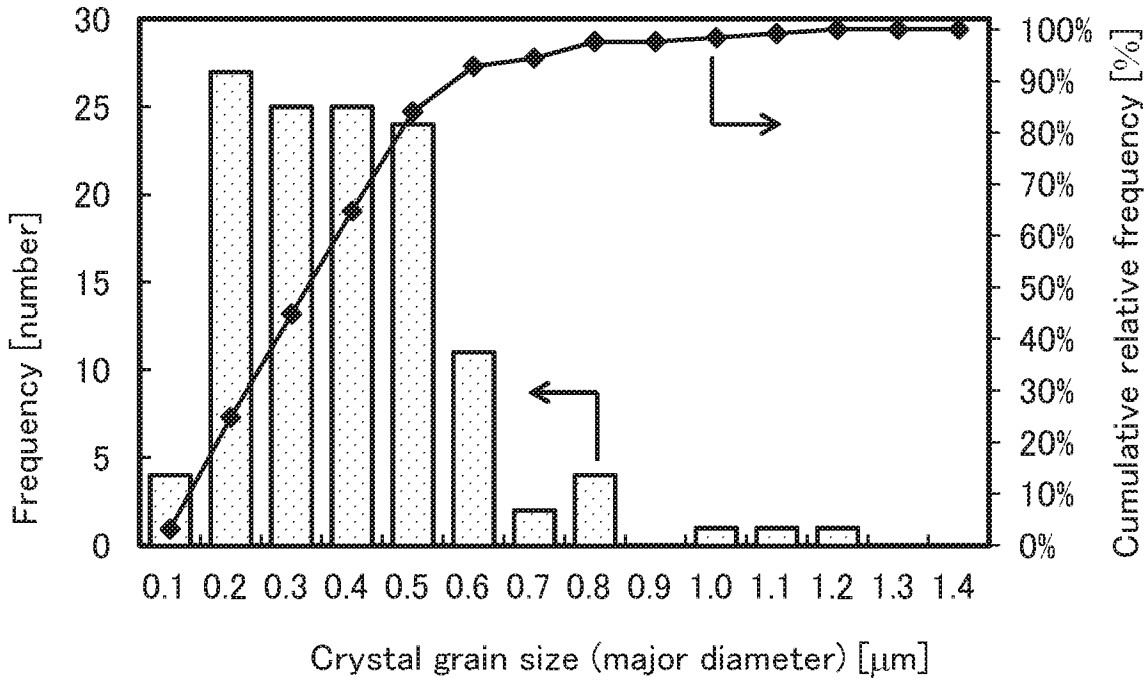


FIG. 26B

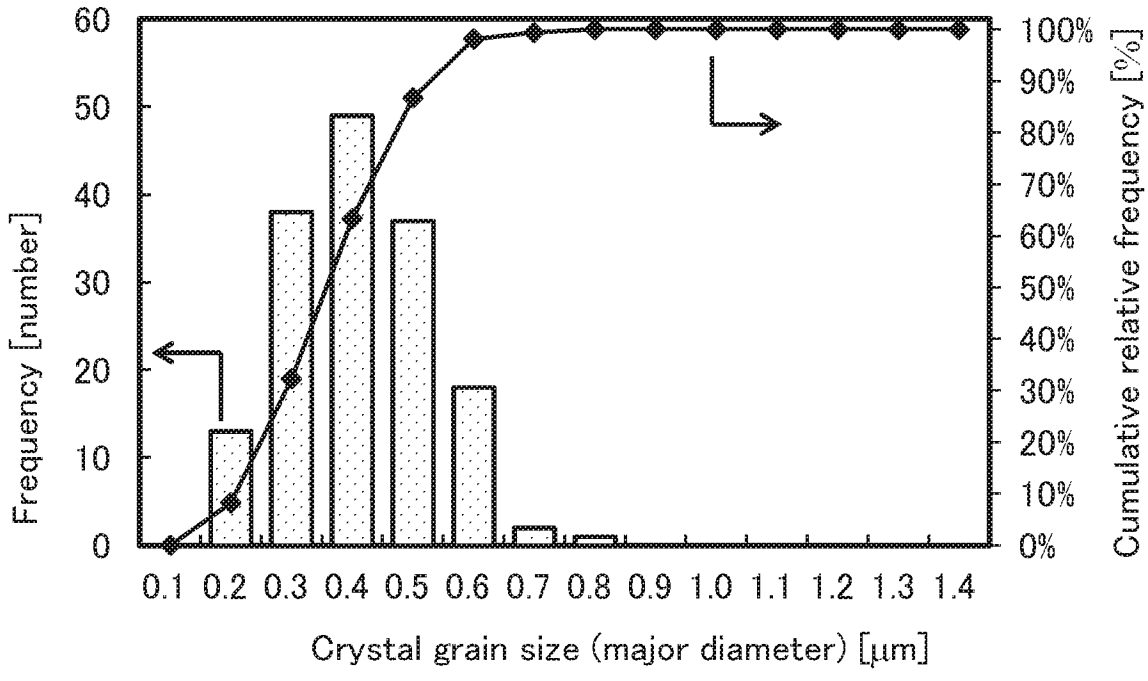


FIG. 27A

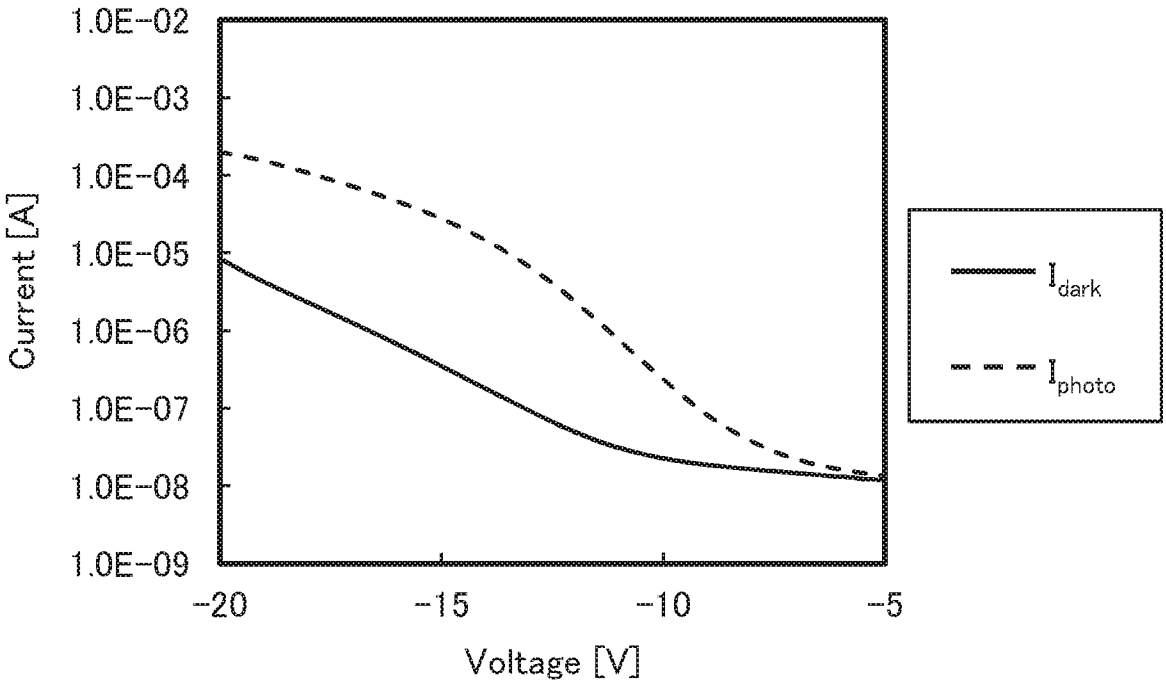


FIG. 27B

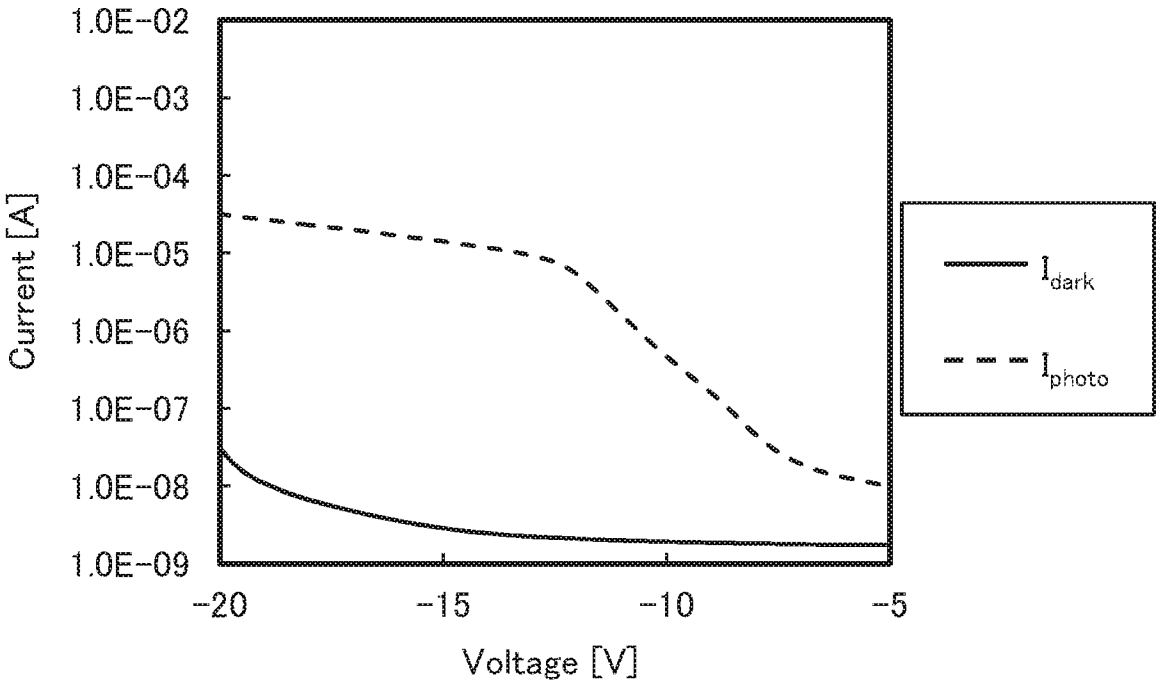


FIG. 28A

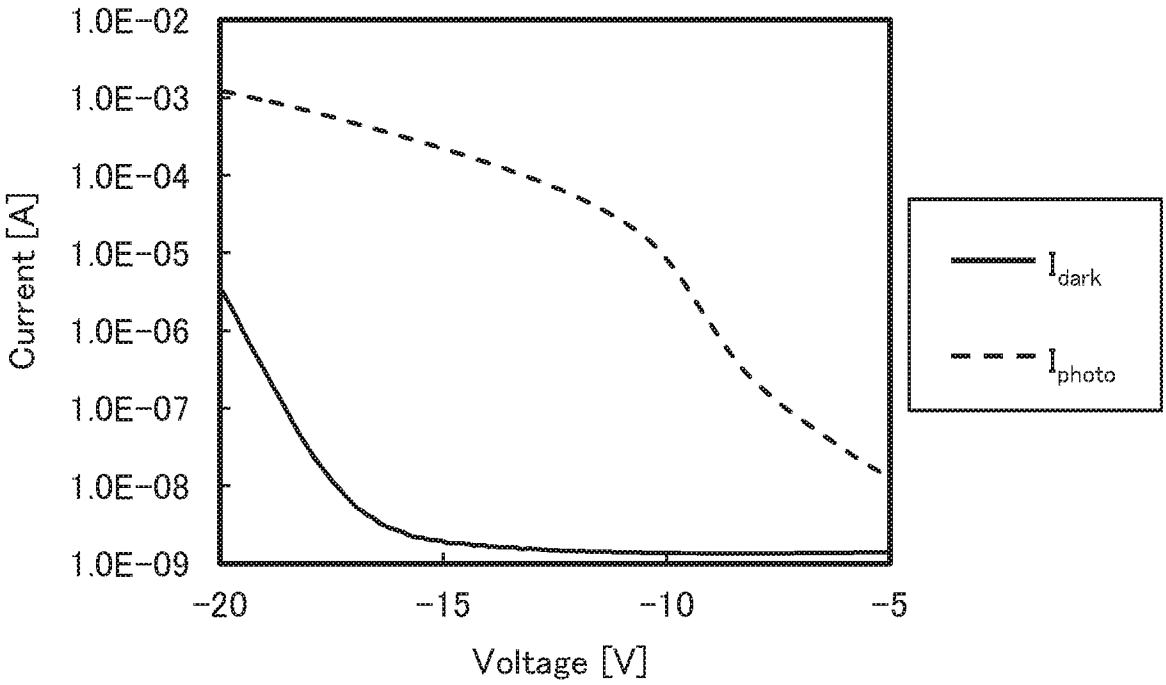


FIG. 28B

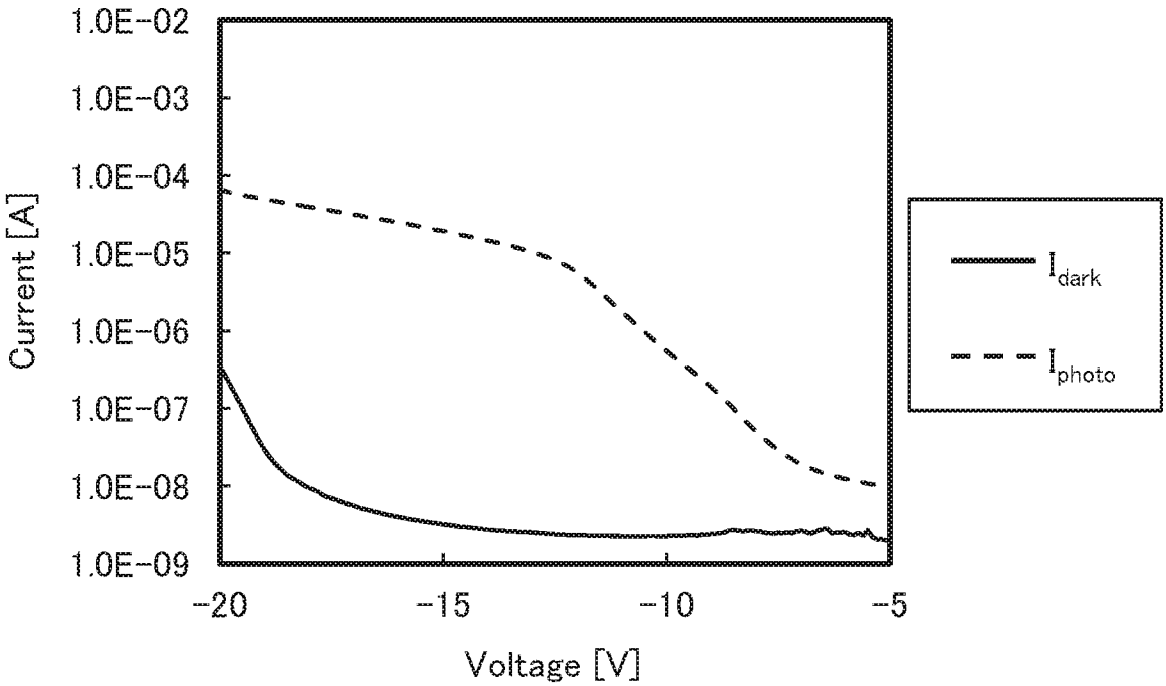


FIG. 29

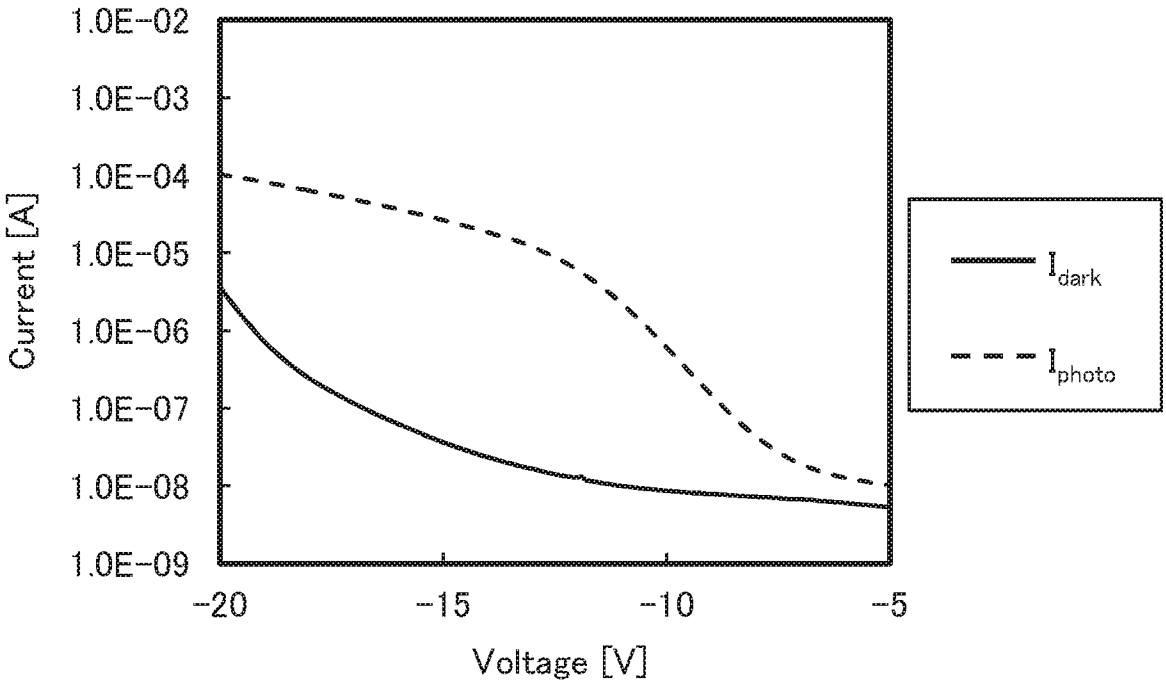

1.0E-02
1.0E-03
1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
Current [A]
-20
-15
-10
-5
Voltage [V]
I_{dark}
I_{photo}

FIG. 30

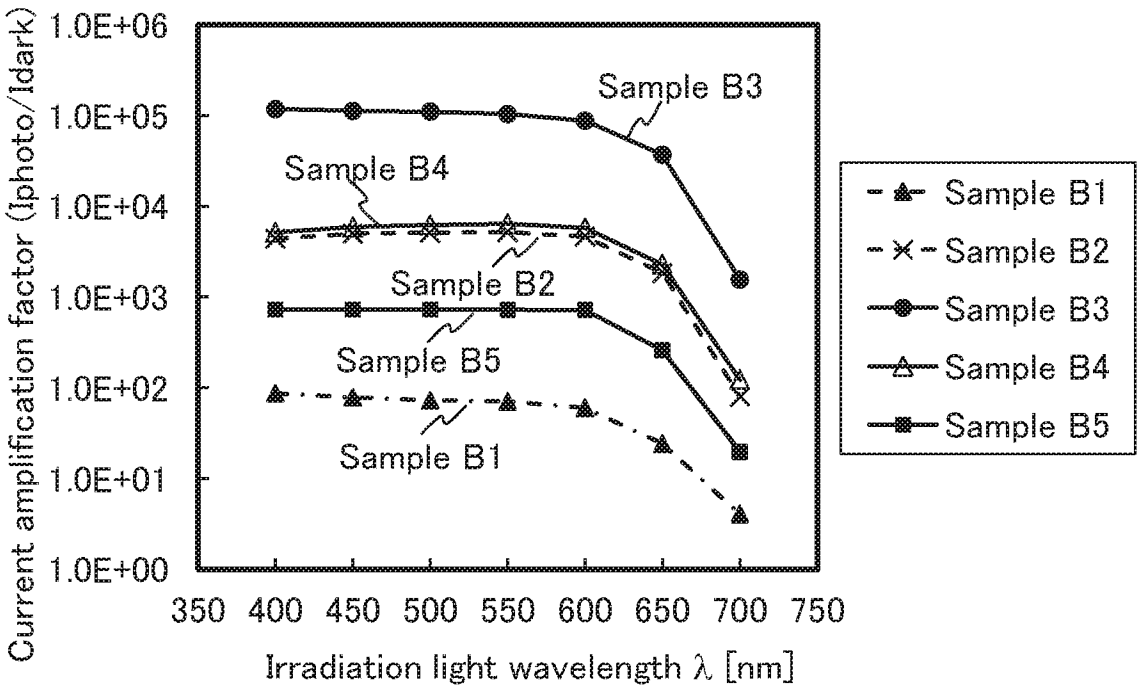

Current amplification factor (Iphoto/Idark)
1.0E+06
1.0E+05
1.0E+04
1.0E+03
1.0E+02
1.0E+01
1.0E+00
350 400 450 500 550 600 650 700 750
Irradiation light wavelength λ [nm]
Sample B3
Sample B4
Sample B2
Sample B5
Sample B1
Sample B1
Sample B2
Sample B3
Sample B4
Sample B5

FIG. 31A

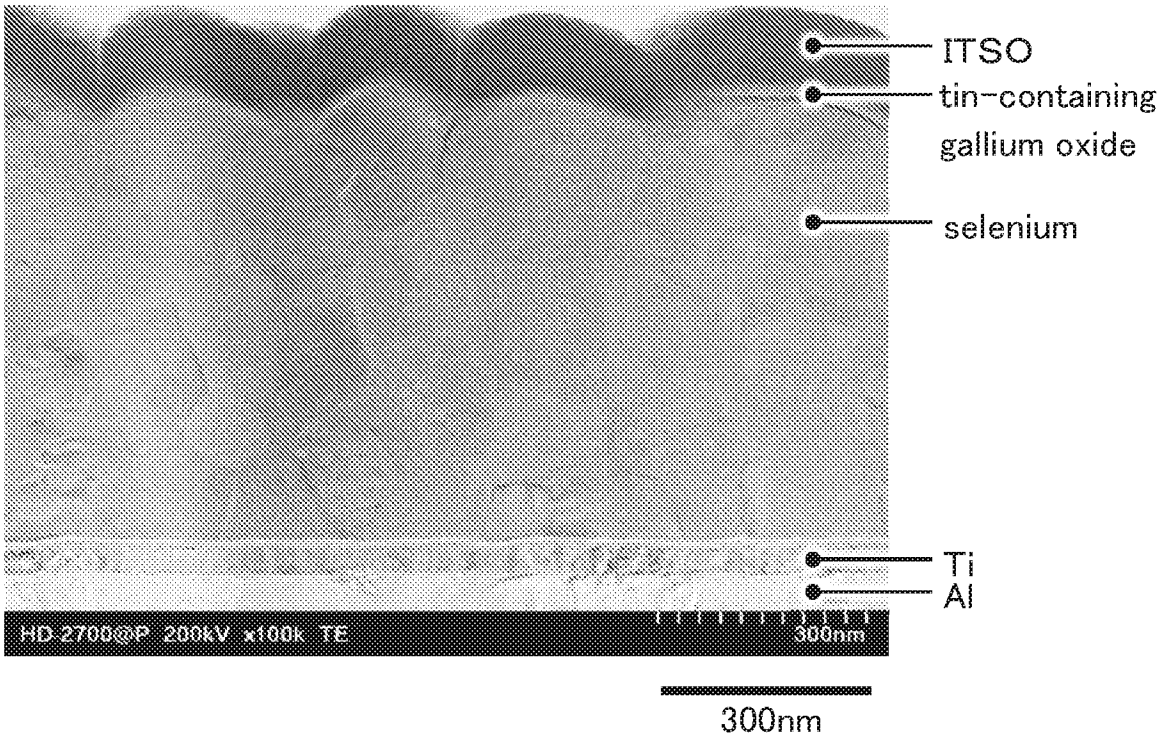


FIG. 31B

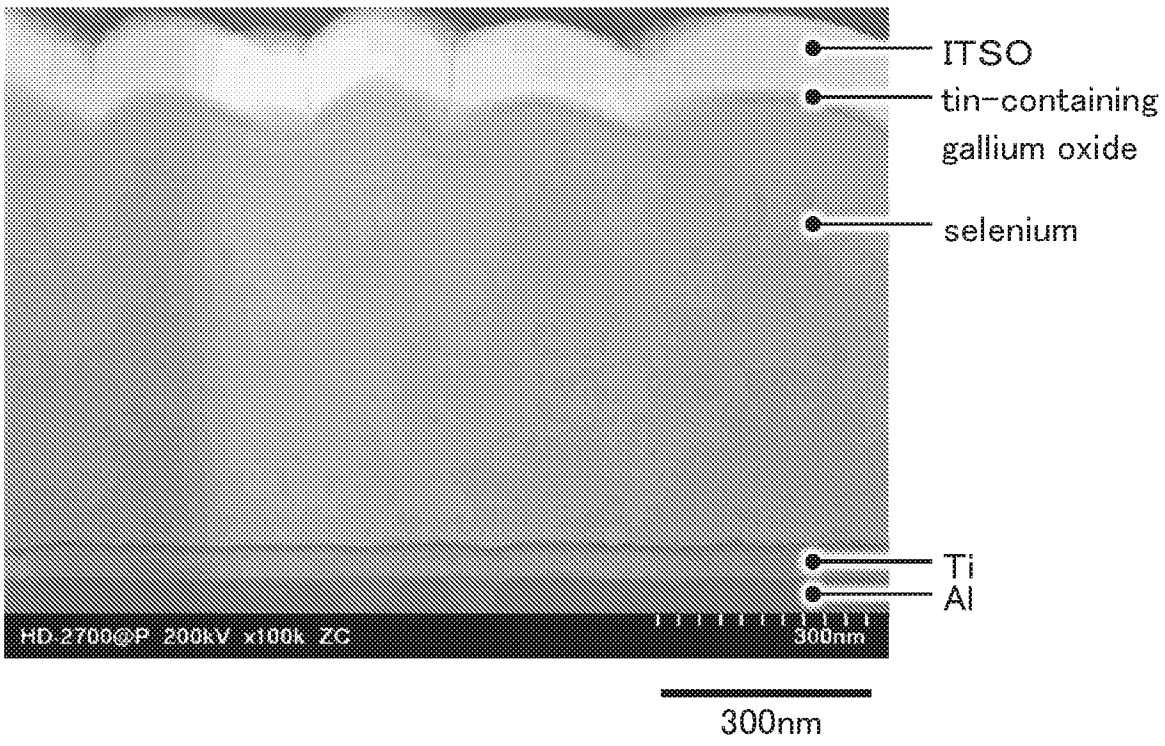


FIG. 32

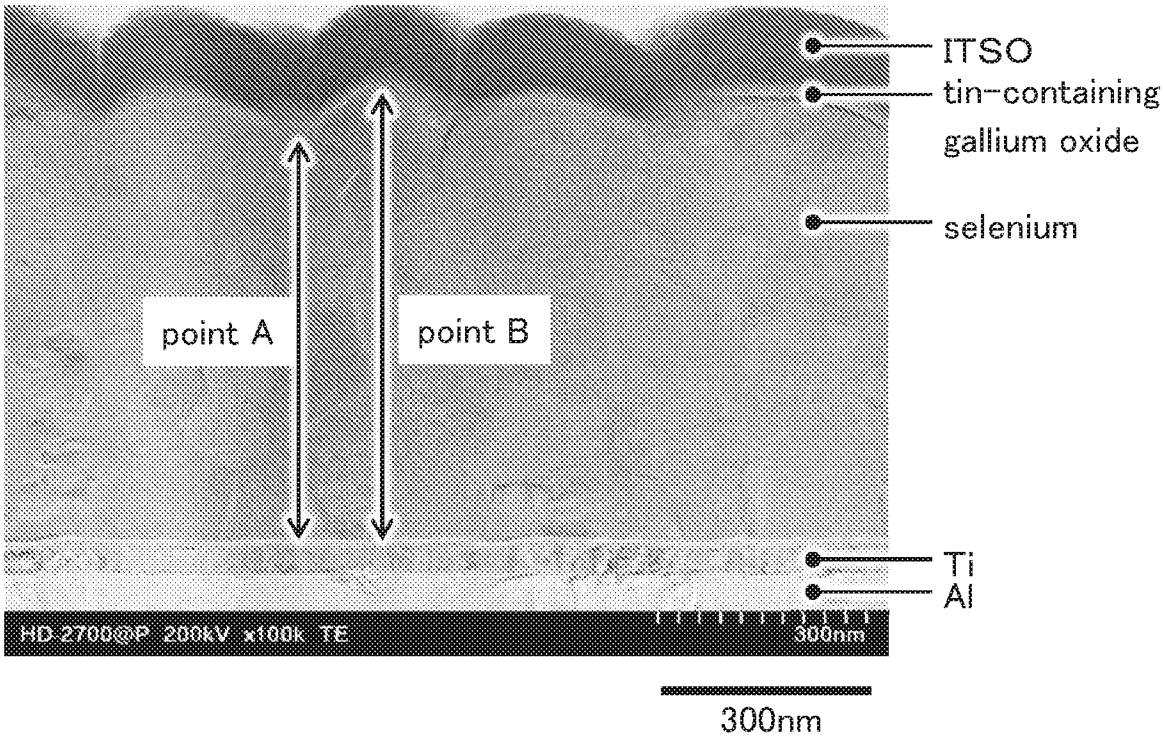

ITSO
tin-containing
gallium oxide
selenium
point A
point B
Ti
Al
HD 2700@P 200kV ×100k TE
300nm
300nm

FIG. 33A

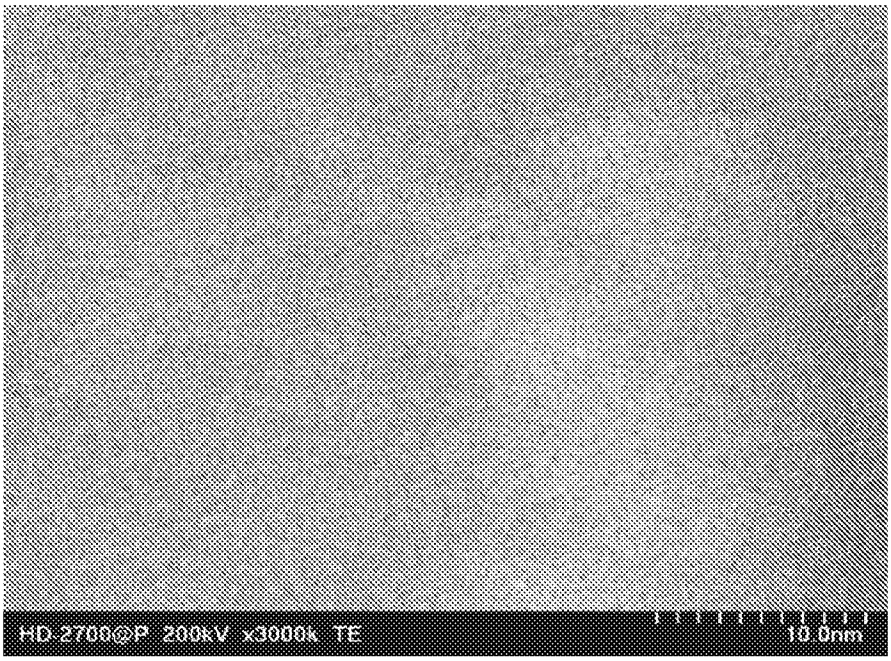


FIG. 33B

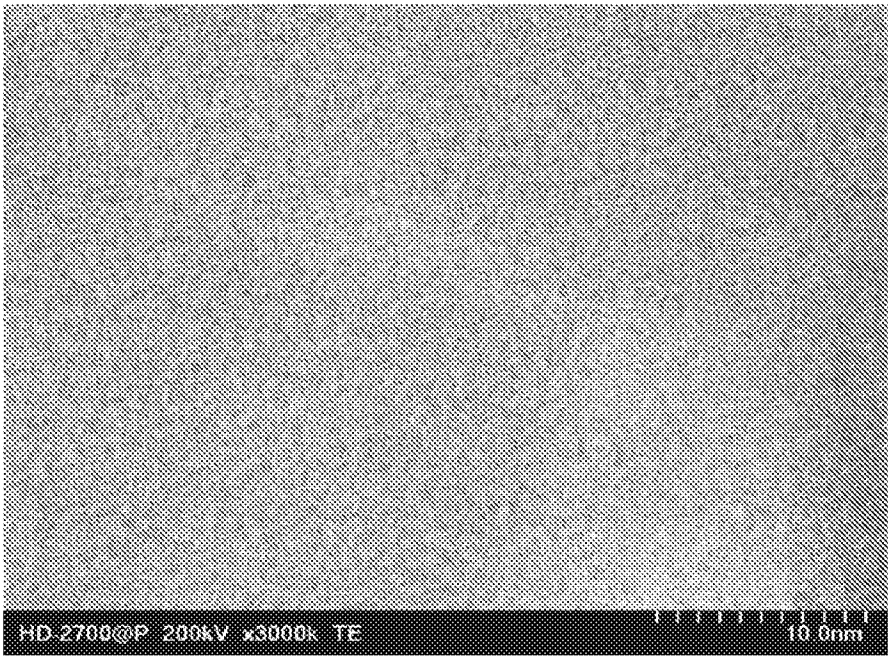


FIG. 34A

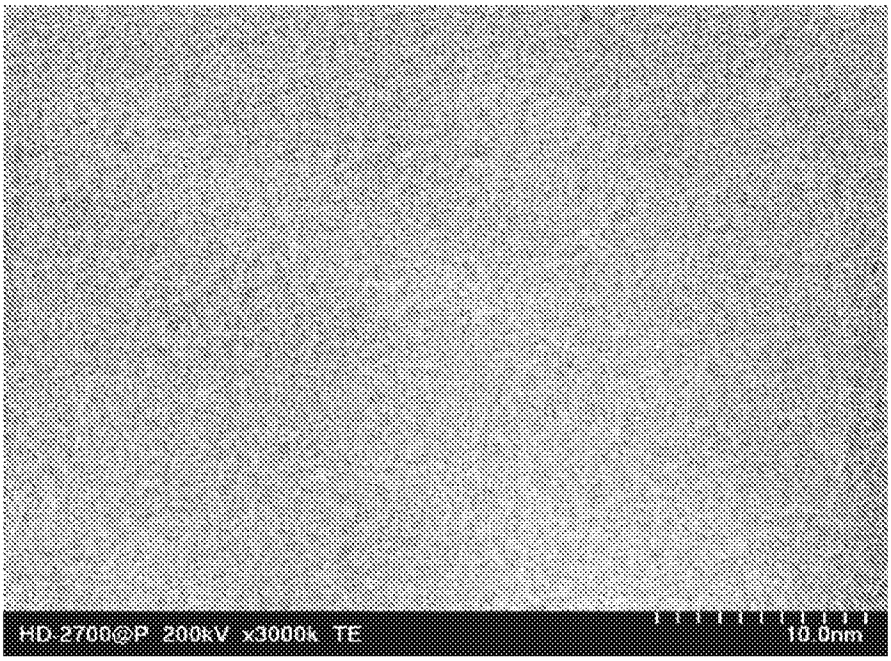


FIG. 34B

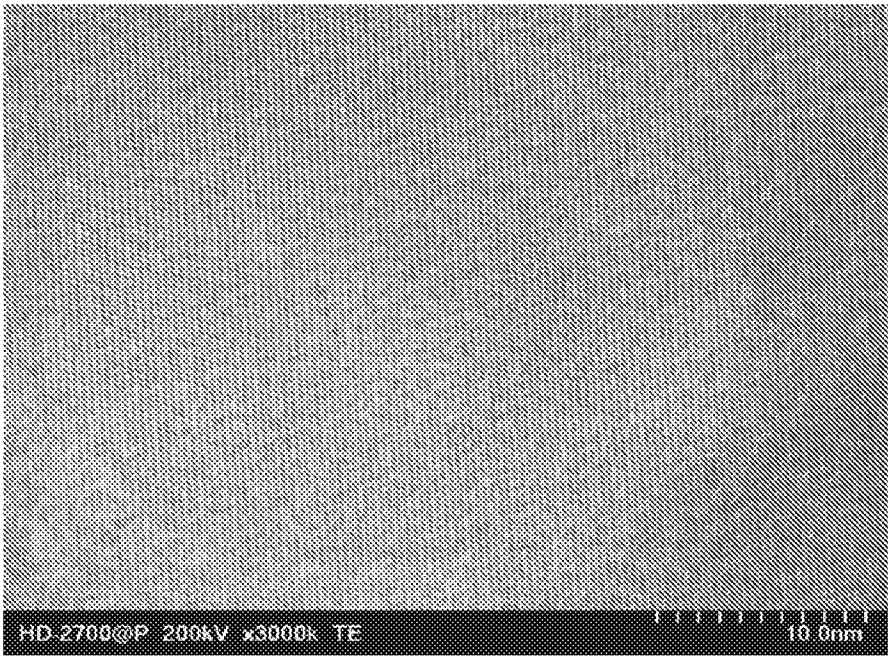


FIG. 35A

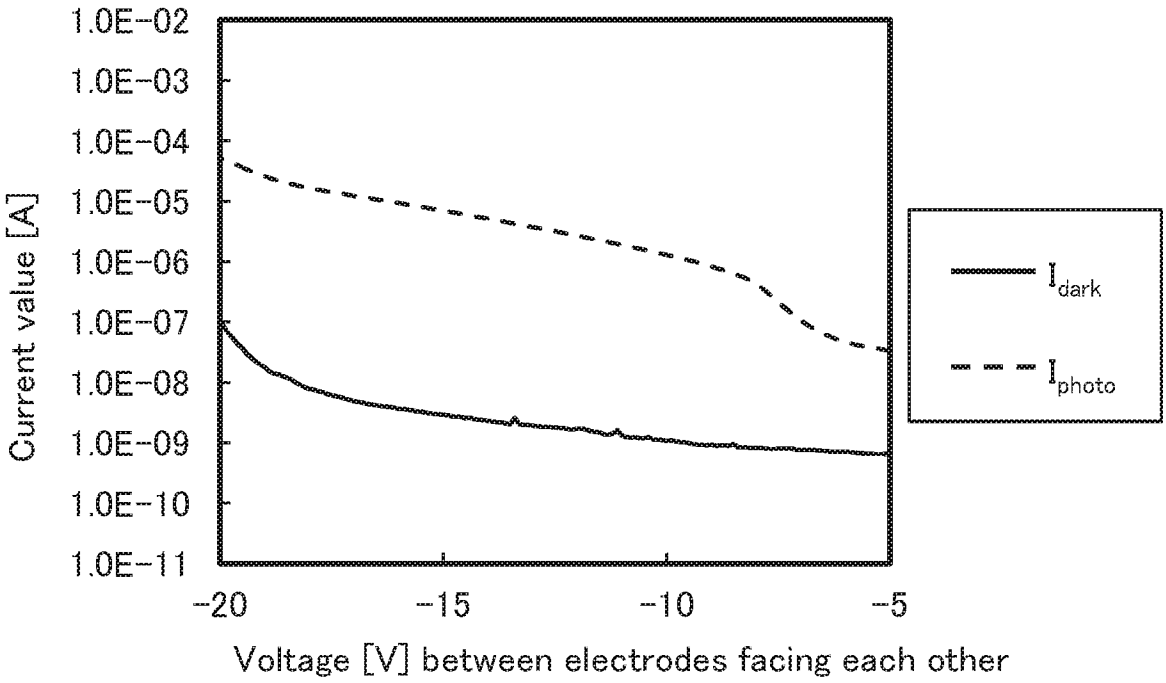


FIG. 35B

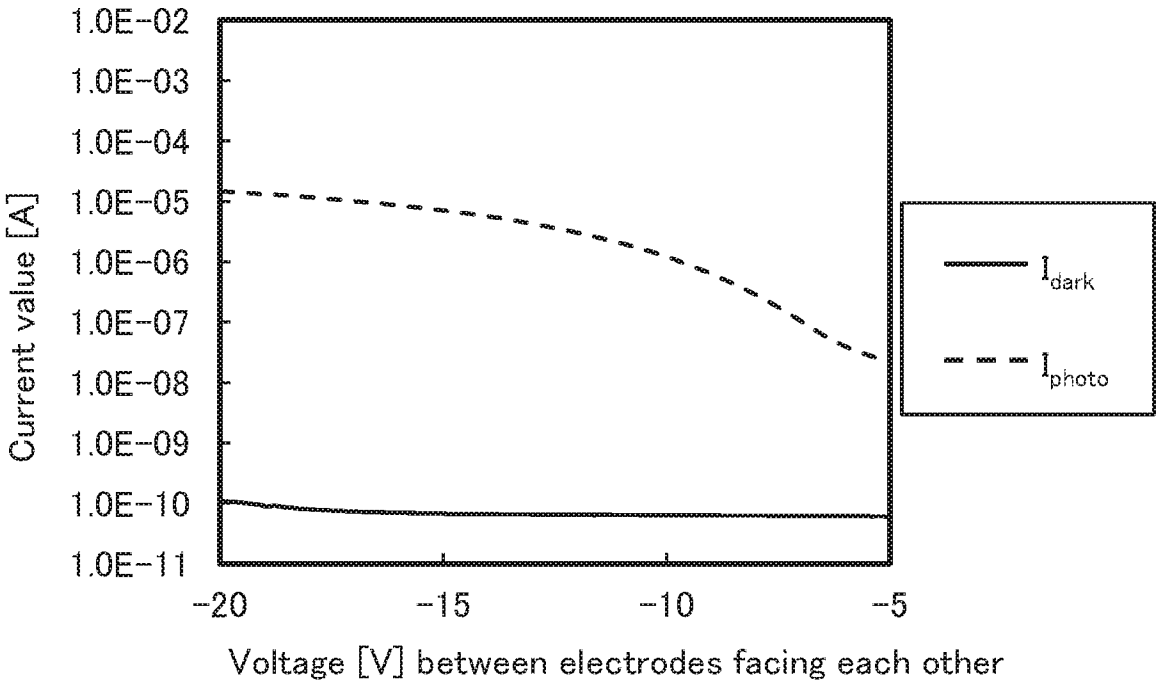


FIG. 36

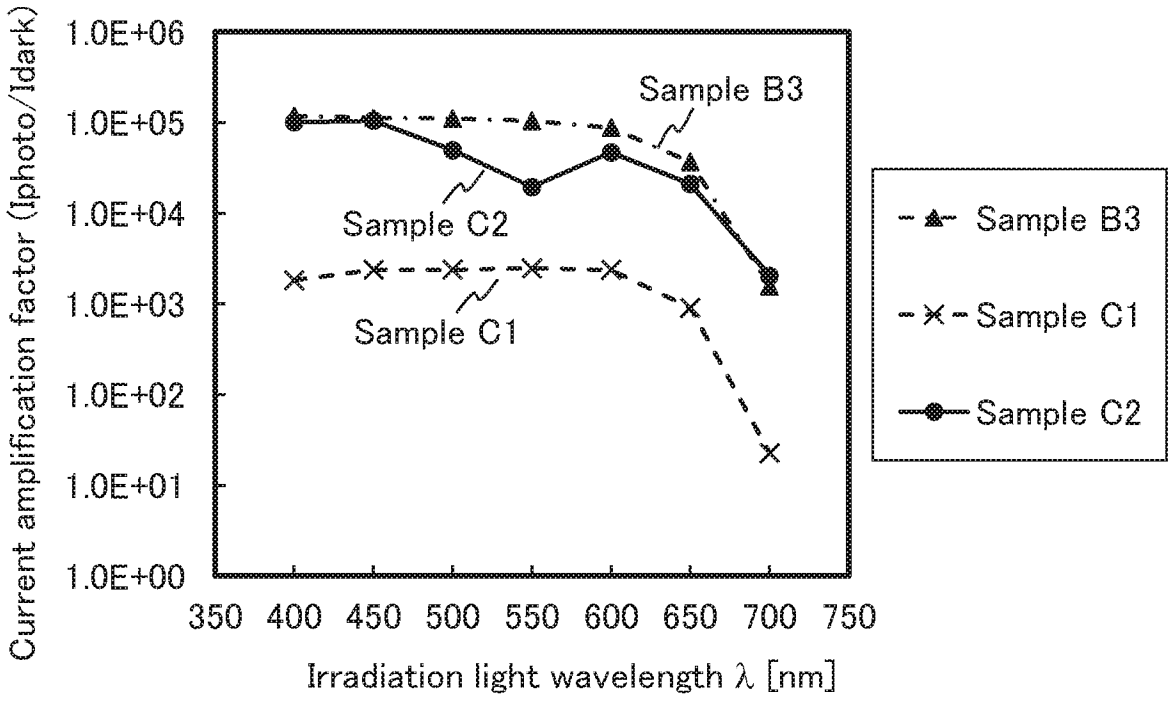

Current amplification factor (Iphoto/Idark)
1.0E+06
1.0E+05
1.0E+04
1.0E+03
1.0E+02
1.0E+01
1.0E+00
350 400 450 500 550 600 650 700 750
Irradiation light wavelength λ [nm]
Sample B3
Sample C2
Sample C1
Sample B3
Sample C1
Sample C2

FIG. 37A

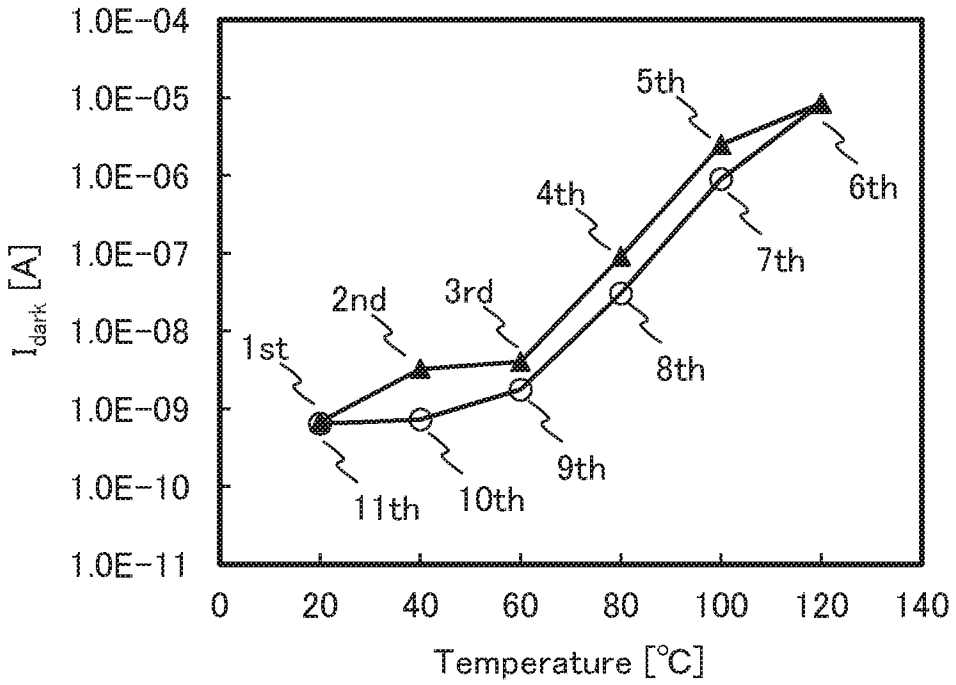


FIG. 37B

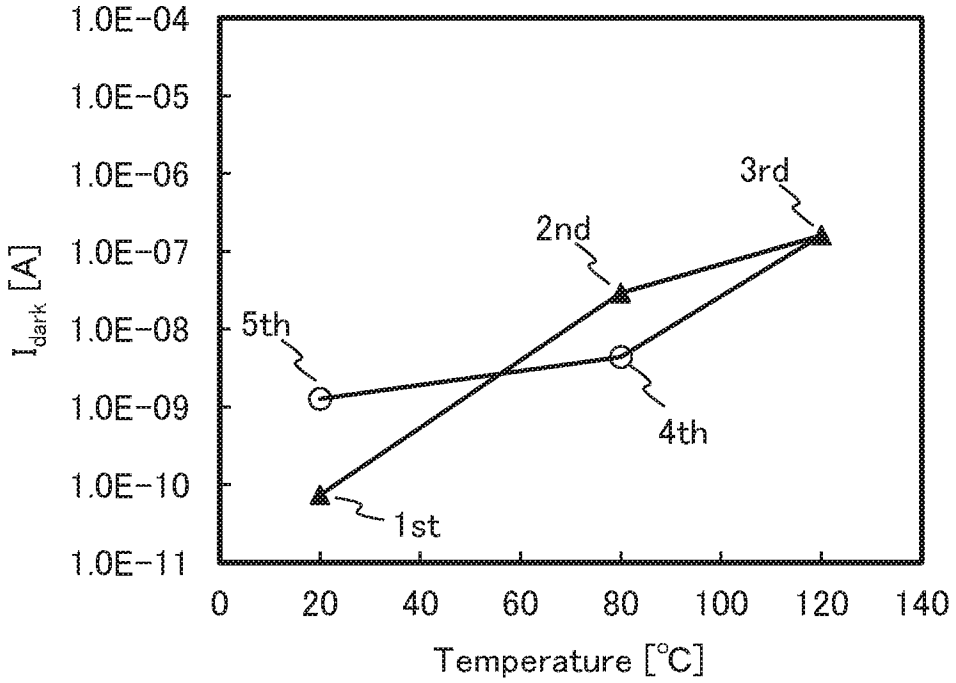


FIG. 38A

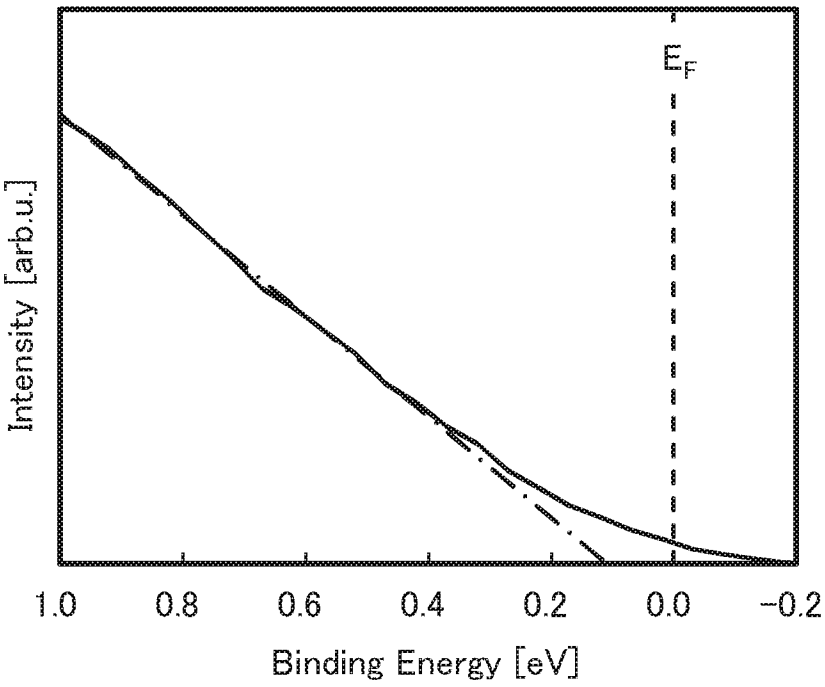
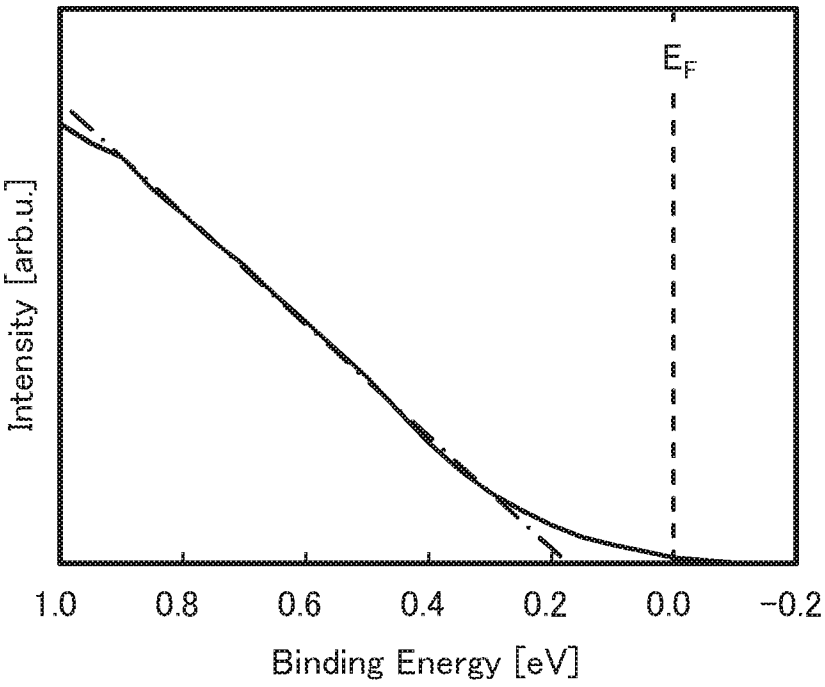


FIG. 38B



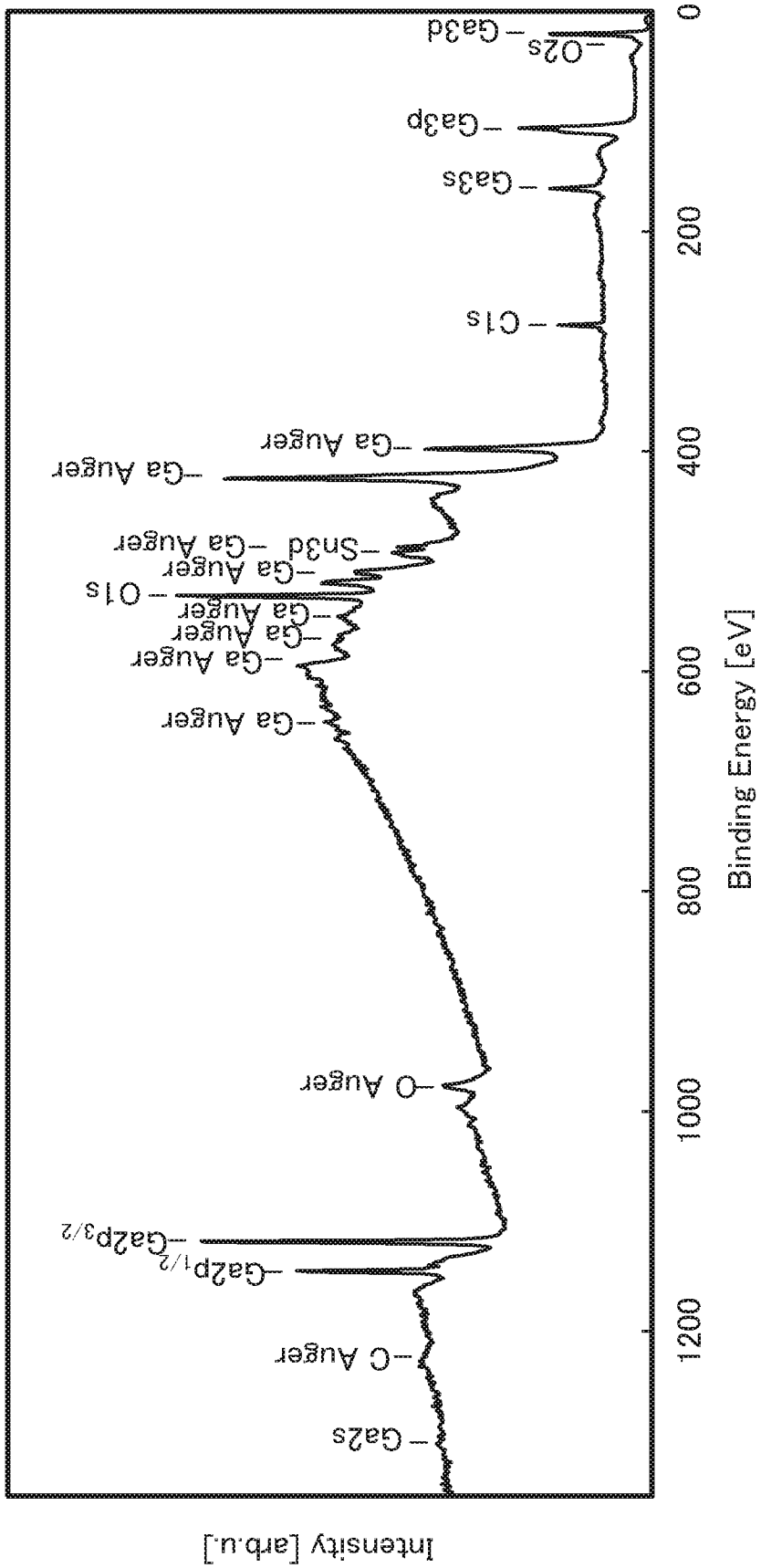

Intensity [arb.u.]
Binding Energy [eV]
0
200
400
600
800
1000
1200
Ga2s
C Auger
Ga2p1/2
Ga2p3/2
O Auger
Ga Auger
Ga Auger
Ga Auger
Ga Auger
Ga Auger
O1s
Ga Auger
Sn3d
Ga Auger
Ga Auger
C1s
Ga3s
Ga3p
O2s
Ga3d

FIG. 39

FIG. 40A

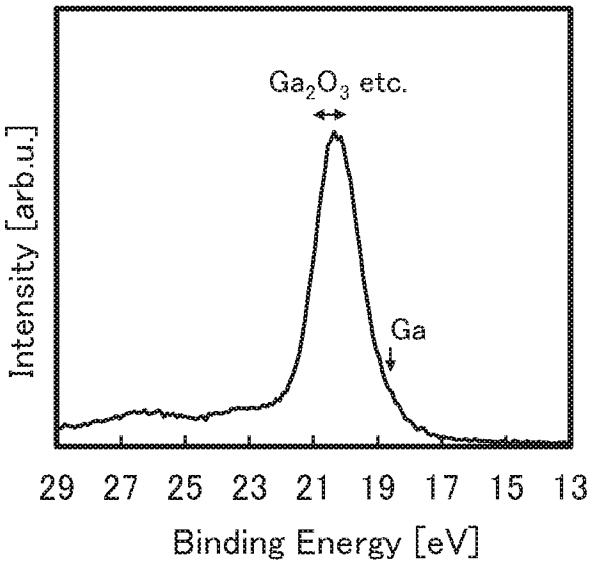


FIG. 40B

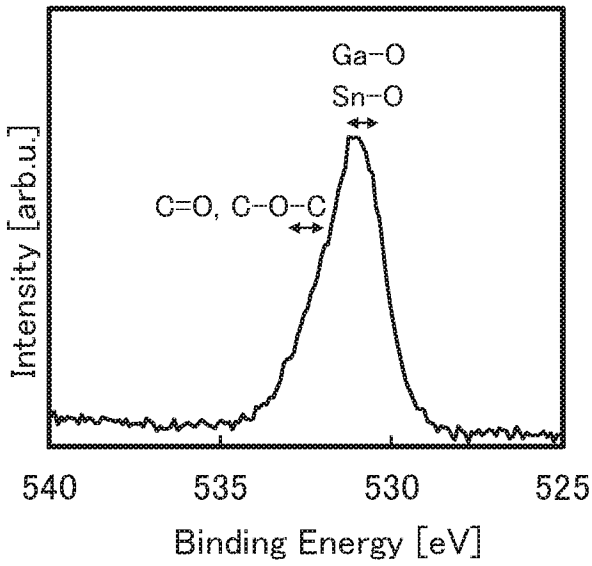


FIG. 40C

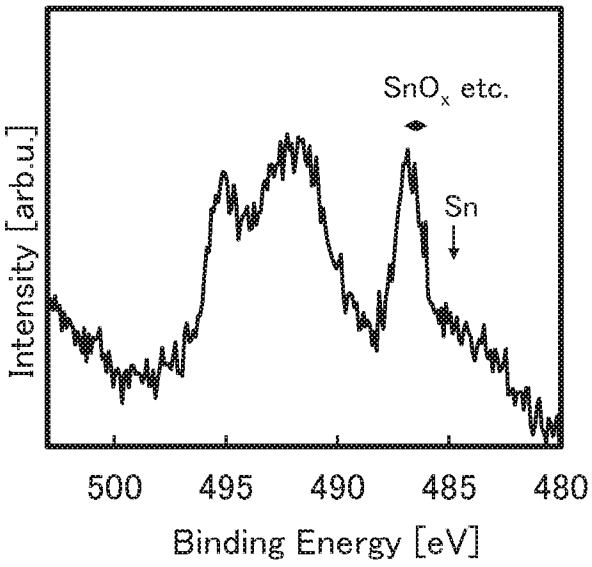


FIG. 40D

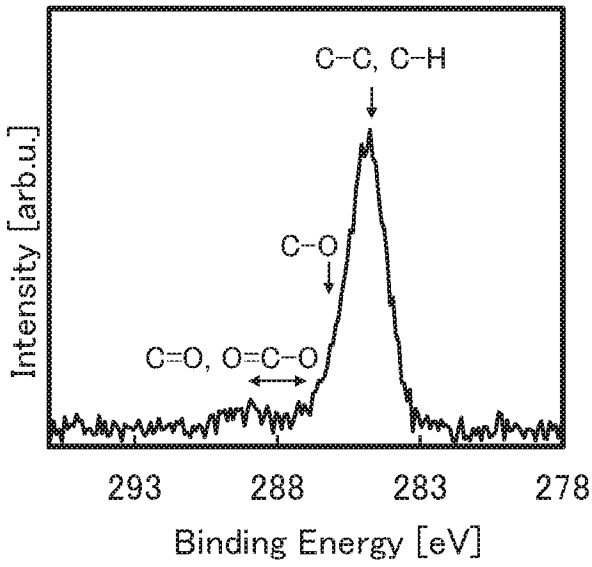


FIG. 41

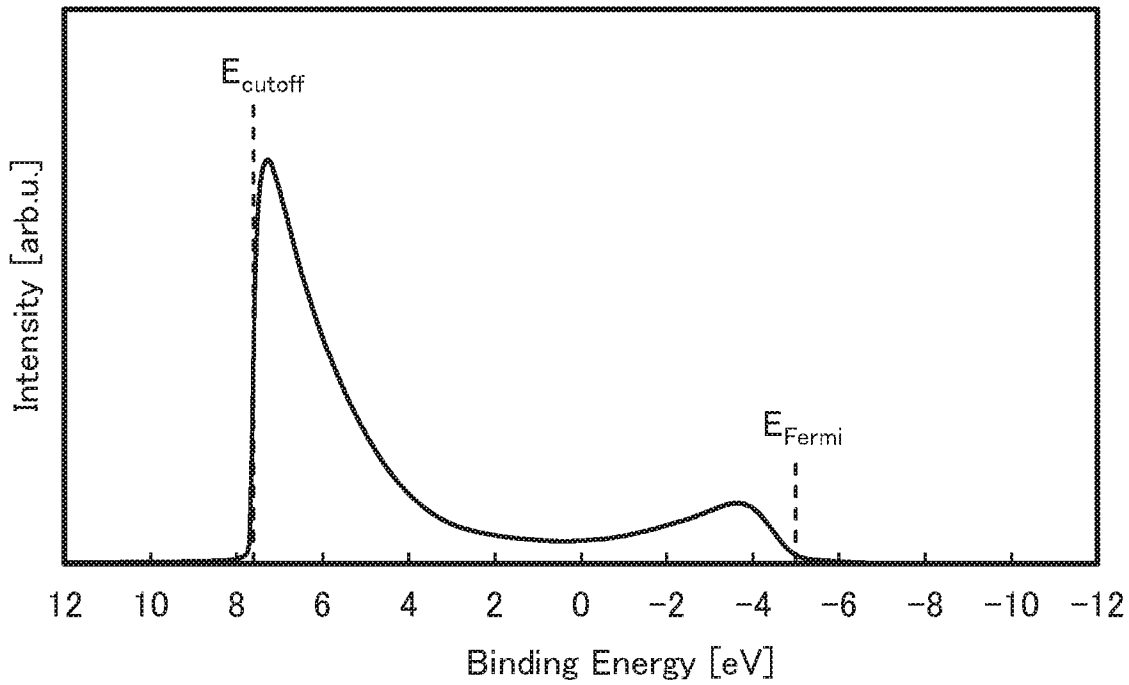

E cutoff
E Fermi
Intensity [arb.u.]
12 10 8 6 4 2 0 −2 −4 −6 −8 −10 −12
Binding Energy [eV]

FIG. 42A

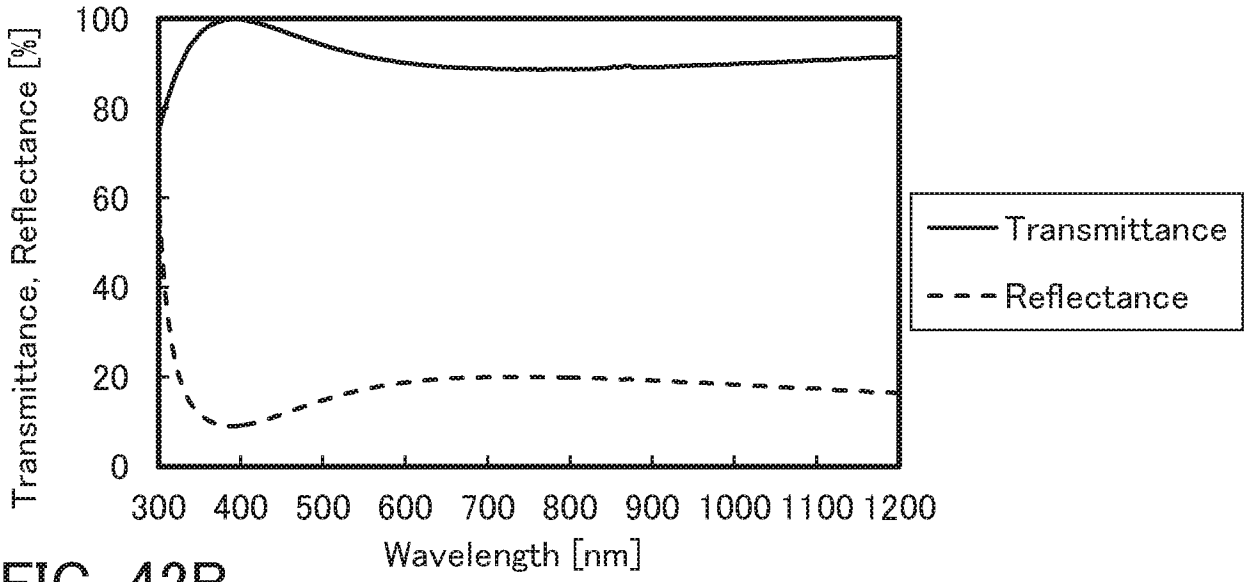


FIG. 42B

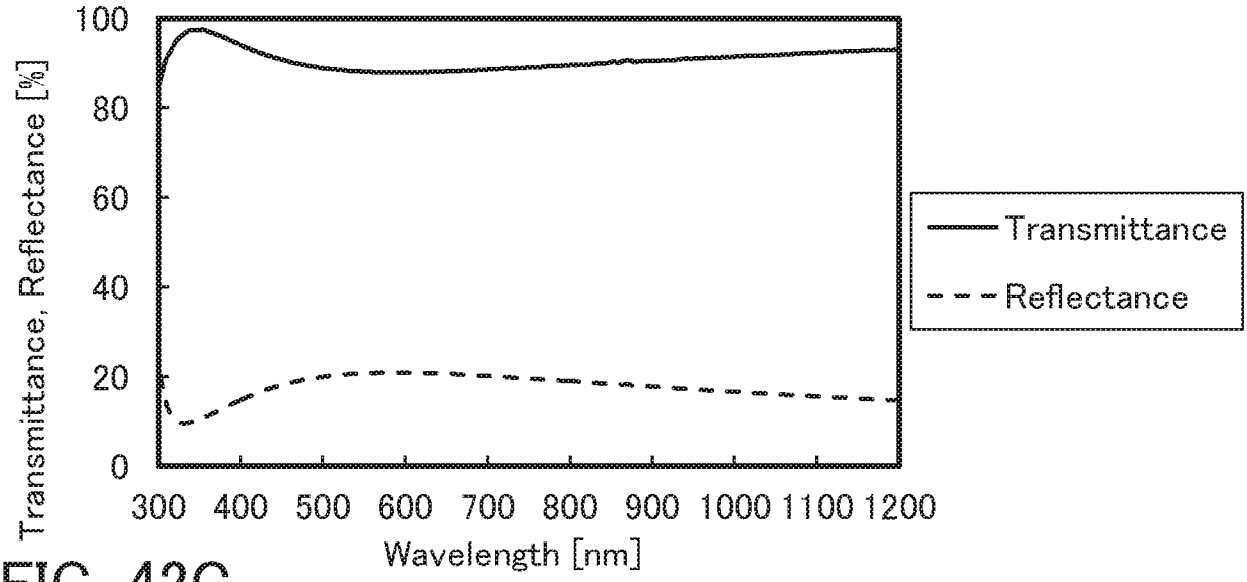


FIG. 42C

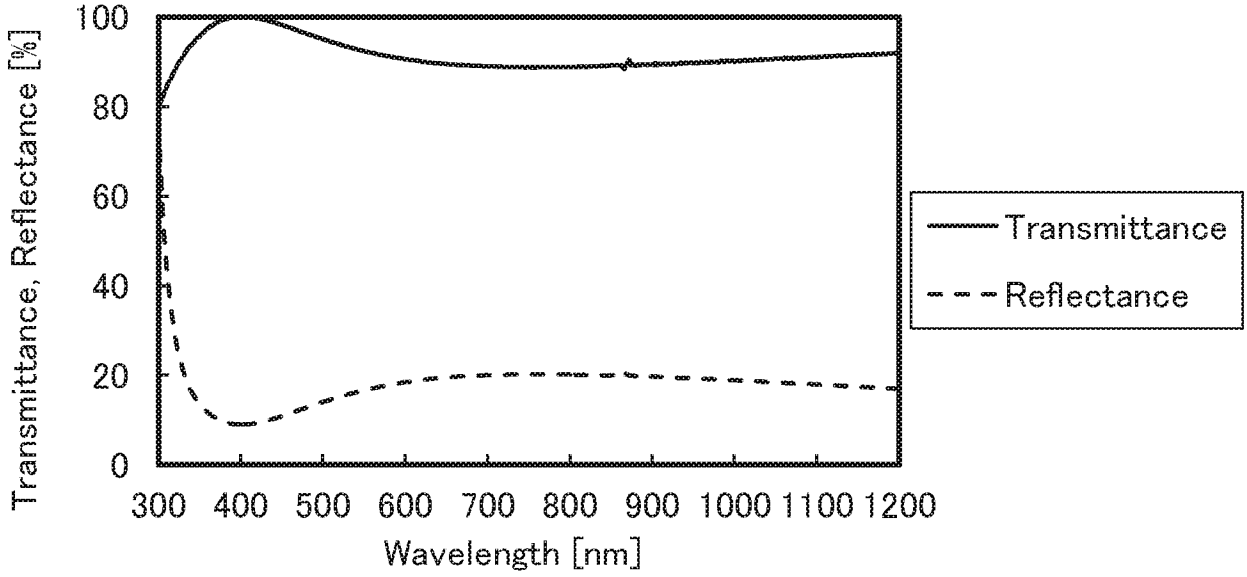


FIG. 43A

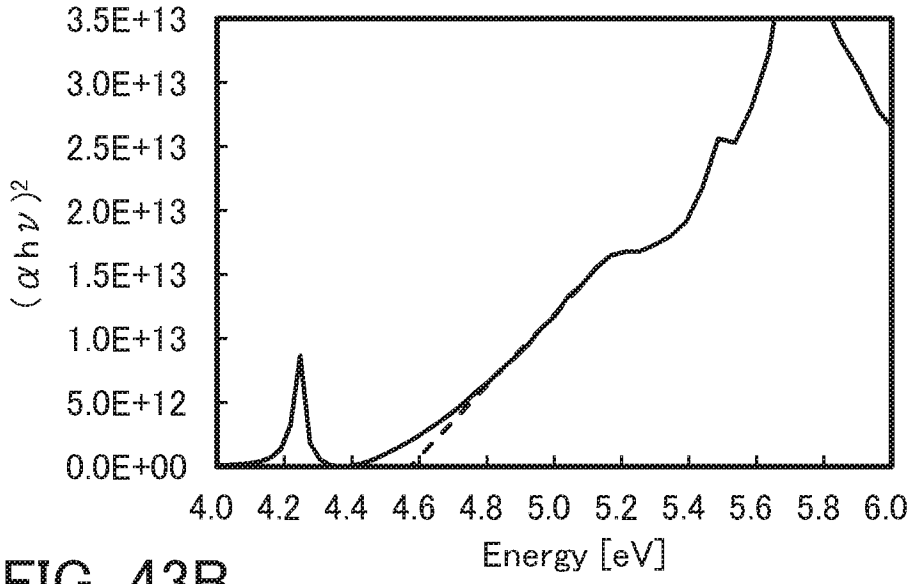


FIG. 43B

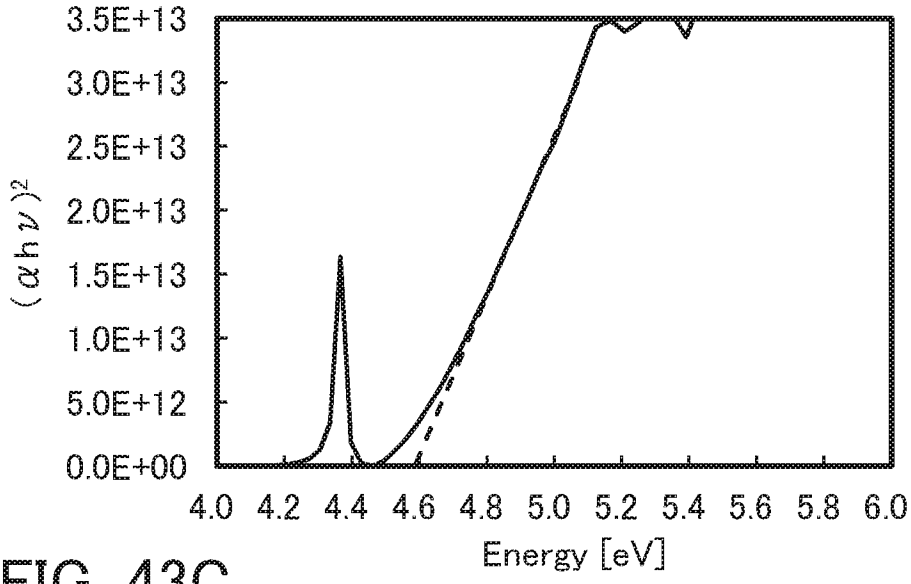


FIG. 43C

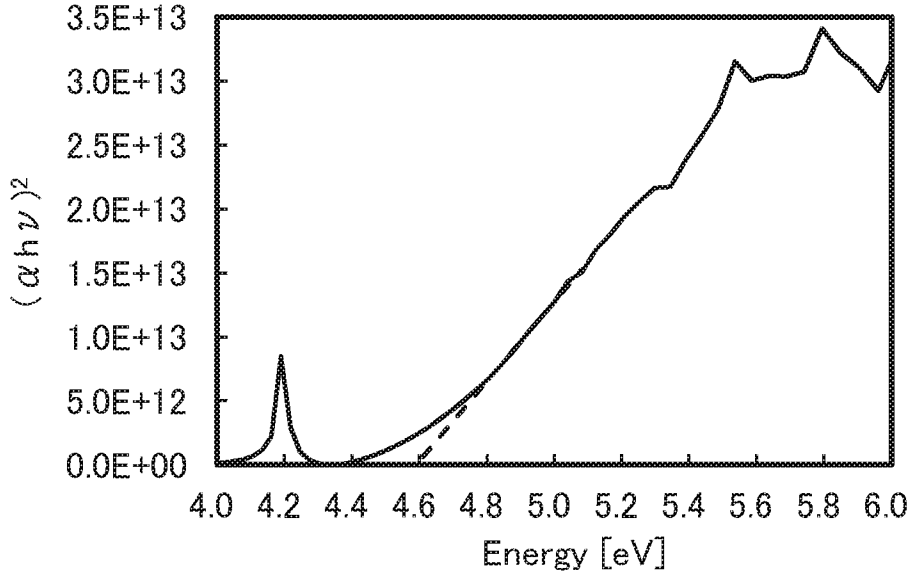


FIG. 44A

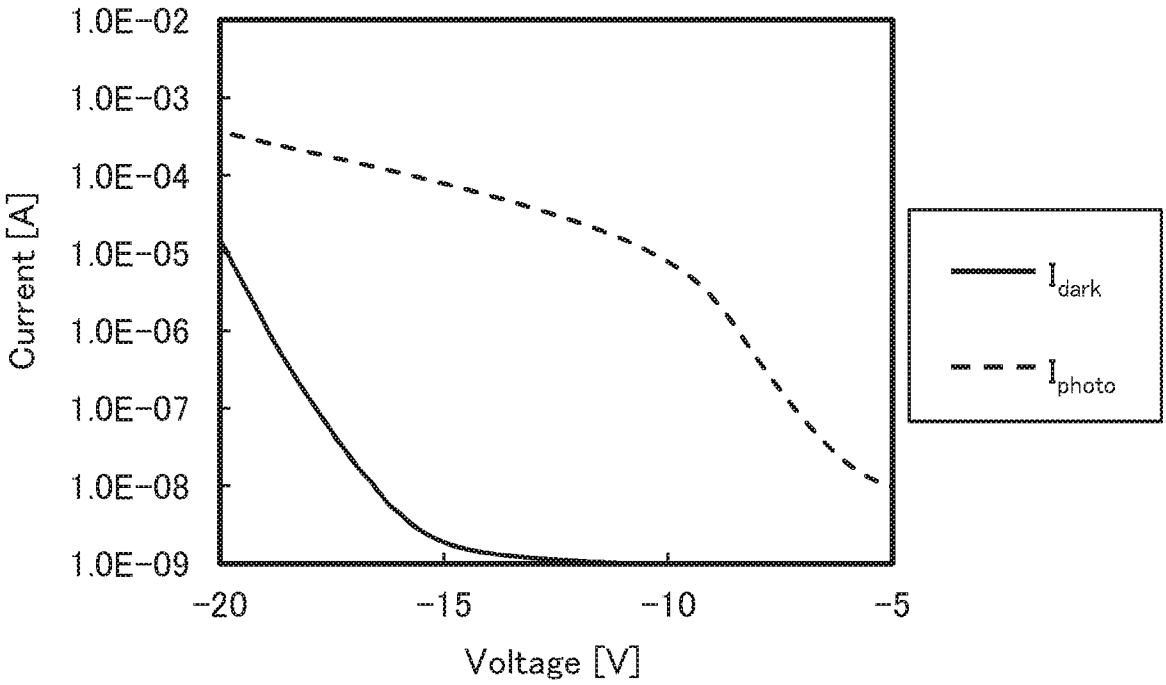


FIG. 44B

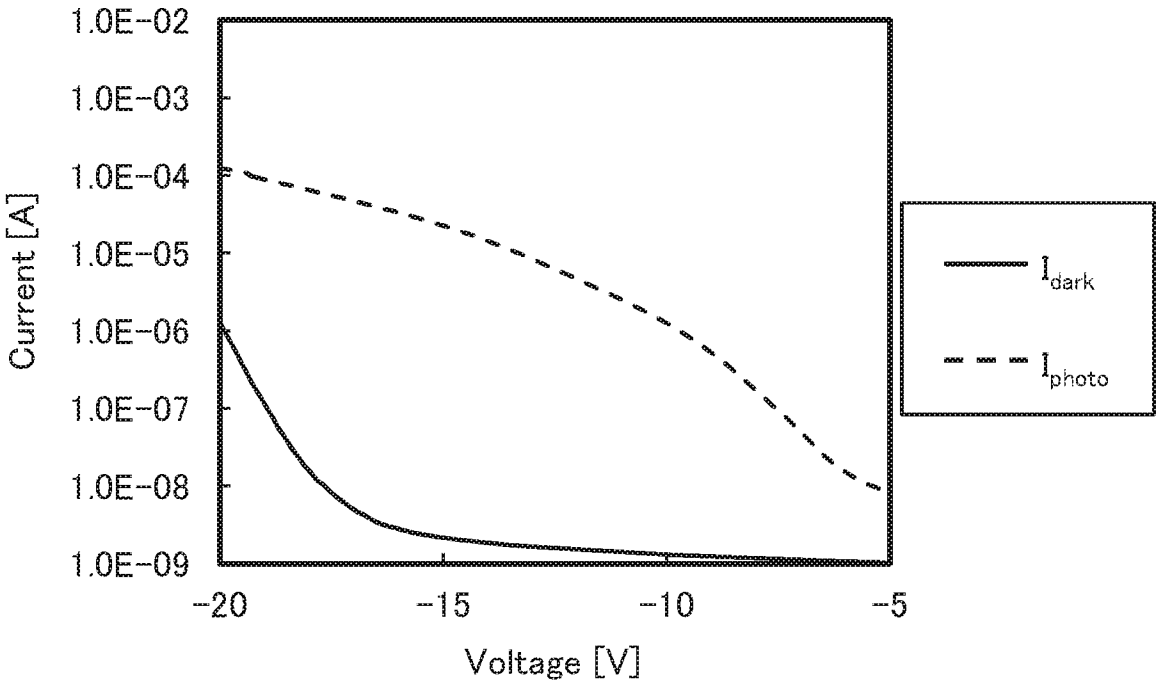


FIG. 45A

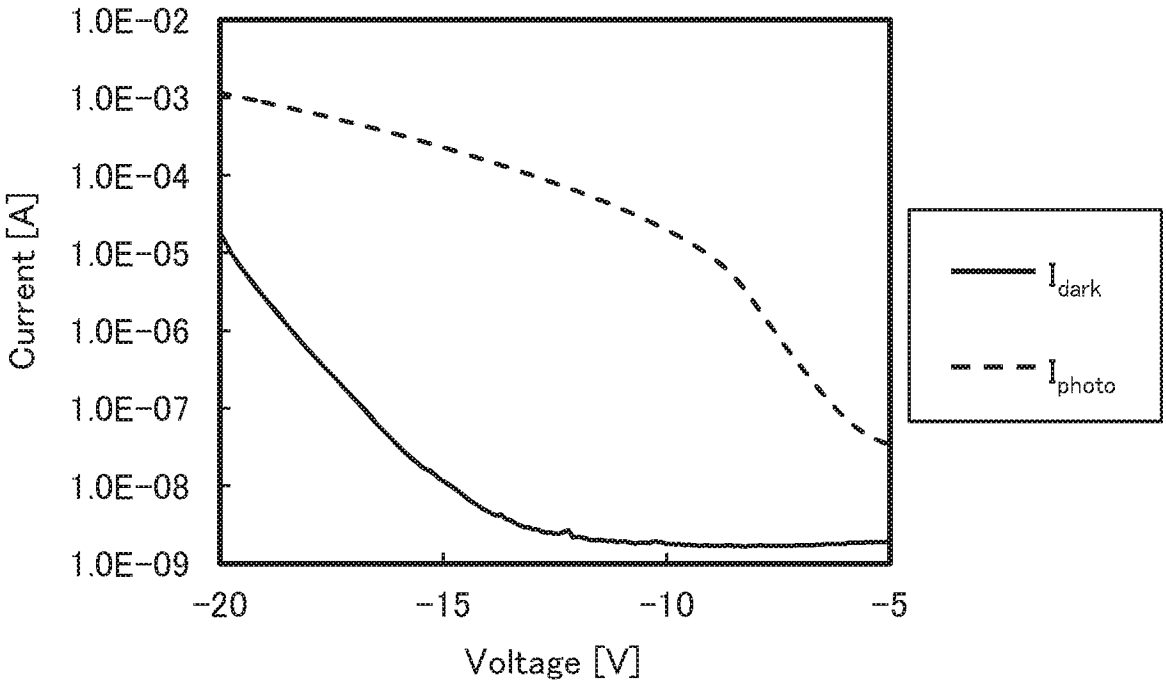


FIG. 45B

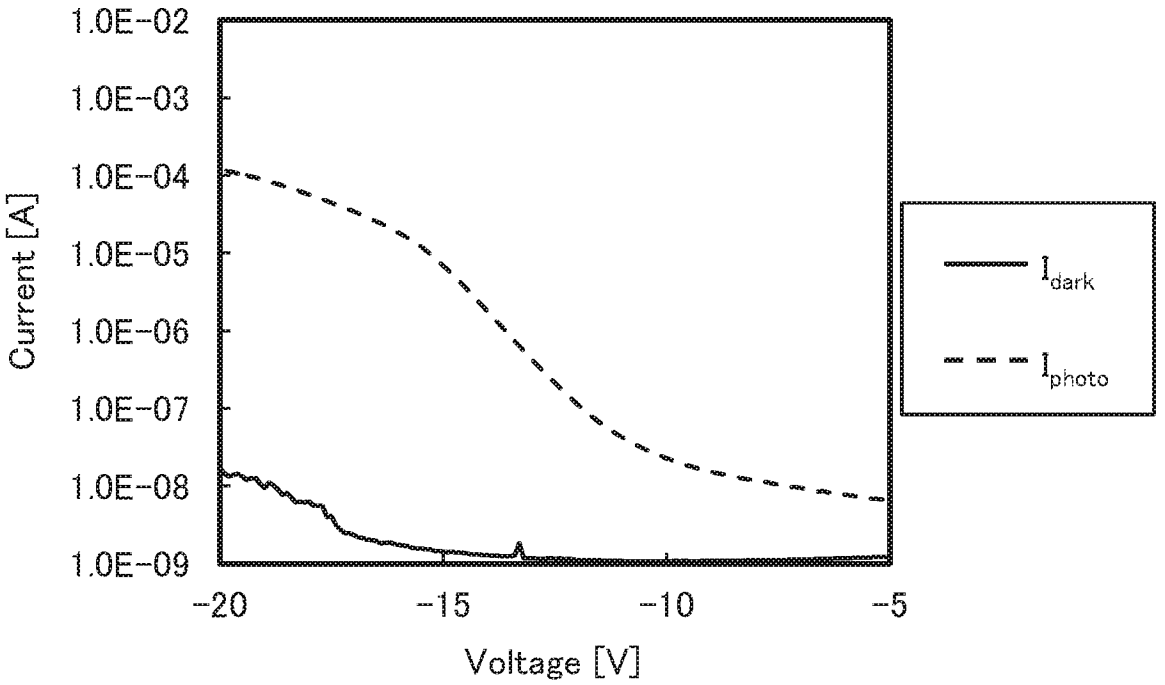


FIG. 46

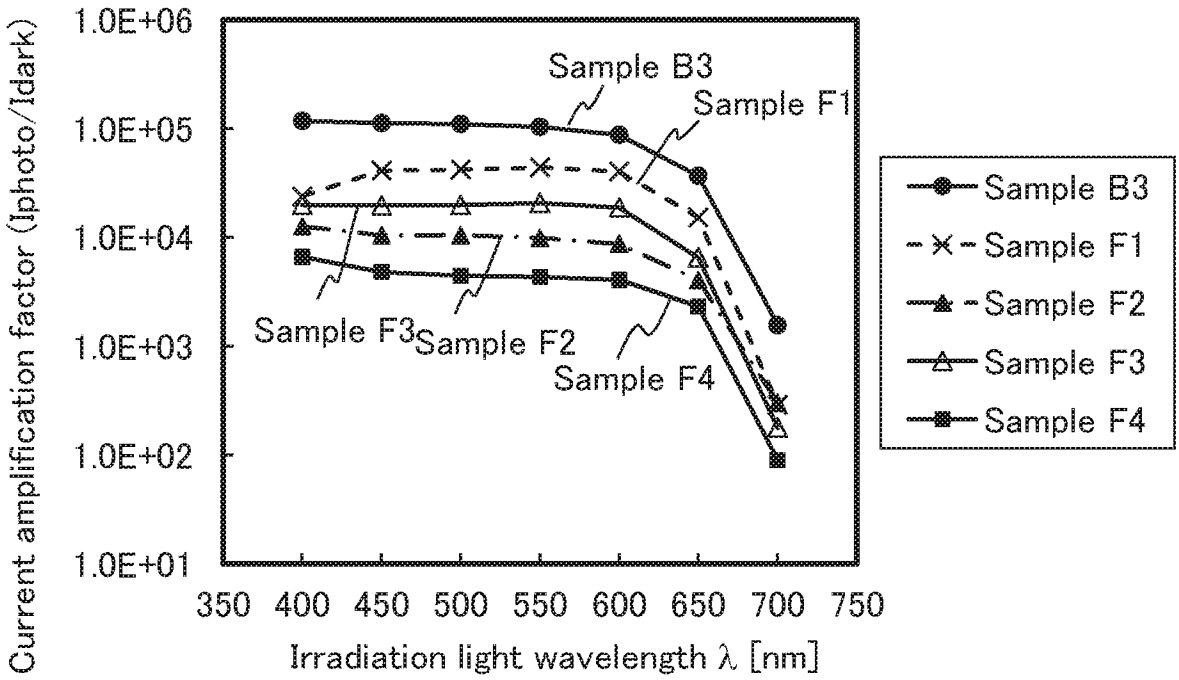

1.0E+06
1.0E+05
1.0E+04
1.0E+03
1.0E+02
1.0E+01
Current amplification factor (Iphoto/Idark)
350 400 450 500 550 600 650 700 750
Irradiation light wavelength λ [nm]
Sample B3
Sample F1
Sample F3
Sample F2
Sample F4
Sample B3
Sample F1
Sample F2
Sample F3
Sample F4

FIG. 47A

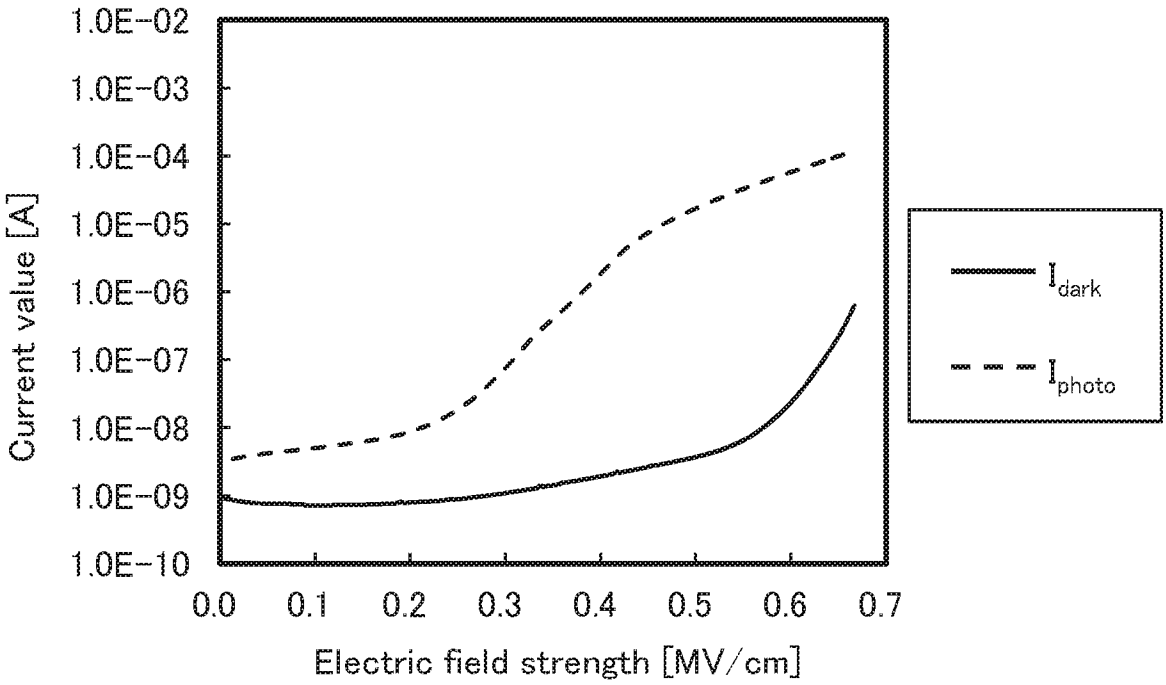


FIG. 47B

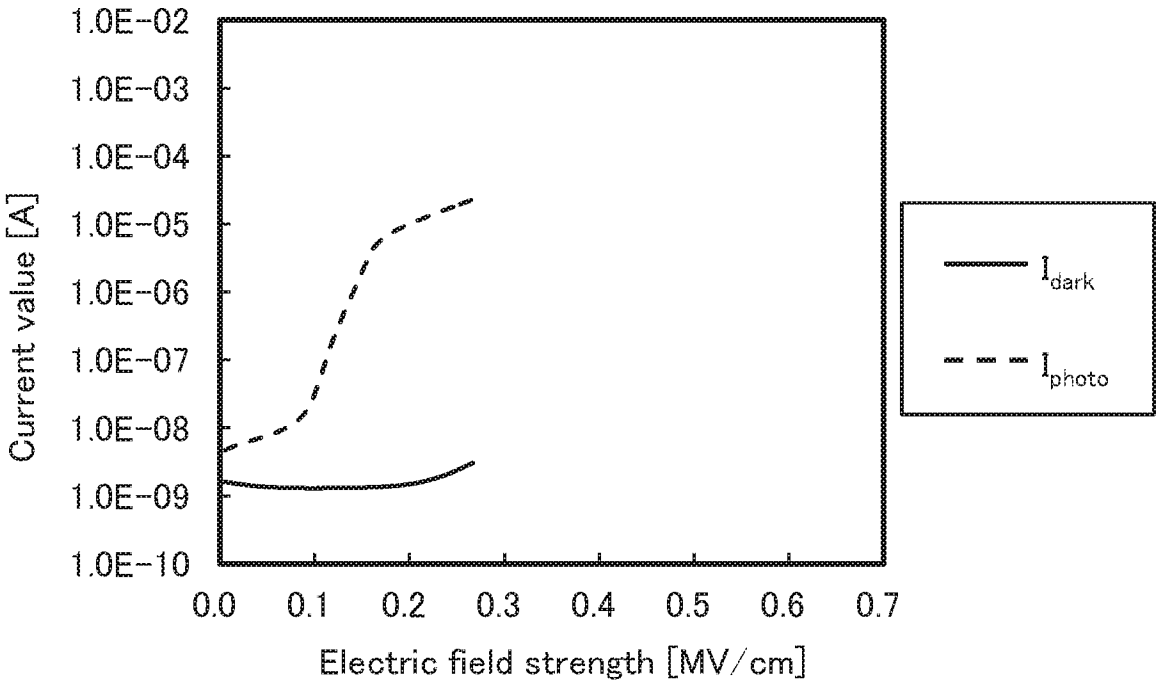


FIG. 48A

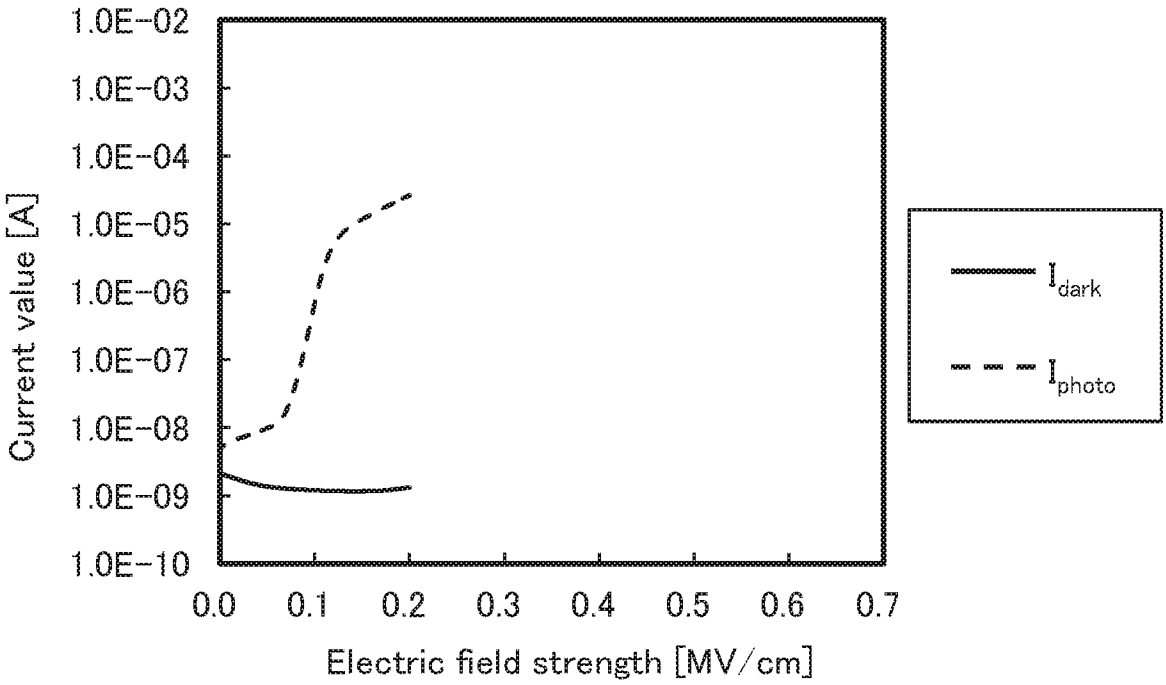


FIG. 48B

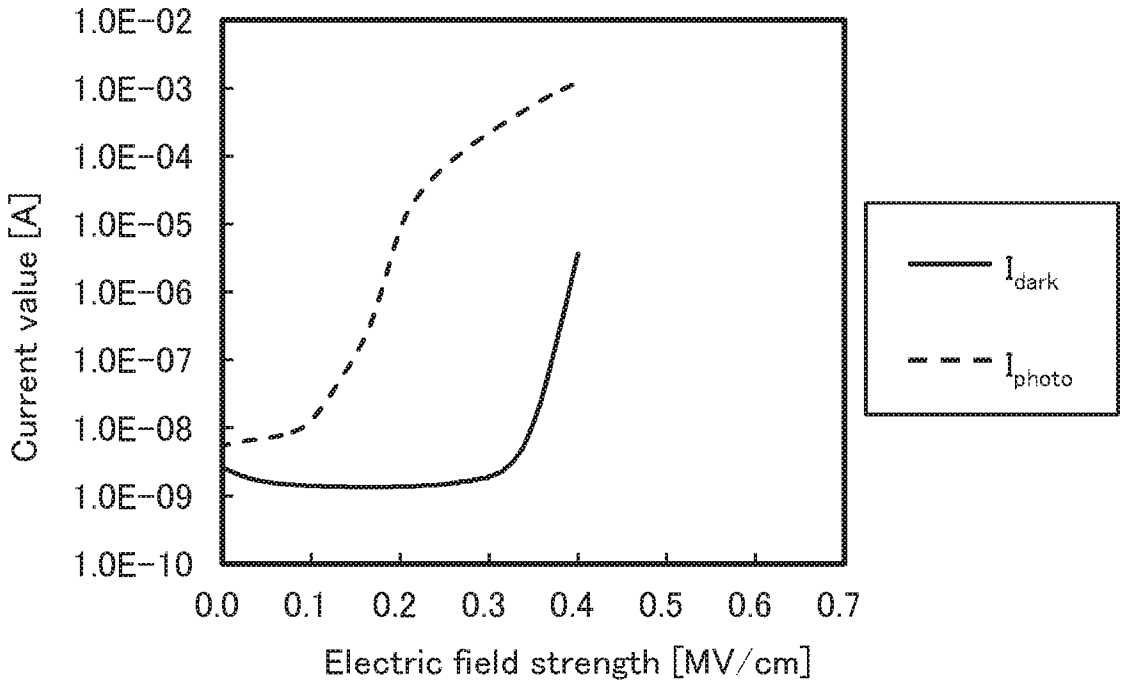
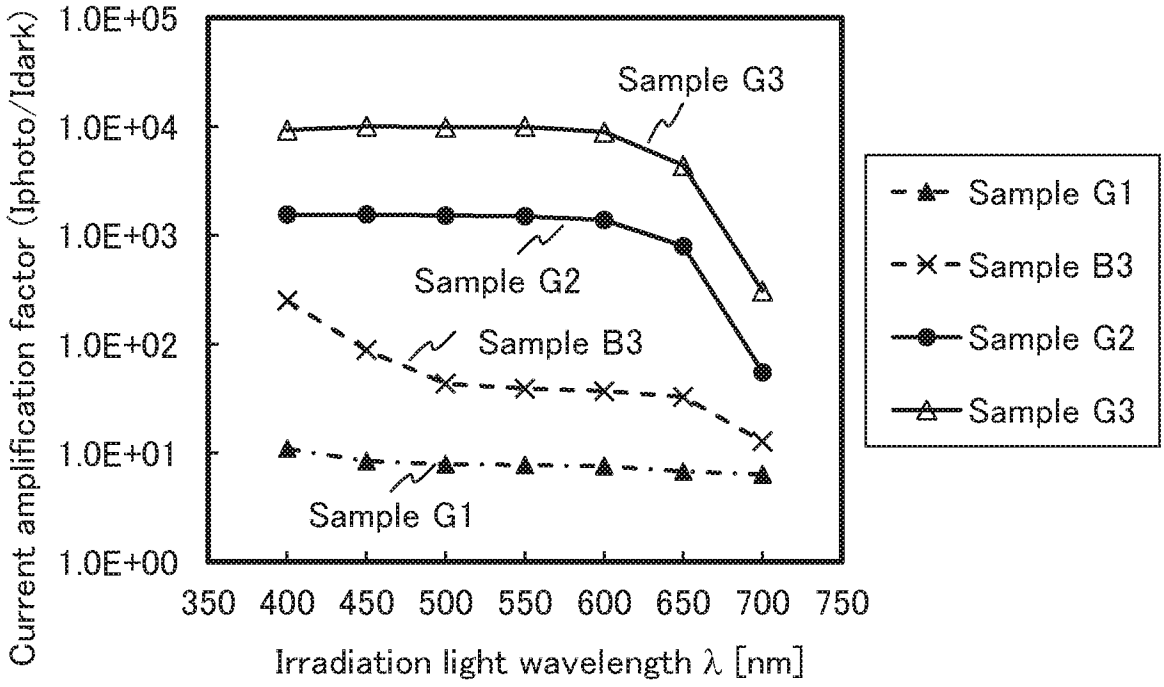


FIG. 49


1.0E+05
1.0E+04
1.0E+03
1.0E+02
1.0E+01
1.0E+00
Current amplification factor (Iphoto/Idark)
350 400 450 500 550 600 650 700 750
Irradiation light wavelength λ [nm]
Sample G3
Sample G2
Sample B3
Sample G1
Sample G1
Sample B3
Sample G2
Sample G3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2018/051594

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L31/107(2006.01)i, H01L21/20(2006.01)i, H01L27/146(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L31/00-31/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2018
Registered utility model specifications of Japan 1996-2018
Published registered utility model applications of Japan 1994-2018

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 2015-99915 A (NIPPON HOSO KYOKAI <NHK>) 2015.05.28, claim 1, paragraphs [0022], [0024], [0026], [0039], [0041], [0058], Fig. 1 (Family: none)	1-3 5-6,9 4,7-8,10-11
Y	US 2015/0255636 A1 (FUJIFILM CORPORATION) 2015.09.10, paragraphs [0060] to [0061] & WO 2014/092001 A1 & CN 104823280 A	5
Y	US 2014/0239156 A1 (FUJIFILM CORPORATION) 2014.08.28, paragraph [0107] & JP 2008-72090 A & JP 2012-19235 A & US 2008/0035965 A1	5
Y	JP 2016-82011 A (NITTO DENKO CORP) 2016.05.16, paragraphs [0031] to [0033] (Family: none)	6

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance
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"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14.05.2018	29.05.2018

Name and mailing address of the ISA/JP	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2018/051594

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010/0210065 A1 (TDK CORPORATION) 2010.08.19, paragraph [0047] & JP 2010-192690 A	9
A	US 2016/0336363 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2016.11.17, & JP 2016-219800 A & KR 10-2016-0134533 A	1-11
A	JP 2017-17191 A (NIPPON HOSO KYOKAI <NHK>) 2017.01.19, (Family: none)	1-11
A	JP 2011-86770 A (IDEMITSU KOSAN CO LTD) 2011.04.28, (Family: none)	1-11
A	JP 2017-45933 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2017.03.02, (Family: none)	1-11