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Image display memory unit.

An image display memory unit having a plurality of display memories (6, 7, 8) connected to a plurality of data lines of data bus (3) one for each display memory chip and addressable for each bit of the data bus comprises a display memory chip selection circuit (13) for selecting the display memory chip for each data bit on the same address, and a write control circuit (16, 17, 18) for controlling writing for each display memory. The dot-by-dot coloring is attained only by a software processing of controlling write information for each display memory and selecting the display memory chip.

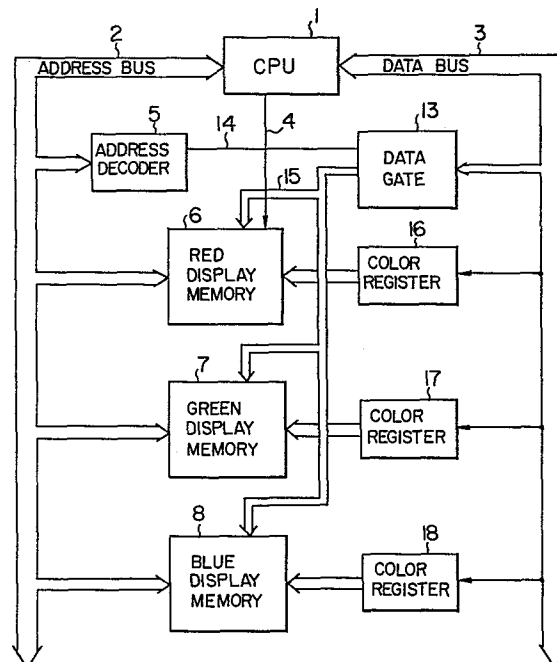


IMAGE DISPLAY MEMORY UNIT

1 The present invention relates to an image display
device capable of displaying color image at a high re-
solution.

 As an apparatus for reading out data written
5 in a display memory of a personal computer, for example,
and graphically displaying the data on a display screen
such as a CRT has been populated, higher resolution of
color display is required and it is necessary to color
picture cells dot by dot.

10 Fig. 1 shows a display screen of such a dot-
by-dot coloring display device and a graphic pattern
displayed on the display screen. Fig. 2 diagrammatically
shows contents of data written in three R. G and B display
memories for three principal colors when the graphic
15 pattern shown in Fig. 1 is displayed on the display screen
with dot-by-dot coloring. The dot-by-dot coloring graphic
display is now explained with reference to Figs. 1 and 2.

 The graphic pattern shown in Fig. 1 illustrates
straight lines shown by solid lines $A_1 - A_4$ and crossing
20 straight lines shown by broken lines $B_1 - B_4$, and the
respective lines are colored as shown in Fig. 2.

 In order to display the colored graphic pattern,
it is necessary to write data representing the aggrega-
tion of dots shown by hatched areas into the R, G and B
25 display memories for the three principal colors.

1 In order to write pattern information of the
line A_1 shown in Fig. 1 in the display memories, only
intensity information for red need be written in the cor-
responding display memory because the color designation
5 of the line A_1 is red. In order to write pattern inform-
ation of the line B_1 shown in Fig. 1 in the display
memories, it is necessary to write both intensity inform-
ation for red and intensity information for green into
the corresponding display memories because the color
10 designation of the line B_1 is yellow. When the intensity
information of the line B_1 is written into the red display
memory, the intensity information of the line A_1 has
already been stored therein. Thus, if the line A_1 and
the line B_1 are to be displayed in superimposition, it is
15 necessary to overwrite the intensity information of the
line B_1 without erasing the stored intensity information
of the line A_1 .

Usually, the addresses of the display memory
are assigned n bytes ($n \times 8$ bits) in horizontal line of
20 the display screen shown in Fig. 1 and the addresses are
sequentially increased starting from left top and ending
at right bottom ($0, 1, \dots, n-1, n, n+1, \dots$) as shown
in Fig. 2. In order to attain the dot-by-dot coloring,
any different coloring of 8-bit brightness information
25 of the same address in the display memory is required as
shown in Fig. 2 (for example, at address 0 in Fig. 2).

In such a case, in order to overwrite the in-
tensity information of the line B_1 on the intensity

1 information of the line A_1 at the same 8-bit address, it
is necessary to logically OR the intensity information
of the line A_1 already stored and the intensity information
of the line B_1 to be newly written and write the
5 ORed intensity information into the display memory.

Fig. 3 shows a block diagram of a display
memory unit having three R, G and B display memories for
attaining the dot-by-dot coloring. In Fig. 3, numeral 1
denotes a CPU, numeral 2 denotes an address bus, numeral
10 3 denotes a data bus, numeral 4 denotes a read/write
selection signal line, numeral 5 denotes an address decoder,
numerals 6, 7 and 8 denote display memories for
three principal colors (R, G and B), numeral 9 denotes
a bilateral buffer, and numerals 10, 11 and 12 denote
15 selection signal lines by which the CPU 1 accesses the
display memories 6, 7 and 8, respectively. Fig. 4 shows
a detailed circuit diagram of the display memory 6 shown
in Fig. 3. The display memories 7 and 8 are similar to
that shown in Fig. 4. In Fig. 4, the display memory 6
20 has the same number of memory positions as the number
of bits of the data bus, that is, eight in the illustrated
example, which are connected to the data bus 3 through
the bilateral buffer 9. The writing of the intensity
information into the display memories in Figs. 3 and 4
25 is now explained.

When the CPU 1 determines that graphic figures
written into the display memory 6 are coloring designations
including "red" of the three principal colors, it

1 addresses the display memory 6 to write the intensity
information of the graphic pattern into the red display
memory 6 and sends a write address to the address bus 2.
The address is decoded by the address decoder 5 so that
5 only the display memory 6 is selected and enabled for
writing by the selection signal 10. Since the read/write
selection signal line 4 from the CPU 1 controls the bi-
lateral buffer 9 such that the data is supplied from the
CPU 1 to the display memory, the data is written into
10 only the display memory 6 addressed by the CPU 1 although
the write data is supplied to the display memories 6, 7
and 8. As shown in Fig. 2, the eight bits on the data
bus 3 are written as they are. Similarly, the green and
blue intensity information are written into the green
15 and blue display memories 7 and 8, respectively, when
they are addressed.

In the apparatus which overwrites the new in-
tensity information on the stored intensity information
at the same address, software processing as shown in
20 Fig. 5 is necessary. This processing is carried out for
each address of the display memory. In the prior art
dot-by-dot coloring display memory unit shown in Figs. 3
and 4, one dot of each of the three R, G and B display
memories corresponds to one dot on the display screen.
25 When the graphic pattern is to be overwritten, the ORed
data to be newly written are different among the R, G
and B display memories because the data of the respective
display memories written at the address corresponding to

1 the address on the display screen are different depending
on the color designation. As a result, the three R, G
and B display memories are arranged in different address
spaces as viewed from the CPU and the software processing
5 for writing into the display memory as shown in Fig. 5
must be carried out three times for each writing of one
graphic data. Accordingly, when the graphic pattern is
to be written over the entire display screen, a very
large number of processings and long time are required.

10 It is an object of the present invention to
provide a display memory unit capable of dot-by-dot
coloring, which does not take a long time in the software
processing in writing the graphic data.

In order to achieve the above object, in ac-
15 cordance with the present invention, a display memory
unit having a plurality of display memories connected
to data lines of a data bus one for each display memory
chip and addressable for each bit of the data bus is
provided, and the display memory unit includes display
20 memory chip selection means for selecting the display
memory chip for each data bit on the same address, and
write control means for controlling writing for each
display memory. Thus, the dot-by-dot coloring is at-
tained only by the software processing of controlling
25 the write information for each display memory and selecting
the display memory chip.

The present invention will be apparent from the
following detailed descriptions taken in conjunction with

1 the accompanying drawings, in which:

Fig. 1 shows a front view of a dot-by-dot coloring display screen in an image display device;

Fig. 2 shows a virtual arrangement illustrating
5 a content of a display memory corresponding to the display screen shown in Fig. 1;

Fig. 3 shows a block diagram of a prior art dot-by-dot coloring display memory unit;

Fig. 4 shows a circuit diagram of a peripheral
10 circuit of the display memory 6 shown in Fig. 3;

Fig. 5 shows a flow chart of a write software in the prior art display memory unit;

Fig. 6 shows a block diagram of one embodiment of a display memory unit of the present invention;

15 Fig. 7 shows a circuit diagram of the display memory 6 shown in Fig. 6 and a peripheral circuit thereof;

Fig. 8 shows a flow chart of a write software in the display memory unit of Fig. 6; and

Fig. 9 shows a block diagram of another embodiment of the present invention.
20

The preferred embodiments of the present invention are now explained with reference to Figs. 6 to 9. Fig. 6 shows a block diagram of one embodiment of the display memory unit of the present invention. The like
25 elements to those of the prior art unit shown in Fig. 3 are designated by the like numerals and the explanation thereof is omitted. In Fig. 6, numeral 13 denotes a data gate circuit which gates the data on the data bus 3 by

1 the display memory select signal 14 from the output of
the address decoder 5. Numeral 15 denotes a data bit
selection signal for selecting a data bit of each of
the display memories 6, 7 and 8 by the output of the data
5 gate circuit 13. Numerals 16, 17 and 18 denote color
registers for instructing writing of data into the
display memories 6, 7 and 8, respectively. The output
signals therefrom are supplied to data input terminals
of the respective display memories.

10 In the display memory unit shown in Fig. 6,
the data gate circuit 13 selects the display memory for
each data bit to be written into the display memories
6, 7 and 8. It gates the data on the data bus 3 by the
display memory selection signal 14 and supplies the output
15 signal to the display memories 6, 7 and 8 as the bit
selection signal for the respective display memories. The
color registers 16, 17 and 18 store color information
of the graphic patterns for instructing whether the
graphic data to be displayed are written into the display
20 memories 6, 7 and 8 or not.

Fig. 7 shows a circuit diagram to illustrate
the connection of the display memory 6, the data gate
circuit 13 and the color register 16 shown in Fig. 6.
The peripheral circuits of the display memories 7 and
25 8 are also connected in the same manner. In Fig. 7, the
data gate circuit 13 comprises eight AND circuits and it
supplies the data on the data bus 3 to the memory chips
of the display memories 6, 7 and 8 as the selection

1 signal 15, by the display memory selection signal 14 from
the output of the address decoder 5. The color register
is a one-bit latch and the output signal thereof is
supplied to the display memory 6 as the data entry
5 signal to the display memory 6.

The writing of the data into the display memories in the display memory unit shown in Figs. 6 and 7 is now explained. The CPU 1 designates the colors of the graphic pattern to be displayed by three bits, one for
10 each of R, G and B, and the color information is stored in the color registers 16, 17 and 18.

The intensity information of the graphic pattern to be displayed is then written at the address of the display memories corresponding to the address on the
15 display screen. The address of the display memory is on the address bus 2 and the address decoder 5 produces the display memory selection signal 14 so that the data gate circuit 13 is opened. On the other hand, the intensity information to be written into the display
20 memory is on the data bus 3, and this data is supplied to the display memories 6, 7 and 8 through the data gate circuit 13 as the memory chip selection signal 15. As a result, the writing of the color information of the color register is permitted for the bit of the display
25 memory to which the "1" intensity information data is supplied, and the writing of the data is not permitted for the bit of the display memory to which the "0" data is supplied. Accordingly, as explained above in connection

1 with Fig. 2, when the new data is overwritten on the
recorded data at the same address of the display memory,
the software processing of writing the ORed data of the
recorded data and the new data as is done in the prior
5 art unit is not necessary but only the data to be newly
written need be written into the display memory. The
data is written only for the data bits merely written,
that is, the bits to which "1" information are supplied,
and the data remains unchanged for those bits which have
10 been recorded.

Fig. 8 shows a flow chart of a data write software for the display memory in the present embodiment.
As shown, the new data can be written into the three R, G
and B display memories without erasing the recorded data,
15 only by writing the color information into the color
registers and the intensity information into the display
memories.

In accordance with the present embodiment, the
software processing is significantly reduced to compare
20 with that of the prior art unit in which the results
of the separate logical operations are written into the
three R, G and B display memories. If the color information of the graphic data does not change, the color
information need not be written into the color registers
25 every time because the color information is retained in
the color registers, but it may be written only when the
color information changes. Thus, the software processing
time can be further reduced. As to the hardware, several

1 logic circuits for the color registers and the data gate
are additionally required to compare with the prior
art unit but the bilateral buffer 9 is not necessary be-
cause the contents of the display memories 6, 7 and 8
5 need not be read out in the present embodiment as opposed
to the prior art unit shown in Figs. 3 and 4. Accordingly,
the hardware scale is about the same.

As described hereinabove, according to the
present embodiment, the software processing in the prior
10 art unit in which the separate data are written into the
three R, G and B display memories is not necessary and
only the processing of writing the color information
into the color registers and the collective writing of
the intensity information into the three R, G and B
15 display memories is required. As a result, the software
processing is reduced. In addition, the software proces-
sing of writing the color information and the intensity
information in a prior art so-called semi-color graphic
display in which the pattern is not colored dot-by-dot
20 but the pattern is colored byte by byte (8 bits) by a
pattern memory for storing pattern information and a
color memory for storing color information, can be direct-
ly applied to the present embodiment. This is a great
advantage in developing softwares.

25 Fig. 9 shows a circuit diagram of another em-
bodiment of the present invention, in which the color
register 16 shown in Fig. 7 is replaced by an 8-bit latch
19. In the present embodiment, the color can be

1 designated for each bit of the intensity information
written into the display memory. Thus, the graphic
patterns which display the bits of the selected address
with different colors such as red and blue can be simul-
5 taneously written into the display memories.

In the above embodiments, three display memo-
ries for R, G and B have been shown. It should be
understood that any number of display memories can be
used in the present invention and the same advantage is
10 equally obtained.

As described hereinabove, according to the
present invention, in the dot-by-dot coloring graphic
display, the processing of writing the data separately
to the plurality of display memories to designate the
15 color picture cell by picture cell is not necessary but
only the processing of writing the color information into
the color registers for controlling the writing for each
display memory and writing the intensity information into
the entire display memory to select the display memory
20 chip individually is needed. Therefore, the processing
time is significantly reduced. In addition, the hard-
ware scale of the present invention does not substantial-
ly increase.

C L A I M S

1. An image display memory unit having a CPU (1) and a plurality of display memories (6, 7, 8) connected to a plurality of data lines (3) of said CPU one for each display memory chip and addressable for each bit of said data lines, comprising:

display memory chip selection means (13) for selecting each of the display memory chips connected to the data lines of said CPU; and

display memory write control means (16, 17, 18) for controlling writing for each of said display memories.

2. An image display memory unit according to Claim 1 wherein said display memory write control means controls writing for each bit.

3. An image display memory unit according to Claim 1 wherein said display memory write means controls simultaneous writing of a plurality of bits.

FIG. 1 PRIOR ART

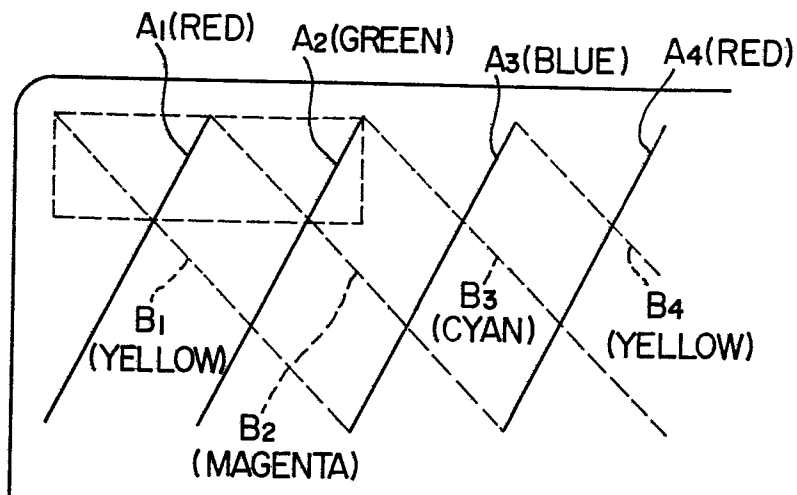


FIG. 2 PRIOR ART

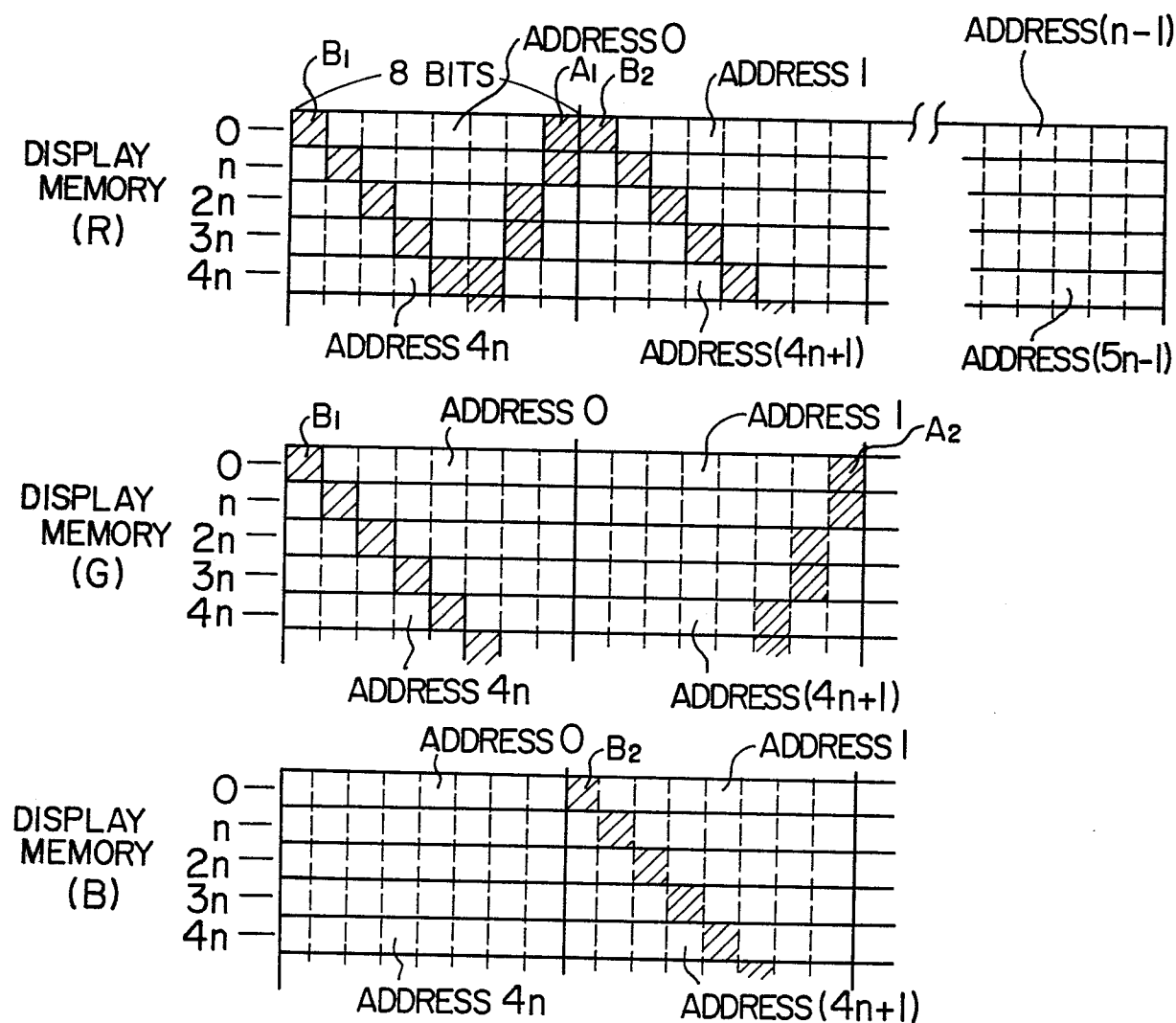


FIG. 3
PRIOR ART

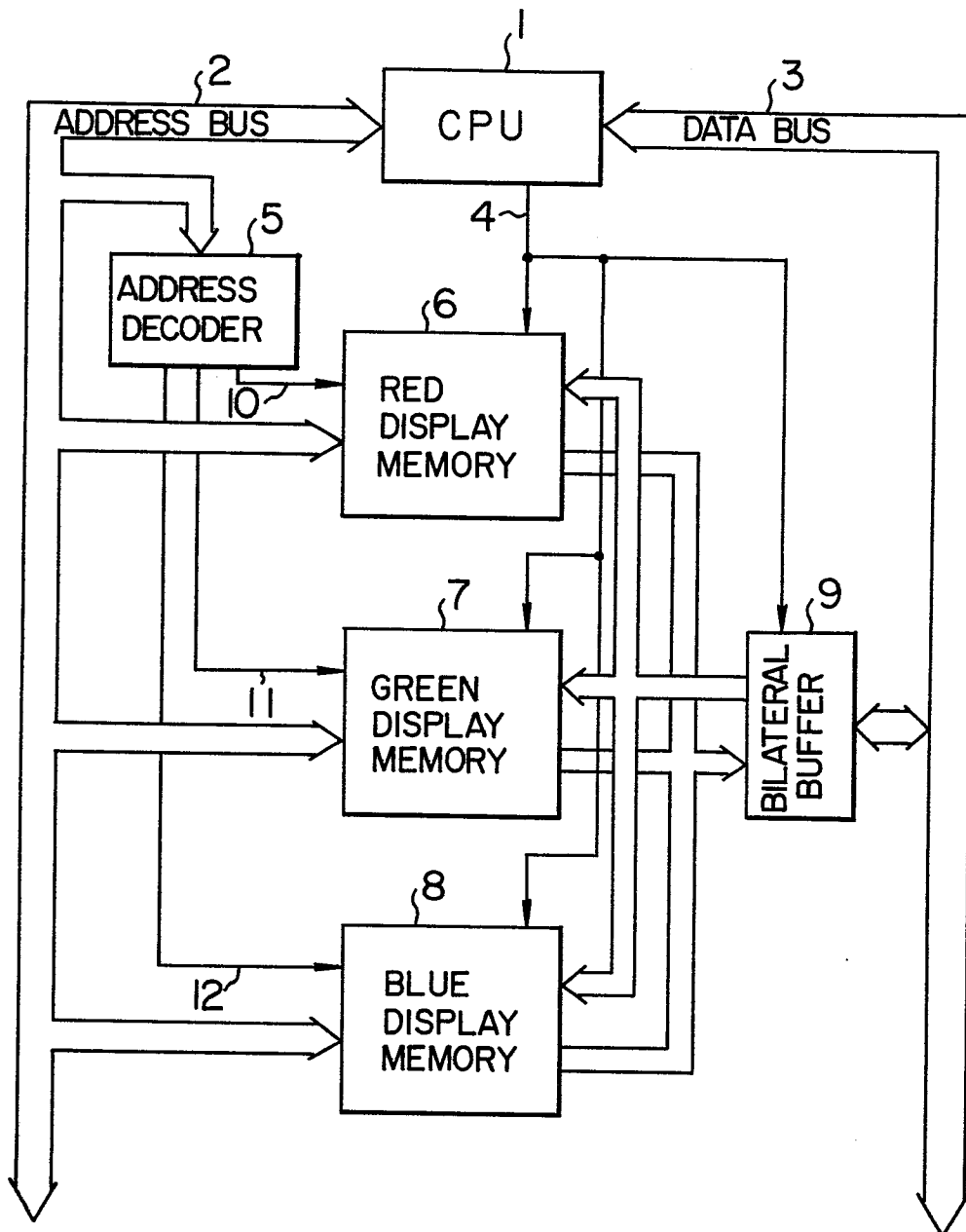


FIG. 4
PRIOR ART

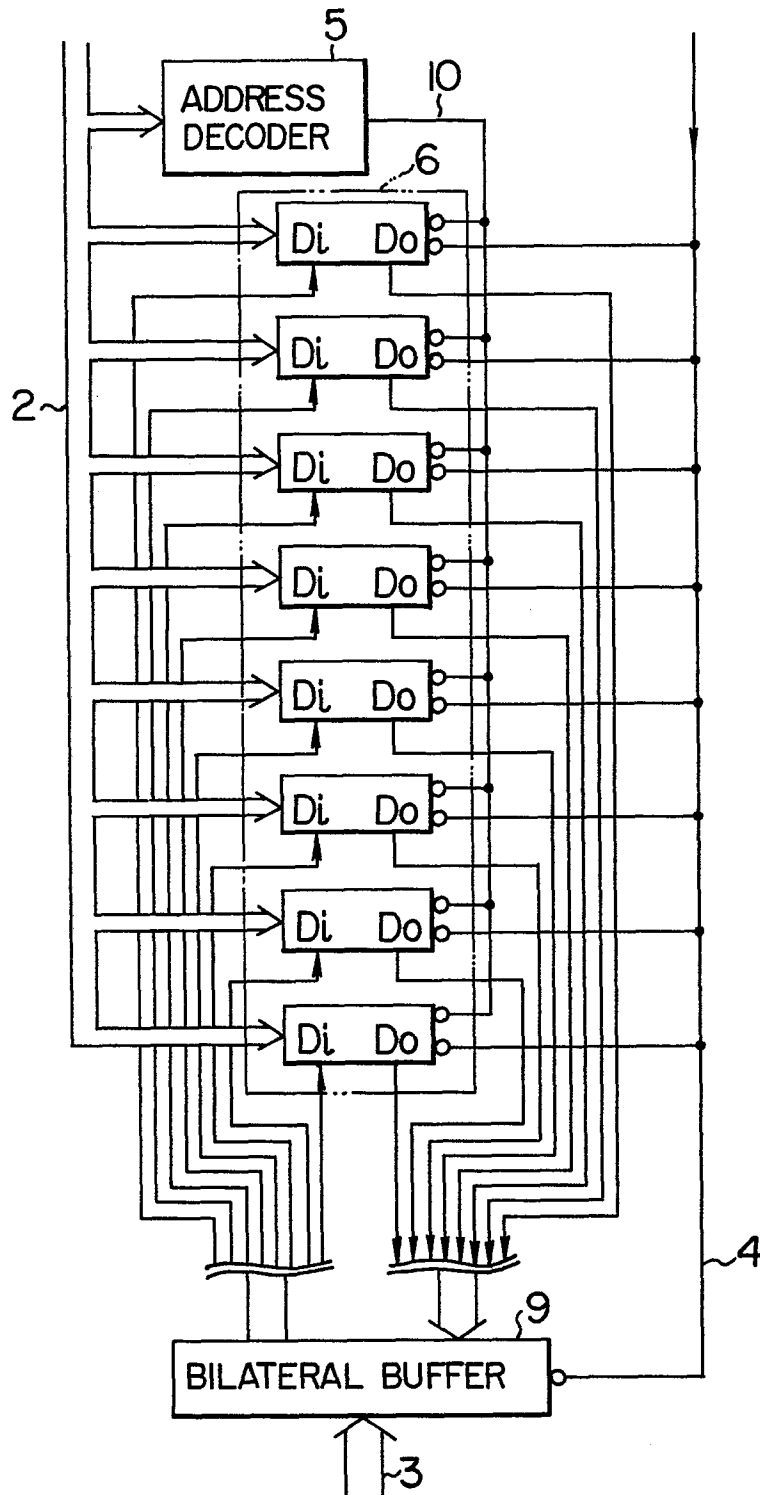


FIG. 5
PRIOR ART

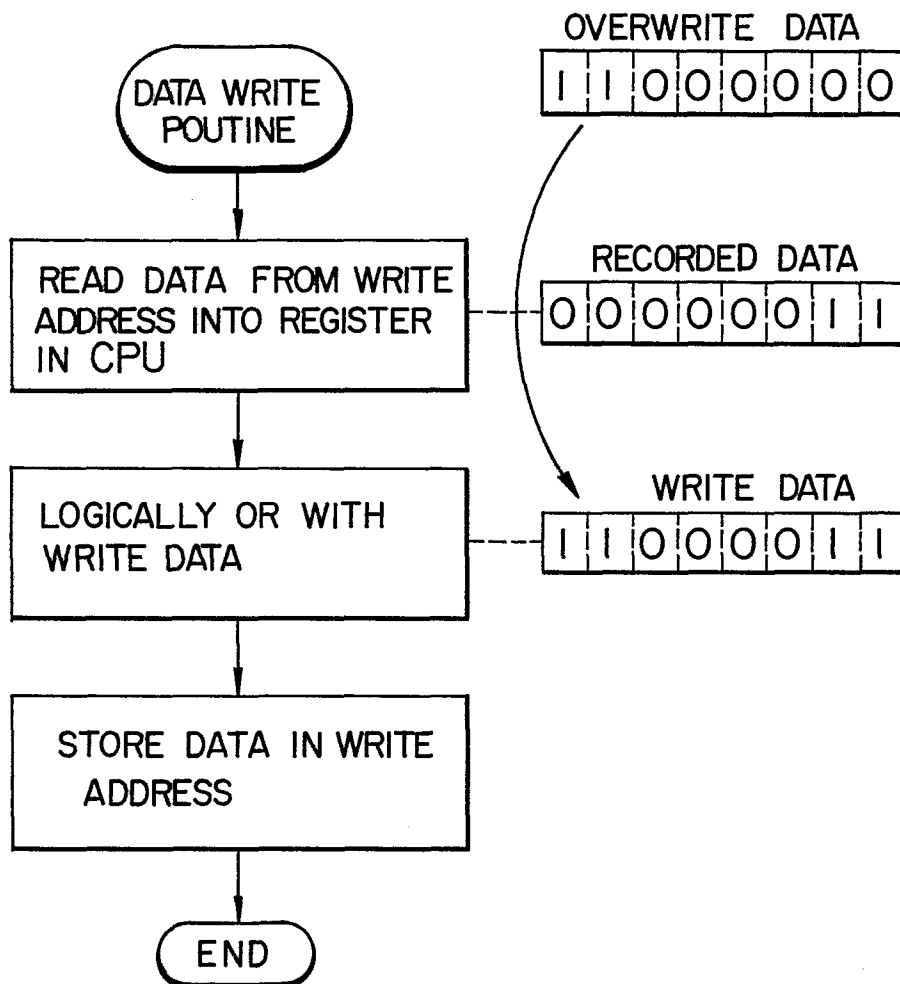


FIG. 6

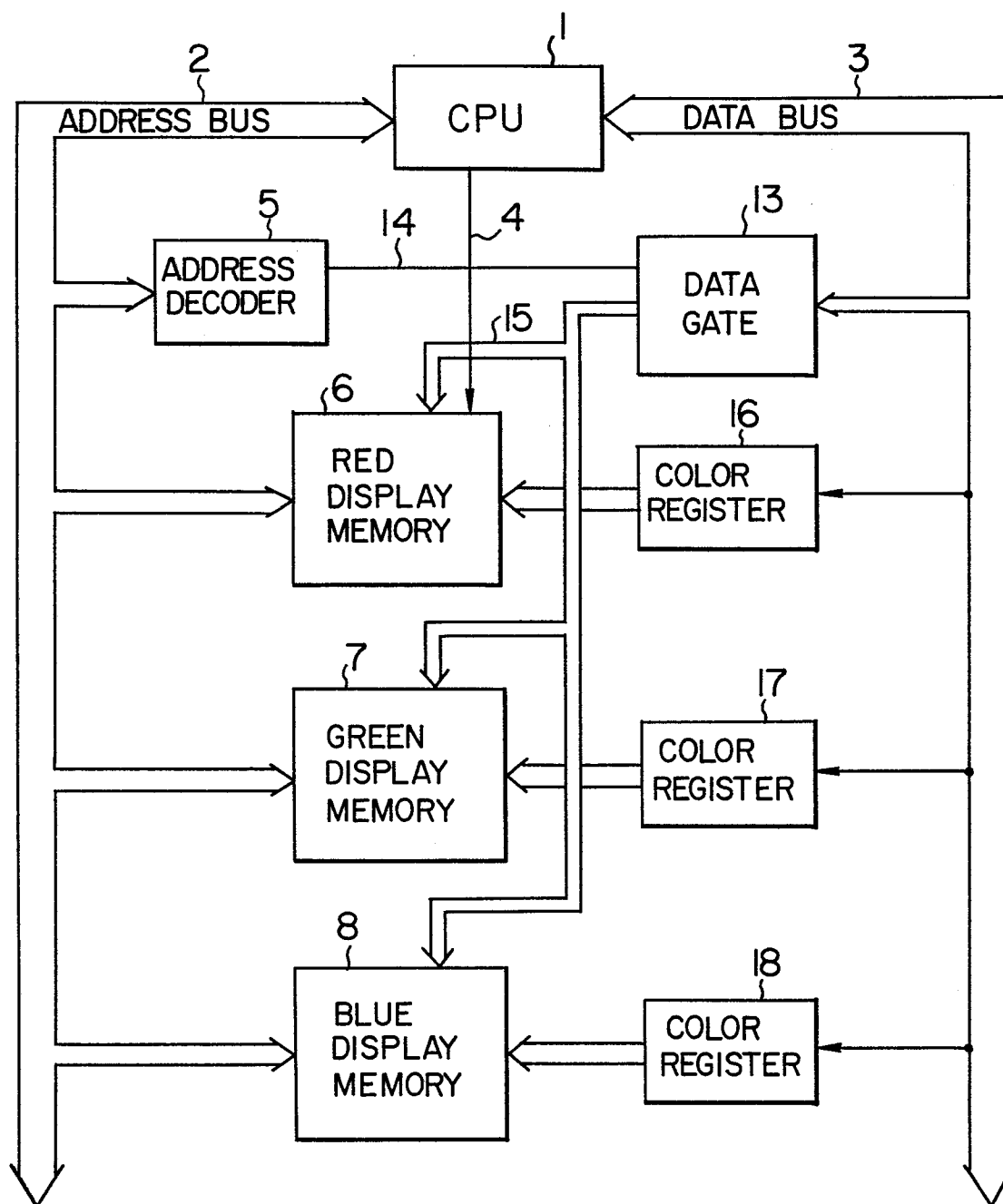


FIG. 7

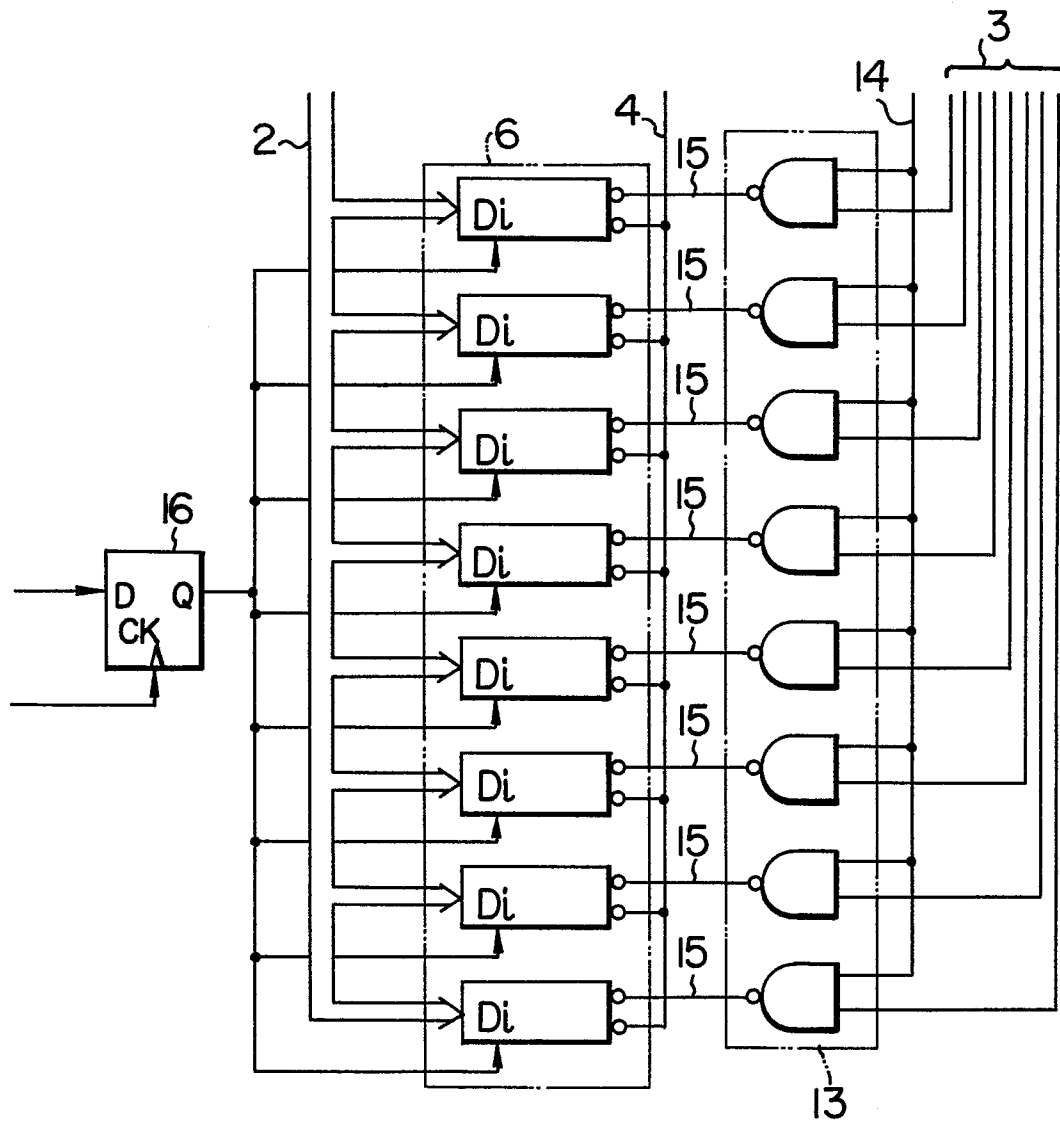


FIG. 8

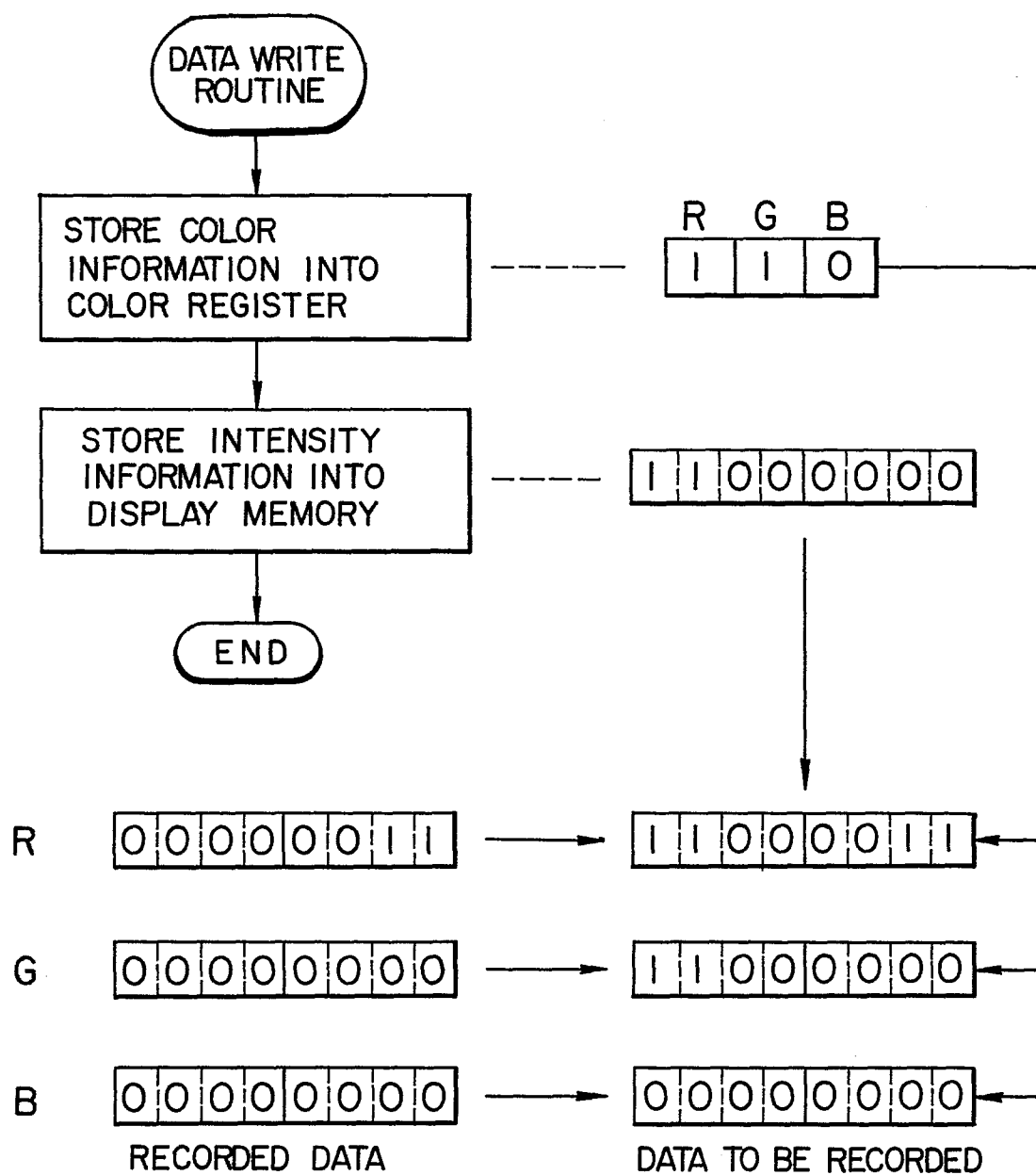


FIG. 9

