DISPLAY SYSTEM WITH COMBINED DYNAMIC AND STATIC DISPLAY

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ABSTRACT

This display system has first and second display means each supported by a display board and providing for the combined display of news-service information in a dynamic manner and of sequentially selected advertising messages each being displayed in a static manner.

6 Claims, 7 Drawing Figures
Fig. 1

10  
12  

EMBASSY, THAT IT HAS  
ALWAYS SOUGHT  
PEOPLE REALLY LIKE  
TO STRIKE THE AIRLIFT  
THE COMBINED ADDITION  
THE 1/2 RV TO DO  
THE AD TO FROM TO LC  

11  

THIS IS FOR  
STATIC DISPLAY  
OF AD COPY  

14
DISPLAY SYSTEM WITH COMBINED DYNAMIC AND STATIC DISPLAY

BACKGROUND OF THE INVENTION

In general, this invention relates to display systems. More particularly, it relates to an advertising display system with combined dynamic display of news-service information and static display of each of a sequence of advertising messages.

Attracting and holding the attention of potential customers is an important goal in any system for disseminating advertising messages. Equally important, of course, is the need to disseminate an advertising message at a small enough cost to be economically justified.

As is evident from their ubiquitousness, illuminated advertising display devices such as neon light signs have been found useful in gaining attention. However, this type of advertising sign suffers from several disadvantages. Such signs are relatively expensive partly because unless they are artfully arranged they seldom succeed in attracting attention. Accordingly, in addition to construction and installation costs, generally, costs are incurred in laying out their design. Moreover, such signs are very inflexible. For each advertising message, a separate sign is required. And the full cost of a sign must generally be borne by a single advertiser.

SUMMARY OF THE INVENTION

A feature of the display system of this invention resides in the dissemination of advertising messages in combination with the dissemination of news-service information so as to draw and focus attention on the advertising content. A further feature resides in the flexibility the invention provides whereby advertising copy to be displayed is easily modified and whereby the cost of the display system need not be borne solely by a single advertiser but can be allocated among a multiplicity of them.

The display system has first and second electrically controllable display means each supported by a display board for the combined display of news-service information in a dynamic manner and of sequentially selected advertising messages, each being displayed in a static manner. Preferably, the first and second display means each comprise a matrix of lamps with each character (i.e., a letter, number or the like) being displayed by illuminating a selected subset of a submatrix of the lamps.

The system has first memory means providing for the storage of signals used to control the first display means. An input of the system serially receives data signals representing characters forming news-service information. Means are provided for responding to the serially received data signals for accumulating in the first memory a plurality of items of line data, each item of line data comprising a plurality of groups of signals, each group being encoded to represent a character of the incoming news-service information.

The system has second memory means and means for storing into it signals representing a plurality of advertising messages. Means are provided for obtaining signals stored in the two memory means and for coupling the signals to the respective display means with the first display means responding to the signals obtained from the first memory means to display a dynamic representation of a plurality of items of line data and with the second display means responding to the signals obtained from the second memory to display in a predetermined sequence static representations of a plurality of advertising messages.

In a preferred feature, the displaying of news-service information is interruptable so that locally generated messages, derived from a signaling device such as a conventional teletypewriter, can be displayed by the first display means.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a display board supporting the electrically controlled display means of this invention;

FIG. 2 is a block diagram of a specific embodiment of this invention;

FIG. 3 is a block diagram of the code converter 25 of FIG. 2;

FIG. 4 is a block and schematic diagram of the multi-state counting register 32 of FIG. 2;

FIG. 5 is a timing diagram illustrating the waveforms of control and timing signals provided by the multi-state counter 32 of FIG. 2;

FIG. 6 is a block and schematic diagram illustrating the construction of the scannable buffer of FIG. 2, and

FIG. 7 is a block diagram illustrating the construction of the portion of the display system that provides control signals for the display means of FIG. 2.

DESCRIPTION OF A SPECIFIC EMBODIMENT

General Description of the Display System

The display system of this invention includes a display board such as that illustrated in FIG. 1 and generally indicated at 10. Display boards for use in this invention can be wall mounted and therefore have only one visible face, but, preferably, the display board is conspicuously located within a building and, has two display faces, display face 11 being visible in FIG. 1. Advantageously, the display board is installed within an airport terminal, a shopping mall, or like building where there is a considerable amount of walk-through traffic.

Supported by the display board is at least one electrically controlled display apparatus comprising display means 12 and 14 with display means 12 advantageously occupying approximately 70 percent of the face 11 of the display board and being located above display means 14 which occupies the remaining portion of the face 11.

Preferably, display means 12 and 14 each comprise a matrix of lamps or display lights, a typical one of which is indicated at 15. In a specific embodiment, there are 12,500 lamps arranged in 100 rows and 125 columns.

Preferably, the display system of this invention has two modes of operation. In one mode of operation (hereinafter the normal mode), the top 70 rows of lamps (identified in FIG. 1 as 16-1 through 16-70) are dedicated to the function of displaying news-service information. In another mode (hereinafter the local mode), these same 70 rows are dedicated to the function of displaying locally generated messages derived from a keyboard of a standard teletypewriter 17 (see FIG. 2). In either mode, the bottom 30 rows (identified in FIG. 1 as 18-1 through 18-30) are dedicated to the function of displaying advertising messages. The col-
umnns of lamps for both display means 12 and 14 are identified as 19-1 through 19-125.

Each character of a message is displayed by illuminating a selected subset of an associated set of 35 lamps, each such associated set being formed by lamps in seven different rows and five different columns. By way of example, the character "T" is displayed by illuminating each lamp in the top row of such an associated set and simultaneously illuminating each lamp in the center column of the associated set. Since in the specific embodiment display means 12 has 8,750 lamps arranged in 70 rows and 125 columns and since each character requires 35 lamps arranged in seven rows and five columns for its display, display means 12 can display as many as 250 characters arranged in 10 lines of copy with 25 characters per line of copy. As will be explained in greater detail, each such single line of copy is dynamically displayed. Preferably, each single line of copy, as a whole, appears to move upwardly on the display means 12 with the line appearing to enter gradually from the bottom of the display means and eventually disappearing gradually at its top. For example, when the character "T" is to be displayed as the first character in a line of copy, initially the horizontal bar of the T first appears by the illumination in row 16-1 of the five lamps in columns 19-1 through 19-5. The bar of the T moves upwardly in these columns by the sequential illumination of five lamps each in rows 16-2 through 16-70. The vertical leg of the T begins to appear in column 19-3 when the bar of the T is displayed by row 16-2 and is in complete display when the bar of the T is displayed by row 16-7.

As shown in block diagram of FIG. 2, the display system has a news-service input 20 for receiving news-service information in the form it is conventionally transmitted over teletype wires. That is, the news-service information is received in the form of digital data which is encoded in a standard format.

This format is sometimes called an eight bit serial-by-bit format wherein each character is represented by six serially transmitted bits of data that are bounded by a "start bit" and a "stop bit." The start stop bits are useful in distinguishing the end of the code for one character from the start of the code for the next character. A two-position selector switch 22 on the teletype-writer 17 is manually operable to place the display system in either the normal mode or the local mode. In its position shown in FIG. 2, selector switch 22 places the system in the normal mode whereby the news-service data signals determine what is to be displayed by display means 12. While in its normal mode, the display system is operative to process the incoming serial-by-bit news-service data signals so as to provide control signals for selectively illuminating the lamps of display means 12 in the dynamic manner described above. This signal processing involves a preliminary serial-by-bit to serial-by-character conversion. A code converter 25 having its input connected to the selector switch 22 cooperates with a conventional start bit detector 30 to perform this preliminary processing. The code converter 25 has an output bus 26 comprising 35 signal leads (not individually shown) on which it provides coded items of character data in a serial-by-character manner with each coded item of character data comprising 35 bits. In this specific embodiment, each item of character data is coded in the following manner. The bus 26, as stated above, serially carries the items of character data and comprises 35 signal leads. Although for clarity of the drawing these signal leads are not individually shown, they are identified herein by reference numerals that correspond to conventional matrix notation. Thus, by way of example, there are signal leads 26-(1,1), 26-(7,1), 26-(7,5), and 26-(1,5), which respectively correspond to the four corners of a 7 x 5 matrix. When the character "T" for example is represented by the item of character data, the signal leads in the top row of the matrix (i.e., 26-(1,1) through 26-(1,5)) and the signal leads in the center column of the matrix (i.e., 26-(1,3) through 26-(7,3)) each carry a binary '1' signal, whereas all the remaining signal leads carry a binary '0.'

The signal processing further includes the accumulation of an item of line data. The term "line data" is used herein to mean an accumulation of data representing a plurality of consecutive characters (including spaces between letters) that are to be displayed on the display means 12 as a single line of copy. In this specific embodiment, data corresponding to 35 consecutively received characters form such an item of line data, and a set of 825 lamps arranged in seven rows and 125 columns are required for complete display of these characters.

A multi-state counting register 32 provides, among other things, for counting the number of characters of incoming news-service information that will be displayed as a single line of copy on the display board. In this specific embodiment, 25 such characters are so displayed, and accordingly the multi-state counter 32 has 25 allowable states. The start bit detector 30, in response to each start bit, provides a clock pulse to cause the multi-state register 32 to change from one state to the next.

To implement the accumulation of an item of line data there is provided a line data accumulation buffer 35. The buffer 35 comprises a matrix of flip-flops (not individually shown) that, in this specific embodiment, are organized into 25 sub-matrices each comprising seven rows and five columns of flip-flops, so that there is a total of 875 such flip-flops. Each time an item of character data is provided by the code converter 25, the item is scanned into the line accumulation buffer. "By scanning into" is meant that the serial-by-character data is transferred character-by-character into sequentially selected sub-matrices of the line data accumulation buffer.

During each period of time defined by one cycle of the multi-state counter 32, a single item of line data is accumulated in the line data accumulation buffer. Upon completion of such accumulation, the item of line data is transferred in its entirety to a scannable buffer 38. The main purpose of the scannable buffer 38 is to effect a conversion from a single item of line data into a sequence of items of row data. The term "row data" is used herein to mean the number of bits of information that is being or is to be displayed by a single row of lamps in display means 12. Since in this specific embodiment there are 125 lamps in each row, each item of row data consists of 125 bits.

In response to control signals provided by the multi-state counter 32, the scannable buffer 38 provides for a serial-by-row item transfer of data into a shifting display memory 45. The memory 45 comprises a matrix of flip-flops (not individually shown) with each flip-flop corresponding to a different one of the lamps in display means 12. In this specific embodiment, the flip-flop
matrix of memory 45 is arranged into 70 registers each corresponding to a different row of lamps in display means 12 and each having 125 flip-flops each corresponding to a different column of lamps in display means 12.

A matrix of conventional lamp driver circuits 47 selectively provides energization current to the display means 12 in accordance with signals obtained from the memory 45.

To implement the dynamic display of news-service information in the manner described above, each item of row data is shifted as a whole upwardly from register to register in the memory 45 in response to a shift signal. An OR gate 49 supplies the shift signal in response to control signals provided (via signal leads not shown) 7 by the multi-state counter 32.

The portion of the display system involved in the display of advertising messages comprises a card reader 50, a local memory 52, a multiplexer 54, the display means 14, and a matrix of lamp driver circuits 56 responsive to the multiplexer for providing energization current to illuminate selected lamps in the display means 14.

As will be explained in greater detail, the signal processing involved in this portion of the display system comprises the conversion of advertising message data represented by pre-punched conventional 80 column punched cards into signals suitable for controlling the lamp driver matrix 56 to illuminate selected lamps in display means 14. Each advertising message is introduced into the system by a different punched card, and a plurality, preferably 32, such messages are stored in the local memory in the form of data encoded as described above with reference to items of character data. In contrast to the display of news-service information, each advertising message, while it is being displayed, is displayed statically. The multiplexer 54 provides for selecting for display in a predetermined cyclical sequence each of the advertising messages and also provides for timing the respective intervals during which the individual advertising messages are displayed. Preferably, each individual advertising message is displayed for at least about 5 seconds.

**DETAILED DESCRIPTION**

The code converter 25, as shown in more detail in FIG. 3, is connected to the wiper arm of the selector switch 22 (FIG. 2) by a signal lead 22W which carries serial-by-bit data signals derived from either the external teletype wires of the teletypewriter keyboard depending upon the mode (normal or local) of the system. The code converter is also connected to the start bit detector 30 (FIG. 2) by signal leads 57-1 and 57-2 which respectively carry start and stop pulses formed by detector 30 in response to the detection of start and stop bits. A flip-flop 59 has a set input (S), a reset input (R) and an output (QS9). Flip-flop 59 provides a '1' signal on its QS9 output during each interval of time intervening between a start pulse (which sets the flip-flop) and the next stop pulse (which resets the flip-flop). An AND gate 60 has one input connected to the QS9 output of flip-flop 59 and another input connected to signal lead 22W. While the flip-flop 59 provides a '1' signal, AND gate 60 is operative to gate to a serial-to-parallel converter 62 the six consecutive data bits that as previously described are transmitted between start and stop bits. The serial-to-parallel converter 62 is of the conventional construction used in the conversion of standard serial-by-bit teletype code into parallel-by-bit, serial-by-character code, and, accordingly its internal construction is not specifically described herein.

The converter 62 provides to a character decoder 63 via a bus 64 its parallel-by-bit output. The decoder in turn provides to a character encoder 65 via a selected signal lead in a bus 66 (the individual signal leads not being shown) a signal identifying which character corresponds to the data stored in the converter 62. The encoder 65 in turn provides to a character copy register 67 via a bus 68 an item of character data, encoded as previously described, corresponding to the data stored in converter 62. The character copy register 67 includes 35 flip-flops arranged in a matrix of seven rows and five columns with each flip-flop being strobed by the stop pulse to copy the item of character data carried by the bus 68. It should be appreciated that the details of the construction of the code converter 25 are a matter of design choice and other arrangements are suitable for implementing its function are known in the art; for example, see the tandem decoding and encoding circuitry disclosed in U.S. Pat. No. 3,594,778.

Each time the character copy register 67 is strobed and is thereby updated to store a new item of character data, its previous contents are scanned into the line accumulation buffer 35 (FIG. 2). The buffer 35 comprises a matrix of flip-flops (not individually shown) that in this specific embodiment are organized into 25 submatrices each comprising seven rows and five columns of flip-flops so that there is a total of 875 such flip-flops. The buffer 35 also includes a conventional input gating arrangement (not separately shown) for distributing sequentially provided items of character data for storage in sequentially selected ones of the submatrices. A conventional output gating arrangement 69 connected by buses 69i and 69o between buffers 35 and 38 provides for transferring each complete item of line data between the buffers. After each such transfer, the line data accumulation buffer is available to accumulate the next item of line data. While for clarity of the drawing, the buses 69i and 69o are each shown as a single line, it should be understood that a plurality of signal leads are provided in each for parallel transfer of the signals making up the item of line data.

The control signal for enabling output gating arrangement to effect these transfers is identified as P25 and is provided the gating arrangement from the multi-state counter 32 by a signal lead not shown.

The multi-state counter 32, as shown in more detail in FIG. 4, is connected to the start bit detector 30 (FIG. 2) by the signal lead 57-1 which serially carries the start pulses. The start pulses are used as clock pulses by the multi-state counter to sequence through its states. The multi-state counter has 25 allowable states S1-S25 and cyclically enters state S1 from S25 at the start of each cycle.

The multi-state counter provides as output control signals P3, P7, P11, P15, P18, P21, and P25, the waveform of each of these control signals being shown in the timing diagram of FIG. 5. Each of these control signals has a binary value of '1' while the multi-state counter is in a corresponding state and a binary value of '0' otherwise.

In the multi-state counter there are five flip-flops 71 through 75 each of the conventional clocked J-K type.
These five flip-flops together with an OR gate 76, AND gates 77 through 81, and inverter 82 are arranged to form a counter that counts in straight binary code.

Five AND gates 83 through 87 perform a purely decoding function and produce the control signals P3, P7, P11, P18, P21, and P24 respectively.

AND gate 81 performs a decoding function to produce control signal P25 and also serves as a part of the counter per se. AND gate 81 has five inputs each of which is connected to one of the complementary outputs of a different one of the flip-flops 71–75. For clarity of the drawing, the signal leads connecting the inputs of AND gate 81 to the outputs of the flip-flops are not shown. Instead, the existence of these signal leads is indicated by reference numerals shown adjacent to the gate. Thus, an indicated, AND gate 81 has its inputs connected by signal leads connected to Q71, Q72, Q73, Q74, and Q75. Control signal P25, produced by AND gate 81, has a binary value of '1' while the counter is in state S25 and a binary value of '0' otherwise. Inverter 82 complements the control signal P25 to provide control signal P25.

Flip-flop 71 forms the lowest order stage of the binary counter and has its K input connected to the output of inverter 82 and has its J input connected to a source 88 of a '1' signal. Being of the J-K type, flip-flop 71 has the property that it toggles back-and-forth between binary states in response to serially received clock pulses so long as its J input and its K input each receive '1' signals. Since its J input continuously receives a '1' signal and its K input receives a '1' signal in each of the states S1 through S24, flip-flop 71 responds to clock pulses to toggle back-and-forth between binary states until the multi-state counter reaches state S25. During state S25, control signal P25 has a binary value of '0' and, accordingly, flip-flop 71 does not change state while the counter changes from state S25 to state S1.

Flip-flop 72 forms the next stage of the binary counter and its J input and its K input are each connected to the output of AND gate 77. The AND gate 77 has two inputs, one input being connected to the output of flip-flop 71 and the other input receiving control signal P25 by virtue of its being connected to the junction of the output of inverter 82 and the K input of flip-flop 71. Accordingly, AND gate 77 provides a '1' signal in response to the coincidence of a binary value of '1' at Q71 and a binary value of '1' for control signal P25. Owing to this arrangement, each time flip-flop 71 changes state such that Q71 switches in binary value from '1' to '0', flip-flop 72 toggles.

Flip-flop 73 forms the next stage and its J input and its K input are each connected to the output of AND gate 78. The AND gate 78 has two inputs, one input being connected to the output Q72 of flip-flop 72 and the other input being connected to the output Q71 of flip-flop 71. Accordingly, AND gate 78 provides a '1' signal in response to the coincidence of a binary value of '1' at Q71 and a binary value of '1' at Q72. Owing to this arrangement, each time both flip-flops 71 and 72 change state such that their outputs Q71 and Q72 switch in binary value from '1' to '0', flip-flop 73 toggles.

Flip-flop 74 forms the next stage. Its J input is connected to the output of AND gate 79 and its K input is connected to the output of OR gate 76. AND gate 79 has one input connected to the output of AND gate 78 and another input connected to the output Q73 of flip-flop 73. Owing to this arrangement, each time the three flip-flops 71–73 change state such that their outputs Q71–Q73 switch in binary value from '1' to '0', flip-flop 74 is set and its output Q74 switches to '1'. OR gate 76 has two inputs connected by signal leads not shown to receive respectively control signals P15 and P25 from AND gates 80 and 81. Thus, whenever the counter is in either state S15 or state S25, flip-flop 74 is reset on the next clock pulse and its output switches to '0'.

Flip-flop 75 forms the highest order stage of the counter. Its J input is connected by a signal lead not shown to receive control signal P15 from AND gate 80, and its K input is connected by a signal lead not shown to receive control signal P25 from AND gate 81. Accordingly, whenever the counter is in state S15, flip-flop 75 is set on the next clock pulse, and whenever the counter is in state S25, flip-flop 75 is reset on the next clock pulse.

The control signal P25 as stated above, provides control for the transfer of each completely accumulated item of line data to the scannable buffer 38. This control signal and control signals P3, P7, P11, P15, P18, and P21 are also used to control the operation of the scannable buffer.

The scannable buffer has a matrix-like structure of flip-flops having a plurality of identically arranged columns of flip-flops, and its construction and operation will be explained with reference to FIG. 6 which shows a single one of the identical columns. Without loss of generality, FIG. 6 illustrates the first of the 125 columns of flip-flops, each of the flip-flops preferably being of the conventional D type.

In the top row of the first column of this matrix there is flip-flop 101-(1,1) which has its output connected to one input of AND gate 103. The other input to AND gate 103 is connected to the multi-state counter (FIG. 4) to receive control signal P3. Accordingly, when control signal P3 has a binary value of '1', the output of AND gate 103 copies (i.e., has the same binary value as) the present output of flip-flop 101-(1,1). During the intervals that control signal P3 has a binary value of '0', the output of AND gate 103 has a binary value of '0' irrespective of the binary value of the output of flip-flop 101-(1,1). The output of AND gate 103 is connected to one input of OR gate 104, the output of which is connected to the input of the shifting display memory 45 (FIG. 2). During state S3 of each cycle of the multi-state counter 32 (FIG. 4), the output of flip-flop 101-(1,1) is scanned out to the memory 45. While not specifically shown because of the identity in construction and operation, at the same time that the output of flip-flop 101-(1,1) is scanned out, each of the flip-flops in the top row of the scannable buffer have their outputs scanned out to the memory 45. The outputs of the other six flip-flops in the first column are sequentially scanned out to memory 45 in the same manner. For example, flip-flop 101-(2,1) is scanned out during state S7 as a result of control signal P7 enabling AND gate 105 to copy the present output of flip-flop 101-(2,1). At the end of each cycle of the multi-state counter (during state S25), flip-flop 101-(7,1) is scanned out as a result of control signal P25 enabling AND gate 110 to copy the present output of flip-flop 101-(7,1).

Also during state S25, each of the flip-flops in the matrix receives on its D input, via a respective one of
the signal leads in bus 42 a corresponding one of the 875 bits of information making up an accumulated item of line data. These 875 bits are clocked into the flip-flops of the matrix as a result of clock pulses received on the clock signal inputs. Signal leads (not shown for clarity of the drawing) carry these clock pulses from a clock pulse driver 112 which is responsive to the stop pulses provided to it from the start bit detector 30 (FIG. 2).

From the foregoing it will be appreciated that for each cycle of the multi-state counter the seven items of row data making up a completely accumulated item of line data are loaded into the scannable buffer and scanned out row-by-row to the memory 45.

The memory 45 in turn responds to a shift signal formed as an OR function of P3-P25 and internally shifts each item of row data from register to register so as to provide the control signals enabling the matrix of lamp drivers 47 (FIG. 2) to display the news-service information in a dynamic manner.

The portion of the display system involved in the display of advertising messages is shown in greater detail in FIG. 7. The card reader is a conventional data processing peripheral device that accepts 80 column punched cards and provides signals corresponding to the arrangement of punched holes in the cards fed to the device. Preferably, the cards are pre-punched for delivery to the installation of the display system and each card is so punched as to represent a single advertising message. Also, control information is punched into each card. This control information includes information relating to the duration of time that the advertising message is to be displayed.

While a card is being read, the card reader has a digital signal output of a parallel-by-bit, serial-by-character form, each character conventionally being represented by a parallel 12-bit code. Conventional card reader interface circuitry 58 provides buffering to accumulate the serial-by-character information into data representing a complete advertising message. In this specific embodiment display means 14 (FIG. 2) has a capacity for displaying 75 characters arranged in three lines of copy. In the same manner as described above with reference to the code converter 25, each item of character data is codable into a five-bit parallel-by-bit code. Accordingly, in this code, a complete advertising message of 75 characters comprises 375 bits of information. The memory 52 is accordingly provided with a capacity to store for each message (preferably 30 to 32 messages) 375 bits. In addition to the message data per se, it is advantageous to store associated control information. This associated control information derived from each punched card, serves as an instruction to the display system to display the advertising message for a desired interval of time. To this end, memory 52 comprises a matrix of memory cells arranged in 32 rows (one row for each different advertising message), 375 data columns (one column for each different bit in an advertising message), and five control columns (one column for each different bit of control information). In conventional manner, the rows of memory cells from addressable locations. A write address decoder 120 responsive to control bits transferred to it from the card reader 80 through interface circuitry 58 selects a different addressable location for storing each different advertising message. This selection is effected in conventional manner through the provision of a write control signal on a selected one of 32 write enable leads 121.

A data write bus 122 couples the data representing an advertising message and the associated control information into the addressed location for storage therein. The contents of the local memory 52 are non-destructively obtained from it in the following manner.

A read address counter 125 cyclically counts through 32 different binary counts in each cycle with each different count identifying a different row of the memory 52. A decoder 127 responsive to the read address counter provides a read-out control signal on a selected one of 32 read enable signal leads 128. In response to a read-out control signal, the selected row is read-out and its contents are carried by a data read bus 130. An interval save register 132 receives the five bits of control information carried by a portion of the bus 130. The register 132 is updated each time a different row is read out. The contents of the register 132 determine the duration of the interval during which an associated advertising message is displayed.

A timing signal generator 135 produces a pulse train, preferably at about 1 pulse per second (pps), to drive a cyclical counter 137 that counts through up to 32 different counts in each cycle. A comparator circuit 139 compares for equality the contents of the register 132 and the counter 137. The output of the comparator circuit 139 is a binary valued signal that equals '1' when equality is detected and is '0' otherwise. The output signal of the comparator circuit 139 is used as a clock signal for the read address counter 125 and as a reset signal for the counter 137. As an example of operation, consider the following. Assume that it is desired to display a particular message for 6 seconds. The control information associated with this message will be coded as 00110, which corresponds to decimal 6. This control information is stored in the interval save register at the same time that the message data is obtained from the memory 45 for display. The counter 137, initially is reset to 00000, and in response to the 1 pps pulse train counts to 00110. At this point of time, comparator 139 detects equality and its output signal causes the read address counter to change count, thereby selecting the next subsequent message for display and simultaneously resets counter 137. An advantage of this arrangement resides in the fact that the amount of time an advertising message is to be displayed is discretely adjustable over a substantial range of time. Accordingly, an advertiser paying to have his advertising message displayed is given an option as to the amount of its exposure and can pay more or less in accordance with the extent of the exposure. Also, if a particular row in the memory 45 does not contain data for an advertising message, by virtue of this arrangement, that row in effect is skipped during each scan of the memory 45.

The advertising message data per se, obtained from the memory 45, is carried by a portion of the bus 130 to a bank (75 in this embodiment) of tandem connected character decode and character encode circuits generally indicated at 150. These circuits, as described above with reference to the code converter 25, convert the five bit parallel-by-bit code into a 7 × 5 matrix code for each item of character data. The outputs of the character encode circuits are connected to the lamp driver matrix 56 (FIG. 2), which respond to selectively illuminate the lamps of display means 14 for the static display of an advertising message. From the foregoing it will be appreciated that the circuitry for obtaining the
stored advertising signals forms a multiplexor that sequentially selects each of the stored advertising messages for display by display means 14.

What is claimed is:

1. A display system for combined display of news-service information and advertising messages, the system comprising:
   - an input to the system for serially receiving from an external news-service line digital data signals representing characters forming incoming news-service information;
   - first and second memory means;
   - means responsive to the serially received signals for accumulating in the first memory means a plurality of items of line data, each item of line data comprising a plurality of groups of signals, each group being encoded to represent a character of the incoming news-service information;
   - means for storing into the second memory means signals representing a plurality of advertising messages;
   - a display board, display apparatus supported by the display board and comprising first display means responsive to signals obtained from the first memory means to display a dynamic representation of a plurality of items of line data and second display means responsive to signals obtained in a cyclical sequence from the second memory means to display in a corresponding sequence static representations of a plurality of selected advertising messages; and
   - means for obtaining the signals from the first memory means to couple them to the first display means and multiplexing means for obtaining the signals from the second memory means to couple them to the second display means so as to display simultaneously the news-service information and an advertising message.

2. A display system according to claim 1, wherein the first and second display means each comprise a matrix of lamps and wherein the system includes a matrix of lamp driver circuits responsive to signals obtained from the first memory means for selectively illuminating lamps in the first display means and a matrix of lamp driver circuits responsive to signals obtained from the second memory means for selectively illuminating lamps in the second display means.

3. A system according to claim 2, wherein each item of line data requires for its display a plurality of rows of lamps in the matrix of the first display means and wherein the system includes means for causing an apparent row-by-row vertical movement of the display of the news-service information.

4. A system according to claim 1, wherein the multiplexing means for obtaining the signals from the second memory includes means for controlling the duration of time that each advertising message is to be displayed.

5. A system according to claim 4, wherein the means for storing signals into the second memory means further includes means for storing control information, the duration controlling means being responsive to such control information for operating in accordance therewith.

6. A system according to claim 1, wherein the displaying of news-service information is interruptable, the system including means for generating local messages for display by the first display means.