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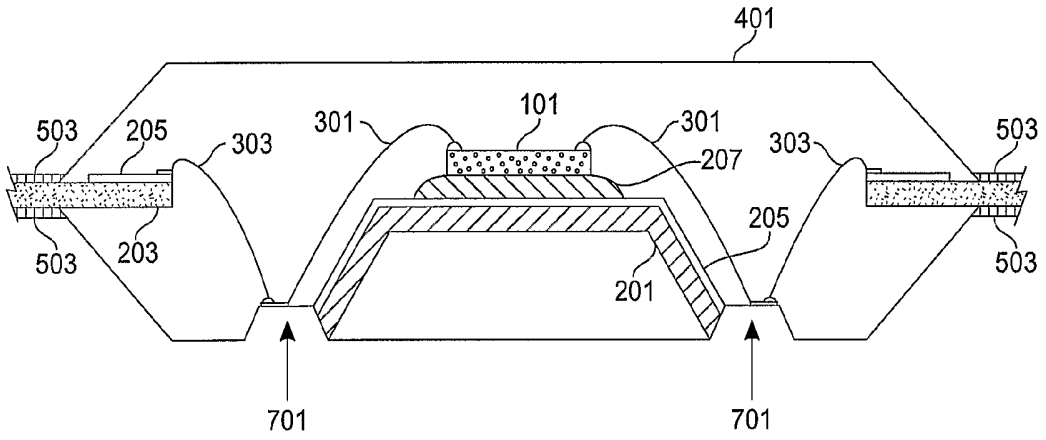
(54) Title: DIE ATTACH PADDLE FOR MOUNTING INTEGRATED CIRCUIT DIE



(57) Abstract: An electrical package for an integrated circuit die (101) which comprises a die-attach paddle (201) for mounting the integrated circuit die (101). The die-attach paddle (201) has at least one down-set area located on a periphery of the die-attach paddle (201). The down-set area has an upper surface and a lower surface, with the upper surface configured to electrically couple a first end of a first electrically conductive lead wire (301). A second end of the first electrically conductive lead wire (301) is bonded to the integrated circuit die (101). The upper surface is further configured to electrically couple a first end of a second electrically conductive lead wire (303) and a second end of the second electrically conductive lead wire (303) is bonded to a lead finger (203) of the electrical package.

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Description

DIE ATTACH PADDLE FOR MOUNTING INTEGRATED CIRCUIT DIE

TECHNICAL FIELD

The present invention relates to packaging of semiconductor integrated circuits. More particularly, the present invention relates to a device and method for preventing electrical shorts between lead wires in integrated circuit packaging.

BACKGROUND ART

As integrated circuit fabrication technology advances, the physical size of an integrated circuit device becomes progressively smaller. A given wafer size can now produce more integrated circuit devices per wafer without increasing a cost of wafer fabrication. One group of technical disciplines is aimed at packaging the devices. As devices become more complex and need to be integrated with additional devices, a universal interconnection scheme becomes more difficult.

Typically, a semiconductor device has fixed input/output (I/O) lines and interconnection with an external package can be difficult. This difficulty may lead to a redesign of an entire integrated circuit to avoid long lead wires from the device to the package. Additionally, any lead lines that cross over each other have a potential for developing an electrical short. Therefore, the interconnection of semiconductor devices with device packages is a major challenge in the art.

The integrated circuit devices are mounted on a surface of a mounting substrate and layers of interconnect lines and vias are formed that connect the devices to surrounding circuitry. Many different

packaging approaches are known and have been used for mounting and interconnecting semiconductor devices, such as Dual-In-Line Packages (DIP), Pin Grid Arrays (PGA), Plastic Leaded Chip Carriers (PLCC) and Quad Flat Packages (QFP).

A maximum allowable bond wire length in package assembly is typically in a 3.8 mm - 4.6 mm (150 mil - 180 mil) range. However, with a smaller integrated circuit die size, a distance between the die on the package lead bond post increases since the standard packages tend to remain the same size. This increase in distance between the integrated circuit package and the integrated circuit die can sometimes result in wire leads in excess of 5 mm (200 mil) or more. This long lead length can create assembly defects of wire-sweep during a molding operation resulting in potential electrical shorts between adjacent lead wires.

Currently, one solution is to convert the package into a stack-die configuration. In this case, a bottom die has metal pads patterned to be used as "jumper" pads. A lead wire would be bonded from a top integrated circuit die onto the bottom jumper die and then, in turn, to the package lead. This breaks up the long wire into two shorter segments. However, this solution also requires design and fabrication of the jumper die. The jumper die, together with a stack die assembly, is a significant cost to a final assembled package.

Fig. 1A shows a cross-section of a typical integrated circuit die 101 mounted into a lead frame package 100 (for example, a QFP). The lead frame package 100 includes a die-attach pad 103, die-attach adhesive 105, a plurality of lead frames 107, electrically-insulating adhesive 109, and a plurality of wire leads 111A. Once the plurality of bond wire leads 111A are

connected from the integrated circuit die 101 to the plurality of lead frames 107, a mold compound 113 is used to encapsulate and complete the lead frame package 100.

Fig. 1B shows a bottom jumper die 115. A plurality of bond wire leads 111B are connected from the integrated circuit die 101 to the bottom jumper die 115 and then to the plurality of lead frames 107, thus eliminating overly long bond wires.

An integrated circuit die, for example, a logic die, with 700 circuits and three layers of wiring has approximately 5 m of aluminum wiring on a chip less than 5 mm square. There are over 17,000 via connections from level to level through an insulator film of SiO_2. Yet, the conductor capacity in the die greatly lags behind the densification of the silicon devices. Most of the area of the die (approximately two-thirds), still serves as a platform for wiring.

Therefore, what is needed is a is way to provide for flexible wiring techniques between semiconductor devices and packages while avoiding problems associated with long lead lines and potentially shorted devices. Additionally, a universal package which may be used with a variety of different semiconductor devices is desirable.

SUMMARY OF THE INVENTION

The present invention eliminates the problem with long lead wires and jumper dice by forming a down-set area on a die-attach paddle to which lead wires may be bonded prior to being connected to lead fingers (i.e., the electrical "pins" of, for example, a quad flat pack) of the electrical package. The die-attach paddle is an apparatus onto which an integrated circuit die is mounted prior to a commencement of wire bonding operations. The present invention therefore comprises a die-attach paddle

for mounting the integrated circuit die. The die-attach paddle has at least one down-set area located on a periphery of the die-attach paddle. The down-set area has an upper surface and a lower surface, with the upper surface configured to electrically couple a first end of a first electrically conductive lead wire. A second end of the first electrically conductive lead wire is bonded to the integrated circuit die. The upper surface is further configured to electrically couple a first end of a second electrically conductive lead wire and a second end of the second electrically conductive lead wire is bonded to a lead finger of the electrical package.

The present invention is also a method for attaching an integrated circuit die to an electrical package. The method comprises forming a down-set on a periphery of a die-attach paddle and adhering the integrated circuit die to an uppermost portion of the die-attach paddle. A first end of a first lead wire is bonded to the integrated circuit die and the second end of the first lead wire is bonded to the down-set portion of the die-attach paddle. A first end of a second lead wire is bonded to the down-set portion of the die-attach paddle and a second end of the second lead wire is bonded to a lead finger of the electrical package. The integrated circuit die and die-attach paddle are then encapsulated with, for example, an epoxy molding compound. Optionally, if the down-set area of the die-attach paddle is configured so as to provide an electrical path between lead wires, any exposed lowermost section of the down-set portion of the die-attach paddle is masked after encapsulation. Exposed areas of the lead fingers are then plated with an electrically conductive material. After plating, the lowermost section of the down-set portion of the die-attach paddle is then unmasked and a lower section of the down-set portion of

the die-attach paddle is removed with a chemical etchant. Additionally, any conductive material plated onto an uppermost surface of the down-set area is removed by chemical etching. Any void left by removing the conductive material and the lower section of the down-set portion of the die-attach paddle is then filled with epoxy.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a cross-section of a prior art integrated circuit package.

Fig. 1B is a cross-section of a prior art integrated circuit package incorporating a jumper die.

Fig. 2 is a cross-section of an exemplary embodiment of the present invention showing the die paddle down-set.

Fig. 3 is the die paddle down-set of Fig. 2 showing bond wire leads attached.

Fig. 4 is the die paddle down-set of Fig. 3 after encapsulation.

Fig. 5 is the die paddle down-set of Fig. 4 incorporating a temporary mechanical mask to prevent plating onto an exposed area of the down-set.

Fig. 6 is the die paddle down-set of Fig. 5 after removal of the temporary mechanical mask and etching of the exposed area of the down-set.

Fig. 7 is the die paddle down-set of Fig. 6 after an etch of exposed plating.

Fig. 8 is the die paddle down-set of Fig. 7 after performing a void filler operation.

Fig. 9 is an exemplary flowchart for a method of mounting an integrated circuit into an electrical package of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention will now be described with reference to preferred embodiments thereof. With reference to Fig. 2, a down-set is formed on a periphery of a die-attach paddle 201. A section of a lead finger 203 is used to electrically couple the integrated circuit die 101 to other parts of a printed circuit board (not shown). A typical material used for fabrication of the die-attach paddle 201 and lead finger 203 is copper, although other materials may readily be employed. An uppermost surface of both the die-attach paddle 201 and the lead finger 203 is plated with a conductive material 205. In one specific embodiment, the conductive material 205 is silver. Alternatively, another noble metal, such as gold or platinum, may be used for the conductive material 205 provided that the conductive material 205 and the bond wire material, described infra, are dissimilar. The integrated circuit die 101 is mechanically fastened to the die-attach paddle 201 through the use of a suitable adhesive 207.

In Fig. 3, a bond wire 301 is attached from the integrated circuit die 101 to the down-set portion of the die-attach paddle 201. A second bond wire 303 is in electrical communication with the tail of the first bond wire 301 and is attached from the down-set portion of the die-attach paddle 201 to the conductive material 205 on the lead finger 203. This arrangement of running the bond wire 301 from the integrated circuit die 101 to the down-set portion of the die-attach paddle 201 and then to the lead finger 203 eliminates a single long lead by breaking the lead wire path into two shorter segments. The shorter segments are unlikely to be able to short together with other bond wire segments (not shown).

Wire bonding techniques are well-known in the industry and are used to attach fine lead wires,

typically 25 μm to 75 μm (1 mil - 3 mil) in diameter, from one bond pad to another to complete an electrical connection in electronic devices. Lead wires are frequently made of gold, aluminum, silver, or copper. Contemporary methods of wire bonding include wedge bonding and ball bonding. Both methods utilize thermocompression, ultrasonic, and/or thermosonic techniques.

A mold compound forms an encapsulated area 401 (Fig. 4) around the lead wire bonded die-attach paddle 201 and lead finger 203. Notice that the encapsulated area 401 leaves a lowermost portion of the down-set area of the die-attach paddle 201 exposed for later processing (to be described, infra).

With respect to Fig. 5, a plating operation (e.g., standard tin-lead or pure tin) serves to provide a plated area 503 adhered to the lead finger 203 for subsequent soldering of a completed integrated circuit package to a printed circuit board. A mechanical mask 501 prevents plating from attaching to a lower-most section of the down-set portion of the die-attach paddle 201. The mechanical mask 501 may be virtually any material capable of standing the plating operation and which can be readily removed after the plating operation is complete. After plating, the mechanical mask 501 is removed.

A chemical etchant is subsequently used to remove the lower-most section of the down-set portion of the die-attach paddle 201 (Fig. 6). For example, if copper is used to construct the die-attach paddle 201, a copper etchant will effectively remove an exposed area of the die-attach paddle 201, leaving a void 601. Notice that, in this example, the copper etchant does not etch the plated area 503, nor does it etch the conductive material 205. An additional chemical etchant step is

used to remove a lower-most portion of the conductive material 205, leaving a larger void 701 (Fig. 7). Notice that the tail and head of the bond wires 301, 303 are in full electrical communication with each other. However, the bond wire 301, 303 pair which was previously in electrical communication with all other pairs of bond wires (not shown) through an electrical coupling provided by the die-attach paddle 201, are now electrically isolated from all other bond wire pairs.

Finally, with reference to Fig. 8, a nonconductive liquid epoxy 801 is used to fill the void 701 left by the chemical etching steps.

The exemplary flowchart 900 of Fig. 9 begins with forming 901 a down-set on a die-attach paddle. The down-set may be applied to one or more edges of a die-attach paddle. Alternatively, the down-set area of the die-attach paddle may have individual legs (i.e., one leg for each wire bond pair) which are electrically isolated from each other. In this case, chemical etching of lower portions of the down-set legs would be necessary.

An integrated circuit die is then attached 903 to an uppermost portion of the die-attach paddle and lead wires are bonded 905 from the die to the down-set area and from the tail of the first lead wire to one or more lead fingers. Standard molding procedures are then employed 907 to encapsulate the die, die-attach paddle, lead wires, and portions of the lead fingers.

If the down-set area of the die-attach paddle incorporates individual, electrically isolated legs, described supra, the process is complete. If, however, a standard die-attach paddle comprising an electrically conductive material is used, optional steps are employed to electrically isolate each of the sets of wire bond pairs from one another. These optional steps include masking 909 a lower-most portion of the down-set area,

performing lead plating 911 (e.g., plating leads with tin-lead or pure tin), etching 913 (e.g., chemically or mechanically etching copper used to construct the die-attach paddle) a lower-most portion of the down-set area, etching 915 (e.g. chemically or mechanically etching) any conductive plating material (e.g., silver) that was used on the die-attach paddle, and filling 917 any down-set void created by the etching processes with filler material (e.g., epoxy).

Although the detailed description and drawings describe a universal interconnect die and applications of the same, one skilled in the art will recognize that other embodiments can readily be contemplated without departing from an intended scope of the present invention described. For example, although the die-attach paddle 201 (Fig. 2) and the conductive material 205 plated thereon are shown as two separate materials for sake of clarity, one skilled in the art can readily envision a single material which may serve both purposes. Therefore, a method of fabrication of the present invention would change accordingly. Thus, the fabrication process described herein is merely exemplary. Other techniques and materials (e.g., laminates or ceramics) may be readily employed and still be within a scope of the present invention. Further, a skilled artisan will recognize that the lead wire bond pairs need not be individual wires, but may simply be one continuous wire in which a center portion of the wire is bonded to an uppermost portion of the down-set area of the die-attach paddle.

Claims

1. An electrical package for an integrated circuit die, comprising:

a die-attach paddle, the die-attach paddle configured to be mechanically or chemically joined to the integrated circuit die; and

at least one down-set area located on a periphery of the die-attach paddle, the at least one down-set area having an upper surface and a lower surface, the upper surface configured to electrically couple a center portion of an electrically conductive bond wire, a first end portion of the electrically conductive bond wire being electrically coupled to the integrated circuit die; and

a lead finger of the electrical package, the lead finger being configured to electrically couple a second end portion of the electrically conductive bond wire.

2. The electrical package of claim 1 further comprising a conductive material plated onto an uppermost surface of the die-attach paddle.

3. The electrical package of claim 2 wherein the conductive material is silver.

4. The electrical package of claim 1 wherein the die-attach paddle is copper.

5. The electrical package of claim 1 wherein the die-attach paddle is substantially encapsulated in a molding compound after having the integrated circuit die joined to the die-attach paddle and the electrically conductive bond wire electrically coupled to the integrated circuit die, the upper surface of the at least one down-set area, and the lead finger.

6. The electrical package of claim 5 wherein the lower surface of the down-set area is left uncovered by the molding compound.

7. The electrical package of claim 6 wherein a lower portion of the down-set area is removed by etching.

8. The electrical package of claim 7 wherein a conductive material plated onto an uppermost surface of the down-set area is removed by etching.

9. The electrical package of claim 8 wherein a void left by etching of the conductive material and the lower portion of the down-set area is filled with epoxy.

10. An electrical package for an integrated circuit die, comprising:

a die-attach paddle, the die-attach paddle configured to be mechanically or chemically joined to the integrated circuit die;

at least one down-set area located on a periphery of the die-attach paddle, the at least one down-set area having an upper surface and a lower surface, the upper surface configured to electrically couple a first end of a first electrically conductive lead wire, a second end of the first electrically conductive lead wire being in electrical communication

with the integrated circuit die, the upper surface further configured to electrically couple a first end of a second electrically conductive lead wire; and

a lead finger of the electrical package, the lead finger being configured to electrically couple a second end of the second electrically conductive lead wire.

11. The electrical package of claim 10 further comprising a conductive material plated onto an uppermost surface of the die-attach paddle.

12. The electrical package of claim 11 wherein the conductive material is silver.

13. The electrical package of claim 10 wherein the die-attach paddle is copper.

14. The electrical package of claim 10 wherein the die-attach paddle is substantially encapsulated in a molding compound after having the integrated circuit die joined to the die-attach paddle and the electrically conductive bond wire electrically coupled to the integrated circuit die, the upper surface of the at least one down-set area, and the lead finger.

15. The electrical package of claim 14 wherein the lower surface of the down-set area is left uncovered by the molding compound.

16. The electrical package of claim 15 wherein the down-set area is removed by etching.

17. The electrical package of claim 16 wherein a conductive material plated onto an uppermost surface of the down-set area is removed by etching.

18. The electrical package of claim 17 wherein a void left by etching of the conductive material and the lower portion of the down-set area is filled with epoxy.

19. A method for attaching an integrated circuit die to an electrical package, comprising:

forming a down-set on a periphery of a die-attach paddle;

adhering the integrated circuit die to an uppermost portion of the die-attach paddle;

bonding a first lead wire from the integrated circuit die to the down-set portion of the die-attach paddle;

bonding a second lead wire from the down-set portion of the die-attach paddle to a lead finger of the electrical package; and

encapsulating the integrated circuit die and die-attach paddle.

20. The method of claim 19 further comprising plating an uppermost portion of the die-attach paddle with an electrically conductive material.

21. The method of claim 19 further comprising:

masking a lowermost section of the down-set portion of the die-attach paddle;

plating exposed areas of the lead fingers;

unmasking the lowermost section of the down-set portion of the die-attach paddle;

removing a lower section of the down-set portion of the die-attach paddle with a chemical etchant;

removing a conductive material plated onto an uppermost surface of the down-set area by chemical etching; and

filling a void left by removing the conductive material and the lower section of the down-set portion of the die-attach paddle with epoxy.

22. A method for attaching an integrated circuit die to an electrical package, comprising:

forming a down-set on a periphery of a die-attach paddle;

adhering the integrated circuit die to an uppermost portion of the die-attach paddle;

bonding a first end of a lead wire to the integrated circuit die;

bonding a center portion of the lead wire to the down-set portion of the die-attach paddle;

bonding a second end of the lead wire to a lead finger of the electrical package; and

encapsulating the integrated circuit die and die-attach paddle.

23. The method of claim 22 further comprising plating an uppermost portion of the die-attach paddle with an electrically conductive material.

24. The method of claim 22 further comprising:

masking any exposed lowermost section of the down-set portion of the die-attach paddle;

plating exposed areas of the lead fingers;

unmasking the lowermost section of the down-set portion of the die-attach paddle;

removing a lower section of the down-set portion of the die-attach paddle with a chemical etchant;

removing a conductive material plated onto an uppermost surface of the down-set area by chemical etching; and

filling a void left by removing the conductive material and the lower section of the down-set portion of the die-attach paddle with epoxy.

25. An electrical package for an integrated circuit die, comprising:

a die-attach paddle, the die-attach paddle configured to be mechanically or chemically joined to the integrated circuit die;

at least one down-set area located on a periphery of the die-attach paddle, the at least one down-set area having an upper surface and a lower surface, the upper surface configured to electrically couple a center portion of an electrically conductive bond wire, a first end portion of the electrically conductive bond wire being electrically coupled to the integrated circuit die and a lead finger of the electrical package being configured to electrically couple a second end portion of the electrically conductive bond wire;

a lead finger of the electrical package, the lead finger being configured to electrically couple a second end portion of the electrically conductive bond wire;

a molding compound substantially encapsulating the integrated circuit die joined to the die-attach paddle and the electrically conductive bond wire electrically coupled to the integrated circuit die, the upper surface of the at least one down-set area, and the lead finger;

a lower portion of the down-set area being left uncovered by the molding compound, the lower portion being removed by etching after applying the molding compound; and

an epoxy, the epoxy filling a void left by etching the lower portion of the down-set area.

26. The electrical package of claim 25 wherein the die-attach paddle is copper.

27. The electrical package of claim 25 further comprising a conductive material plated onto an uppermost surface of the die-attach paddle.

28. The electrical package of claim 27 wherein the conductive material is silver.

29. The electrical package of claim 28 wherein a conductive material plated onto an uppermost surface of the down-set area is removed by etching.

30. An electrical package for an integrated circuit die, comprising:

a die-attach paddle, the die-attach paddle configured to be mechanically or chemically joined to the integrated circuit die;

at least one down-set area located on a periphery of the die-attach paddle, the at least one down-set area having an upper surface and a lower surface, the upper surface configured to electrically couple a first end of a first electrically conductive lead wire, a second end of the first electrically conductive lead wire being in electrical communication with the integrated circuit die, the upper surface further configured to electrically couple a first end of

a second electrically conductive lead wire;

a lead finger of the electrical package, the lead finger being configured to electrically couple a second end of the second electrically conductive lead wire;

a molding compound substantially encapsulating the integrated circuit die joined to the die-attach paddle and the electrically conductive bond wire electrically coupled to the integrated circuit die, the upper surface of the at least one down-set area, and the lead finger;

a lower portion of the down-set area being left uncovered by the molding compound, the lower portion being removed by etching after applying the molding compound; and

an epoxy, the epoxy filling a void left by etching the lower portion of the down-set area.

31. The electrical package of claim 30 wherein the die-attach paddle is copper.

32. The electrical package of claim 30 further comprising a conductive material plated onto an uppermost surface of the die-attach paddle.

33. The electrical package of claim 32 wherein the conductive material is silver.

34. The electrical package of claim 33 wherein a conductive material plated onto an uppermost surface of the down-set area is removed by etching.

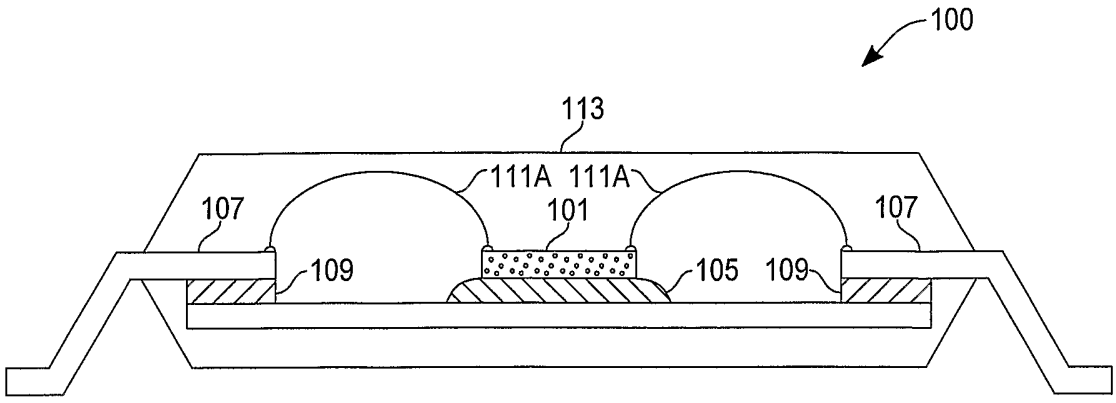


Fig._1A (Prior Art)

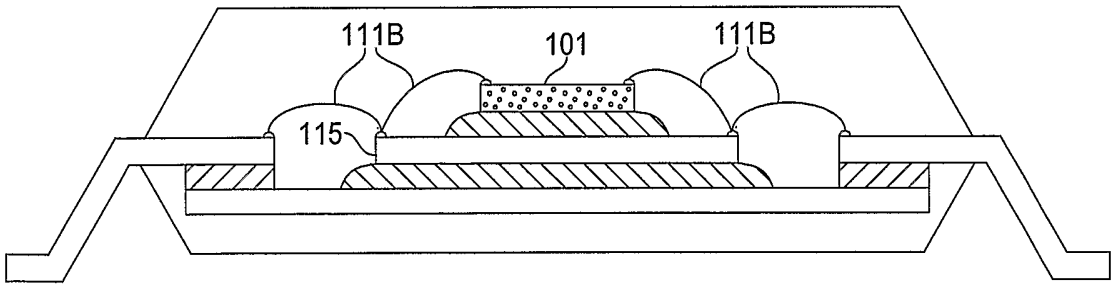
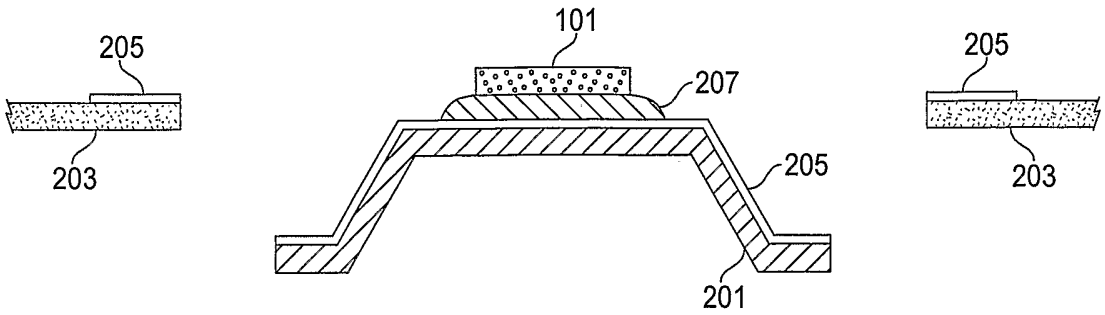


Fig._1B (Prior Art)


205
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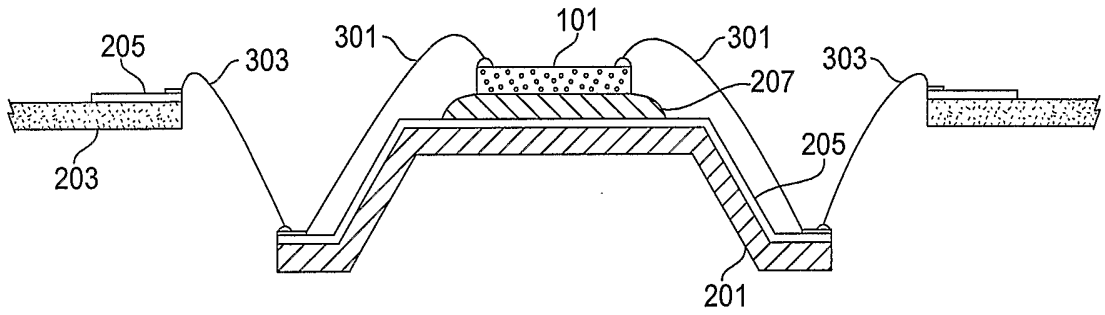
201

Fig._2


205
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301
101
301
303
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205
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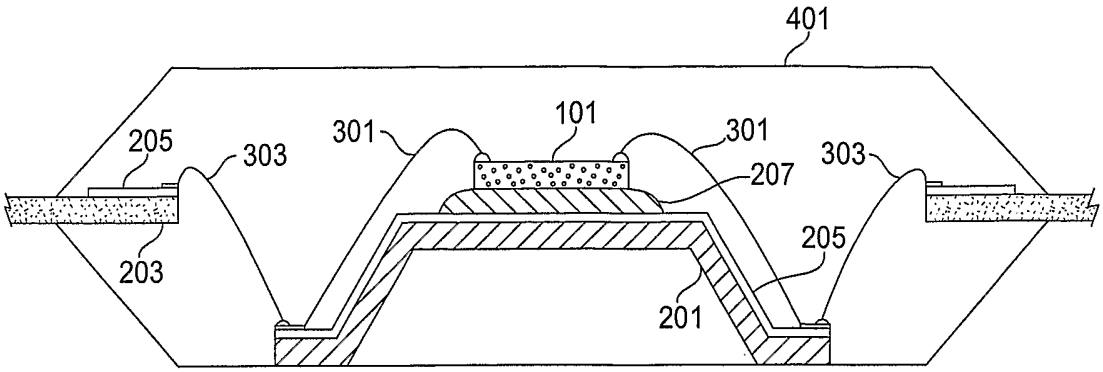
Fig._3


401
205
303
301
101
301
303
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205
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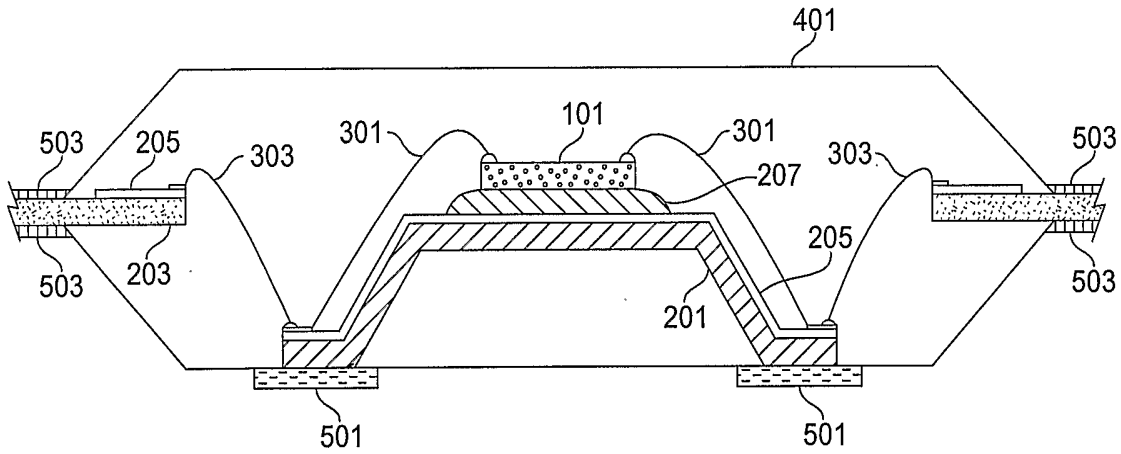
Fig._4


401
503
205
303
301
101
301
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503
207
205
503
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201
501
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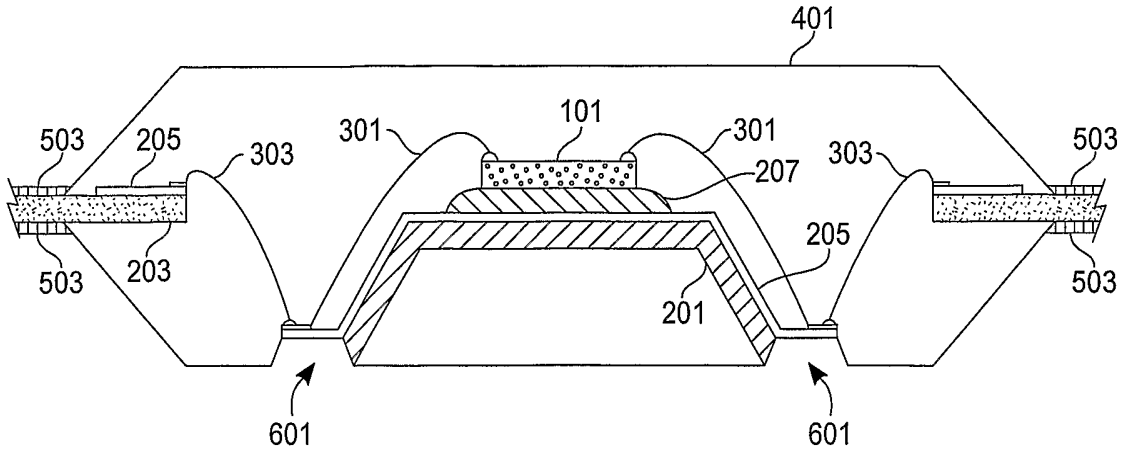
Fig._5


401
503
205
303
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101
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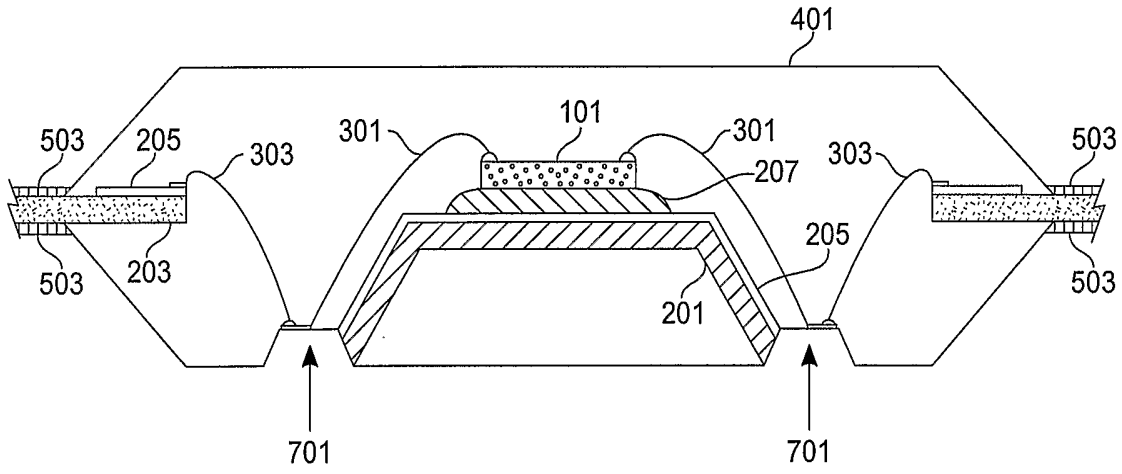
Fig._6


401
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205
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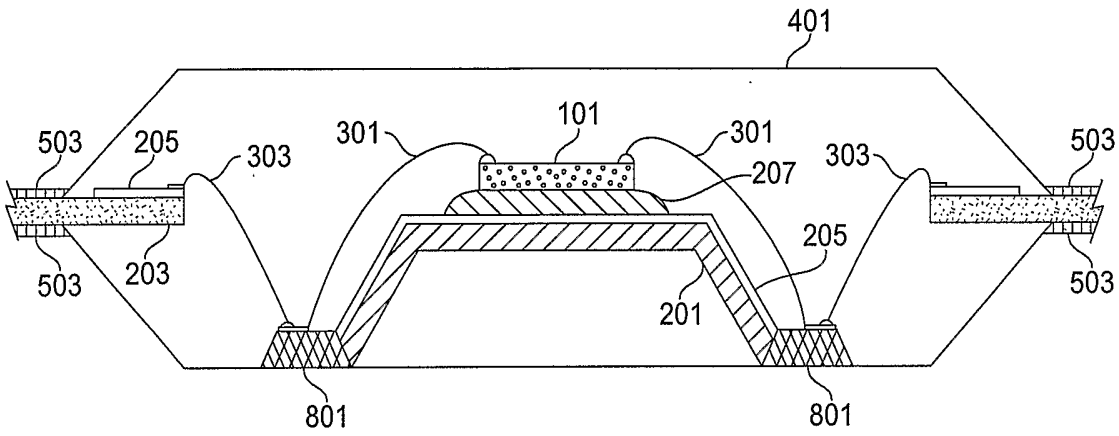
Fig._7


401
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801

Fig._8

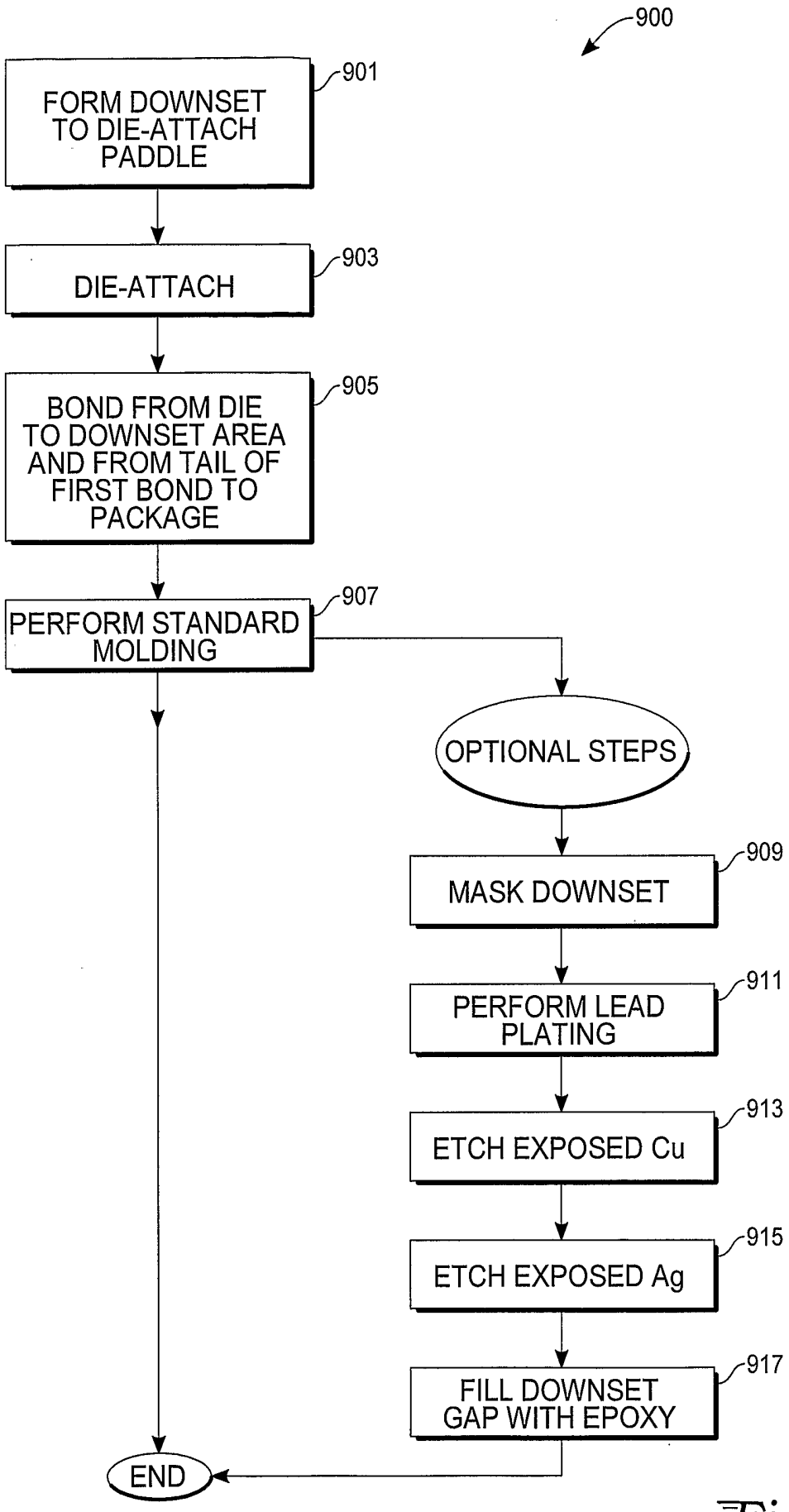
900
FORM DOWNSET TO DIE-ATTACH PADDLE
901
DIE-ATTACH
903
BOND FROM DIE TO DOWNSET AREA AND FROM TAIL OF FIRST BOND TO PACKAGE
905
PERFORM STANDARD MOLDING
907
OPTIONAL STEPS
MASK DOWNSET
909
PERFORM LEAD PLATING
911
ETCH EXPOSED Cu
913
ETCH EXPOSED Ag
915
FILL DOWNSET GAP WITH EPOXY
917
END

Fig._9