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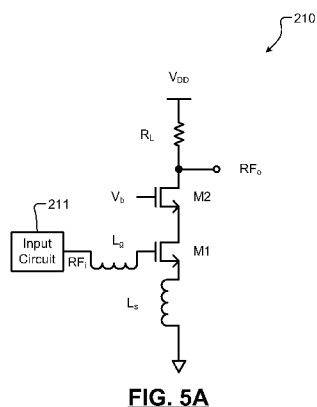


FIG. 5A

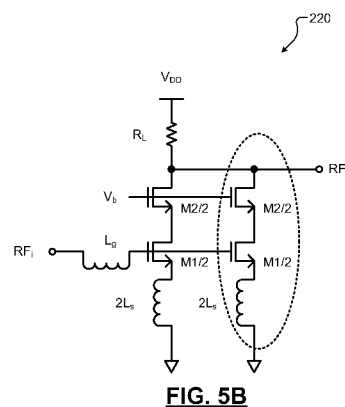


FIG. 5B

(57) Abstract: An amplifier integrated circuit (IC) includes a push-pull configuration including a push stage and a pull stage. A first loop of wire is configured to form a first degeneration inductance of the push stage. A second loop of wire is configured to form a first degeneration inductance of the pull stage. The first and second loops are concentric.

PUSH-PULL LOW-NOISE AMPLIFIER WITH AREA-EFFICIENT
IMPLEMENTATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S.
5 Patent Application No. 12/772,654, filed May 3, 2010, which
claims the benefit of U.S. Provisional Application No.
61/177,759, filed May 13, 2009. The disclosures of the
above applications are incorporated herein by reference in
their entirety.

10 FIELD

[0002] The present disclosure relates communication
devices and more particularly to push-pull low-noise
amplifiers (LNAs) used in the communication devices.

BACKGROUND

15 **[0003]** The background description provided herein is
for the purpose of generally presenting the context of the
disclosure. Work of the presently named inventors, to the
extent the work is described in this background section, as
well as aspects of the description that may not otherwise
20 qualify as prior art at the time of filing, are neither
expressly nor impliedly admitted as prior art against the
present disclosure.

[0004] Communication devices include cellular devices,
Bluetooth® (BT) devices, global positioning system (GPS)
25 devices, and network devices. The network devices may
comply with various standards such as those set forth by
the Institute of Electrical and Electronics Engineers
(IEEE), the third Generation Partnership Project (3GPP),
and other standards organizations. The communication
30 devices typically transmit and receive radio frequency (RF)
signals via RF transceivers. The RF transceivers may be

occasionally integrated into integrated circuits (ICs) used in the devices.

[0005] Referring now to FIG. 1, a communication device 10 comprises transceivers 12-1, 12-2, . . . , and 12-N (collectively transceivers 12), where N is an integer greater than 1. The transceivers 12 may comply with different communication standards. For example, the transceiver 12-1 may comply with the BT standard, the transceiver 12-2 may comply with the 3GPP standard, and so on. Occasionally, the communication device 10 may communicate via multiple frequency bands. Accordingly, some of the transceivers 12 may be multi-band transceivers.

[0006] Referring now to FIG. 2A, an RF transceiver 100 comprises a transmitter 102 that transmits RF signals and a receiver 104 that receives RF signals via an antenna 105. The transmitter 102 may be a super-heterodyne transmitter, a direct conversion transmitter, or other suitable transmitter. The receiver 104 may be a super-heterodyne receiver, a direct conversion receiver, or other suitable receiver.

[0007] Although a single antenna is shown, the RF transceiver 100 may transmit and receive the RF signals via a plurality of antennas. For example, the plurality of antennas may be arranged in a multiple-input multiple-output (MIMO) configuration.

[0008] Referring now to FIG. 2B, the receiver 104 typically includes an RF front-end module 106 and an RF downconverter module 108. The RF front-end module 106 typically includes a low-noise amplifier (LNA) 110 and a filter 112. The LNA 110 amplifies the RF signals received via the antenna 105. The filter 112 filters the output of the LNA 110.

[0009] The RF downconverter module 108 typically includes an LNA 114 and a downconversion mixer 116. The LNA 114 amplifies the output of the filter 112. The downconversion mixer 116 may downconvert RF signals to
5 baseband signals using mixers 118 and 120, which are arranged in a quadrature configuration. An oscillator 122 and a 90-degree phase shifter 124 generate clock signals that clock the mixers 118 and 120, respectively. The mixers 118 and 120 generate in-phase (I) and quadrature (Q)
10 outputs, respectively, which are input to baseband processing circuits for further processing.

[0010] Thus, transceivers typically include a plurality of LNAs. Further, multi-band transceivers typically include a plurality of LNAs per band.

15 SUMMARY

[0011] An amplifier integrated circuit (IC) comprises a push-pull configuration including a push stage and a pull stage. A first loop of wire is configured to form a first degeneration inductance of the push stage. A second loop
20 of wire is configured to form a first degeneration inductance of the pull stage. The first and second loops are concentric.

[0012] In other features, the amplifier IC further comprises a first trace configured to input a first signal
25 to the amplification stage and a second trace configured to input a second signal to the amplification stage. The first trace is adjacent and proximate to a first portion of the first loop. The second trace is adjacent and proximate to a second portion of the first loop. The second portion
30 is arranged across from and opposite to the first portion.

[0013] In other features, the first and second loops each have a first terminal and a second terminal. The pull

stage comprises a first transistor having a first terminal configured to connect to the first terminal of the first loop, a second terminal, and a control terminal. The push stage comprises a second transistor having a first terminal
5 configured to connect to the first terminal of the second loop, a second terminal, and a control terminal. The second terminals of the first and second loops are configured to connect to a common potential and a supply voltage, respectively.

10 **[0014]** In other features, the pull stage further comprises a third transistor having a first terminal configured to connect to the second terminal of the first transistor, and a second terminal. The push stage further comprises a fourth transistor having a first terminal
15 configured to connect to the second terminal of the third transistor, and a second terminal configured to connect to the second terminal of the second transistor.

[0015] In other features, the amplifier IC further comprises an input inductance having a first terminal
20 configured to receive an input signal and a second terminal configured to connect to the control terminal of the first transistor. The amplifier IC further comprises a capacitance having a first terminal configured to connect to the control terminal of the first transistor and a
25 second terminal configured to connect to the control terminal of the second transistor.

[0016] Further areas of applicability of the present disclosure will become apparent from the detailed description, the claims and the drawings. The detailed
30 description and specific examples are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF DRAWINGS

[0017] The present disclosure will become more fully understood from the detailed description and the accompanying drawings, wherein:

5 [0018] FIG. 1 is a functional block diagram of a communication device according to the prior art;

 [0019] FIG. 2A is a functional block diagram of a transceiver according to the prior art;

10 [0020] FIG. 2B is a functional block diagram of a receiver according to the prior art;

 [0021] FIG. 3 is a schematic of a differential low-noise amplifier (LNA);

 [0022] FIG. 4 is a schematic of a differential LNA comprising an inductance formed using a loop of wire;

15 [0023] FIG. 5A-5D depict building blocks of single-ended and differential push-pull LNAs;

 [0024] FIG. 6 is a schematic of a differential push-pull LNA comprising two separate loops used to form inductances of amplification and push-pull stages;

20 [0025] FIGs. 7A-7D depict an area-efficient implementation of inductances that is used when push-pull LNAs are integrated in integrated circuits (ICs);

 [0026] FIG. 8 is a schematic of a differential push-pull LNA comprising the area-efficient implementation of
25 inductances;

 [0027] FIG. 9A is a schematic of a single-ended push-pull LNA;

 [0028] FIG. 9B is a schematic of a single-ended push-pull LNA comprising two separate loops used to form
30 inductances of amplification and push-pull stages;

 [0029] FIG. 9C is a schematic of a single-ended push-pull LNA comprising the area-efficient implementation of inductances;

[0030] FIG. 10A is a schematic of a single-ended LNA without a cascode transistor;

[0031] FIG. 10B depicts layout of a spiral inductor used to implement a source degenerating inductance when the
5 single-ended LNA of FIG. 10A is integrated in an IC;

[0032] FIG. 10C is a schematic of a single-ended push-pull LNA without cascode transistors;

[0033] FIG. 10D depicts layout of concentric spiral inductors used to implement source degenerating inductances
10 when the single-ended push-pull LNA of FIG. 10C is integrated in an IC;

[0034] FIG. 10E depicts formation of the concentric spiral inductors of FIG. 10D by slicing the spiral inductor of FIG. 10B;

[0035] FIGS. 11A-11C depict examples of different
15 shapes of the spiral inductors shown in FIG. 10B, 10D, and 10E;

[0036] FIG. 12 depicts an IC comprising a differential push-pull LNA that uses the area-efficient implementation
20 of inductances;

[0037] FIG. 13 depicts layout of the area-efficient inductances in the IC of FIG. 12;

[0038] FIG. 14 depicts layout of the area-efficient inductances and traces used to feed input signals to the
25 differential push-pull LNA in an IC;

[0039] FIG. 15 depicts layout of the area-efficient inductances and traces that are proximate to the area-efficient inductances in an IC;

[0040] FIG. 16 depicts an IC comprising a differential
30 push-pull LNA that includes the area-efficient inductances and traces as shown in FIG. 15; and

[0041] FIG. 17 depicts coupling between the traces and the area-efficient inductances of FIG. 16.

DESCRIPTION

[0042] The following description is merely exemplary in nature and is in no way intended to limit the disclosure, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A or B or C), using a non-exclusive logical OR. It should be understood that steps within a method may be executed in different order without altering the principles of the present disclosure.

[0043] Referring now to FIG. 3, a low-noise amplifier (LNA) 200 is shown. For example only, the LNA 200 may be implemented using complementary metal-oxide semiconductor (CMOS) field-effect transistors (FETs). For example only, the present disclosure includes examples of LNAs that use negative MOS (NMOS) transconductance amplifiers and NMOS cascode transistors. One of ordinary skill in the art would understand, however, that the LNAs shown and described in the present disclosure may instead comprise PMOS transconductance amplifiers and PMOS cascode transistors.

[0044] In FIG. 3, for example, the LNA 200 comprises NMOS transistors M1-M4 arranged in a cascode configuration. Transistors M1 and M3 are transconductance amplifiers. The transistor M1 receives an input RF_{in} (negative) via an inductance L_g . The transistor M3 receives an input RF_{ip} (positive) via an inductance L_g .

[0045] An inductance L_s is connected to a source of each transistor M1, M3. A resistive load R_L is connected to each cascode transistor M2 and M4. Outputs RF_{op} (positive) and RF_{on} (negative) are generated across the resistive loads

connected to the cascode transistors M2 and M4, respectively.

[0046] The LNA 200 uses inductive source degeneration to match the input impedance of the LNA 200 to an impedance of an input circuit 150 that inputs RF_{in} and RF_{ip} into the LNA 200. Specifically, a transconductance (g_m) of the transistors M1 and M3 and a reactance of the inductances L_s generate the input impedance of the LNA 200. A real component of the input impedance approximately matches the impedance of the input circuit 150 that inputs RF_{in} and RF_{ip} into the LNA 200. Accordingly, the inductances L_s are called source degenerating inductances.

[0047] When the LNA 200 is integrated in an integrated circuit (IC) in differential form, the source degenerating inductances L_s are implemented as a loop of wire having an inductance of $2L_s$. The loop may include one or more turns of wire. The loop has a center tap and ports a and b that connect to points a and b of the LNA 200, respectively.

[0048] Referring now to FIG. 4, an LNA 201 that may be integrated into an IC is shown. The LNA 201 differs from the LNA 200 of FIG. 3 in at least one respect. In the LNA 201, the source degenerating inductances L_s of the LNA 200 are implemented as a loop 202 of wire having an inductance of $2L_s$. The loop 202 may include one or more turns of wire. The loop 202 has a center tap 203 and ports a and b that connect to points a and b of the LNA 201, respectively. The loop 202 is connected to a common potential as shown. Accordingly, the inductance across the source of each of the transistors M1 and M3 and the common potential is L_s .

[0049] Typically, a transceiver may comprise a plurality of LNAs. For example, the RF front-end module and the RF downconverter module of the transceiver may each comprise an LNA. Each LNA may comprise a loop. When the

transceiver is integrated in an IC, the loops of the LNAs occupy a large area of the IC.

[0050] Additionally, the LNAs are generally input amplifiers (i.e., amplifiers used in input stages of the transceiver). Accordingly, the LNAs do not use a push-pull configuration that is typically used in output amplifiers (i.e., amplifiers used in output stages). For example, the push-pull configuration is typically used in power amplifiers such as class A and class B amplifiers used in output stages. The push-pull configuration, however, increases efficiency and decreases power consumption of amplifiers. Accordingly, without the push-pull configuration, the LNAs have lower efficiency and higher power consumption.

[0051] The present disclosure relates to high-efficiency and area-efficient LNAs. Specifically, the LNAs use the push-pull configuration to increase the efficiency of the LNAs. Particularly, the power consumption of the LNAs is reduced since the LNAs with the push-pull configuration use only half the current used by conventional LNAs. Further, the gains in efficiency and power consumption are achieved without substantially trading off linearity and noise levels of the LNAs.

[0052] Additionally, the LNAs according to present disclosure use an area-efficient implementation of inductors that reduces the area occupied by the loops in ICs. The area-efficient implementation is further optimized (i.e., area of inductor layout is further reduced) by coupling input lines of the LNAs to the inductors.

[0053] The present disclosure is organized as follows. In FIGs. 5A-5D, the push-pull configuration of the LNAs is shown in further detail. In FIGs. 6-8, the area-efficient

implementation of inductors in differential LNAs is shown. In FIGs. 9A-11C, area-efficient implementation of inductors in single-ended LNAs is shown. In FIGs. 12-17, the area of inductor layout is further reduced by coupling input lines
 5 of the LNAs to the inductors.

[0054] Referring now to FIGs. 5A-5D, building blocks of single-ended and differential push-pull LNAs are shown. In FIG. 5A, a single-ended LNA 210 is shown. In FIG. 5B, the single-ended LNA 210 is split into two parallel
 10 sections forming an LNA 220. In FIG. 5C, one of the sections of the amplifier of FIG. 5B is converted from NMOS to PMOS forming a single-ended push-pull LNA 230. In FIG. 5D, a differential push-pull LNA 240 is formed using the single-ended push-pull LNA 230 of FIG. 5C.

[0055] In FIG. 5A, the single-ended LNA 210 comprises NMOS transistors M1 and M2 arranged in a cascode configuration. The transistor M1 is a transconductance amplifier and receives an input RF_i via an inductance L_g . A source degenerating inductance L_s is connected to a source
 15 of the transistor M1. A resistive load R_L is connected to a cascode transistor M2. A bias voltage V_b biases the cascode transistor M2. An output RF_o is generated across the resistive load R_L .
 20

[0056] The single-ended LNA 210 uses inductive source degeneration to match the input impedance of the single-ended LNA 210 to an impedance of an input circuit 211 that
 25 inputs RF_i into the single-ended LNA 210. Specifically, the transconductance (g_m) of the transistor M1 and the reactance of the source degenerating inductance L_s generate the input impedance of the single-ended LNA 210. A real component of the input impedance approximately matches the impedance of the input circuit 211 that inputs RF_i into the single-ended
 30 LNA 210.

[0057] In FIG. 5B, the single-ended LNA 210 is split into two sections, and the two sections are connected in parallel to form the LNA 220. Thus, the LNA 220 essentially comprises two sections of the single-ended LNA 210. The inductances $2L_s$ connected to each source of transistors M1/2 effectively form a parallel combination with a net inductance of L_s .

[0058] In FIG. 5C, the section of the LNA 220 identified by a dotted oval is converted from NMOS to PMOS. The PMOS section is connected to the NMOS section as shown to form the single-ended push-pull LNA 230. The PMOS section may be called a push stage, and the NMOS section may be called a pull stage of the single-ended push-pull LNA 230.

[0059] A bias voltage V_{bn} is used to bias the NMOS transistor M2/2, which is the cascode transistor of the NMOS section. A bias voltage V_{bp} is used to bias the PMOS transistor MP2, which is the cascode transistor of the PMOS section. An AC coupling capacitor C_{ac} is used to couple the input RF_i to the PMOS transistor MP1, which is the transconductance amplifier of the PMOS section.

[0060] The NMOS section includes a source degenerating inductance $2L_s$ connected to the source of the NMOS transistor M1/2. The PMOS section includes a source degenerating inductance $2L_s'$ connected to the source of the PMOS transistor MP1. The source degenerating inductances $2L_s$ and $2L_s'$ may be equal or approximately equal. The NMOS transistor M1/2 and the PMOS transistor MP1 may each have a transconductance (g_m). The input impedance generated by the g_m of MP1 and the reactance of $2L_s'$ is the same as the input impedance generated by the g_m of M1/2 and the reactance of $2L_s$.

[0061] The single-ended push-pull LNA 230 comprises two source degenerating inductances each having twice the source degenerating inductance of the single-ended LNA 210. Accordingly, when the single-ended push-pull LNA 230 is used in an IC, the source degenerating inductances of the single-ended push-pull LNA 230 occupy more area of the IC than the source degenerating inductance of the single-ended LNA 210.

[0062] In FIG. 5D, the differential push-pull LNA 240 is formed using the single-ended push-pull LNAs 230. The two PMOS sections of the differential push-pull LNA 240 comprising transistors MP1a, MP2a, MP1b, and MP2b may be called a push stage of the differential push-pull LNA 240. The two NMOS sections of the differential push-pull LNA 240 comprising transistors M1a/2, M2a/2, M1b/2, and M2b/2 may be called a pull stage of the differential push-pull LNA 240.

[0063] The differential push-pull LNA 240 comprises four source degenerating inductances: two inductances of value $2L_s$ and two inductances of value $2L_s'$. Accordingly, when the differential push-pull LNA 240 is used in an IC, the source degenerating inductances of the differential push-pull LNA 240 occupy more area of the IC than the source degenerating inductance of the single-ended push-pull LNA 230.

[0064] Referring now to FIG. 6, a differential push-pull LNA 250 includes a first implementation of inductances. The differential push-pull LNA 250 differs from the differential push-pull LNA 240 of FIG. 5D in at least one respect. In the differential push-pull LNA 250, the two inductances each of value $2L_s$ connected to the sources of transconductance amplifiers M1a/2 and M1b/2 are implemented as a loop 252 having an inductance of $4L_s$. The

loop 252 may include one or more turns of wire. The loop 252 has a center tap 254 and ports a and b that connect to points a and b of the differential push-pull LNA 250, respectively. The loop 252 is connected to a common potential as shown. Accordingly, the inductance across the source of each of the transistors M1a/2 and M1b/2 and the common potential is $2L_s$.

[0065] Additionally, in the differential push-pull LNA 250, the two inductances each of value $2L_s'$ connected to the sources of transconductance amplifiers MP1a/2 and MP1b/2 are implemented as a loop 262 having an inductance of $4L_s'$. The inductances $4L_s$ and $4L_s'$ may be equal or approximately equal. The loop 262 may include one or more turns of wire. The loop 262 has a center tap 264 and ports c and d that connect to points c and d of the differential push-pull LNA 250, respectively. The loop 262 is connected to a supply voltage V_{DD} as shown. Accordingly, the inductance across the source of each of the transistors MP1a/2 and MP1b/2 and the supply voltage V_{DD} is $2L_s'$. The inductances $2L_s$ and $2L_s'$ may be equal or approximately equal.

[0066] The differential push-pull LNA 250 uses only about half the current used by the LNA 201 of FIG. 4. Accordingly, the differential push-pull LNA 250 consumes less power than the LNA 201 of FIG. 4. Additionally, the linearity and noise levels of the differential push-pull LNA 250 are substantially the same as the linearity and noise levels of the LNA 201. When integrated in an IC, however, the differential push-pull LNA 250, which uses two loops 252 and 262, occupies a larger area of the IC than the LNA 201.

[0067] Referring now to FIG. 7A-7D, the area occupied by an LNA in an IC can be reduced by using a second implementation of inductances as follows. The

second implementation includes cutting or slicing a loop that is used to implement an inductance into two halves. The wire used to form the loop is sliced along the length of the wire. For example, the wire may be sliced at the center. The resulting two halves are concentric. Each half loop has the same or approximately the same inductance as the whole loop.

[0068] Accordingly, a single loop having an inductance L , when cut into two concentric halves, may be used as two loops each having the inductance L . Thus, one of the two loops 252 and 262 of the differential push-pull LNA 250 may be eliminated, and the area occupied by the differential push-pull LNA 250 in an IC may be reduced.

[0069] In FIG. 7A, for example, the loop 202 having an inductance $2L_s$ is shown. In FIG. 7B, the loop 202 is sliced into half as shown by a dotted circle. A wire of width W that is used to form the loop 202 may be sliced along the length of the wire. The wire may be sliced at the center of the width so that the resulting halves (concentric loops) 204 and 206 each have a width of $W/2$.

[0070] For example, the loop 202 formed using the wire may have an outer radius $R1$ and an inner radius $R2$. The width W of the wire may be defined as $W = (R1 - R2)$. The loop 202 may be sliced along the length of the wire at the center of the width W so that the resulting concentric loops 204 and 206 each have a width of $W/2$.

[0071] The loop 202 is shown to be circular in shape for example only. Other shapes are contemplated. A non-exclusive list of the other shapes includes ovals, triangles, quadrangles, and polygons.

[0072] When the loop 202 having an inductance $2L_s$ is sliced into half as described, the resulting concentric loops 204 and 206 each have the inductance $2L_s$. This is

because changing the width/diameter of the wire by slicing the wire into half does not change or only slightly changes the inductance of the concentric loops 204 and 206. Changing the width changes only a parasitic resistance of the resulting concentric loops 204 and 206.

[0073] One of the concentric loops 204 and 206 may be connected to the nodes a and b while the other half may be connected to the nodes c and d of the differential push-pull LNA 250 of FIG. 6. When the concentric loops 204 and 206 are separated by a small space, no current (DC or AC) flows across the dotted line (i.e., from one half to another and vice versa). Accordingly, when the concentric loops 204 and 206 are separated by a small space, each half can be at a different DC potential. An AC potential difference between the nodes a and b, however, can be and is the same as the AC potential difference between the nodes c and d. Thus, while the DC properties of the concentric loops 204 and 206 can be varied, the RF properties of the concentric loops 204 and 206 are the same as the RF properties of the loop 202.

[0074] In FIG. 7C, the concentric loops 204 and 206 are shown in a schematic form. Accordingly, the dotted circle is omitted. Each of the concentric loops 204 and 206 has an inductance of $2L_s$. Further, a coupling coefficient K of the concentric loops 204 and 206 is approximately 1 (i.e., $K \approx 1$). Additionally, a mutual inductance of the concentric loops 204 and 206 is approximately $2L_s$. Thus, the concentric loops 204 and 206 each have an effective inductance of $4L_s$.

[0075] Accordingly, the concentric loops 204 and 206 can be connected to the nodes a-d of the differential push-pull LNA 250 as shown in FIG. 7D. The outer and inner concentric loops 204 and 206 may be connected to the common

potential and the supply voltage V_{DD} as shown, respectively. A DC current flows into the differential push-pull LNA 250 via the nodes c and d and returns via the nodes a and b as shown.

5 **[0076]** Referring now to FIG. 8, a differential push-pull LNA 260 comprises the concentric loops 204 and 206. Similar to the differential push-pull LNA 250, the differential push-pull LNA 260 uses only half the current used by the LNA 201 of FIG. 4. Accordingly, the
10 differential push-pull LNA 260 consumes less power than the LNA 201 of FIG. 4. Additionally, the linearity and noise levels of the differential push-pull LNA 260 are substantially the same as the linearity and noise levels of the LNA 201 and of the differential push-pull LNA 250.

15 **[0077]** The differential push-pull LNA 260, however, differs from the differential push-pull LNA 250 in at least one respect. When integrated in an IC, the differential push-pull LNA 260, which uses two concentric loops 204 and 206, occupies less area of the IC than the differential
20 push-pull LNA 250, which uses two separate loops 252 and 262.

[0078] Throughout the present disclosure, differential implementations of the LNAs are shown for example only. The teachings of the present disclosure can also be applied
25 to single-ended LNAs. Accordingly, similar gains in area and power consumption can be achieved without trading off linearity and noise in single-ended LNAs.

[0079] Referring now to FIGs. 9A-9C, for example, a single-ended push-pull LNA according to the present
30 disclosure is shown. In FIG. 9A, the single ended push-pull LNA 230 of FIG. 5C is redrawn for convenience. In FIG. 9B, a single ended push-pull LNA 231 uses two separate

loops 234 and 235 having inductances $2L_s$ and $2L_s'$ to implement the inductances $2L_s$ and $2L_s'$, respectively.

[0080] In FIG. 9C, a single ended push-pull LNA 232 uses concentric loops 208 and 209 according to the present disclosure. The concentric loops 208 and 209 replace the inductances $2L_s$ and $2L_s'$ shown in FIG. 9A and the loops 234 and 235 shown in FIG. 9B. The concentric loops 208 and 209 are formed by slicing a loop having an inductance L_s as explained with reference to FIGs. 7A-7D. As explained with reference to FIGs. 7A-7D, the effective inductance of the concentric loops 208 and 209 is $2L_s$.

[0081] The single-ended push-pull LNAs 230, 231, and 232 use only about half the current used by the single-ended LNA 210 of FIG. 5A. Accordingly, the single-ended push-pull LNAs 230, 231, and 232 consume less power than the single-ended LNA 210 of FIG. 5A. Additionally, the linearity and noise levels of the single-ended push-pull LNAs 230, 231, and 232 are substantially the same as the linearity and noise levels of the single-ended LNA 210.

[0082] The single-ended push-pull LNA 232, however, differs from the single-ended push-pull LNA 231 in at least one respect. When integrated in an IC, the single-ended push-pull LNA 232, which uses two concentric loops 208 and 209, occupies less area of the IC than the single-ended push-pull LNA 230, which uses two loops 234 and 235.

[0083] Referring now to FIGs. 10A-10E, spiral inductors may be used to implement source degenerating inductances of single-ended LNAs. For simplicity of illustration, the single-ended LNAs are shown without the cascode configuration. One of ordinary skill in the art will understand, however, that the cascode configuration can be used with the single-ended LNAs as shown in FIGs. 9A-9C, for example.

[0084] In FIG. 10A, a single-ended LNA 233 without cascode configuration is shown. In FIG. 10B, a spiral inductor 234 is shown. When the single-ended LNA 233 is integrated in an IC, the source degenerating inductance L_s of the single-ended LNA 233 is implemented using the spiral inductor 234 to save space in the IC.

[0085] In FIG. 10C, a single-ended push-pull LNA 235 without cascode configuration is shown. In FIG. 10D, a concentric spiral inductor 236 is shown. The concentric spiral inductor 236 may be formed by slicing the spiral inductor 234 as shown in FIG. 10E. When the single-ended push-pull LNA 235 is integrated in an IC, the source degenerating inductances L_s of the single-ended push-pull LNA 235 are implemented using the concentric spiral inductor 236 to save space in the IC.

[0086] Referring now to FIGs. 11A-11C, the spiral inductors shown in FIGs. 10B, 10D, and 10E can have other shapes. For example, portions of the spiral inductors, such as a portion 234-1 of the spiral inductor 234 shown in FIG. 11A, can be bent at various angles as shown in FIG. 11B. For example only, FIG. 11B shows that a portion of the inductor is bent at one place. The portion, however, can be bent at more than one place. Alternatively, portions of the spiral inductors can be curved as shown in FIG. 11C. Still other shapes and configurations are contemplated.

[0087] Referring now to FIG. 12, an IC 300 comprising a differential push-pull LNA according to the present disclosure is shown. The inductances L_{p1} and L_{p2} are implemented by the outer loop 204 shown in FIG. 7D. The inductances L_{n1} and L_{n2} are implemented by the inner loop 206 shown in FIG. 7D. Typically, components external to the IC 300 are used to match the input impedance of the

differential push-pull LNA to an external input circuit 301 that inputs RF_{ip} and RF_{in} to the IC 300. For example, a shunt inductance L1 and a pair of series capacitances C1 external to the IC 300 may be used.

5 **[0088]** The two PMOS sections of the differential push-pull LNA comprising transistors MP1a, MP2a, MP1b, and MP2b may be called a push stage of the differential push-pull LNA. The two NMOS sections of the differential push-pull LNA 240 comprising transistors MN1a, MN2a, MN1b, and MN2b
10 may be called a pull stage of the differential push-pull LNA.

[0089] Referring now to FIG. 13, a layout of the IC 300 is shown. V_{DD} and V_{ss} are applied to center points of the widths of the concentric loops 204 and 206 as shown,
15 respectively. A transformer 302 comprising the concentric loops 204 and 206 is positioned adjacent to an edge 300-1 of the IC 300. The edge 300-1 is closer to the amplification stage than to the push-pull stage of the differential push-pull LNA. Thus, the transformer 302 is
20 positioned between the amplification stage of the differential push-pull LNA and the edge 300-1.

[0090] Referring now to FIG. 14, a first example of the transformer 302 is shown. In the first example, a transformer 302-1 is a two-element transformer that is used
25 to implement the concentric loops 204 and 206. The input lines or traces that feed RF_{in} and RF_{ip} into the differential push-pull LNA of the IC 300 are routed around the transformer 302-1 as shown. Specifically, a distance is maintained between the traces and the concentric loops 204
30 and 206. The distance is called a keep out distance.

[0091] The distance is kept to ensure that signals via the traces do not affect the performance of the concentric loops 204 and 206. In other words, the distance ensures

that there is no coupling between the traces and the concentric loops 204 and 206. The distance may be of the order of a few tens of microns. When the IC 300 comprises N differential push-pull LNAs (e.g., in multi-band transceivers), where N is an integer greater than 1, N times the keep out distance is used in the IC 300.

[0092] Referring now to FIG. 15, a second example of the transformer 302 is shown. In the second example, a transformer 302-2 is a three-element transformer. Two of the three elements are used to implement the concentric loops 204 and 206. A third element is used to implement the traces that feed RF_{in} and RF_{ip} into the differential push-pull LNA of the IC 300.

[0093] Effectively, the traces are routed adjacent and proximate to the concentric loops 204 and 206 without the keep out distance separating the traces from the concentric loops 204 and 206. Thus, the keep out distance is eliminated, and area in the IC 300 is freed for other uses. The freeing of area by eliminating the keep out distance is called compacting input lines or traces to the source degenerating inductors. The compacting reduces inductance values and lowers Q factors of the inductances implemented by the transformer 302-2.

[0094] In FIGs. 14 and 15, for example only, each loop comprises more than one turn of wire. Typically, an IC may have multiple metal layers. Crossovers connect the turns in different metal layers. When a loop includes a single turn of wire, the turn is implemented in one of the metal layers of the IC, and a crossover is unnecessary. Regardless of the number of turns, metallic substances in the area below and surrounding the turns is cleared to avoid interference with inductive properties of the loops due to coupling.

[0095] Referring now to FIG. 16, an IC 310 comprises a differential push-pull LNA that uses the three-element transformer 302-2 shown in FIG. 15. The transformer 302-2 shown in FIG. 15 implements the inductances L_{n1} , L_{n2} , L_{p1} , L_{p2} , L_{in+} , and L_{in-} as shown in FIG. 16. The traces used to feed RF_{in} and RF_{ip} into the differential push-pull LNA are replaced by elements of the transformer 302-2. The elements of the transformer 302-2 that replace the traces are identified as inductances L_{in+} and L_{in-} in FIG. 15. The inductances L_{in+} and L_{in-} are schematically shown in FIG. 16.

[0096] A coupling exists between the inductances L_{in+} and L_{in-} and the source degenerating inductances of the differential push-pull LNA. The coupling can be beneficial when the inductances are arranged with proper polarities as shown in FIG. 16.

[0097] The transformer 302-2 comprising the concentric loops 204 and 206 and the traces is positioned adjacent to the edge of the IC 310 that is closer to the amplification stage than to the push-pull stage. In other words, the transformer 302-2 is positioned between the amplification stage of the differential push-pull LNA and the edge of the IC 310 that is closer to the amplification stage than to the push-pull stage.

[0098] Referring now to FIG. 17, an example of coupling between the inductances L_{in+} and L_{in-} and the source degenerating inductances L_{n1} and L_{n2} is shown. As V_{ip} increases, V_1 decreases, and V_2 increases due to inductor coupling (K_{pp} and K_{nn}). Accordingly, the coupling boosts the V_{GS} across the transistor MN1a. Similar result obtains with opposite polarities with respect to V_{in} . Thus, the coupling between the inductances L_{in+} and L_{in-} and the source degenerating inductances increases the gain of the LNA. Consequently, the coupling improves noise filtering.

Additionally, the coupling increases Q factors of impedance matching circuits.

[0099] The broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification, and the following claims.

CLAIMS

What is claimed is:

1. An amplifier integrated circuit (IC) comprising:
a push-pull configuration including a push stage
5 and a pull stage;
a first loop of wire configured to form a first
degeneration inductance of the push stage; and
a second loop of wire configured to form a first
degeneration inductance of the pull stage, wherein the
10 first and second loops are concentric.
2. The amplifier IC of claim 1 further comprising:
a first trace configured to input a first signal
to the amplification stage, wherein the first trace is
15 adjacent and proximate to a first portion of the first
loop; and
a second trace configured to input a second
signal to the amplification stage, wherein the second trace
is adjacent and proximate to a second portion of the first
20 loop, and wherein the second portion is arranged across
from and opposite to the first portion.
3. The amplifier IC of claim 2, wherein the first
and second loops and the first and second traces are
25 arranged between the amplification stage and an edge of the
amplifier IC.
4. The amplifier IC of claim 1, wherein the first
loop is configured to form a second degeneration inductance
30 of the pull stage, and wherein the second loop is

configured to form a second degeneration inductance of the push stage.

5 5. The amplifier IC of claim 1, wherein the first and second loops have shapes of one of circles, spirals, and polygons, and wherein the first loop has a greater area than the second loop.

10 6. The amplifier IC of claim 1, wherein the first loop is connected to a common potential, and wherein the second loop is connected to a supply voltage.

15 7. The amplifier IC of claim 1, wherein:
 the first and second loops each have a first terminal and a second terminal;
 the pull stage comprises a first transistor having a first terminal configured to connect to the first terminal of the first loop, a second terminal, and a control terminal;
20 the push stage comprises a second transistor having a first terminal configured to connect to the first terminal of the second loop, a second terminal, and a control terminal; and
 the second terminals of the first and second
25 loops are configured to connect to a common potential and a supply voltage, respectively.

30 8. The amplifier IC of claim 7, wherein:
 the pull stage further comprises a third transistor having a first terminal configured to connect to the second terminal of the first transistor, and a second terminal; and

the push stage further comprises a fourth transistor having a first terminal configured to connect to the second terminal of the third transistor, and a second terminal configured to connect to the second terminal of the second transistor.

9. The amplifier IC of claim 8 further comprising:

an input inductance having a first terminal configured to receive an input signal and a second terminal configured to connect to the control terminal of the first transistor; and

a capacitance having a first terminal configured to connect to the control terminal of the first transistor and a second terminal configured to connect to the control terminal of the second transistor.

10. The amplifier IC of claim 1, wherein:

the first and second loops each have a first terminal and a second terminal;

the pull stage comprises:

a first transistor having a first terminal configured to connect to the first terminal of the first loop, a second terminal, and a control terminal configured to receive a first input signal, and

a second transistor having a first terminal configured to connect to the second terminal of the first loop, a second terminal, and a control terminal configured to receive a second input signal; and

the push stage comprises:

a third transistor having a first terminal configured to connect to the first terminal of the second loop, a second terminal, and a control terminal, and

a fourth transistor having a first terminal configured to connect to the second terminal of the second loop, a second terminal, and a control terminal.

5 11. The amplifier IC of claim 10, wherein:
the pull stage further comprises:

a fifth transistor having a first terminal configured to connect to the second terminal of the first transistor, and a second terminal, and

10 a sixth transistor having a first terminal configured to connect to the second terminal of the second transistor, and a second terminal; and

the push stage further comprises:

15 a seventh transistor having a first terminal configured to connect to the second terminal of the fifth transistor, and a second terminal configured to connect to the second terminal of the third transistor, and

20 an eighth transistor having a first terminal configured to connect to the second terminal of the sixth transistor, and a second terminal configured to connect to the second terminal of the fourth transistor.

12. The amplifier IC of claim 11 further comprising:

25 a first capacitance having a first terminal configured to connect to the control terminal of the first transistor and a second terminal configured to connect to the control terminal of the third transistor; and

30 a second capacitance having a first terminal configured to connect to the control terminal of the second transistor and a second terminal configured to connect to the control terminal of the fourth transistor.

13. The amplifier IC of claim 1, wherein the pull stage includes metal-oxide semiconductor field-effect transistors (MOSFETs) of a first polarity, and wherein the push stage includes MOSFETs of a second polarity that is
5 opposite to the first polarity.

14. A transceiver comprising the amplifier IC of claim 1, wherein the transceiver includes a receiver, wherein the receiver includes at least one low-noise
10 amplifier (LNA), and wherein the at least one LNA includes the amplification stage and the push-pull stage.

15. A communication device comprising the transceiver of claim 14.
15

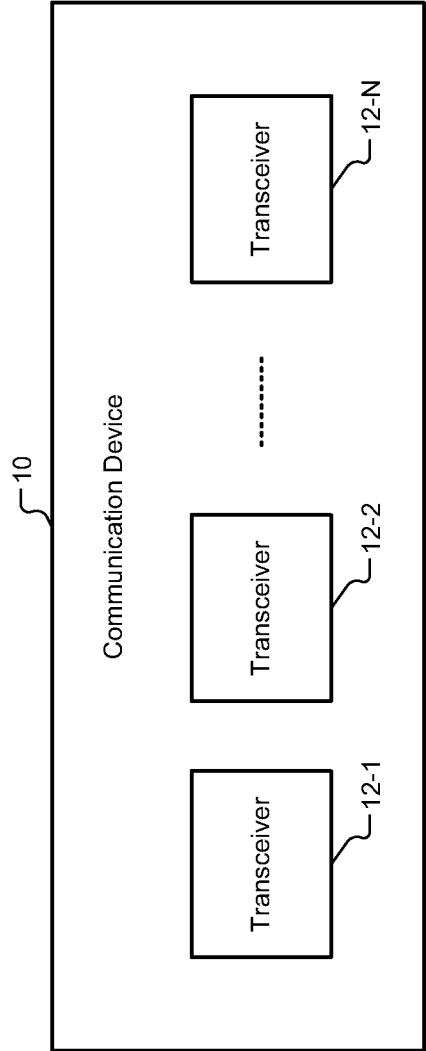


FIG. 1
Prior Art

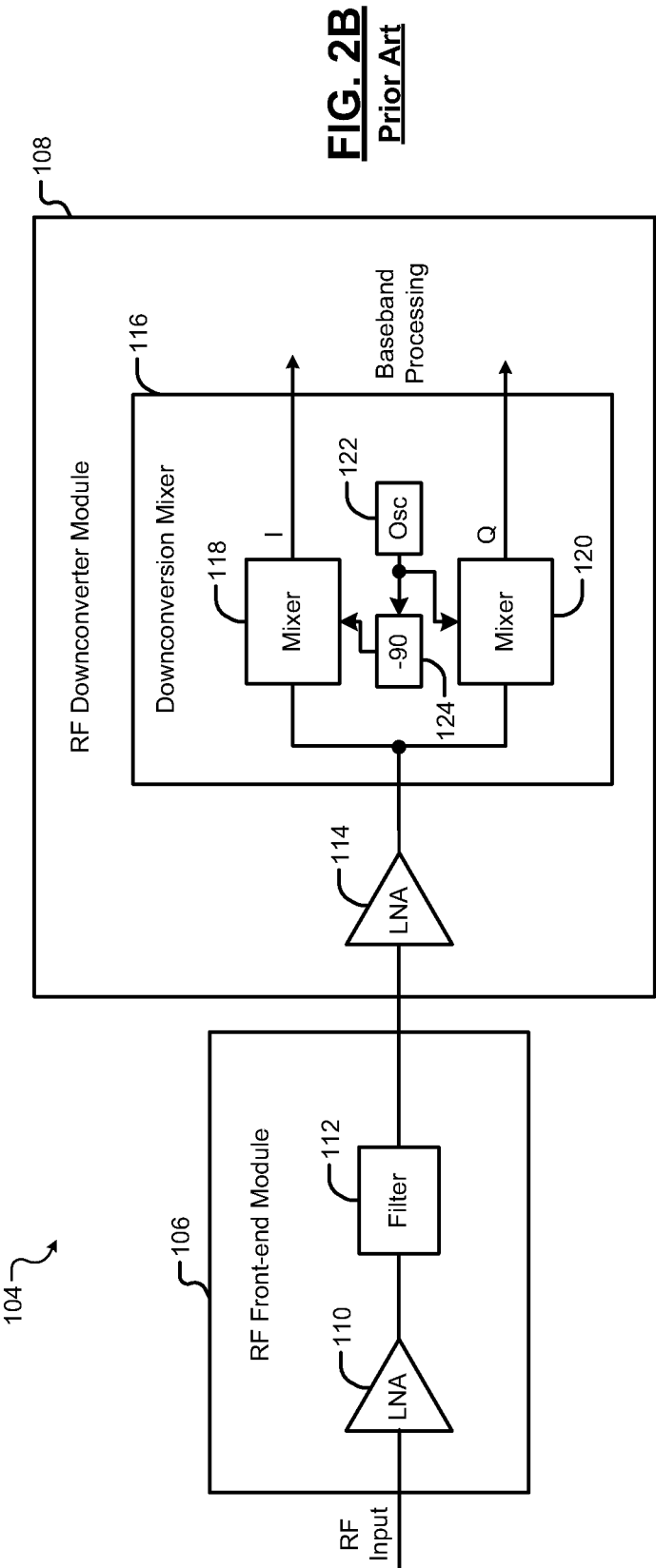
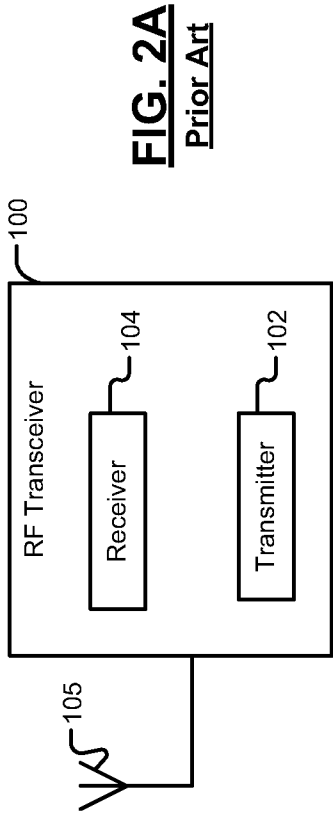


FIG. 2B

Prior Art

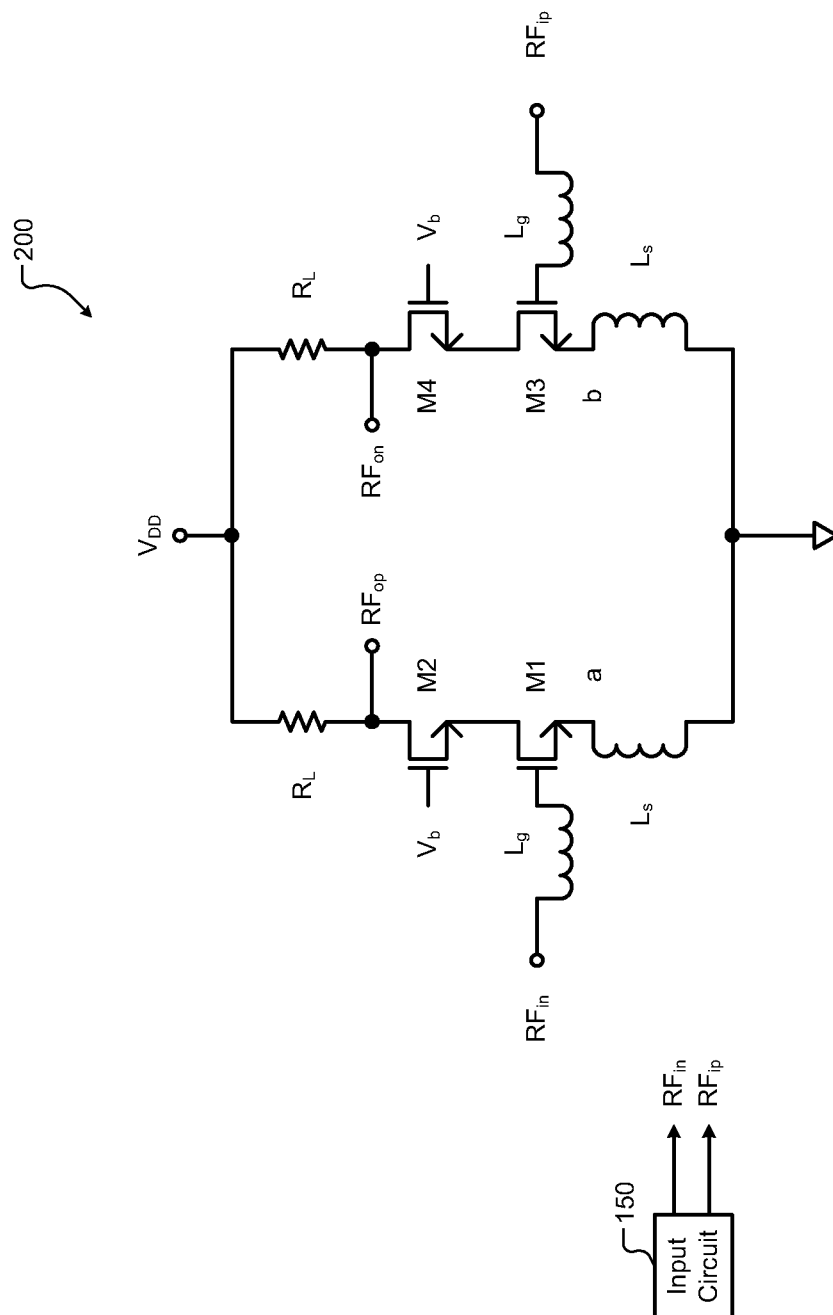


FIG. 3

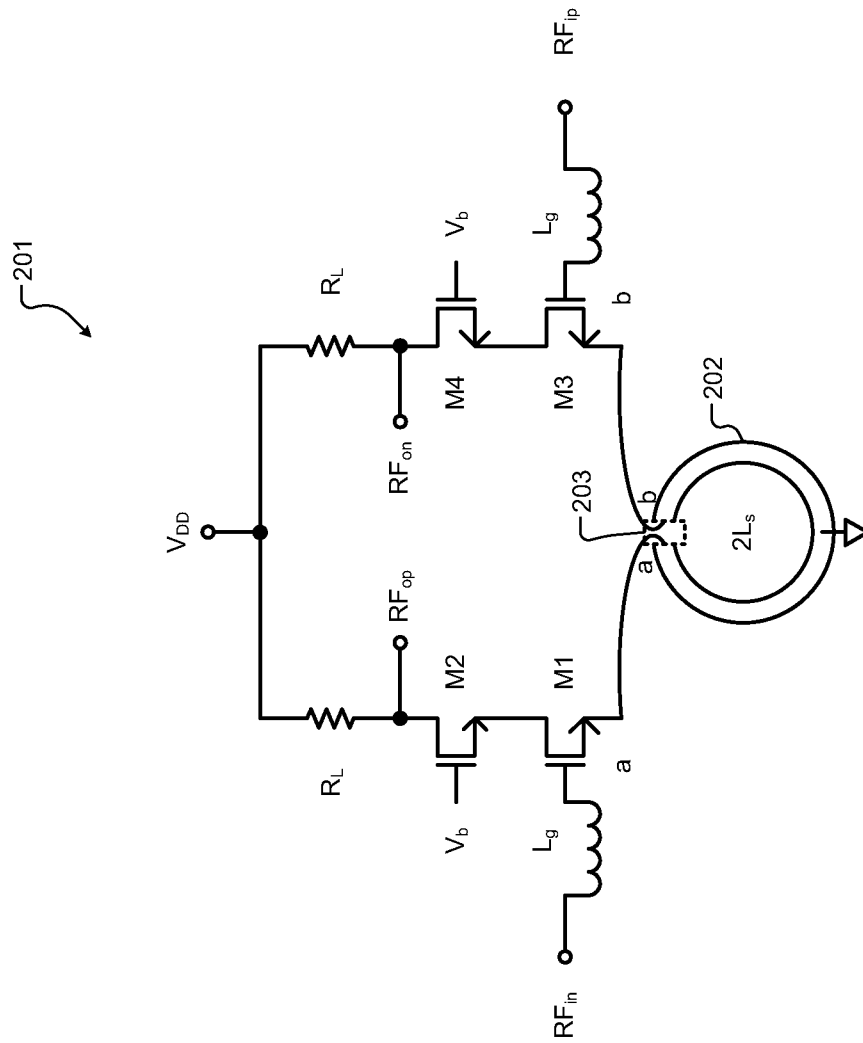


FIG. 4

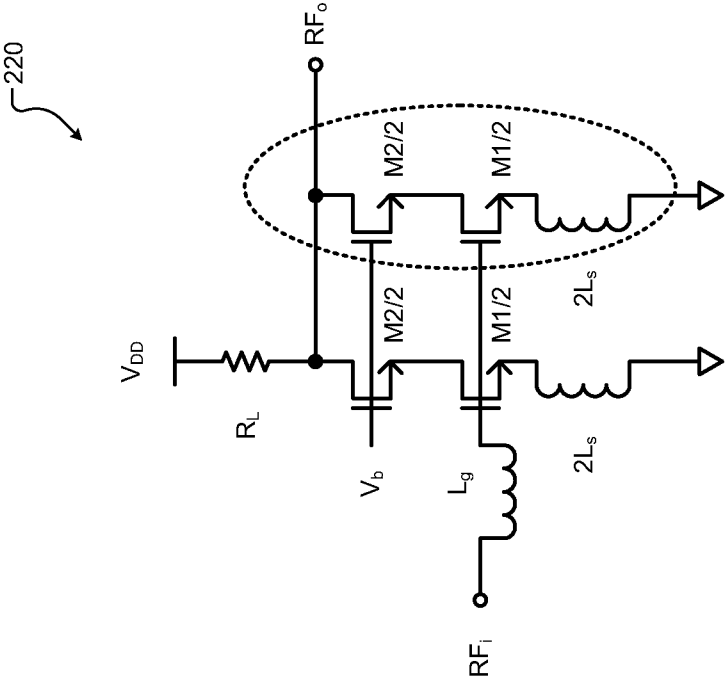


FIG. 5B

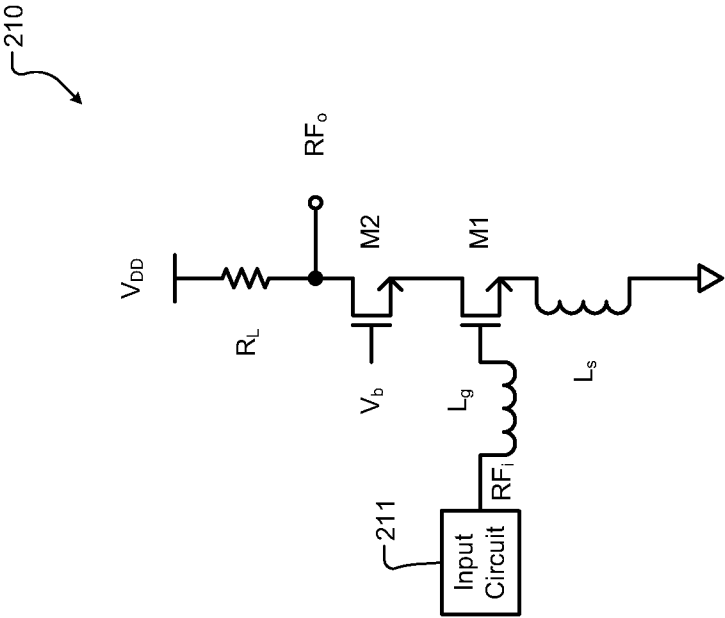


FIG. 5A

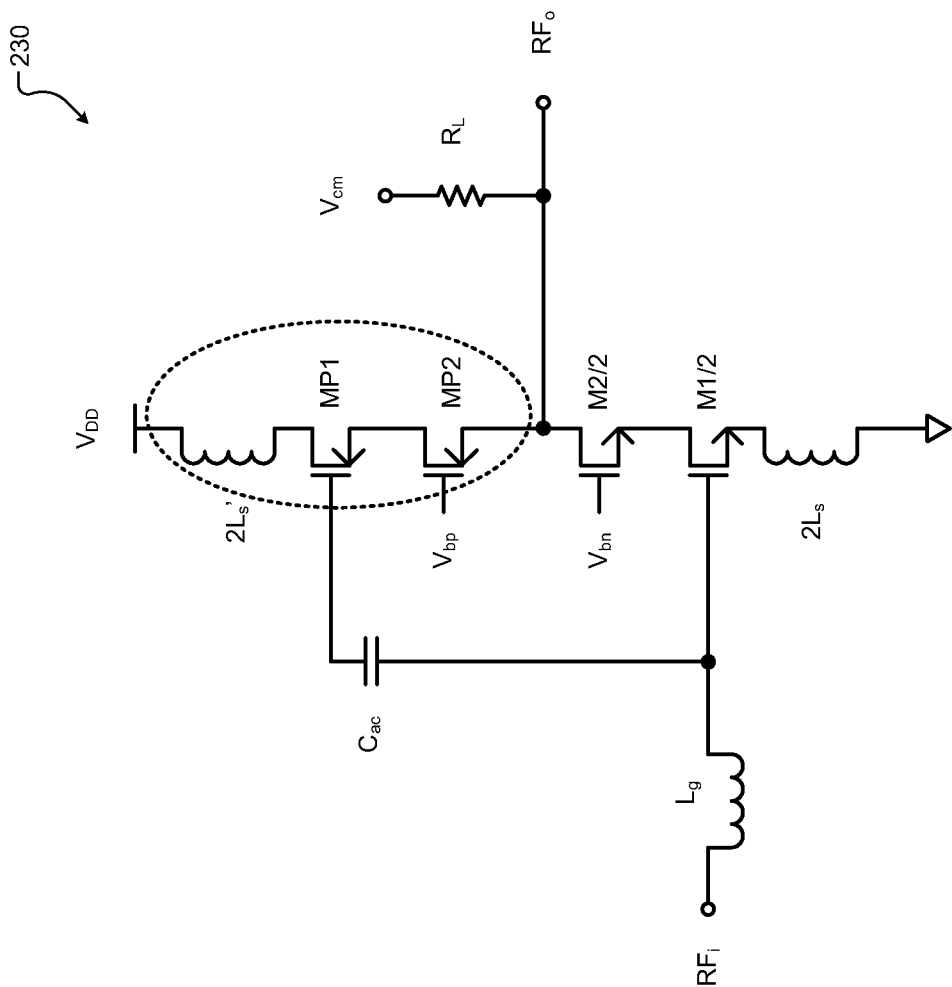


FIG. 5C

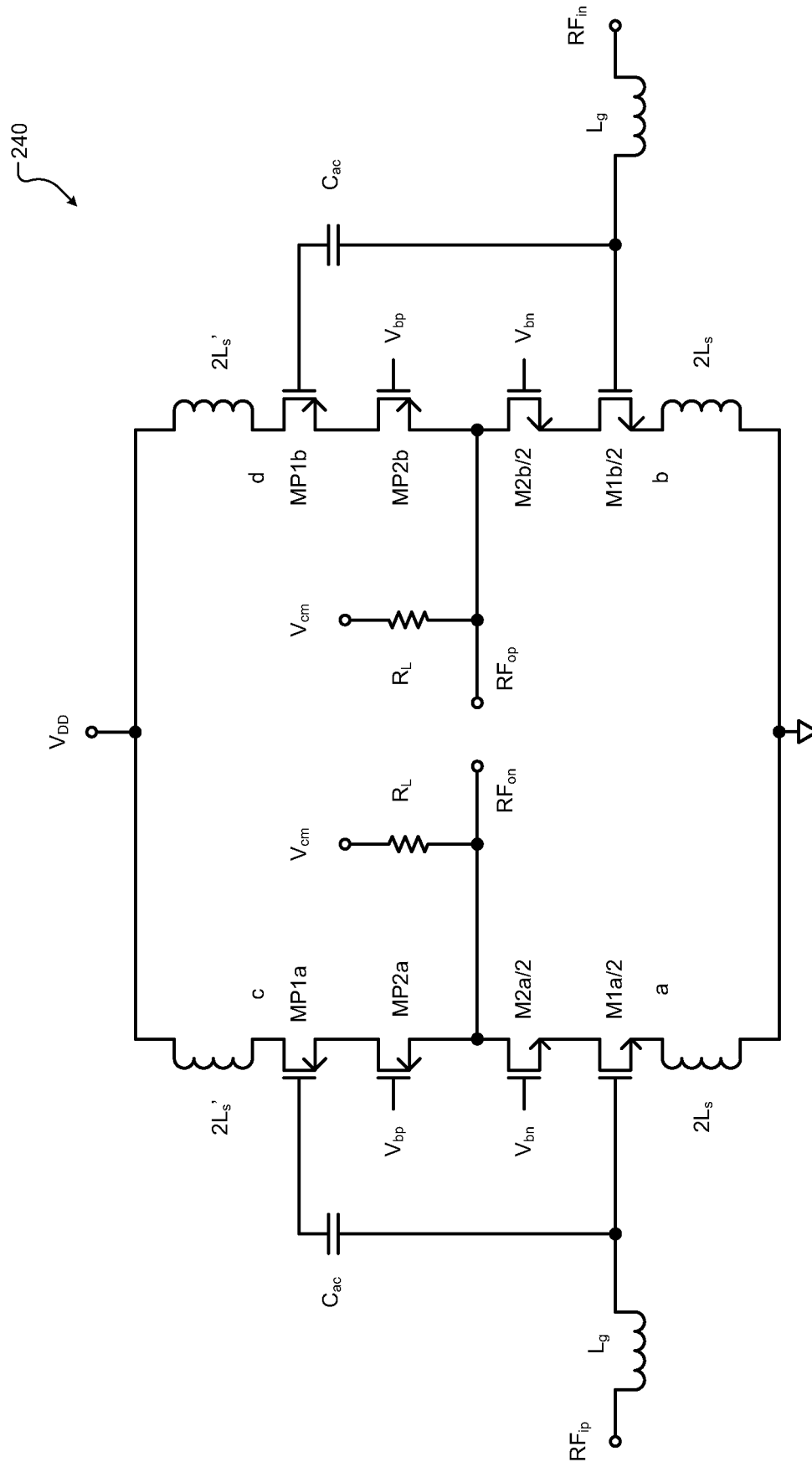


FIG. 5D

8/22

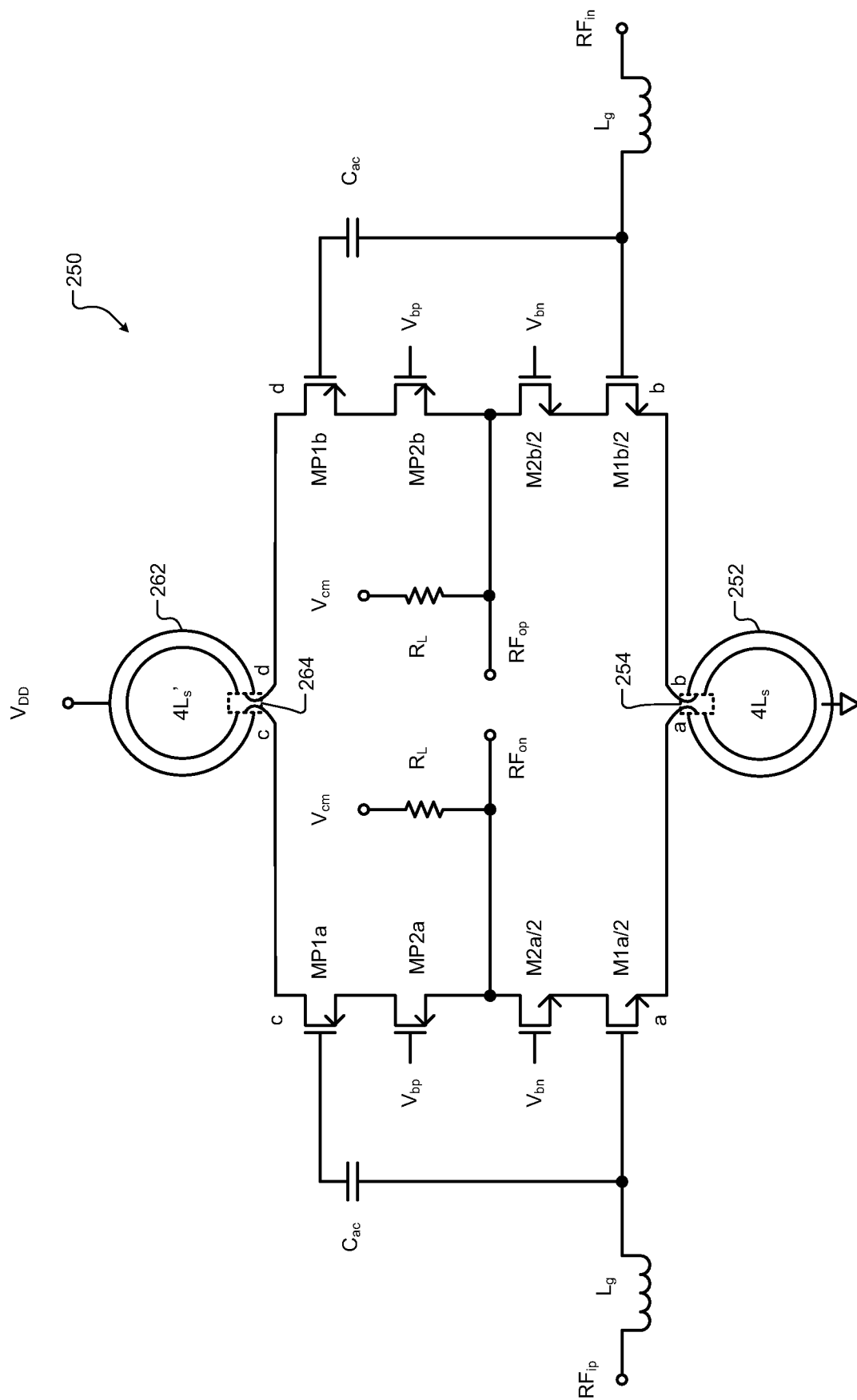


FIG. 6

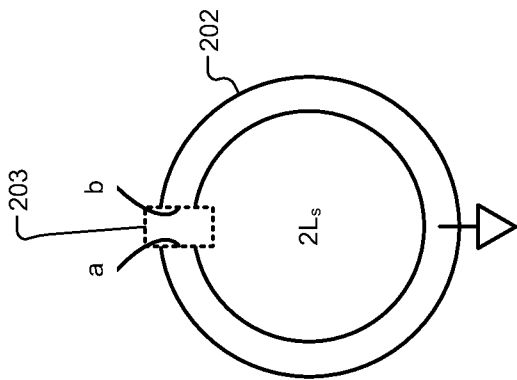


FIG. 7A

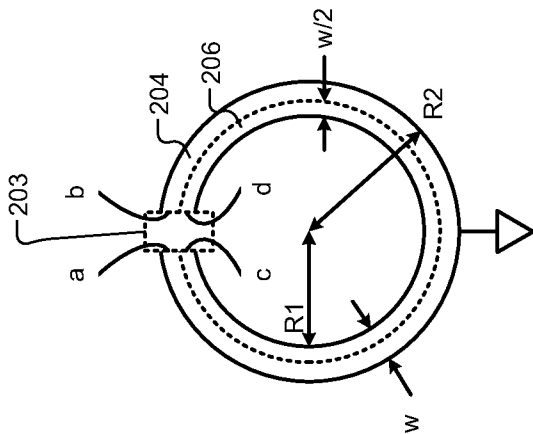


FIG. 7B

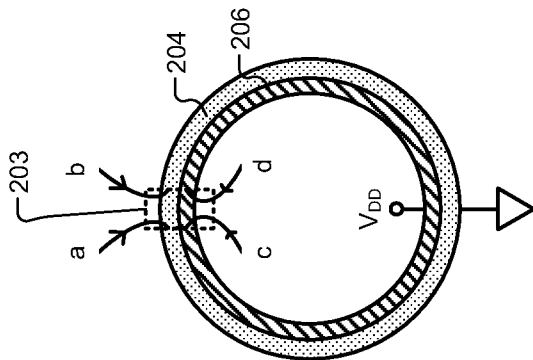


FIG. 7D

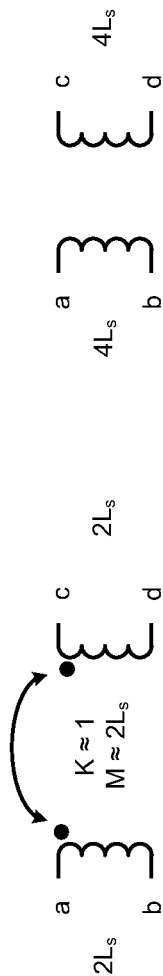


FIG. 7C

10/22

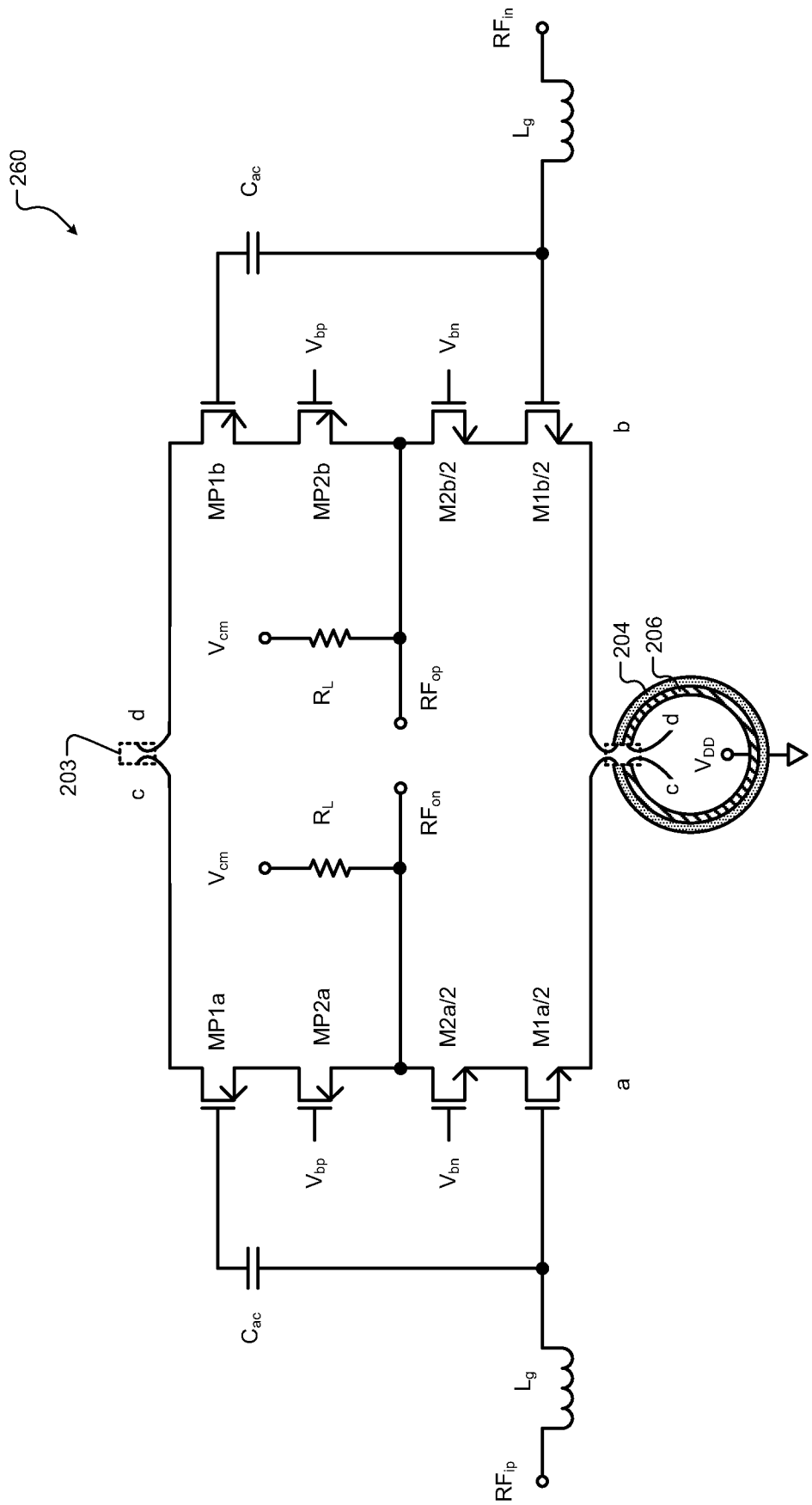


FIG. 8

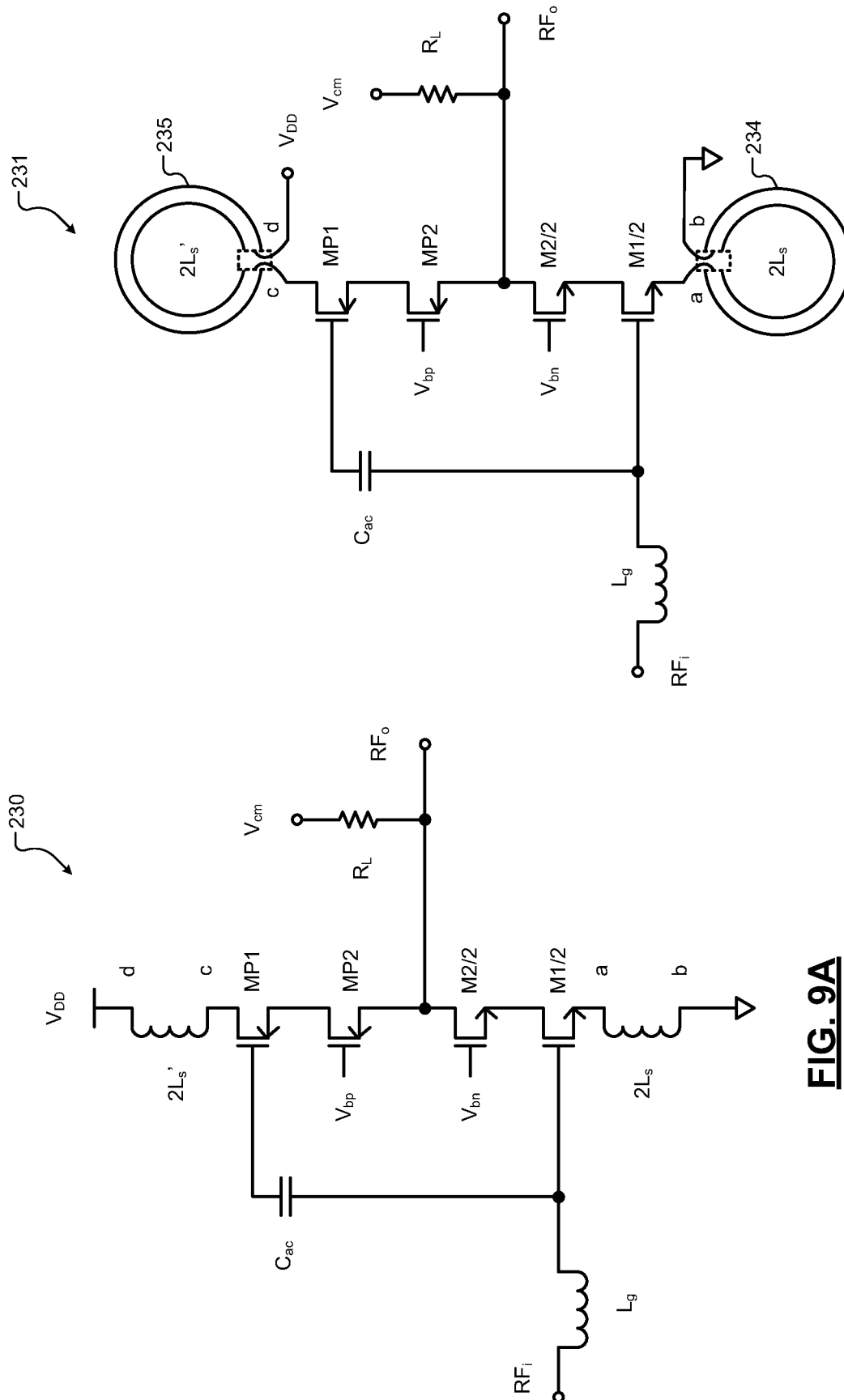


FIG. 9B

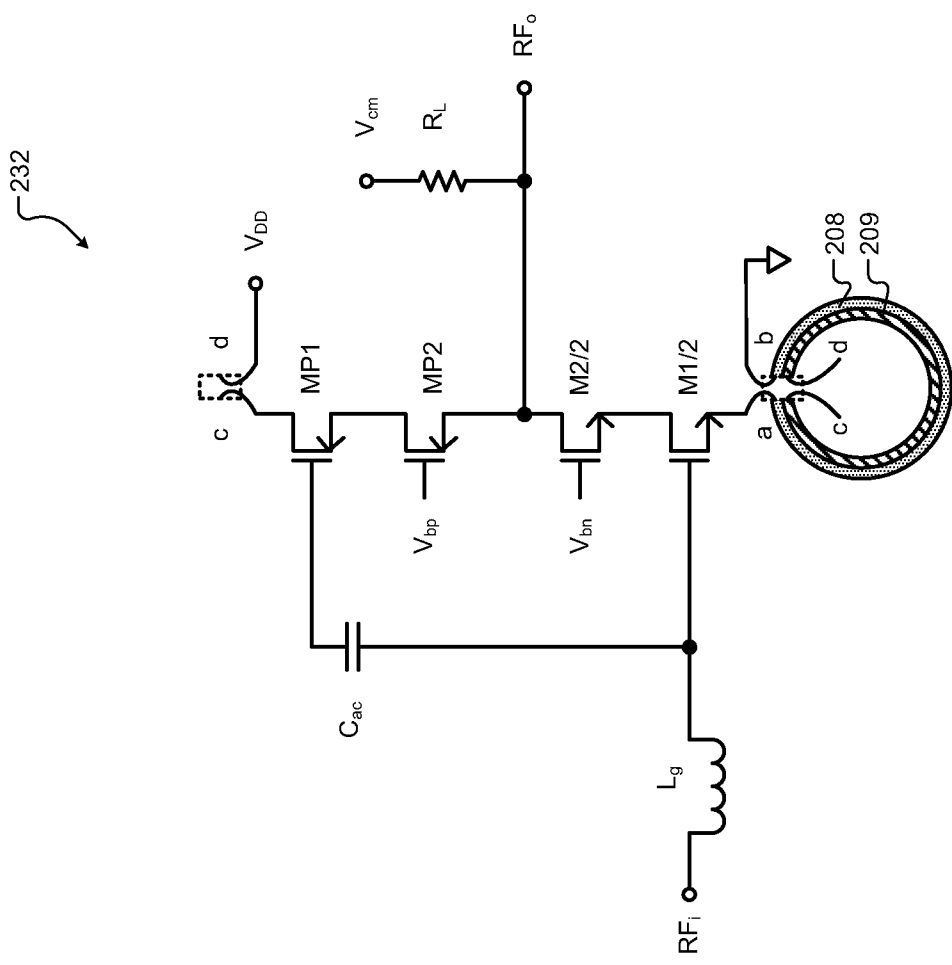


FIG. 9C

233

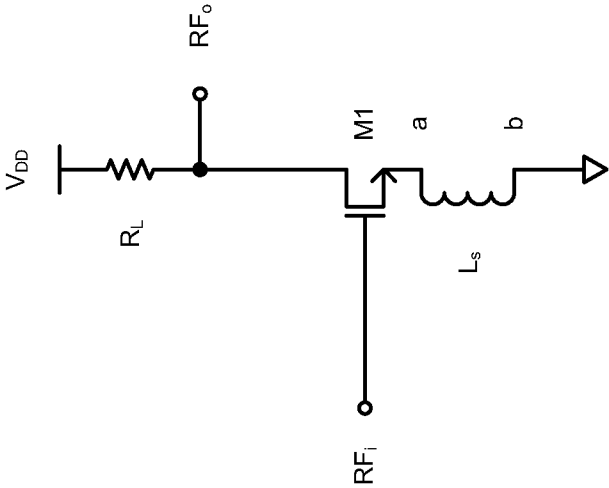


FIG. 10A

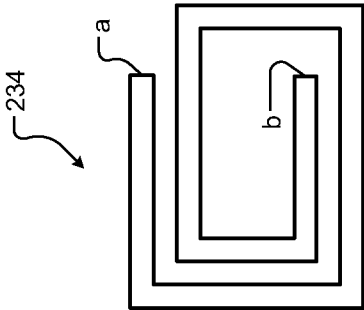


FIG. 10B

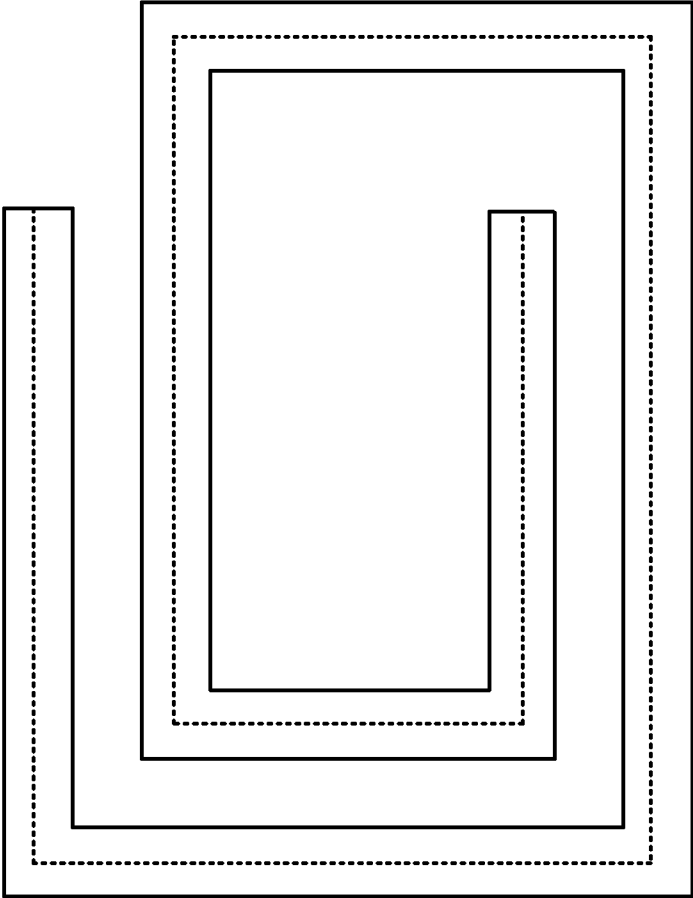


FIG. 10E

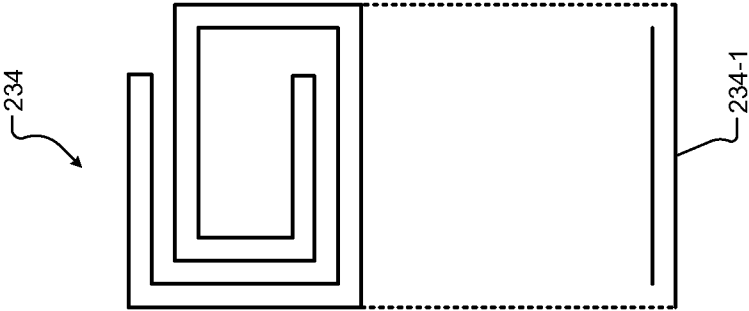


FIG. 11A

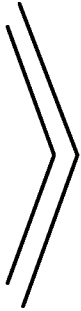


FIG. 11B

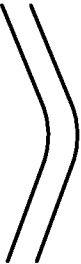


FIG. 11C

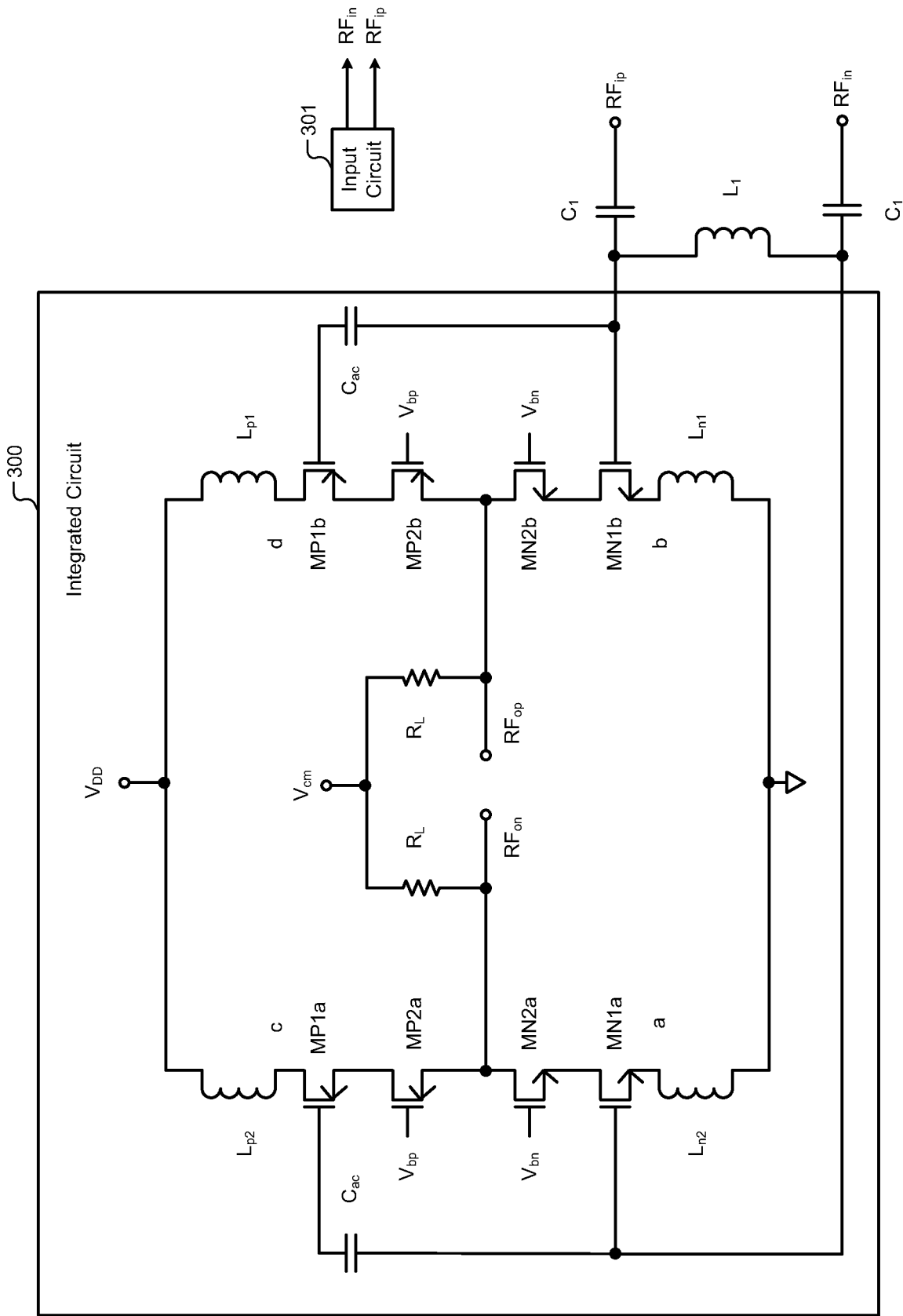


FIG. 12

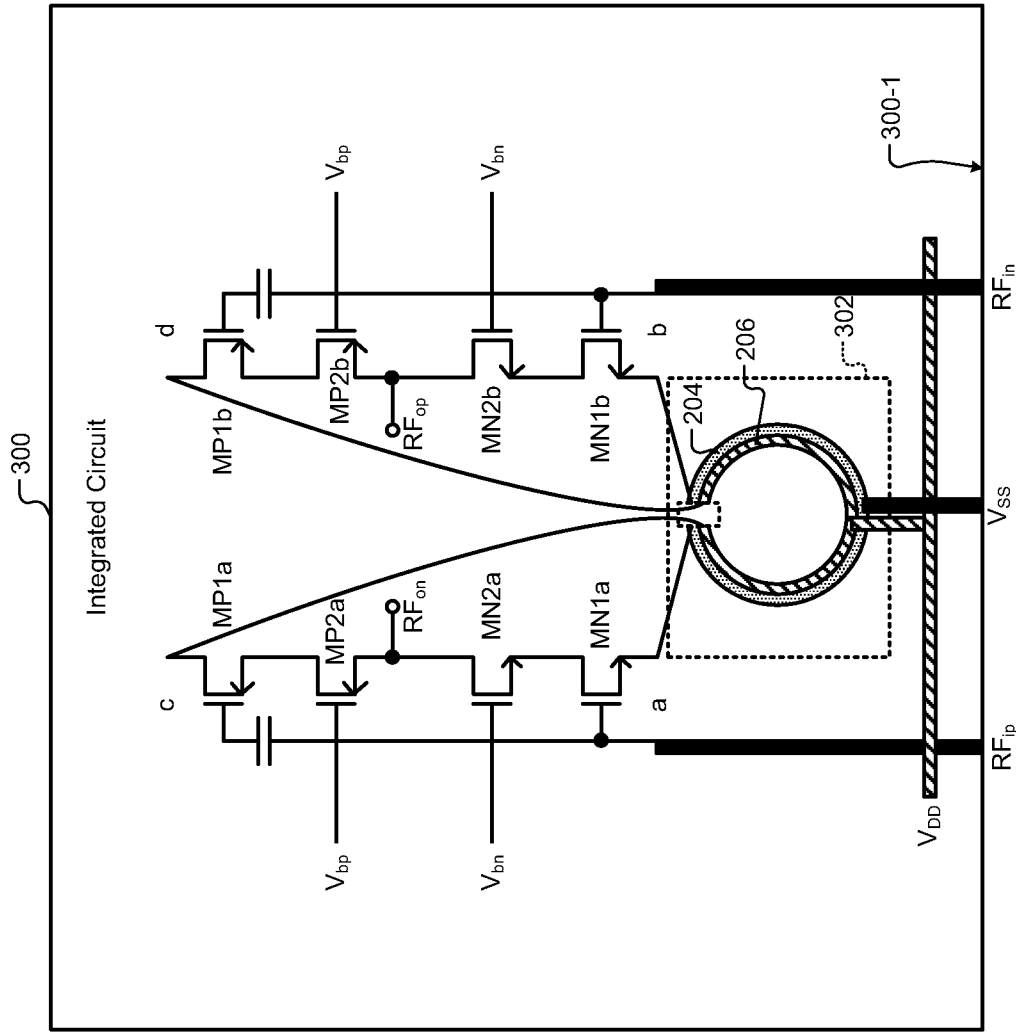


FIG. 13

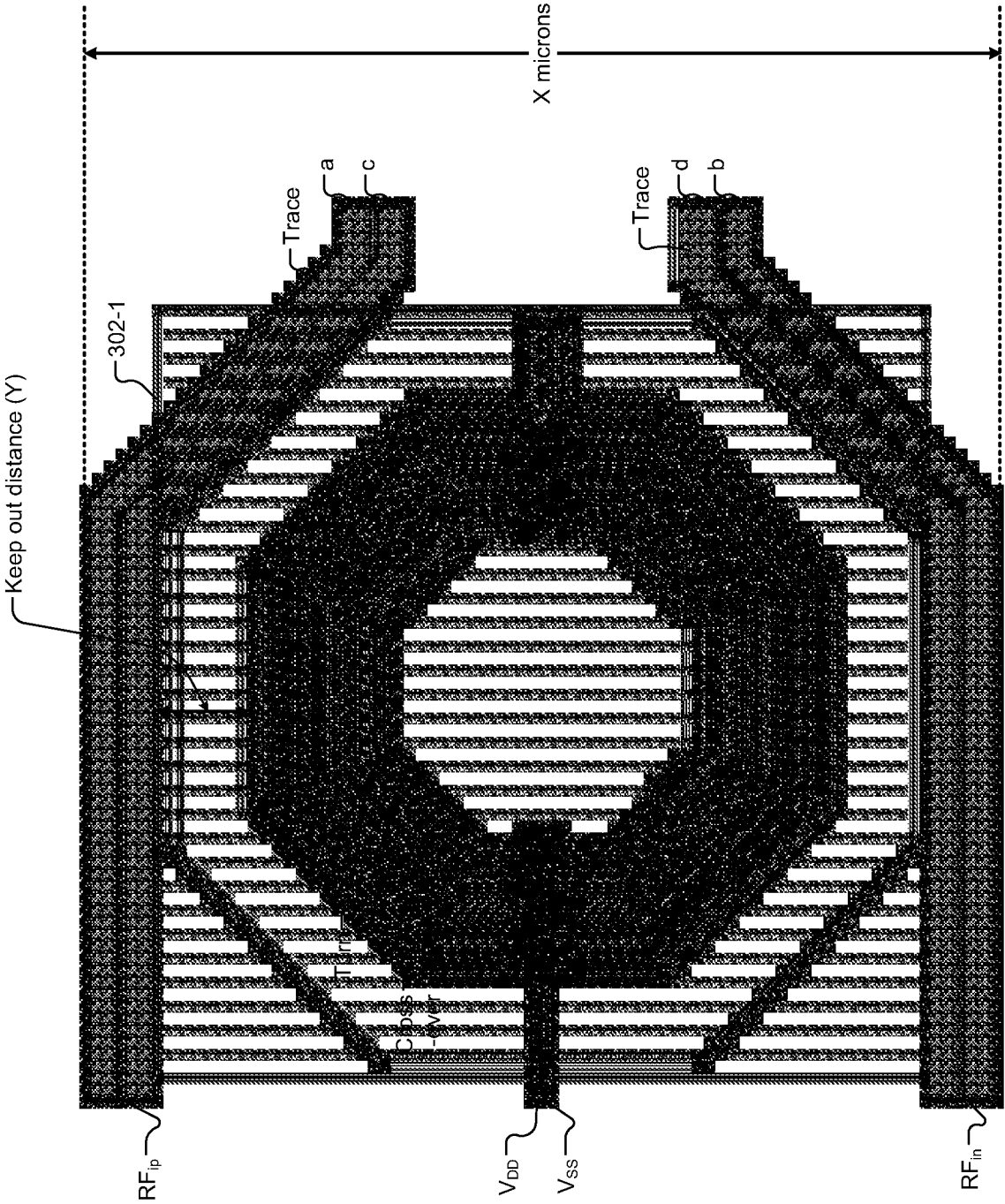


FIG. 14

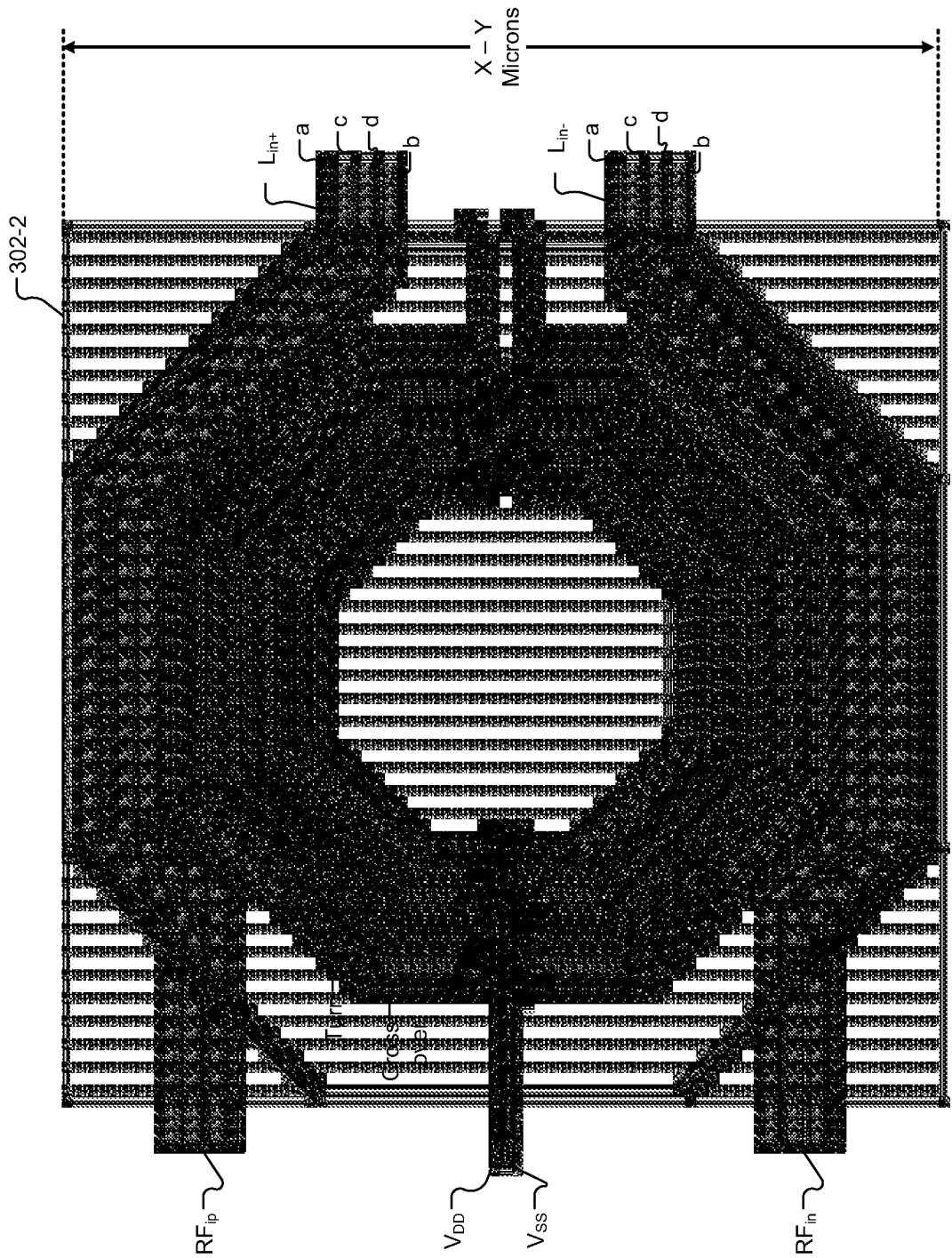


FIG. 15

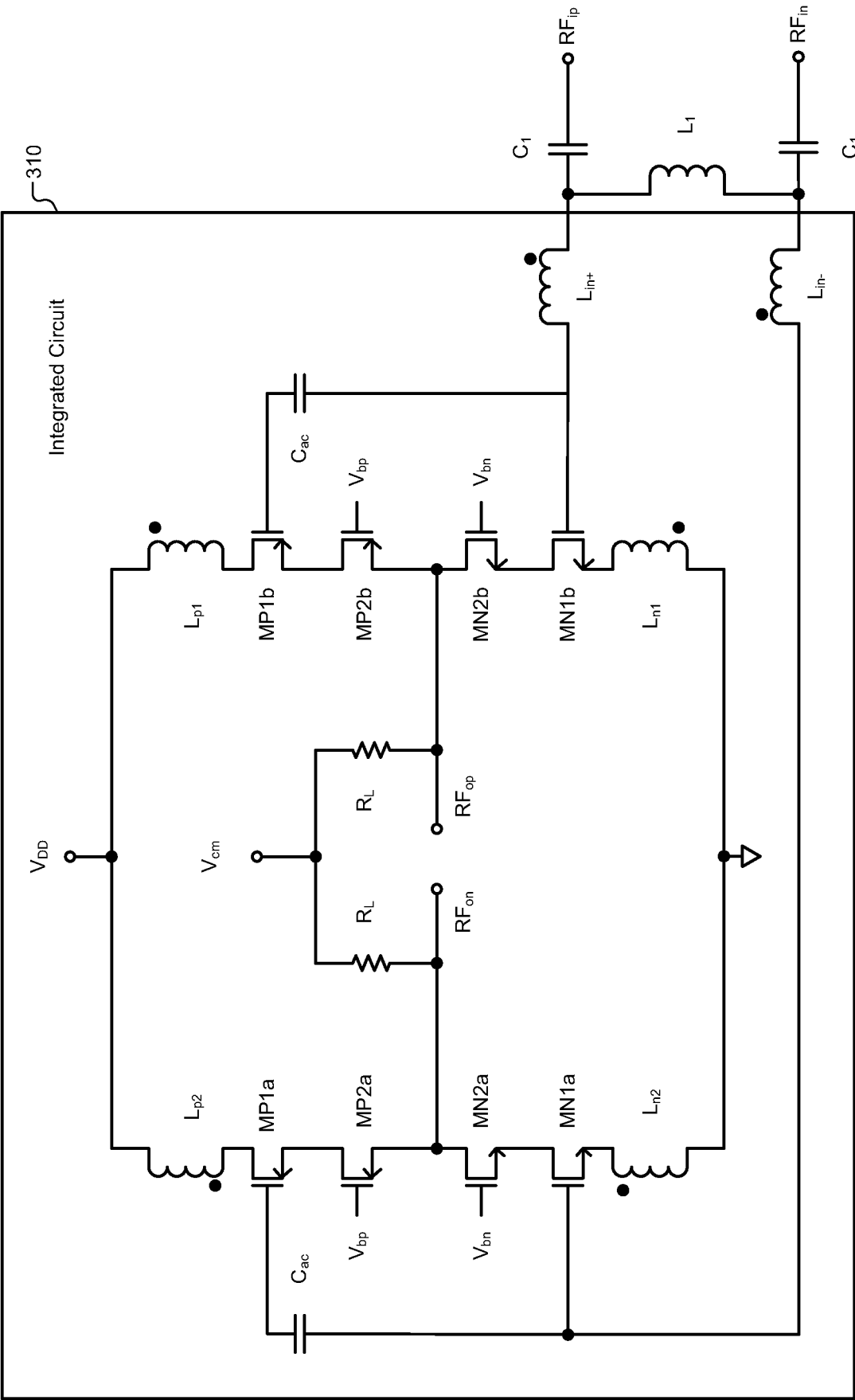


FIG. 16

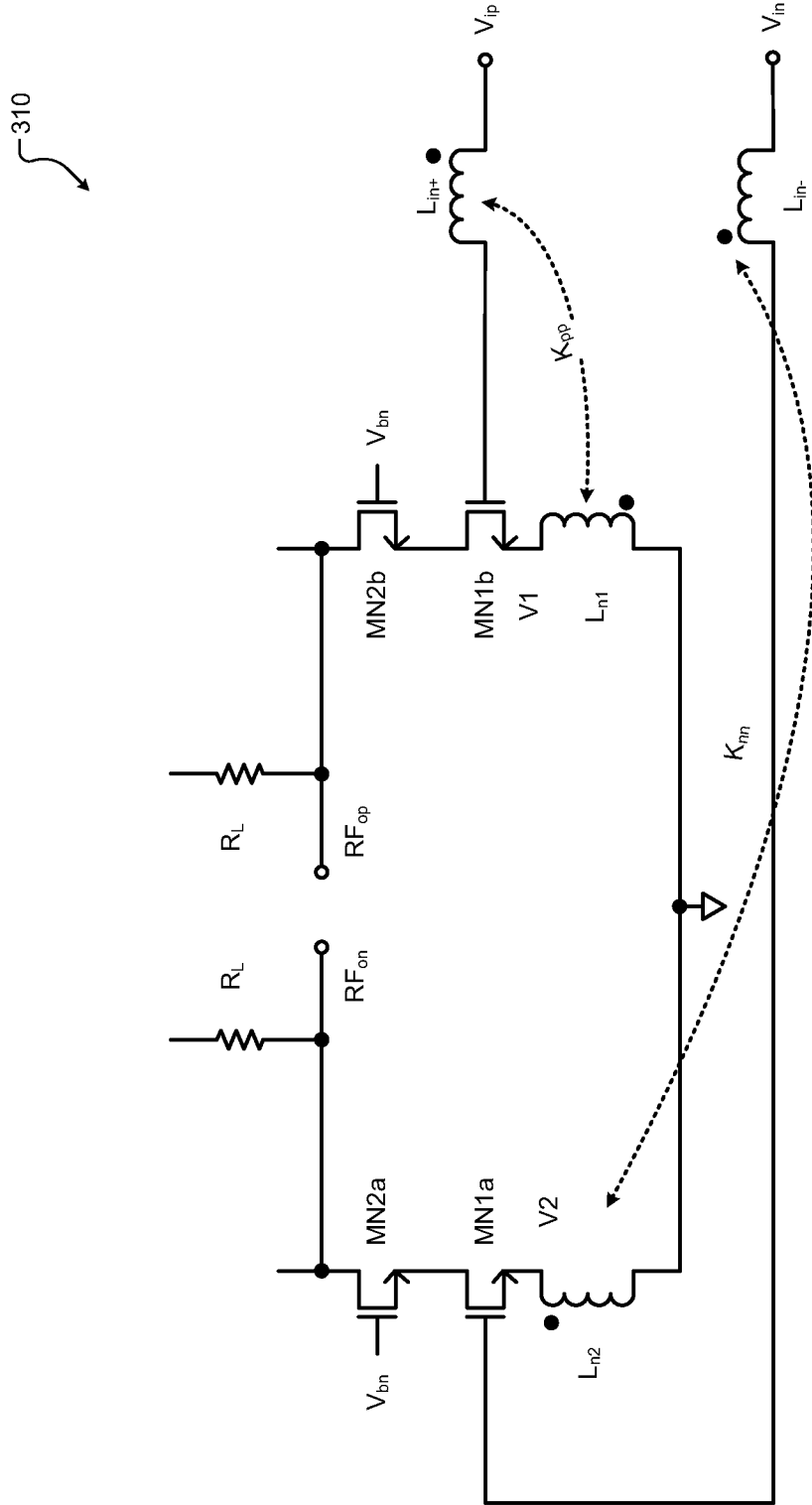


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/034200

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/30
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 2008/096516 A1 (MUN HYUN-WON [KR] ET AL) 24 April 2008 (2008-04-24) paragraph [0064] - paragraph [0074]; figures 6,7	1-15
A	US 2007/290754 A1 (LEE DONG HYUN [KR] ET AL) 20 December 2007 (2007-12-20) paragraph [0046] - paragraph [0049]; figure 4	1-15
A	US 5 656 849 A (BURGHARTZ JOACHIM NORBERT [US] ET AL) 12 August 1997 (1997-08-12) the whole document	1,4,5
A	US 6 087 900 A (LEE KWEY-RO [KR] ET AL) 11 July 2000 (2000-07-11) column 4, line 14 - line 61; figure 5	1,13
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Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

29 July 2010

Date of mailing of the international search report

04/08/2010

Name and mailing address of the ISA/

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Authorized officer

Kurzbauer, Werner

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/034200

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US B 530 813 I5 (BELL TELEPHOPONE LABORATORIES) 17 February 1976 (1976-02-17) figure 1	1,13

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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