Feb. 2, 1971 W. MILLEKER ET AL 3,560,861

ELECTRONIC SENSING SYSTEM FOR SELECTIVELY ENERGIZING AND DE-ENERGIZING APPARATUS

Filed Jan. 16, 1969

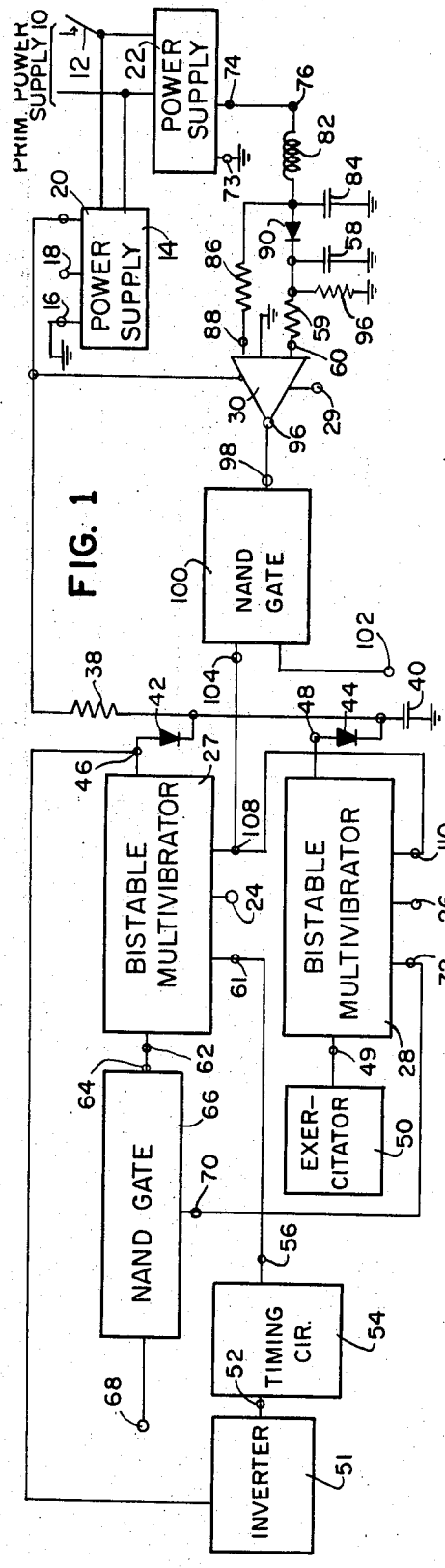


FIG. 1

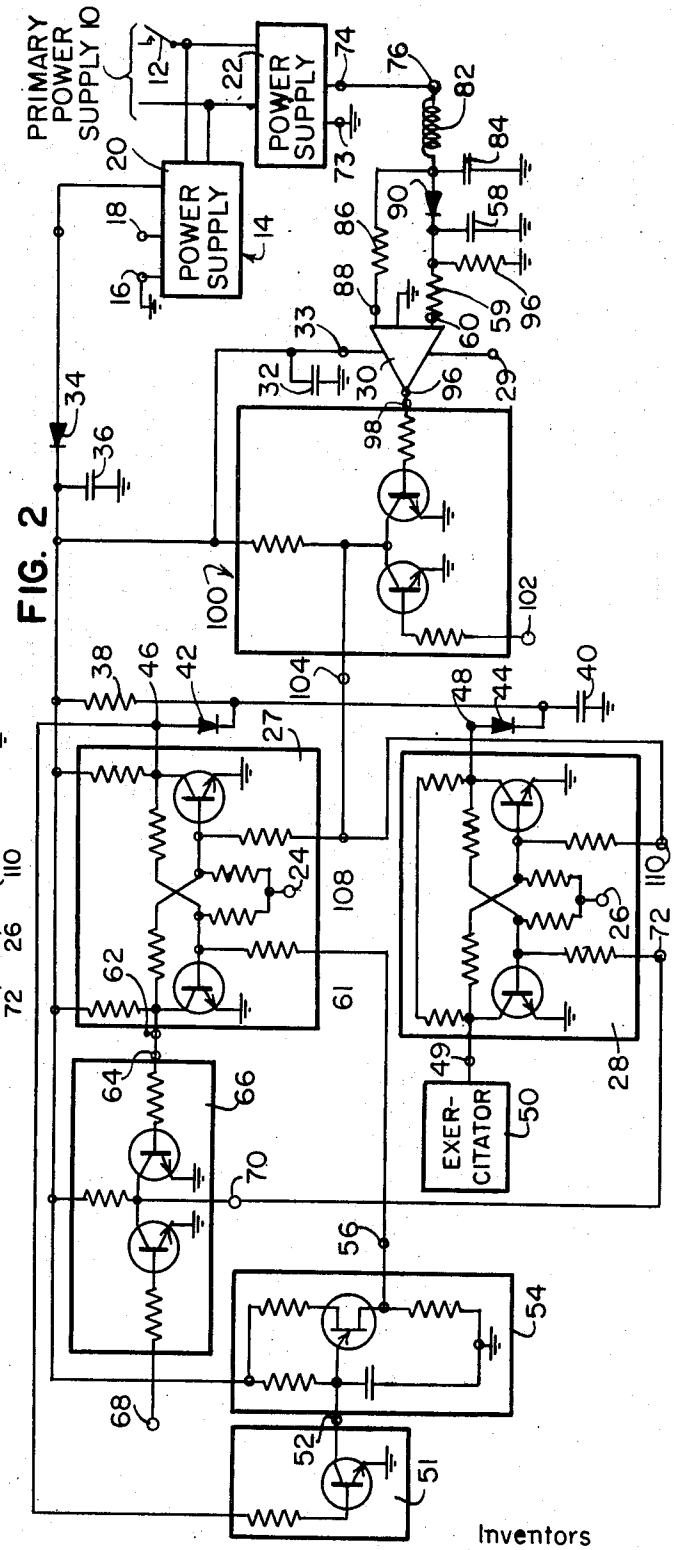


FIG. 2

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United States Patent Office 3,560,861 Patented Feb. 2, 1971

3,560,861

ELECTRONIC SENSING SYSTEM FOR SELECTIVELY ENERGIZING AND DE-ENERGIZING APPARATUS

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Filed Jan. 16, 1969, Ser. No. 791,555
Int. Cl. H03k 17/28
U.S. Cl. 328—74 6 Claims

ABSTRACT OF THE DISCLOSURE

The electronic sensing system selectively energizes an electrical apparatus a predetermined time after the electrical power is applied to the system and in synchronism with a signal indicating the apparatus is ready to be energized. The electrical apparatus is de-energized in response to both a sudden decrease in amplitude of a monitored voltage which activates a trigger circuit, and in synchronism with a subsequent signal indicating the apparatus is ready to be de-energized. A sensing circuit compares the voltage being monitored with a reference derived from this voltage to activate the trigger circuit.

BACKGROUND OF THE INVENTION

There are many applications for a system which can be used to enable and disenable electrical and mechanical apparatus whose operation is begun and terminated according to happenings which can either directly or indirectly produce electrical signals. For example, an electromechanical apparatus such as a washing machine that is programmable to go through various modes of operation must be controlled so that some portions of the machine are selectively enabled at the beginning of one mode and selectively disenabled at the end of another mode. Alternatively, the apparatus can be electronic in nature such as a magnetic core memory exercitator which "writes" data into and "reads" data out of a core memory in synchronism with signals provided by the system with which the core memory is used.

It is well-known to use a matrix of magnetic cores as a binary memory in electrical systems such as calculators, data processors, and display systems. This type of core memory can be used to supply binary data to a display system which is comprised of a character generator operating in cooperation with a television (TV) monitor receiver to display alphanumeric information. At the beginning of a horizontal scan line of the beam in the cathode ray tube (CRT) of the TV receiver, the exercitator reads binary data out of the core memory and places it in a display register which includes a temporary memory whose retention of binary data is dependent on the continuous application of external energy. The binary data is then selectively read out of the display register and used to generate an alpha numeric display on the CRT. The data is also returned to the core memory with each write operation.

There are problems associated with the de-energization and energization of this kind of an exercitator. When the primary power is interrupted for any cause, the DC operating power derived therefrom will subsequently decay until it is below a critical level at which the operation of the memory exercitator and display register becomes sporatic. Consequently, data stored in the temporary memory of the display register after the time of primary power interruption might be destroyed or lost unless the exercitator is disenabled at the end of the horizontal scan line of the CRT when all the data is in the core memory. Also, when the primary power is first applied to the DC

power supplies, the amplitude of their output voltages will be unstable for a short period of time thereby resulting in intermittent operation of the character display system which might result in the loss of data if the exercitator is enabled during this period of time.

BRIEF SUMMARY OF THE INVENTION

It is an object of the invention to provide an inexpensive, simple, and reliable sensing system to apply enabling and disenabling signals to electrical apparatus in synchronism with predetermined happenings in the apparatus.

It is another object of the present invention to apply a disenabling signal to the electrical apparatus after its primary power is interrupted, in coincidence with a synchronizing signal, and before the amplitude of a monitored voltage decays to a critical level.

It is a further object of the present invention to apply an enabling signal to the electrical apparatus a predetermined time after the operating power is applied thereto and in coincidence with a synchronizing signal so that the power supplies and other circuitry have time to stabilize.

In order that its advantages might be appreciated, the invention is described in relation to its operation as a power sensing circuit to enable and disenable a core memory exercitator in accordance with synchronizing (sync) pulses, and in response to changes in the amplitude of a primary supply voltage providing power to DC supplies, which in turn provide operating power for the exercitator. The sensing operation resulting in the selective disenablement of the exercitator depends in part on the substantially different rates at which the output voltages of two DC power supplies decrease after the primary voltage has been disconnected. The first power supply provides operating and bias voltages to the exercitator and to the sensing system of the invention. The second power supply provides an output voltage to be monitored to one input of the sensing system and a reference voltage to another input. For use in other applications, the monitored voltage could be derived elsewhere. If the primary power is interrupted for any cause, the amplitude of the monitored voltage of the second power supply decreases more rapidly than the amplitude of the exercitator operating voltage of the first power supply.

In the sensing system, the amplitude of the monitored voltage is constantly compared to the amplitude of the reference voltage by a differential amplifier to produce a voltage that is dependent on the difference therebetween. Whenever the amplitude of this difference voltage exceeds a predetermined amount, a DC danger voltage is delivered to one input of a two input gate, and sync signals are applied to the other input. The next sync pulse after the DC danger voltage causes a danger signal to be applied from the output of the gate to set first and second bistable multivibrators (bistables). The setting of the first bistable disenables the memory exercitator at an instant in time corresponding to the occurrence of the sync signal. At this time all of the binary data is permanently stored in the core memory matrix, and the operating and bias voltages have not decayed below their critical amplitudes.

A feature of the invention is the provision wherein the reference voltage is directly derived from the voltage to be monitored. The monitored voltage is directly connected to the first of two inputs of a comparator trigger circuit and indirectly connected through a diode to the second input thereby developing a reference voltage across a capacitor which is connected between the second input and ground. When the amplitude of the monitored voltage at the first input of the comparator suddenly decreases, the reference voltage at the second input cannot correspondingly suddenly decrease because the capacitor cannot rapidly discharge through the reverse

biased diode or through the high input impedance of the comparator trigger circuit. The amplitude difference between the reference and the monitored voltages is sensed by the comparator to provide a trigger or danger voltage which is utilized to disenable the exercitator as described above.

The circuit for energizing the core memory exercitator includes a unijunction timer that begins its timing cycle with the initial application of bias power for the exercitator. This initial application of power sets the two bistables thereby temporarily keeping the exercitator from operating. After a predetermined interval of time, during which the amplitude of the DC power supply output voltages and other voltages can stabilize, the timer ends its timing cycle and produces a delayed output pulse which resets the second bistable to apply a DC ready voltage to one input of a two input gate. Sync signals are continuously applied to the other input of the gate. Consequently, upon the application of the next sync signal after the DC ready voltage, a ready signal at the output of the gate resets the first bistable and thereby enables the exercitator. Data is thus kept in the core memory a predetermined interval of time after the power supply voltages are applied to the exercitator and until the occurrence of a sync signal which signifies that the character generator is ready to receive data from the exercitator.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the system of the invention; and

FIG. 2 is a schematic diagram of the system shown by the block diagram.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIGS. 1 and 2, the sensing system of the invention first will be described in relation to its enabling function. Power from primary power supply **10** is connected through switch **12** to first DC power supply **14** which has output terminals **16**, **18** and **20**, and to second DC power supply **22**. Output **16** of power supply **14** is grounded, and output **18** provides operating power of a first polarity to bias terminals **24** and **26** of bistables **27** and **28**, and to terminal **29** of the comparator trigger circuit **30**. To simplify the drawing the connecting lines from output **18** of power supply **14** are not shown. Output terminal **20** provides operating power of the second polarity through diode **34** and across capacitor **36** to the logic circuitry of the invention and to the initial condition determining network comprised of the serial connection of resistor **38** and capacitor **40**. Since capacitor **40** is initially uncharged, a ground potential is initially applied respectively through diodes **42** and **44** to set the initial voltage output levels at output terminals **46** and **48**of bistables **27** and **28** to low levels. By regenerative action the low level at output terminal **48** forces a high level at output terminal **49** of bistable **28** which render the memory exercitator **50** connected thereto inoperative so that it does not read data from or write data into a core memory.

Since output terminal **46** of bistable **27** is connected to the input of inverter **51**, the initial low level at output terminal **46** provides a high at output terminal **52** of the inverter which is connected to the input of unijunction timer **54**. The high level at terminal **52** enables timer **54** to begin its timing cycle during which the output voltages of power supplies **14** and **22** stabilize and reference voltage capacitor **58**, which is connected through resistor **59** to input **60** of comparator trigger **30**, charges up. After a predetermined interval of time, unijunction timer **54** completes its timing cycle and produces a pulse at its output terminal **56** which is applied through its connection to input terminal **61** thus resetting bistable **27** and thereby resulting in a high level at output terminal **46** which is connected back through inverter **51** to provide a low level at terminal **52** that deactivates timer **54**. Also when the output terminal **46** is at a high level the level at output terminal **62** is low and this low level or DC ready voltage is applied to input terminal **64** of first NAND gate **66**. Sync signals are applied to input **68** of NAND gate **66**. Consequently, the next sync signal occurring after the DC ready voltage produces a ready signal at NAND gate output terminal **70** which is connected to input **72** of bistable **28** thus resetting this bistable to cause a low level or an enabling signal at output **49** which renders exercitator **50** operative; and, as a result it now can read data from or write data into a core memory.

Therefore, the exercitator is enabled in synchronism with the first sync signal occurring a predetermined interval of time after the application of the power to the invention. This interval of time allows the power supplies to stabilize and the reference voltage to be developed across capacitor **58**.

The invention will now be described in relation to its disenabling function. Output **73** of power supply **22** is grounded, and output **74** is connected to input **76** of the sensing circuit. When the amplitude of the voltage of primary power supply **10** decays rapidly or switch **12** is opened, the output voltage of power supply **22** decreases more rapidly than the output voltages of DC power supply **14**. The output voltage of power supply **22** is constantly monitored by comparing it to a reference voltage to sense when primary power supply **10** has a reduced voltage as described below.

Input terminal **76** is connected to a filter network comprised of inductor **82** and capacitor **84** which together form a low pass filter for eliminating any spurious noise signals applied to terminal **76**. The monitored voltage across capacitor **84** is applied through current limiting resistor **86** to input **88** of comparator trigger circuit **30**. Also, the monitored voltage across capacitor **84** is applied through diode **90** to charge capacitor **58** to a reference voltage which is applied through current limiting resistor **59** to input **60** of comparator trigger circuit **30**. While the system of the invention is operative resistor **96** provides a high resistance current path for diode **90**, and after the system becomes inoperative resistor **96** provides a high resistance discharge path for capacitor **58**.

When the primary voltage from primary power supply **10** rapidly decreases, or when power supply **22** fails, the amplitude of the voltage applied to comparator trigger input terminal **88** will likewise decrease. The reference voltage at input terminal **60**, however, cannot accordingly decrease because capacitor **58** is unable to rapidly discharge through the high resistance of resistor **96** or through the high input impedance of comparator trigger **30** or through diode **90** which will be reversed biased because the voltage across capacitor **58** will have a greater amplitude than the decaying voltage of output **74** of power supply **22**.

Included in comparator trigger circuit **30** is a high gain differential amplifier having essentially a trigger circuit output. The output of the differential amplifier is dependent on the difference between the amplitudes of the monitored voltage at input terminal **88** and the reference voltage at terminal **60**. When the amplitude of the voltage (between inputs **60** and **88**) exceeds a predetermined limit the differential amplifier circuit output will produce a DC danger voltage or low level at output **96** which is connected to one input **98** of two input NAND gate **100**. Since sync signals are applied continuously to the other input **102** of gate **100**, the next sync signal after the DC danger voltage causes a danger signal at output **104** of NAND gate **100**. This signal is connected to the second inputs **108** and **110** of bistables **27** and **28** to set the same. As a result, a high level at output **49** of bistable **28** disenables exercitator **50**.

Thus the exercitator is disenabled after a monitored voltage, which in this case is the output voltage of power

supply 22, has decreased below a predetermined amplitude but before the output voltages provided by any of the power supplies decrease to a critical value below which the exercitator is subject to sporatic operation. The exercitator is disenabled in synchronism with a sync signal applied to input 102 of gate 100 which occurs at a time when all the data has been returned to a core memory and will be preserved therein.

What has been described, therefore, is a simple sensing system for selectively enabling and disenabling a core memory exercitator. There are many other applications where the sensing system can be used to advantage for providing control of electrical apparatus in response to predetermined happenings which are manifested by electrical signals. Furthermore, the invention is easy to build, reliable, and portions of its can utilize integrated circuits to reduce costs.

What is claimed is:

1. An electrical system for respectively providing enabling and disenabling voltages to electrical apparatus in synchronism with selected first and second signals provided to the electrical system, such electrical system including in combination, electrical power supply means providing an operating voltage, timing means for producing a first output pulse an interval of time after the operating voltage from said electrical power supply means is applied to the system, switching means responsive to said first output pulse and to the first signal occurring after said first output pulse to provide the enabling voltage, voltage supply means providing a direct current voltage, means deriving a reference voltage from said direct current voltage, comparator trigger means having first and second inputs, means applying said reference voltage to said first input, means applying said direct current voltage to said second input, said comparator trigger means being responsive to change in the amplitude of said direct current voltage to provide a second output pulse when said amplitude changes a predetermined amount with respect to said reference voltage, said switching means being responsive to said second output pulse and to the second signal to produce the disenabling voltage.

2. An electrical system in accordance with claim 1 further including, capacitor means for providing said reference voltage, electron control means connecting the direct current voltage to said capacitor means to charge the same to provide said reference voltage, said electron control means acting to isolate the amplitude of said reference voltage on said capacitor means from the amplitude of the direct current voltage when the amplitude of the direct current voltage diminishes a predetermined amount at a given rate.

3. The electrical system of claim 1 wherein said switching means includes two bistable multivibrator means, and two gating means which cooperate with said two bistable multivibrator means to provide said enabling and dis-enabling voltages at an output of one of said bistable multivibrator means.

4. The electrical system of claim 3 further including, an electrical network having resistive means and capacitive means connected in series, said electrical network being connected between said electrical power supply means and ground, both of said bistable multivibrator means being connected to the junction of said resistive means and said capacitive means, said network determining the initial conditions of the output voltage levels of both of said bistable multivibrator means.

5. An electrical system for preserving data stored in a memory by selectively applying enabling and disenabling signals to the memory exercitation means at intervals of time after primary supply means for the memory exercitation means is respectively operative and inoperative, and wherein first and second synchronizing signals are provided to the electrical system, such electrical system including in combination, first and second direct current power supply means obtaining energy from the primary power supply means, said first direct current power supply means having an output voltage amplitude that decreases at a substantially slower rate than the output voltage amplitude of said second power supply means in response to decrease in the voltage amplitude of the primary supply means, said first direct current power supply means providing operating power for the electrical system and the memory exercitation means, said second direct current power supply means providing a monitored direct current voltage, sensing circuit means responsive to the first synchronizing signal to produce an enabling signal to render the memory exercitation means operative, said sensing circuit means being responsive also to a predetermined decay of the amplitude of said monitored direct current voltage and to a second synchronizing signal occurring thereafter to produce a disenabling signal to render the memory exercitation means inoperative.

6. An electrical system corresponding to claim 5 wherein said first and second power supply means provide output voltages having amplitudes which stabilize an interval of time after the primary power source is connected thereto, and wherein said sensing circuit means includes timing means responsive to the application of operating power to the memory exercitation means to thereby provide a delayed output pulse, switching means connected to said timing means and responsive to said delayed output pulse to produce a triggering voltage, and gating means connected to said switching means and producing said enabling signal in response to the application thereto of said triggering voltage and the next subsequently occurring first synchronizing signal.

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U.S. Cl. X.R.

235—153; 307—130, 301; 317—22, 31; 328—72