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[54] **SYSTEM FOR THE TRANSMISSION OF INTELLIGENCE BY MEANS OF SCRAMBLED AUDIOSIGNALS**

[72] Inventors: **Seth Johan Ronald Lundin,** Vallingby; **Bengt Harry Bjorkman,** Sollentuna, both of Sweden

[73] Assignee: **U.S. Philips Corporation,** New York, N.Y.

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May 14, 1969 Sweden 6921/69

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[51] **Int. Cl.** **H04m 1/70**

[58] **Field of Search** ....179/1.5 SM; 178/22

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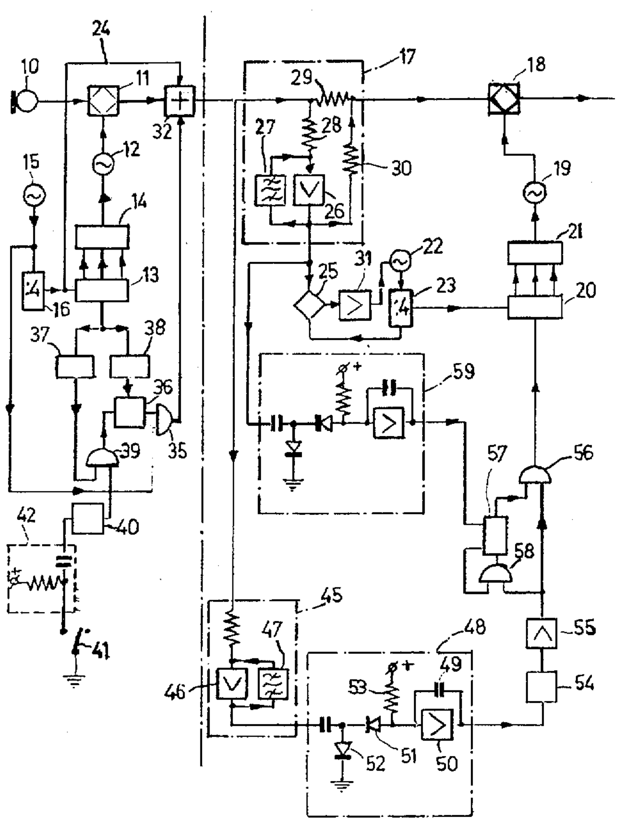
Primary Examiner—Benjamin A. Borchelt
Assistant Examiner—H. A. Birmiel
Attorney—Frank R. Trifari

[57] **ABSTRACT**

A system for the transmission of intelligence signals by means of scrambled audio signals comprising a transmitter, that employs the frequency shift generator to also produce a control signal that is added to the scrambled audio signals to be transmitted to the receiver. The receiver separates the control signal from the scrambled audio signals and employs this control signal to synchronize the receiver with the transmitter thereby effecting the demodulation of the scrambled audio signals by the receiver.

6 Claims, 4 Drawing Figures



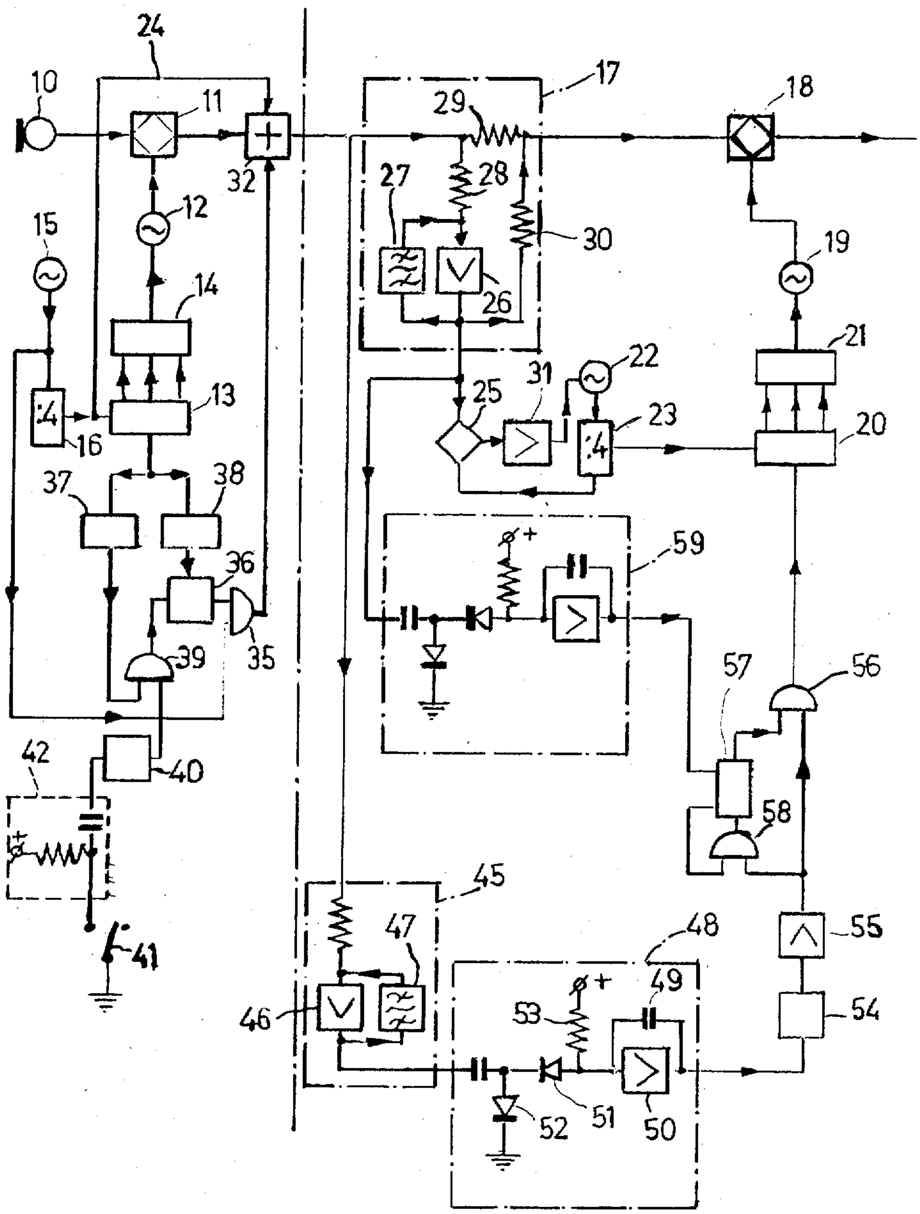


Fig.1

INVENTORS
SETH J.R. LUNDIN
BENGT H. BJORKMAN
BY
AGENT

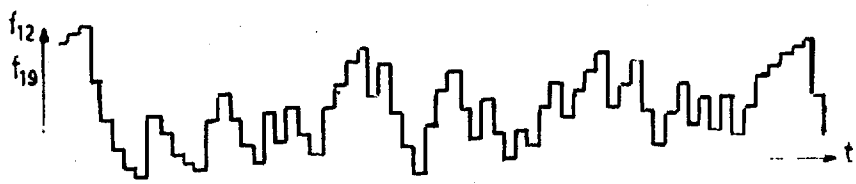


Fig.2

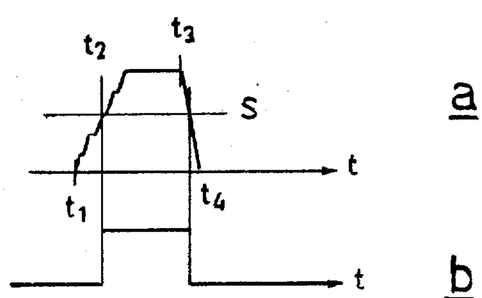


Fig.3

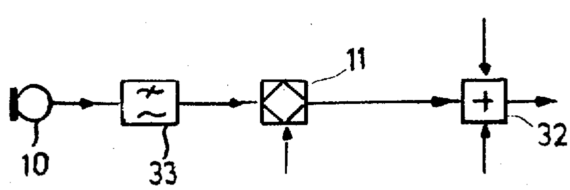


Fig.4

INVENTORS
SETH J.R. LUNDIN
BENGT H. BJORKMAN
BY
AGENT

SYSTEM FOR THE TRANSMISSION OF INTELLIGENCE BY MEANS OF SCRAMBLED AUDIOSIGNALS

The present invention relates to a system for the transmission of intelligence by means of scrambled audiosignals, comprising a transmitter and a receiver each of which includes an oscillator, a shift register connected in feedback and controlled by a shift pulse generator, means connecting said shift register to said oscillator to produce a predetermined frequency variation of said oscillator output signal, means in said transmitter for combining the oscillator output signal with the audiosignal to produce said scrambled audiosignal to be transmitted, and means in said receiver for combining said oscillator output signal with said received scrambled audiosignal to effect demodulation thereof.

In such a system the shift registers serve as control elements, and they will due to their feedback continuously repeat their cycle of operation, the duration of which is determined by the number of stages in the register. The output of the last stage of the register is a rectangular wave having an irregular pattern which is produced once for each cycle of operation. The magnitude of the distortion in each moment is determined by the stored "digit" represented by the condition of the individual stages. The individual stages of the shift register can for this purpose be connected through an adding network to the frequency determining circuit of the oscillator, the output frequency of which is combined with the audiosignals to be transmitted. In the receiver there is a similar oscillator controlled by a shift register which is connected in the same manner as at the transmitter end. In order that the demodulation shall give the desired result the frequency added in the receiver must in each moment be exactly equal to the frequency added in the transmitter, i.e. the shift registers must operate synchroneously.

A system of this kind is described in the Swedish Patent application No. 11,907/67 (PHN 1863). In this system the synchronization between the shift registers is effected in that the pulse pattern generated by the shift register in the transmitter is combined with the scrambled audiosignal and transmitted therewith. In the receiver the incoming signal thus containing the pulse pattern of the shift register of the transmitter is correlated with the pulse pattern derived from the shift register of the receiver. Only that component of the incoming signal, which corresponds to the pulse pattern of the shift register, will then produce a correlation product other than zero. If the shift registers operate in exact synchronism the correlation product will be maximum and it is in this manner possible to control the shift register of the receiver so that synchronization is achieved.

With this synchronization method a continuous monitoring of the function of the function of the shift registers is obtained but this method has the drawback that the said pulse pattern to be transmitted contains a relatively large information quantity and requires a large band width. In practice great difficulty is encountered when this information quantity has to be transmitted through conventional speech lines. This synchronization method is therefore less suitable.

The object of the invention is to provide a system of the above indicated type in which a minimum of information is required for the synchronization and in which the band width required for the transmission of this information is narrow so that this information can be transmitted through conventional speech channels.

According to the invention this object is obtained in that the transmitter further comprises means for adding to the scrambled audiosignal a control signal derived from the shift pulse generator of the transmitter, said control signal having a frequency within the frequency band of the audiosignals to be transmitted and a phase which is representative of the shift pulses produced by the shift pulse generator of the transmitter and in that the receiver further comprises means adapted to select the said control signal before said demodulation and means for applying said selected control signal to the shift pulse generator of the receiver for controlling the said generator to establish phase coincidence between the output signal of said generator and said control signal.

Thus in this case synchronization only requires transmission of one single discrete frequency, namely the sinus shaped fundamental component of the control voltage from which the shift pulses at the transmitter are derived. This ensures that the shifting occurs synchronously in the receiver and transmitter. Setting of the mutual phase of the shift registers in their respective cycles of operation takes place in special intervals, fir example one single interval before information transmission, by means of pulses of a single discrete repetition frequency and which pulses define a predetermined starting condition of the register of the transmitter.

When a carrier wave is used for the transmission frequency variations in the demodulated frequency can make it necessary to transmit two discrete frequencies for the synchronization, the useful information representing the time positions for the shift pulses of the register in the transmitter being formed by the difference between the two transmitted frequencies, which difference signal varies with possible changes in the absolute values of the frequencies.

The invention is illustrated in the accompanying drawings, in which

FIG. **1** shows a block diagram of a transmission equipment for transmission of scrambled speech signals, in accordance with the invention,

FIG. **2** shows an example of a pulse signal derived from a shift register included in the equipment according to FIG. **1**, which signal is utilized for the speech scrambling and

FIG. **3** shows some voltage curves appearing in the receiver of the device according to FIG. **1**.

FIG. **4** shows a modification of the signal input circuit of the transmitter of applicants'invention.

In FIG. **1** the transmitter is shown on the left and the receiver on the right hand side of the dotted lined.

According to FIG. **1** the speech signal from a microphone **10** is fed to a modulator **11** in the form of a symmetric mixer. In this device the speech signal is mixed with the output voltage from an oscillator **12**, the frequency of which is varied between different levels. The instantaneous frequency of the oscillator **12** is determined by a continuously operating shift register **13**, which is connected in feedback and the individual stages of which are connected to the frequency determining means of the oscillator **12** through an adding device 14. The shift register 13 which can be connected in the same manner as shown in the Patents (Swedish Patent applications 11,907/67, PHN 1863 and 12,524/67, PHN 1906) is operated by shift pulses from a shift pulse generator consisting of a driving oscillator 15 and a divider 16 arranged between the driving oscillator and the shift input of the shift register. The driving oscillator 15 may for example operate at a frequency of 2.5 kc/s and the divider 16 can produce a frequency division of 1 : 4, whereby the shift register will operate at a shift frequency of 625 c/s.

The oscillator 12 can operate conveniently at a center frequency lying at the upper limit of the speech spectrum, for example 3 kc/s and the frequency jumps produced by the shift register 13 may for example amount to maximum $\pm$ 400 c/s, whereby the oscillator will deliver an output frequency which varies between different levels in an irregular but predetermined manner between the limits 26 and 34 kc/s. An example of the frequency variation of the oscillator 12 as function of time is shown in FIG. 2.

The utilized mixing product from the mixer 11 is the lower side band, i.e. the instantaneous frequency of the oscillator 12 minus the frequency of the speech signal. The mixer 11 will therefore also produce an inversion of the speech spectrum, which makes it difficult to interprete such a distorted message without the proper listening apparatus.

The scrambled speech signal can be transmitted directly or by modulation on a carrier to the receiver.

In the receiver the distorted speech signal is fed through a filter 17 to a modulator or mixer 18 of the same construction as the modulator 11 in the transmitter.

The function of filter 17 will be explained more fully in the following. To the mixer 18 is also applied the output voltage from an oscillator 19, which corresponds to the oscillator 12 in the transmitter. Oscillator 19 is frequency controlled from a shift register 20 via an adding device 21. The shift pulses for the register 20 are produced by a shift pulse generator comprising a driving oscillator 22 which is connected to the shift input of the register 20 through a divider 23. The shift register 20 is connected in the same manner as the shift register 13 in the transmitter and produces the same pulse pattern. Provided the shift register 13 and 20 operate in synchronism demodulator 18 will add a frequency which in each moment is exactly equal to the frequency applied to the modulator 11 in the transmitter. Demodulator 18 will thus produce a mixing product which corresponds to the initial speech signal.

In order to ensure synchronization of the shift registers of the transmitter and receiver the following measures are taken.

In the transmitter the control signal is derived from the divider 16 and applied to register 13. In the given example this control signal has a frequency of 625 c/s. This control signal now is also fed through a lead 24 directly to a device 32, where it is combined with the scrambled speech signal. The said control signal having the shape of a rectangular wave can if desired be filtered before being combined with the speech signal, so that only the sinus shaped fundamental component is transmitted. The transmission of this control signal may be continuous as long as speech signals are transmitted or if desired may be transmitted only intermittently if the shift pulse generator of the receiver is sufficiently frequency stable.

In the receiver the incoming signal consisting of the scrambled speech signal and the control signal of the shift register is as mentioned fed through a filter 17. This is so shaped that the said control signal is selected and fed to a phase detector 25. Furthermore the filter 17 ensures that the control signal cannot occur at the input of demodulator 18. Filter 17 has a very narrow band width amounting to some cycles per second on each side of the frequency of the control signal. The suppression of the speech signal produced within this band will not really influence the quality of the speech signal.

For achieving the described filter function, filter 17 is constituted by an amplifier 26 which is fed back through a double T-net 27 and furthermore there is an input resistance 28 and a resistance 29 in the transmission path for the speech signal and a resistance 30 which is connected in feedback from the output of the amplifier to the output side of the resistance 29.

In phase detector 25 the selected control signal of 625 c/s is compared with the output signal of divider 23 which is used for shifting the register 20. The output signal of the phase detector representing the phase difference between the two compared signals is after amplification in an amplifier 31 fed to the frequency determining means of the oscillator 22. In the closed loop circuit thus formed the output signal of phase detector 25 tends to make the phase difference equal to zero by negative feedback. Accordingly the control signal at the output of divider 23 will be in phase with the corresponding control signal at the output of divider 16 in the transmitter and the two shift registers will be shifted exactly synchronously.

Though they are shifted synchronously these shift registers can still assume mutually different positions in their respective cycles of operation. In order to make them operate both in the same position, pulses time synchronized with the cycle of shift register 13 in the transmitter are fed to the line during a speech-free interval, preferably an interval preceding the transmission of speech signals. These pulses are in the shown embodiment derived from the driving oscillator 15 and thus have a frequency 25 kc/s. The length of the pulses and their moment of occurrence is determined by an AND-gate 35 connecting the output of oscillator 15 to the device 32. The gate 35 is opened and closed by means of a flip-flop 36, which is controlled by two decoder units 37, 38 in turn. Decoder unit 37 is connected to the set-input of bistable flip-flop 36 through and AND-gate 39, while the second decoder unit 38 is connected to the reset-input of flip-flop 36. AND-gate 39 is enabled by means of the voltage from a monostable circuit 40. Said monostable circuit 40 is controlled by means of a switch 41, which produces a trigger pulse which is fed through a differentiating circuit 42 to said monostable circuit 40. The switch 41 is for example actuated when the operator pushes the starting button at the beginning of speech signal transmission.

The decoder units 37 and 38 are connected to all stages in the shift register 13 and thus sense the instantaneous content of the register. Each decoder unit is adapted to produce an output pulse in response to a certain content of the register. The decoder unit **38** for example produces an output pulse the moment all stages in the register **13** have been switched, i.e. have assumed a position which is designated binary "1." Decoder unit 37 produces an output pulse a number of shift pulse periods prior to said moment. Provided gate 39 is open flip-flop 36 will be triggered when the content of shift register 13 is such that decoder unit 37 reacts. A small interval later the condition is reached for which the decoder unit 38 is sensitive, whereby the flip-flop 36 is reset. In the interval during which flip-flop 36 is in its set-position gate 35 will be enabled to pass a signal of for example a frequency of 2,500 c/s to the device 32, in which it is combined with the control signal of 625 c/s. The trailing edge of the synchronization pulse of 2,500 c/s defines the moment when shift register **13** assumes its predetermined starting condition which in the given example involves that all stages assume the position **1**.

The pulse produced by monostable circuit **40** has a duration such that during this pulse a number, for example 3–5, synchronization pulses are passed onto the line. The moment monostable circuit **40** returns to its original state gage **39** will be closed, so that flip-flop **36** can no longer be triggered and the synchronization pulses will cease since they cannot pass gate **35**.

In the receiver the synchronization pulses are selected by means of filter **45**, which is tuned to a frequency of 2,500 c/s of the pulses. Filter **45** is constituted by an amplifier **46** which is connected in feedback through a double T-network **47**. The selected synchronization pulses are applied to an integrator **48** consisting of an amplifier **50** connected in feedback through a capacitor **49** and having two diodes **51**, **52** arranged at the input side. The output voltage of integrator **49** increases stepwise in rhythm with the periods of the applied AC-voltage. At its output the integrator has a limiter, for limiting the integrator output voltage to a certain level. When the synchronization pulse ceases the capacitor **49** is discharged through a resistance **53**, the discharge time being determined by the capacitor **49** and the resistance **53**.

The integrator **48** controls a Schmitt-trigger stage **54**, which produces an output voltage as long as the output voltage of the integrator exceeds a certain level. After amplification in an amplifier **55** this voltage pulse from the Schmitt-trigger stage **54** is fed through an AND-gate **56** to the control input of shift register **20**. At the appearance of a voltage pulse from gate **56** the individual stages of the shift register **20** are forced to assume a certain position, for example in the given example all the stages are set in the position "1." Immediately after this pulse the shift register is released so that it starts to operate in rhythm with the shift pulses from divider **23**.

The output voltage from the integrator **48** is shown in FIG. **3***a* and the output voltage from the Schmitt-trigger stage is shown in FIG. **3***b*. The level of the output voltage of integrator **48**, at which the Schmitt-trigger stage is activated, is in FIG. **3***a* designated S. The moment t_1 coincides with the beginning of a synchronization pulse, when the voltage at the output of integrator **48** begins to increase. At the moment t_2 the Schmitt-trigger stage **54** is switched. At the moment t_3 the synchronization pulse ceases and immediately thereafter, at the moment t_4, the voltage at the output of the Schmitt-trigger stage disappears.

Provided gate **56** has been kept open during the synchronization pulse, the shift register will be set in the predetermined starting position at the end of the pulse.

Gate **56** is controlled by means of a counter **57** to which the synchronization pulses appearing at the output of the amplifier **55** are applied through an AND-gate **58**. The counter **57** is connected in feedback to an input of the gate **58** in a manner such that the gate is automatically closed the moment a certain number, for example 3–5 synchronization pulses, have been counted. During the counting interval gate **56** will be kept open. When the predetermined number of pulses has been counted gate **56** is closed and thus no longer able to pass pulses to the shift register **20**.

The counter **57** is reset by means of an integrator **59** of the same construction as the integrator **48**. Integrator **59** is controlled by the selected control signal of 625 c/s used for synchronization of the shifting of the registers. At the beginning of speech signal transmission the voltage is built up at the output of the integrator **59** in the same manner as shown for integrator **48**. The voltage is then kept on this level during the whole speech, whereby the counter **57** can carry through the described operation cycle. Ceasing of the voltage from integrator **59** at the end of speech signal transmission results in zeroing of the counter **57**.

The operation is as follows.

When the control voltage used for shifting the register **13** in the transmitter is transmitted to the receiver. The controlled oscillator **22** with divider **23** in the receiver will be locked to the received control voltage so that divider **23** will produce a shift signal which is exactly in phase with the shift signal from the divider **16** of the transmitter.

When the operator pushes the button for speech signal transmission illustrated by the switch **41** in FIG. **1**, the monostable circuit **40** will be triggered so that gate **39** is opened. Flip-flop **36** is triggered when the content of shift register **13** is such that the decoder unit **37** produces a setting signal and immediately thereafter the flip-flop **36** is reset when the register content is such that decoder unit **38** produces a reset signal. During the set period of flip-flop **36** gate **35** is enabled to pass synchronization pulses having a recurrence frequency of 2,500 c/s to the line. Gate **35** is closed after a predetermined number of synchronization pulses have been fed to the line.

In the receiver each individual synchronization pulse produces an output voltage (FIG. **3***a*) at the output of integrator **48**. During the interval when the Schmitt-trigger stage **54** delivers output voltage according to FIG. **3***b* the shift register will receive a voltage on its control input via the amplifier **55** and gate **56**, which voltage compulsorily sets the stages in the register **20** in the predetermined position. At the end of each synchronization pulse the shift register **20** will be released so that it starts to operate on the shift pulses from the divider **23**. The starting condition of register **20** which is set during the synchronization pulse is chosen to be equal to the condition, for which the decoder unit **38** is responsive. Since the decoder unit **38** determines the moment when the synchronization pulse is interrupted the shift register **20** will be set to the same starting condition as the shift register **13** at the moment of interruption of the synchronization pulse. After reception of a predetermined number of synchronization pulses gate **56** will be closed and the register **20** will thereafter operate in response to the shift pulses from divider **23**. Provided that the shift pulses maintain their synchronization and that the last synchronization pulse has produced correct setting of the shift register **20**, the shift registers in the transmitter and receiver will thereafter operate in complete synchronism.

Instead of a single setting operation of the shift register in the receiver prior to the speech signal transmission and then trusting that the synchronization is maintained during the speech signal transmission, it is also possible if required to repeat the said setting operation intermittently a number of times during the speech, in which case for each such setting the speech signal is interrupted for a short interval. The repeating of the setting operation may be required in information transmission systems that are liable to suffer from fading due to which the receiver may lose its synchronization.

At transmission on carrier frequency the described system with transmission of one single discrete frequency representing the control signal of the shift register on the transmitter side is not reliable. At the combination with the carrier it cannot be avoided that the frequency of the control voltage after demodulation can vary somewhat on each side of the desired frequency. But as the information lies in the phase of the control voltage, frequency variations can of course not be allowed. This difficulty can be overcome by transmitting instead of one single frequency two frequencies, for example 600 and 1,200 c/s, in which case the difference between these two signals carries the information about the phase position of the control voltage of the shift register on the transmitter side. Even if the absolute value of the transmitted signals should vary somewhat the difference between the signals will be constant and transmit the required information to the receiver.

In order to increase the secrecy it is possible to replace the device connecting the shift register to the oscillator so as to vary the added frequency from time to time. Such a replacement should of course be accomplished at the same time in both the transmitter and receiver. A different way to produce from time to time varying pattern for the frequency variations consists in that the shift registers in the transmitter and receiver are connected in a different manner.

In conjunction with the synchronization measures described a further improvement of the secrecy may be obtained by inserting a filter **33** (see FIG. **4**) between the microphone **10** and the modulator **11**, said filter being a lowpass filter which acts as a damping network for mainly the higher frequencies of the speech signal, the cut-off frequency of said filter being situated within the frequency band to be transmitted. In FIG. **4** this cut-off frequency is for instance 1 kc/s.

In order to make the interpretion of the synchronization pulses difficult the two decoder units in the transmitter can be adjustable so that the synchronization pulses will appear at different moments of the operation cycle of the shift register in the transmitter. In the receiver this can be compensated by means of a time delay between the device that detects the synchronization pulses and the setting device producing the predetermined setting of the shift register in the receiver.

The described system is not limited to the transmission of scrambled speech signals but can also be used where the information has to be kept secret, for example in data transmission by audiosignals or frequency shift. The system according to the invention can also be modified for transmission using the three-out-of-five code or the like, where each information element is represented by a frequency within the audio spectrum.

What is claimed is:

1. A system for the transmission of intelligence signals by means of scrambled audiosignals, comprising a transmitter and a receiver, said transmitter comprising signal input means for said intelligence signals, a source of auxiliary information signals having a periodic pulse pattern not correlated with said intelligence signals, said source comprising an oscillator, a feedback connected shift register coupled to said oscillator to produce a predetermined frequency variation by varying the frequency of said oscillator, and a frequency shift generator coupled to control said shift register and provide a control signal at a frequency within the frequency band of said intelligence signals and a phase representing the shift pulses produced by said shift pulse generator, means for combining said intelligence signals and said auxiliary information signals to produce a scrambled audiosignal, means for adding said control signal to said scrambled audiosignals for transmission to said receiver, said receiver comprising signal input means for receiving said scrambled audiosignals with said control signal, means for separating said scrambled audiosignals from said control signal, a source of auxiliary information signals having a periodic pulse pattern identical to the periodic pulse pattern of said transmitter, said source comprising an oscillator, a shift register coupled to said oscillator to produce a predetermined frequency variation by varying the frequency of said oscillator, and a frequency shift generator coupled to control said shift register, means for applying said control signal to said frequency shift generator to control said generator to establish phase coincidence between the output signal of said generator and said control signal, and means for combining said source of auxiliary information signals with said scrambled audiosignal to effect demodulation of said intelligence signals.

2. A transmission system as claimed in claim **1** wherein the frequency shift generator of said receiver further comprises a closed loop comprising a phase detector for receiving said control signal and the output of said frequency shift generator to control said frequency shift generator thereby maintaining a predetermined mutual phase position between said control signal and the output of said frequency shift generator.

3. A system as claimed in claim **1** wherein said control signal is formed by the difference signal obtained by comparison of two signals having a difference frequency within the frequency band of the intelligence signal.

4. A system as claimed in claim **1** wherein synchronizing transmitter is provided with means for synchronizing the shift registers controlled by the shift

registers for generating and transmitting to the receiver during at least one interval at the beginning of said intelligence signal transmission, pulses having a frequency within the transmitted frequency band, said pulses being synchronized in time with the shift register in said transmitter so that it appears at a predetermined condition of said register, and the receiver is provided with means for receiving said synchronizing pulse to ensure the corresponding setting of the shift register of the receiver in the period of time determined by the pulse thereby syncrhonizing the periodic pulse pattern of said receiver with the periodic pulse pattern of the transmitter. trailing **5**. A system as claimed in claim **4** wherein the trailng edge of said synchronizing pulses define the period of time when the predetermined condition in the shift register of the transmitter occurs, and means in the receiver sensitive to said synchronization pulses to set and maintain the shift register in a predetermined condition during the occurrence of said synchronizing pulses and release the register when said synchronizing pulses terminate.

6. A transmission system as claimed in claim **1** wherein the signal input of said transmitter further comprises a filter functioning as a low pass filter, said filter acting as a clamping network for mainly the higher frequencies of said intelligence signals, the cutoff frequency of said filter being within the frequency band to be transmitted.

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