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INTERCONNECT WITH ENHANCED RELIABILITY AND LIFETIME THROUGH RELIABILITY MONITOR AND SELF REPAIR

FIELD OF THE DISCLOSURE

[0001] This disclosure relates generally to electrical interconnect reliability, and, more particularly, to methods and apparatus for electrical interconnect with enhanced reliability and lifetime through reliability monitor and self repair.

BACKGROUND

[0002] In electrical circuits, a through-silicon via (TSV) is a vertical electrical connection (also referred to as a “via”) passing through a silicon wafer or die. TSVs provide a high performance interconnect that can be used as an alternative to wire-bond and flip chips to create three-dimensional (3D) packages and 3D integrated circuits with higher density and shorter interconnection length compared to alternatives such as package-on-package integrated circuit (IC) packaging.

[0003] For example, a 3D package (e.g., a System in a Package, Chip Stack Multi-Chip Module (MCM), etc.) includes two or more chips (ICs) stacked vertically to occupy less space and/or have greater connectivity. Alternatively, ICs are not stacked but a carrier substrate containing TSVs is used to connect multiple ICs together in a package.

[0004] Alternatively, a 3D integrated circuit (3D IC) is a single integrated circuit built by stacking silicon wafers and/or dies and

interconnecting them vertically with TSVs so that the stacked wafers and/or dies behave as a single device. The wafers and/or dies in the stack may be homogeneous (e.g., same type) and/or heterogeneous (e.g., combining CMOS logic, DRAM and III-V materials into a single IC, etc.).

[0005] Interconnect scaling (e.g., reducing size of interconnects in an integrated circuit) and 3D integration using TSV technology enables further increase in device density of ICs. However, metal-interconnect scaling presents increased reliability issues, and, while 3D ICs offer a multitude of benefits, reliability issues also surrounding TSVs cause significant concern. For example, different types of failures, such as electromigration, voiding, and thermomechanical failures, arise due to scaling and aging of interconnects and TSVs. These failures cause the resistance of an interconnect to degrade overtime. The degradation in resistance increases the interconnect's delay in response.

[0006] While manufacturing process controls may catch infant mortality and some reliability stress failures in interconnects, marginally and slowly degrading units may get passed onto the customers from the production line. Variations in manufacturing, environment, and usage patterns also make it challenging to model the degradation rate of interconnects analytically, which make it more difficult to catch failures in-line both during and after manufacture. Additionally, runtime interconnect failures in the field may be catastrophic, causing computational errors which may result in overall system failure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIGS. 1A-B illustrate example circuits including a reliability monitor and self-repair logic.

[0008] FIG. 2 illustrates an example plot of voltage across a capacitor versus time for two example resistance values.

[0009] FIG. 3 illustrates an example implementation of the local control and allocation logic of FIGS. 1A-1B.

[0010] FIG. 4 shows an example implementation of the converter of FIG. 3 including a current sensor.

[0011] FIG. 5 shows a more detailed diagram of the converter, ring oscillator, and counter of FIG. 3 in a low current mode.

[0012] FIG. 6 shows an example delay output obtained from an example device stage with respect to device resistance.

[0013] FIG. 7 shows a more detailed diagram of the converter, ring oscillator, and counter of FIG. 3 in a high current mode.

[0014] FIG. 8 shows an example of output bias voltage from a current-to-voltage converter with respect to device resistance.

[0015] FIG. 9 shows an example response of ring oscillator frequency with respect to ring oscillator voltage bias.

[0016] FIG. 10 shows an example plot of a device based on output ring oscillatory frequency versus device resistance.

[0017] FIG. 11 illustrates an example implementation of a current-to-voltage converter of FIG. 3.

[0018] FIG. 12 illustrates an example implementation of a ring oscillator of FIG. 3.

[0019] FIG. 13 provides an example implementation of a current-starved inverter of FIG. 12.

[0020] FIG. 14 provides an example implementation of a current-starved NAND of FIG. 12.

[0021] FIGS. 15-18 are flowcharts representative of example processes to monitor, diagnose, and remedy faulty interconnects in a die.

[0022] FIG. 19 is a schematic illustration of an example processor platform that may execute instructions with respect to FIGS. 15-18 to implement or help facilitate monitoring, diagnosis, and repair of devices shown in or referenced by FIGS. 1-14.

DETAILED DESCRIPTION

[0023] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific examples that may be practiced. These examples are described in sufficient detail to enable one skilled in the art to practice the subject matter, and it is to be understood that other examples may be utilized and that logical, mechanical, electrical and/or other changes may be made without departing from the scope of the subject matter of this disclosure. The following detailed description is, therefore, provided to describe example implementations and not to be taken as limiting on the scope of the subject matter described in this disclosure. Certain features from different aspects of

the following description may be combined to form yet new aspects of the subject matter discussed below.

[0024] When introducing elements of various embodiments of the present disclosure, the articles “a,” “an,” “the,” and “said” are intended to mean that there are one or more of the elements. The terms “comprising,” “including,” and “having” are intended to be inclusive and mean that there may be additional elements other than the listed elements.

[0025] Certain examples provide devices, apparatus, systems, and associated methods to diagnose and treat defects in interconnects including a through-silicon via (TSV) passing vertically through a silicon wafer or die. Certain examples provide an electrical interconnect with enhanced reliability and lifetime through reliability monitor and self-repair.

[0026] Certain examples provide in-field fault detection and repair. Certain examples provide an on-die, interconnect health monitor. Certain examples predict possible TSV failures, which allows performing repairs (e.g., by redundant lines or TSVs, increased voltage, etc.) immediately before the failure occurs. An on-die reliability feature also helps ensure a circuit design's performance over time (e.g., after 5-10 years, etc.), as TSV lanes experience a gradual degradation rather than a massive failure (e.g., in Internet of Things (IoT)-related applications, automotive applications, etc.).

[0027] TSV health is typically monitored during the manufacturing process but not during operation of the circuit including the TSV. X-ray optical inspection and structural boundary scan testing are the primary techniques used to test interconnects, but these methods mainly address the

presence or absence (e.g., open or short) of the connection. Such methods do not provide information regarding the electrical reliability of the interconnect and are not available to end users. Electrical characterization of the connection using analog harmonic tests, junction techniques, and radio frequency (RF) induction may be used, but these techniques are not suited for embedded applications due to a long learning phase that is needed to properly tune the system for identification of TSV failure.

[0028] Certain examples provide a TSV controller system including a combination of a current-based ring oscillator (RO) and a counter to measure a change in resistance with respect to a TSV being monitored. The combination of RO and counter works by converting a current that is passing through a device under test (DUT), such as a metal interconnect TSV structure (e.g., included in a memory (e.g., random access memory (RAM), Dynamic RAM (DRAM), etc.), logic chip, system on a chip (SOC), etc.), into a voltage signal that modulates an on/off time delay and/or a frequency of the ring oscillator. A change in time delay and/or frequency varies a number of counts incremented by the counter, and the counter value can be compared to a comparison value or threshold to identify a defect, deficiency, failure, decline, etc., in the associated TSV.

[0029] Certain examples provide a metal interconnect health monitoring feature within a silicon wafer or die. A change in resistance is measured using a digital ring oscillator and counter to enable in-field monitoring of the wafer/die, which can significantly improve chip reliability

when implemented with a built-in self-repair algorithm to repair degrading and/or faulty interconnects, for example.

[0030] An on-die repair feature enables a reduction in quality and/or reliability guard band that is added in to a circuit design. For example, a timing and voltage guard band can be added to a die to help ensure that the circuit continues working after 10 years of operation despite degradation. In certain examples, the on-die reliability monitor can alleviate a need for such guard bands, and removal of the guard bands can result in improved performance. An on-die reliability feature also helps ensure that the design performs after 5-10 years of operation since the TSV lanes will experience gradual degradation instead of massive failure. The reliability feature can be useful for Internet of Things (IoT) and automotive markets, for example.

[0031] Some methods to test interconnects only address a presence or absence of a connection, but do not provide information regarding reliability of the connection over time. Such methods cannot be embedded in individual die or units. These methods are mostly available only during the manufacturing process, rather than monitoring system health during operation. Certain examples remedy these deficiencies.

[0032] FIG. 1A illustrates an example circuit 100 including a reliability monitor and self-repair logic. The example circuit 100 includes a plurality of TSV interconnects 102, 104, 106, 108 start from a base 110 and extend through a plurality of memory devices or layers 112, 114, 116, 118 to interconnect the layers 112-118. Each TSV lane 102-108 is controlled by a local control and allocation (LCA) logic block 120, 122, 124, 126. The LCA

blocks 120-126 are controlled by a TSV controller 130, which generates a TSV pass/fail mapping 140 and triggered by a test access port (TAP) 150. While the example circuit 100 of FIG. 1A is depicted, for purposes of illustration only, as a memory circuit, the circuit 100 can implement other processor, device, and/or logic chip to manipulate and/or store data.

[0033] As shown in the example of FIG. 1A, each LCA block 120-126 includes a current-based ring oscillator (RO) and a counter to measure a change in resistance. Each LCA 120-126 receives a current that is passing through the device under test (DUT), such as the memory devices 112-118, and converts the current into a voltage signal. The converted voltage signal can modulate 1) an on/off time delay and/or 2) a frequency of the ring oscillator. A change in time delay and/or frequency varies a number of counts by which the counter increments.

[0034] Failing TSV lanes 102-106 can be repaired and replaced with redundant TSV lanes 108. Alternatively, TSV lanes 102-106 that are marginal can be fixed by modulating the voltage. Repair and/or replacement is facilitated by repair allocation logic in the TSV controller 130. Failing TSV lanes 102-106 can also be recorded in a TSV pass/fail mapping 140 into non-volatile memory that can be on-die or off-die 100, for example. Operation and TSV 102-108 analysis can be triggered by an input via the TAP 150, for example.

[0035] FIG. 1B illustrates a second view of the example circuit 100 including additional detail regarding the TSV controller 130. The illustration of FIG. 1B includes TSV lanes 102-108, base 110, device layers 112-118,

LCA 120-126, TSV controller 130, pass/fail mapping 140, and TAP 150. As shown in the example of FIG. 1B, the TSV controller 130 includes a TSV control finite state machine (FSM) 132, repair/allocation logic and voltage control 134, and compare logic and failure map 136.

[0036] In the example of FIG. 1B, input to the TAP 150, such as a hardware tester (e.g., at manufacture or production, etc.), a Basic Input/Output System (BIOS) and/or other firmware (e.g., during operation, etc.), etc., triggers an evaluation of the TSV lanes 102-108 in the die 100. The TSV control FSM 132 of the TSV controller 130 receives the TAP input and responds to a control sequence in the input from the TAP 150 to analyze the TSVs 102-108 in the circuit 100. The TSV control FSM 132 includes a plurality of states (e.g., 16 states, 8 states, 20 states, etc.) to control normal operation, TSV test, TSV repair/replacement, etc.

[0037] Based on input from the TAP 150 (e.g., a request for TSV test, etc.), the TSV control FSM 132 generates instruction for the repair/reallocation controller 134. For example, the FSM 132 triggers the controller 134 to power on and exercise each LCA 120-126 to evaluate each TSV 102-108. Each TSV lane 102-108 responds via its corresponding LCA logic 120-126 to the compare logic 136. The LCA 120-126 is a local controller controlling a test function with an RO and counter. The compare logic 136 examines an output of each LCA 120-126 to determine whether a TSV has failed or is failing (e.g., is to be replaced or repaired) or is operating normally. The LCA 120-126 output can include a counter value, pass/fail indicator (e.g., binary indicator, etc.), etc., for example.

[0038] The compare logic 136 compares the LCA 120-126 output (e.g., stored in a memory) to a state of each TSV 102-108 (e.g., good, bad, failing, counter value, etc.). The compare logic 136 can include a failure map including counter values, and/or a pass/fail bit (e.g., whether a count value is higher or lower than a threshold indicating a TSV failure, etc.), etc. If the counter value associated with a particular TSV 102-108 continues to increment, then the incrementing counter is an indicator that the channel is becoming more degraded than other channels and can be identified as a channel that is failing next, for example.

[0039] A TSV pass/fail mapping 140 generated by the compare logic 136 can be stored in a memory on and/or off the die 100 and provided to the repair/allocation logic 134. Based on the pass/fail mapping 140 information (e.g., TSV failure, TSV failing, TSV okay, etc.), the control 134 can communicate with the LCA(s) 102-108 to replace a failed or failing TSV 102-106 with a redundant TSV 108, attempt to repair a failing TSV 102-106 by increasing and/or otherwise modulating its voltage (which increases the current flowing through the TSV), etc. A failing TSV 120-106 can be recorded into memory, such as non-volatile memory, that can be located on- and/or off-die 100, for example. As shown in the examples of FIGS. 1A and 1B, the circuit 100 includes a plurality of TSVs 102-106 and at least one redundant TSV 108 that is available to be switched on in the event of a TSV 102-106 failure to maintain current flow between the layers 112-118, for example.

[0040] Thus, as illustrated in FIGS. 1A and 1B, metal interconnect health monitoring 120-126, 130, 140 is included within the die 100. The LCA logic 120-126 measures a change in resistance using digital ring oscillators associated with counters. Using the LCA 120-126 and TSV controller 130, the die 100 can be monitored at the time of manufacture, as well as when it is deployed for use in the field, for example. Such dynamic health monitoring, combined with built-in self-repair algorithms, enable the die 100 to diagnose and repair degrading and/or otherwise faulty interconnects 102-108 on-the-fly.

[0041] As discussed above, the LCA logic 120-126 uses a combination of a digital ring oscillator and a counter to measure resistance, which is indicative of a health or usable status of each TSV 102-108. In certain examples, the LCA logic 120-126 and compare logic 136 operates according to two modes. In a first mode, a low current mode, a voltage is used to change an on/off time delay for analysis to determine TSV fault or failure (e.g., to determine whether the TSV is short or not). In a second mode, a high current mode, the voltage is used to change a frequency of oscillation to determine TSV fault or failure (e.g., to continuously monitor the health of the TSV).

[0042] The low current mode uses resistor-capacitor (RC) decay in order to relate the resistance of a DUT to time delay. A rate of charging and discharging of a capacitor is directly related to a product of its capacitance and series resistance. Therefore, a capacitor with a lower series resistance will have a faster rate of decay.

[0043] FIG. 2 illustrates an example plot 200 of voltage 210 across a capacitor versus time 220 for two example resistance values. As illustrated in

the example of FIG. 2, a first plot 230 is for a first resistor having a lower resistance than the second resistor represented by the second plot 240. The first resistor of the first plot 230 has a shortened run time due to excessive leakage resulting from a lower resistance value when compared to a nominal run time associated with the second resistor associated with the second plot 240.

[0044] The high current mode converts a reference current to a voltage that, depending upon resistance, biases the RO. An analysis of RO frequency (e.g., as reflected in a count of oscillating RO frequency pulses by the counter) can be used to identify a failed or failing interconnect.

[0045] FIG. 3 illustrates an example implementation of the LCA logic 120-126. For purposes of example illustration only, the LCA logic shown in FIG. 3 is represented as LCA 122, connected to LCA 120 and LCA 124. Each of the LCA 120-126 includes similar components to test their corresponding TSV lane 102-108.

[0046] As shown in the example of FIG. 3, a data input 302 (e.g., from the TSV controller 130) is provided to a test control register 310, which stores the TSV test instructions/parameters to facilitate testing by the LCA 122. The information in the test control register 310, and resulting feedback, is provided to a TSV pass/fail register 320, as well as a TSV repair/test multiplexer (mux) 330 (e.g., as a mux selector 312) and a ring oscillator 340 (e.g., as an enable 314). Based on an output of a converter 350 and data input 332, 334 (e.g., provided from the TSV controller 130), as well as the mux selector 314, the mux 330 controls a DUT (e.g., the TSV 104 corresponding to LCA 122)

and/or a reference voltage (Iref) 336 to repair the TSV 104 (e.g., using the reference voltage 338), replace the TSV 104 with the spare TSV 108 (e.g., turn the TSV 104 off), or continue normal operation (e.g., keep the TSV 104 on), for example.

[0047] Depending upon the mode (e.g., low current mode or high current mode), the converter 350 generates a control signal to turn on or off the RO 340 (e.g., in a low current mode) and/or generates a bias voltage for the RO 340 (e.g., in a high current mode). The RO 340 generates an output signal to trigger a counter 360 (e.g., a pulse counter). The counter 360 outputs its count to a TSV count register 370, which provides that count as a data output 372 to a next LCA 124 and/or the TSV controller 130, for example. Data 332, 334 provided by the previous LCA 120 and/or TSV controller 130 can also be relayed as an output 380 to the next LCA 124, for example.

[0048] As discussed above, the converter 350 can have different configurations depending upon a mode in which the converter is operating. In certain examples, the converter 350 is customized for a particular mode (e.g., masked and manufactured according to a low current mode part (e.g., referred to herein as 350A or a high current mode part (e.g., referred to herein as 350B), etc.). In other examples, the converter includes circuitry for both low current and high current modes of operation.

[0049] FIG. 4 shows an example implementation of the converter 350 including a current sensor 410. The current sensor 410 measures a current 420 input from the die 100 and analyzes the current 420 to determine whether the circuit 100 is operating in a low current mode (e.g., current below a threshold)

or a high current mode (e.g., current above a threshold). Based on the current analysis, the current sensor 410 enables a low current mode circuit 350A or a high current mode circuit 350B.

[0050] FIG. 5 shows a more detailed diagram of the converter 350 when the converter is configured for a low current mode (shown in the example of FIG. 5 as 350A), RO 340, and counter 360 in a low current mode. As shown in the example of FIG. 5, when the low current mode is enabled 502 (ENB), the transistor P1 (e.g., a p-channel metal-oxide-semiconductor (PMOS) field effect transistor (FET) 504, etc.) is enabled to pull up the DUT 104 between P1 504 and n-channel MOSFET N1 506. A capacitor 508 associated with P1 504 is charged to an initial voltage V_{DUT} 510. Once the enable 502 is asserted, the RO 340 and the counter 360 activate, and the capacitor 508 discharges through the DUT 104. A rate of decay in the capacitor 508 (e.g., the RC decay) is determined by measuring the DUT resistance level. Consequently, the voltage across the capacitor 508 also decays, which turns off the RO 340 once a turn-off voltage threshold is reached. The counter 360 holds its last value reached before the RO 340 is deactivated. Counter output 372 is read via scan chain, for example, to capture counter 360 values in the TSV count register 370 and process the count. When the resistance from the DUT 104 is high, a higher output count is obtained from the counter 370 because the corresponding RC decay and the on-time of the RO 340 and the counter 360 are longer.

[0051] FIG. 6 shows an example RC delay output 600 obtained from an example DUT stage with respect to DUT resistance. As shown in the

example of FIG. 6, time delay 610 decreases with increasing resistance 620.

For at least this reason, analyzing the RC decay/delay is suitable for a low current (e.g., high resistance) mode of circuit operation.

[0052] FIG. 7 shows a more detailed diagram of the converter 350 when the converter is configured for a high current mode (shown in the example of FIG. 7 as 350B), RO 340, and counter 360 in a high current mode. In the example of FIG. 7, the converter 350B is configured as a current to voltage (I to V or IDV) converter 350B to bias the RO 340 based on the generated voltage output from the converter 350B. In the high current mode shown in the example of FIG. 7, the DUT 104 establishes a reference current 336 that is fed into the I to V converter 350B (e.g., a beta multiplier circuit, etc.). As shown the example 800 of FIG. 8, resistance 810 has an inverse relationship with output bias voltage 820. That is, a low resistance produces a high current; thus, the I-to-V converter 350B outputs a high bias voltage 702. The generated voltage 702 is then used to bias the ring oscillator 340, when the RO 340 is enabled 704. FIG. 9 shows an example response 900 of RO frequency 910 with respect to RO voltage bias 910 of a sample RO circuit 340. As shown in the example of FIG. 9, the RO frequency 910 has a direct relation to the bias voltage 920. The RO output signal is then fed into the digital counter 360, which counts the number of pulses of the RO signal. A high frequency results in a high count. The counter output is read (e.g., using a scan chain) and provided as a digital output 372 from the count register 370.

[0053] FIG. 10 shows the overall response of the DUT 104 with converter 350B and the RO 304 together. The example plot 1000 shows that a

frequency of the RO output signal 1010 is inversely related to DUT resistance 1020. As shown in the example of FIG. 10, a change in frequency 1010 becomes significantly worse at higher resistance levels 1020. For at least this reason, an analysis of resulting RO frequency is suitable for a high current (e.g., low resistance) mode of circuit operation.

[0054] FIG. 11 illustrates an example implementation of the I to V converter 350B. In the example of FIG. 11, converter circuitry is provided between a supply voltage (VCC) 1102 and ground (gnd) 1104 to generate a bias voltage from the reference current. As shown in the example of FIG. 11, a first PMOS 1110 and NMOS 1112 pair and a second PMOS 1120 and NMOS 1122 pair generate, with respect to a resistance 1130, voltages vbp 1140 and vbn 1142. The voltage vbp 1140 is applied to a third PMOS 1150, while the voltage vbn 1142 is applied to a third NMOS 1152 to generate an bias voltage 1160 for the RO 340.

[0055] FIG. 12 illustrates an example implementation of the RO 340. FIG. 12 illustrates a current-starved implementation of the RO 340. The RO 340 includes a plurality of delay stages, with an output of the last stage fed back into an input of the first stage (e.g., forming a loop or ring). To achieve oscillation, the components of the RO 340 provide a phase shift and unity voltage gain at an oscillation frequency. Oscillation can be sustained by the RO 340 until the RO 340 is disabled 314 and/or the bias voltage 1160 (formed by the vbp 1140 and vbn 1142) is removed, for example.

[0056] The example RO 340 implementation of FIG. 12 includes a NAND gate 1210 which receives the enable/disable signal 314 and output

from a ring of inverters 1220, 1222, 1224, 1226, 1228, 1230 arranged in series from the NAND 1210 back the NAND 1210. Additionally, output of the series of inverters 1220-1230 is provided to a buffer 1240 to form an output 1250. The logic gates of the RO 340 (e.g., the NAND 1210, inverters 1220-1230, and buffer 1240) are powered by a supply voltage (VCC) 1260.

[0057] A number of inverters 1220-1230 and a propagation time to route a signal from the NAND 1210 through the sequence of inverters 1220-1230 determines a period and associated oscillation frequency of the RO 340. The oscillation frequency can be adjusted by varying the number of inverters 1220-1230, the time delay associated with each inverter 1220-1230 and the buffer 1240, for example. In certain examples, oscillation frequency can be controlled using a current-starved (e.g., current-limited) ring oscillator 340 which controls an amount of current available to charge or discharge each stage (e.g., the NAND 1210, inverter(s) 1220-1230, the buffer 1240, etc.) in the RO 340. The available current is dictated by the available voltage 1260 provided to pull up and pull down the transistors forming the components of the RO 340. For example, a large voltage 1260 allows a large current to flow, which produces a small resistance resulting in a small delay. Reducing the voltage 1260 allows a smaller current to flow, which increases the resistance and increases the delay. As the signal propagates through the ring of inverters 1220-1230, gated by the enable signal 314 provided to the NAND gate 1210, the output 1250 provided via the buffer 1240 is supplied to the counter 360 to generate the digital output 372 for analysis to determine TSV 102-108 status, for example.

[0058] FIG. 13 provides an example implementation of a current-starved inverter 1220 (e.g., also applicable to invertors 1222, 1224, 1226, 1228, and/or 1230). In the example of FIG. 13, voltages vbp 1302 and vbn 1304 operate as control voltages with respect to PMOS transistor 1310 and NMOS transistor 1312 to increase resistance and, therefore, delay with respect to PMOS transistor 1320 and NMOS transistor 1322 operating to invert input 1330 to generate output 1332. The voltages vbp 1302 and vbn 1304 can be generated from a control current (e.g., using a current mirror) and/or supplied externally as one or more bias voltages, for example.

[0059] FIG. 14 provides an example implementation of a current-starved NAND 1210. As in the example of FIG. 13, control voltages vbp 1402 and vbn 1404 operate as control voltages with respect to PMOS transistor 1410 and NMOS transistor 1412 to increase resistance and, therefore, delay with respect to PMOS transistors 1420, 1422 and NMOS transistors 1424, 1426 operating to process input 1430, 1432 to perform a binary “Not AND” operation to generate an output 1434, which is a value of “1” unless both inputs 1430, 1432 match at “1”, in which case the output 1434 is “0”. The voltages vbp 1302 and vbn 1304 can be generated from a control current (e.g., using a current mirror) and/or supplied externally as one or more bias voltages, for example.

[0060] While example implementations of the die 100 and its components are illustrated in FIGS. 1-14, one or more of the elements, processes and/or devices illustrated in FIGS. 1-14 may be combined, divided, re-arranged, omitted, eliminated and/or implemented in any other way.

Further, the example LCA 120-126, example TSV controller 130, example pass/fail mapping 140, example TAP 150, and/or, more generally, the example die 100 of FIGS. 1-14, may be implemented by hardware, software, firmware and/or any combination of hardware, software and/or firmware. Thus, for example, any of the example LCA 120-126, example TSV controller 130, example pass/fail mapping 140, example TAP 150, and/or, more generally, the example die 100 of FIGS. 1-14 can be implemented by one or more analog or digital circuit(s), logic circuits, programmable processor(s), application specific integrated circuit(s) (ASIC(s)), programmable logic device(s) (PLD(s)) and/or field programmable logic device(s) (FPLD(s)). When reading any of the apparatus or system claims of this patent to cover a purely software and/or firmware implementation, at least one of the example LCA 120-126, example TSV controller 130, example pass/fail mapping 140, example TAP 150, and/or, more generally, the example die 100 of FIGS. 1-14 is/are hereby expressly defined to include a tangible computer readable storage device or storage disk such as a memory (e.g., a read only memory (ROM), hard drive, flash memory, other volatile and/or non-volatile memory, etc.), a digital versatile disk (DVD), a compact disk (CD), a Blu-ray disk, etc. storing the software and/or firmware. Further still, the example apparatus of FIGS. 1-14 may include one or more elements, processes and/or devices in addition to, or instead of, those illustrated in FIGS. 1-14, and/or may include more than one of any or all of the illustrated elements, processes and devices.

[0061] Flowcharts representative of example processes to be executed in conjunction with the die/circuit 100 of FIGS. 1-14 are shown in FIGS. 15-

18. In these examples, the processes can be executed by the die 100 and/or by a processor, such as the processor 1912 shown in the example processor platform 1900 discussed below in connection with FIG. 19, operating in conjunction with the die 100. The program may be embodied in software stored on a tangible computer readable storage medium such as a CD-ROM, a floppy disk, a hard drive, a DVD, a Blu-ray disk, or a memory associated with the processor 1912, but the entire program and/or parts thereof could alternatively be executed by a device other than the processor 1912 and/or embodied in firmware or dedicated hardware. Further, although the example programs are described with reference to the flowcharts illustrated in FIGS. 15-18, many other methods of implementing the example system 100 may alternatively be used. For example, the order of execution of the blocks may be changed, and/or some of the blocks described may be changed, eliminated, or combined.

[0062] As mentioned above, the example processes of FIGS. 15-18 may be implemented using coded instructions (e.g., computer and/or machine readable instructions) stored on a tangible computer readable storage medium such as a hard disk drive, a flash memory, a ROM, a CD, a DVD, a cache, a random-access memory (RAM) and/or any other storage device or storage disk in which information is stored for any duration (e.g., for extended time periods, permanently, for brief instances, for temporarily buffering, and/or for caching of the information). As used herein, the term tangible computer readable storage medium is expressly defined to include any type of computer readable storage device and/or storage disk and to exclude propagating signals

and to exclude transmission media. As used herein, "tangible computer readable storage medium" and "tangible machine readable storage medium" are used interchangeably. Additionally or alternatively, the example processes of FIGS. 15-18 may be implemented using coded instructions (e.g., computer and/or machine readable instructions) stored on a non-transitory computer and/or machine readable medium such as a hard disk drive, a flash memory, a read-only memory, a compact disk, a digital versatile disk, a cache, a random-access memory and/or any other storage device or storage disk in which information is stored for any duration (e.g., for extended time periods, permanently, for brief instances, for temporarily buffering, and/or for caching of the information). As used herein, the term non-transitory computer readable medium is expressly defined to include any type of computer readable storage device and/or storage disk and to exclude propagating signals and to exclude transmission media. As used herein, when the phrase "at least" is used as the transition term in a preamble of a claim, it is open-ended in the same manner as the term "comprising" is open ended.

[0063] FIG. 15 is a flowchart representation of an example process 1500 for monitoring and repairing TSV function as part of manufacturing a semiconductor die (e.g., die 100 of FIGS. 1A-1B (and sub-parts shown in FIGS. 3, 4, 5, 7, and 11-14)). The example process begins at block 1502. At block 1502, an interconnect analysis is initiated. For example, a manufacturing test mode is initiated. For example, an instruction from the TAP 150 triggers a manufacturing test mode for the TSV 102-108 in the die 100. As another example, a field repair mode is initiated. For example, an

instruction from the TAP 150 triggers a field repair mode for the TSV 102-108 in the die 100.

[0064] At block 1504, an operating characteristic associated with the semiconductor interconnect (e.g., a TSV, etc.) is measured. For example, in a high current mode, a current-to-voltage induced frequency can be measured by each LCA 120-126 for each associated TSV 102-108. As another example, in a low current mode, a rate of capacitor discharge can be measured by each LCA 120-126 for each associated TSV 102-108. In some examples, a mode setting or variable is analyzed and/or a mode is determined by current measurement to configure measurement according to a low current mode or a high current mode (and/or a manufacturing mode vs. an in-field analysis mode, etc.).

[0065] At block 1506, the measured operating characteristic is compared to a reference. For example, in a manufacturing test mode, the measured operating characteristic is compared to a failure map and/or other threshold to identify a failed/faulty interconnect. In a field repair mode, the measured operating characteristic is compared to an initial reference value threshold to identify a failed/faulty interconnect.

[0066] At block 1508, the comparison is processed for each interconnect. For example, each LCA 120-126 reports regarding each TSV 102-108, and the LCA 120-126 repairs and/or replaces its associated TSV 102-108 if indicated by the comparison (and available based on hardware usage on the die 100).

[0067] FIG. 16 provides additional detail regarding measuring the interconnect characteristic at block 1504 of the example of FIG. 15. In the example of FIG. 16, at block 1602, the LCA 120-126 is instructed to measure the characteristic. For example, the TSV controller 130 instructs the LCAs 120-126 to measure frequency for each TSV 102-108. For example, based on the TAP 150 instructions, the TSV control FSM 132 instructs each LCA 120-126 to measure a current-to-voltage induced frequency for their respective TSV 102-108. In certain examples, frequency is measured in a high current mode, while a rate of RC decay is measured in a low current mode.

[0068] At block 1604, each LCA 120-126 is activated and configures test conditions for interconnect analysis. For example, each LCA 120-126 is activated and sets up test conditions for TSV 102-108 analysis (e.g., reference current generated along the TSV 102-108, etc.).

[0069] At block 1606, the characteristic is measured. For example, each LCA 120-126 processes the reference current with respect to the resistance 1130 of the TSV 102-108 to generate a bias voltage 1160 which drives the RO 340 and triggers the counter 360 for measurement. Alternatively or in addition, the LCA 120-126 can enable a charging and discharging of a capacitor 508 through the TSV 102-108 to measure a rate of decay using the RO 340 and counter 360, for example.

[0070] FIG. 17 provides additional detail regarding comparing the measured interconnect characteristic to a reference at block 1506 of the example of FIG. 15. In the example of FIG. 17, at block 1702, measurement information is stored. For example, frequency and/or decay information is

stored. For example, the counter 360 stores count information corresponding to the frequency (and/or decay) in the TSV count register 370 for that TSV 102-108.

[0071] At block 1704, the compare logic 136 analyzes the measurement information to determine whether the TSV 102-108 passes or fails. For example, the compare logic 136 compares the stored data 372 to a failure map and/or other threshold to identify a failed/faulty TSV 102-108 and/or a failing TSV 102-108 that is partially working but not completely working according to specification.

[0072] In certain examples, information is stored (block 1702) followed by analysis (block 1704) when the circuit is in manufacturing test mode. When the circuit is operating in field analysis mode, however, the order is reversed. That is, the measurement (e.g., the measured frequency and/or on/off sequence from the RO indicating RC decay, etc.) is compared to a reference to determine whether the TSV 102-108 passes or fails. For example, the compare logic 136 compares the measured frequency from the RO 340 to a time 0 reference value (e.g., an initial value measured at time of production, installation, initial operation, etc.) to determine whether the TSV 102-108 passes or fails. The information is then stored.

[0073] FIG. 18 provides additional detail regarding comparing the measured interconnect characteristic to a reference at block 1508 of the example of FIG. 15. In the example of FIG. 18, at block 1802, the results of the compare logic 136 for each LCA 120-126 associated with each TSV 102-108 are analyzed to identify which TSV 102-108 have passed and which TSV

102-108 have failed. If all TSV 102-108 have passed then, at block 1804, a pass/fail map 140 is stored (e.g., to volatile and/or non-volatile memory on the die 100, at a tester, at a connected processor, etc.).

[0074] However, if one or more TSV 102-108 have failed, then, at block 1806, the failed/failing TSV 102-108 is evaluated to determine whether its operating voltage should be increased. For example, if a TSV 102-108 is partially operational but partially failing, an increase in operating voltage may repair the TSV 102-108, at least temporarily. If the operating voltage is to be increased, then, at block 1808, the LCA 120-126 increases the operating voltage of its TSV 102-108 to repair the TSV 102-108.

[0075] However, if the TSV 102-108 has failed or an increase in voltage is not desired (and/or is not permitted), then, at block 1810, a repair mode is invoked. At block 1812, the LCA 120-126 facilitates replacement of the faulty TSV 102-106 with a redundant TSV 108. For example, if the die 100 includes one or more redundant TSV 108, those TSV are used for replacement if/when a TSV 102-106 in use becomes faulty. For example, suppose the TSV 104 is determined to be faulty. Then, the LCA 122 associated with the TSV 104 deactivates the TSV 104 (e.g., via the mux 330) and sends a signal (e.g., data out 380) to the LCA 126 associated with redundant TSV 108 to activate (e.g., via the mux 330) the TSV 108 in place of the now deactivated TSV 104, for example. After the faulty TSV 104 has been replaced, control reverts to block 1504 to make sure the replacement TSV 108 is operating properly (e.g., within defined limits/values for operation, etc.).

[0076] In some examples, an alert can be sent (e.g., via the TAP 150) to indicate the failure, replacement, repair, etc., to an external tester, processor, control, etc.

[0077] FIG. 19 is a schematic illustration of an example processor platform that may execute instructions with respect to FIGS. 15-18 to implement or help facilitate monitoring, diagnosis, and repair of devices shown in or referenced by FIGS. 1-14.

[0078] The processor platform 1900 can be, for example, a part of a circuit or semiconductor die 100, an attached monitor, tester, and/or other processor (e.g., to generate commands via the TAP 150, control the TSV controller 130, etc.). The processor platform 1900 of the illustrated example includes a processor 1912. The processor 1912 of the illustrated example is hardware. For example, the processor 1912 can be implemented by one or more integrated circuits, logic circuits, microprocessors or controllers from any desired family or manufacturer. In the illustrated example, the processor 1912 is structured to include the example LCA 120-126, the example TSV controller 130, the example pass/fail mapping 140, and/or the example TAP 150.

[0079] The processor 1912 of the illustrated example includes a local memory 1913 (e.g., a cache). The processor 1912 of the illustrated example is in communication with a main memory including a volatile memory 1914 and a non-volatile memory 1916 via a bus 1918. The volatile memory 1914 may be implemented by Synchronous Dynamic Random Access Memory (SDRAM), Dynamic Random Access Memory (DRAM), RAMBUS Dynamic

Random Access Memory (RDRAM) and/or any other type of random access memory device. The non-volatile memory 1916 may be implemented by flash memory and/or any other desired type of memory device. Access to the main memory 1914, 1916 is controlled by a memory controller.

[0080] The processor platform 1900 of the illustrated example also includes an interface circuit 1920. The interface circuit 1920 may be implemented by any type of interface standard, such as an Ethernet interface, a universal serial bus (USB), and/or a peripheral component interconnect (PCI) express interface.

[0081] In the illustrated example, one or more input devices 1922 are connected to the interface circuit 1920. The input device(s) 1922 permit(s) a user to enter data and commands into the processor 1912. The input device(s) 1922 can be implemented by, for example, one or more sensors, pins connectors, etc.

[0082] One or more output devices 1924 are also connected to the interface circuit 1920 of the illustrated example. The output devices 1924 can be implemented, for example, by display devices (e.g., a light emitting diode (LED), an organic light emitting diode (OLED), a liquid crystal display, a cathode ray tube display (CRT), a touchscreen, a tactile output device), pin-based connectors, etc.

[0083] The interface circuit 1920 of the illustrated example also includes a communication device such as a transmitter, a receiver, a transceiver, a modem and/or network interface card to facilitate exchange of data with external machines (e.g., computing devices of any kind) via a

network 1926 (e.g., an Ethernet connection, a digital subscriber line (DSL), a telephone line, coaxial cable, a cellular telephone system, etc.).

[0084] The processor platform 1900 of the illustrated example also includes one or more storage devices 1928 for storing software and/or data. Examples of such storage devices 1928 include DRAM, RAM, ROM, flash memory, floppy disk drives, hard drive disks, compact disk drives, Blu-ray disk drives, RAID systems, and digital versatile disk (DVD) drives.

[0085] The coded instructions 1932 with respect to FIGS. 15-18 (e.g., to generate control commands via the TAP 150, the control the TSV controller 130 and/or LCA 120-126, operate an attached tester and/or other processor, etc.) may be stored in the mass storage device 1928, in the volatile memory 1914, in the non-volatile memory 1916, and/or on a removable tangible computer readable storage medium such as a CD or DVD.

[0086] From the foregoing, it will be appreciated that the above disclosed methods, apparatus and articles of manufacture provide oscillator-based reliability detection and calibration. Certain examples involve routing an analog voltage (e.g., a bias voltage generated from a reference current through a monitored interconnect, etc.) to an oscillator (e.g., a ring oscillator, etc.) with proper shielding. Thus, certain examples provide a self-consistent loop with ring oscillators, counters, and TSV voltage control to facilitate interconnect reliability monitoring and correction. Certain examples provide instructions in the BIOS and/or operating system (OS) to facilitate self-testing and adjustment via the die 100.

[0087] Certain examples provide a dedicated, on-die repair apparatus that reduces additional guard band(s) added to the circuit design. With an on-die reliability monitor, circuit performance can be improved by removing additional guard band(s). Providing an on-die reliability feature also helps ensure longevity in design performance, as TSV lanes likely experience gradual degradation after 5-10 years of use, rather than massive failure. Memory and other logic chips can use this on-die technology to identify and repair interconnect degradation and prolong the usable life of the circuit, for example.

[0088] Example 1 is an apparatus including a local control and allocation logic connected to an electrical interconnect. The local control and allocation logic of example 1 is to evaluate operation of the electrical interconnect and generate a first output indicative of an operating characteristic of the interconnect. The local control and allocation logic of example 1 includes a ring oscillator to generate a second output based on an interaction with the interconnect; and a counter to increment a count based on the second output of the ring oscillator, the first output generated based on the count. The apparatus of example 1 also includes a controller to process the first output indicative of an operating characteristic of the interconnect. The controller of example 1 is to initiate repair of the interconnect when the first output does not satisfy a threshold.

[0089] Example 2 includes the subject matter of example 1, wherein the electrical interconnect includes a through-silicon via.

[0090] Example 3 includes the subject matter of example 1, wherein the repair of the interconnect includes at least one of a) repairing the interconnect by increasing an operating voltage across the interconnect or b) deactivating the interconnect and activating a redundant interconnect in place of the deactivated interconnect.

[0091] Example 4 includes the subject matter of example 3, wherein the repair is implemented by the local control and allocation logic.

[0092] Example 5 includes the subject matter of example 1, wherein the controller and local control and allocation logic operates according to a selected one of a plurality of operating modes.

[0093] Example 6 includes the subject matter of example 5, wherein the plurality of modes include at least one of a low current mode, a high current mode, a manufacturing test mode, or a field repair mode.

[0094] Example 7 includes the subject matter of example 6, wherein different hardware is configured in the local control and allocation logic depending on the mode.

[0095] Example 8 includes the subject matter of example 7, wherein the local control and allocation logic further includes a converter to generate, based on the interconnect, an input for the ring oscillator.

[0096] Example 9 includes the subject matter of example 8, wherein the local control and allocation logic analyzes a resistor-capacitor decay associated with the interconnect generated by the converter to turn the ring oscillator on and off in the low current mode.

[0097] Example 10 includes the subject matter of example 8, wherein the local control and allocation logic analyzes an oscillation frequency produced in the ring oscillator by a bias voltage generated by the converter and associated with the interconnect in the high current mode.

[0098] Example 11 includes the subject matter of example 1, wherein the ring oscillator is a current-starved ring oscillator implemented using a NAND gate and a plurality of current-starved inverters.

[0099] Example 12 is a method to monitor interconnect function in a silicon die. The method of example 12 includes evaluating operation of an electrical interconnect using a local control and allocation logic including a ring oscillator and a counter. The method of example 12 includes generating a first output indicative of an operating characteristic of the interconnect by: generating, using the ring oscillator, a second output based on an interaction with the interconnect; and incrementing, using the counter, a count based on the second output of the ring oscillator. The method of example 12 includes generating the first output based on the count. The method of example 12 includes processing the first output indicative of an operating characteristic of the interconnect. The method of example 12 includes initiating repair of the interconnect when the first output does not satisfy a threshold.

[00100] Example 32 includes the subject matter of example 12, wherein the electrical interconnect includes a through-silicon via.

[00101] Example 14 includes the subject matter of example 12, wherein the repair of the interconnect includes at least one of a) repairing the interconnect by increasing an operating voltage across the interconnect or b)

deactivating the interconnect and activating a redundant interconnect in place of the deactivated interconnect.

[00102] Example 15 includes the subject matter of example 12, wherein the local control and allocation logic operates according to a selected one of a plurality of operating modes.

[00103] Example 16 includes the subject matter of example 15, wherein the plurality of modes include at least one of a low current mode, a high current mode, a manufacturing test mode, or a field repair mode.

[00104] Example 17 includes the subject matter of example 16, wherein different hardware is configured in the local control and allocation logic depending on the mode.

[00105] Example 18 includes the subject matter of example 17, further including analyzing, using the local control and allocation logic, a resistor-capacitor decay associated with the interconnect generated by the converter to turn the ring oscillator on and off in the low current mode.

[00106] Example 19 includes the subject matter of example 17, further including analyzing, using the local control and allocation logic, an oscillation frequency produced in the ring oscillator by a bias voltage generated by the converter and associated with the interconnect in the high current mode.

[00107] Example 20 is a device including a local control and allocation logic connected to a through-silicon via (TSV), the local control and allocation logic to evaluate operation of the TSV depending upon a mode and generate a first output indicative of an operating characteristic of the TSV. In

example 20, the local control and allocation logic includes a ring oscillator to generate a second output based on an interaction with the TSV; and a counter to increment a count based on the second output of the ring oscillator, the first output generated based on the count. The device of example 20 also includes a controller to process the first output indicative of an operating characteristic of the TSV, the controller to instruct the local control and allocation logic to repair the TSV when the first output does not satisfy a threshold.

[00108] Example 21 includes the subject matter of example 20, wherein the mode includes at least one of a low current mode and a high current mode, and wherein the local control and allocation logic a) analyzes a resistor-capacitor decay associated with the interconnect generated to turn the ring oscillator on and off in the low current mode, and b) analyzes an oscillation frequency produced in the ring oscillator by a bias voltage generated by the converter and associated with the interconnect in the high current mode.

[00109] Example 22 is a system including a means for local control and allocation connected to an electrical interconnect, the means for local control and allocation to evaluate operation of the electrical interconnect and generate a first output indicative of an operating characteristic of the interconnect. The system of example 22 includes a means for processing the first output indicative of an operating characteristic of the interconnect, the controller to instruct the local control and allocation logic to repair the interconnect when the first output does not satisfy a threshold.

[00110] Although certain example methods, apparatus and articles of manufacture have been disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the claims of this patent.

What Is Claimed Is:

1. An apparatus comprising:

a local control and allocation logic connected to an electrical interconnect, the local control and allocation logic to evaluate operation of the electrical interconnect and generate a first output indicative of an operating characteristic of the interconnect, the local control and allocation logic including:

a ring oscillator to generate a second output based on an interaction with the interconnect; and

a counter to increment a count based on the second output of the ring oscillator, the first output generated based on the count; and

a controller to process the first output indicative of an operating characteristic of the interconnect, the controller to initiate repair of the interconnect when the first output does not satisfy a threshold.
2. The apparatus of claim 1, wherein the electrical interconnect includes a through-silicon via.
3. The apparatus of claim 1, wherein the repair of the interconnect includes at least one of a) repairing the interconnect by increasing an operating voltage across the interconnect or b) deactivating the interconnect and activating a redundant interconnect in place of the deactivated interconnect.

4. The apparatus of claim 3, wherein the repair is implemented by the local control and allocation logic.

5. The apparatus of claim 1, wherein the controller and local control and allocation logic operates according to a selected one of a plurality of operating modes.

6. The apparatus of claim 5, wherein the plurality of modes include at least one of a low current mode, a high current mode, a manufacturing test mode, or a field repair mode.

7. The apparatus of claim 6, wherein different hardware is configured in the local control and allocation logic depending on the mode.

8. The apparatus of claim 7, wherein the local control and allocation logic further includes a converter to generate, based on the interconnect, an input for the ring oscillator.

9. The apparatus of claim 8, wherein the local control and allocation logic analyzes a resistor-capacitor decay associated with the interconnect generated by the converter to turn the ring oscillator on and off in the low current mode.

10. The apparatus of claim 8, wherein the local control and allocation logic analyzes an oscillation frequency produced in the ring oscillator by a bias voltage generated by the converter and associated with the interconnect in the high current mode.

11. The apparatus of claim 1, wherein the ring oscillator is a current-starved ring oscillator implemented using a NAND gate and a plurality of current-starved inverters.

12. A method to monitor interconnect function in a silicon die, the method comprising:

evaluating operation of an electrical interconnect using a local control and allocation logic including a ring oscillator and a counter;

generating a first output indicative of an operating characteristic of the interconnect by:

generating, using the ring oscillator, a second output based on an interaction with the interconnect; and

incrementing, using the counter, a count based on the second output of the ring oscillator; and

generating the first output based on the count;

processing the first output indicative of an operating characteristic of the interconnect; and

initiating repair of the interconnect when the first output does not satisfy a threshold.

13. The method of claim 12, wherein the electrical interconnect includes a through-silicon via.

14. The method of claim 12, wherein the repair of the interconnect includes at least one of a) repairing the interconnect by increasing an operating voltage across the interconnect or b) deactivating the interconnect and activating a redundant interconnect in place of the deactivated interconnect.

15. The method of claim 12, wherein the local control and allocation logic operates according to a selected one of a plurality of operating modes.

16. The method of claim 15, wherein the plurality of modes include at least one of a low current mode, a high current mode, a manufacturing test mode, or a field repair mode.

17. The method of claim 16, wherein different hardware is configured in the local control and allocation logic depending on the mode.

18. The method of claim 17, further including analyzing, using the local control and allocation logic, a resistor-capacitor decay associated with the interconnect generated by the converter to turn the ring oscillator on and off in the low current mode.

19. The method of claim 17, further including analyzing, using the local control and allocation logic, an oscillation frequency produced in the ring oscillator by a bias voltage generated by the converter and associated with the interconnect in the high current mode.

20. A device comprising
a local control and allocation logic connected to a through-silicon via (TSV), the local control and allocation logic to evaluate operation of the TSV depending upon a mode and generate a first output indicative of an operating characteristic of the TSV, the local control and allocation logic including:

a ring oscillator to generate a second output based on an interaction with the TSV; and
a counter to increment a count based on the second output of the ring oscillator, the first output generated based on the count; and
a controller to process the first output indicative of an operating characteristic of the TSV, the controller to instruct the local control and allocation logic to repair the TSV when the first output does not satisfy a threshold.

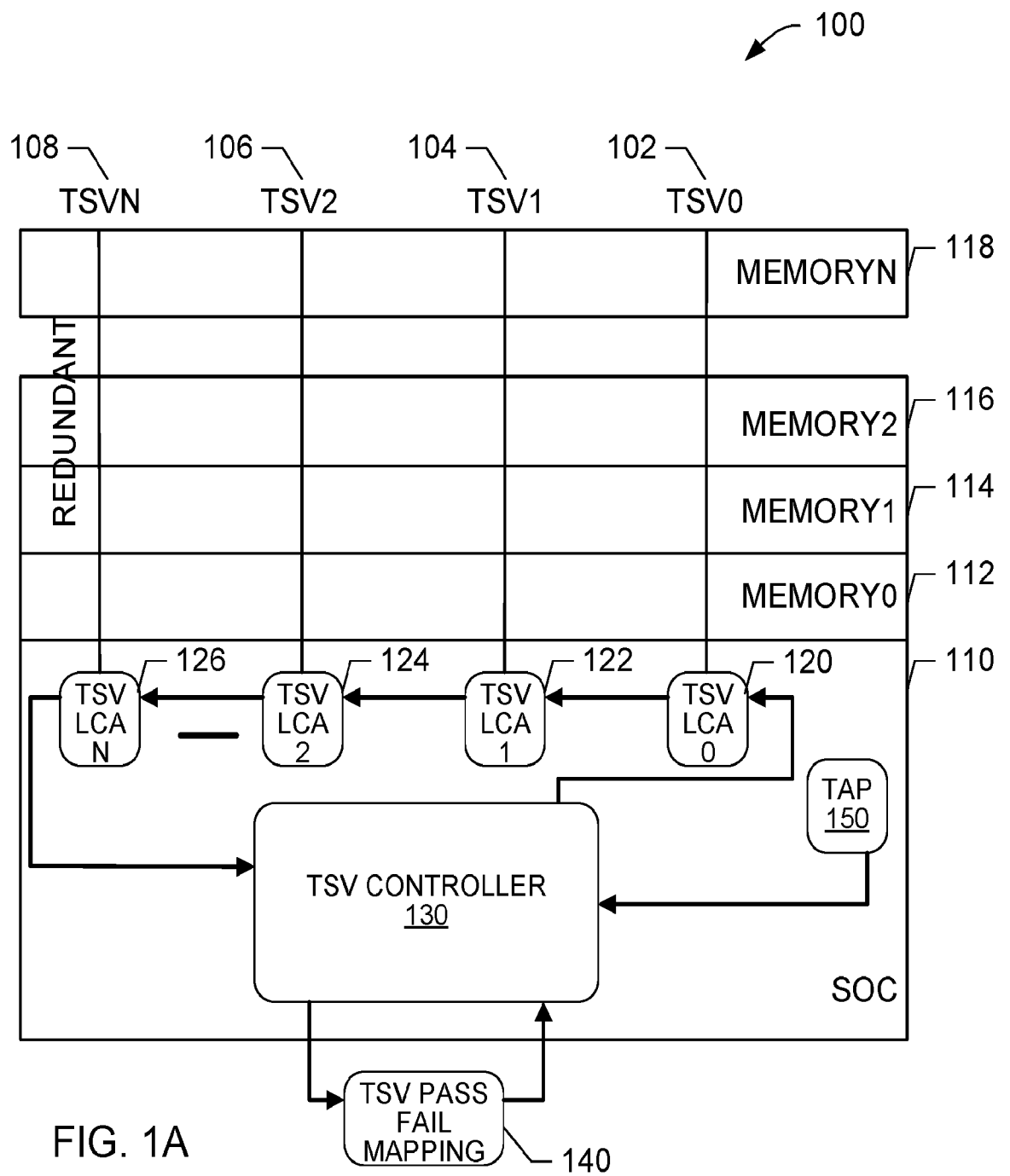
21. The device of claim 20, wherein the mode includes at least one of a low current mode and a high current mode, and wherein the local control and allocation logic a) analyzes a resistor-capacitor decay associated with the interconnect generated to turn the ring oscillator on and off in the low current

mode, and b) analyzes an oscillation frequency produced in the ring oscillator by a bias voltage generated by the converter and associated with the interconnect in the high current mode.

22. A system comprising:

a means for local control and allocation connected to an electrical interconnect, the means for local control and allocation to evaluate operation of the electrical interconnect and generate a first output indicative of an operating characteristic of the interconnect; and

a means for processing the first output indicative of an operating characteristic of the interconnect, the controller to instruct the local control and allocation logic to repair the interconnect when the first output does not satisfy a threshold.



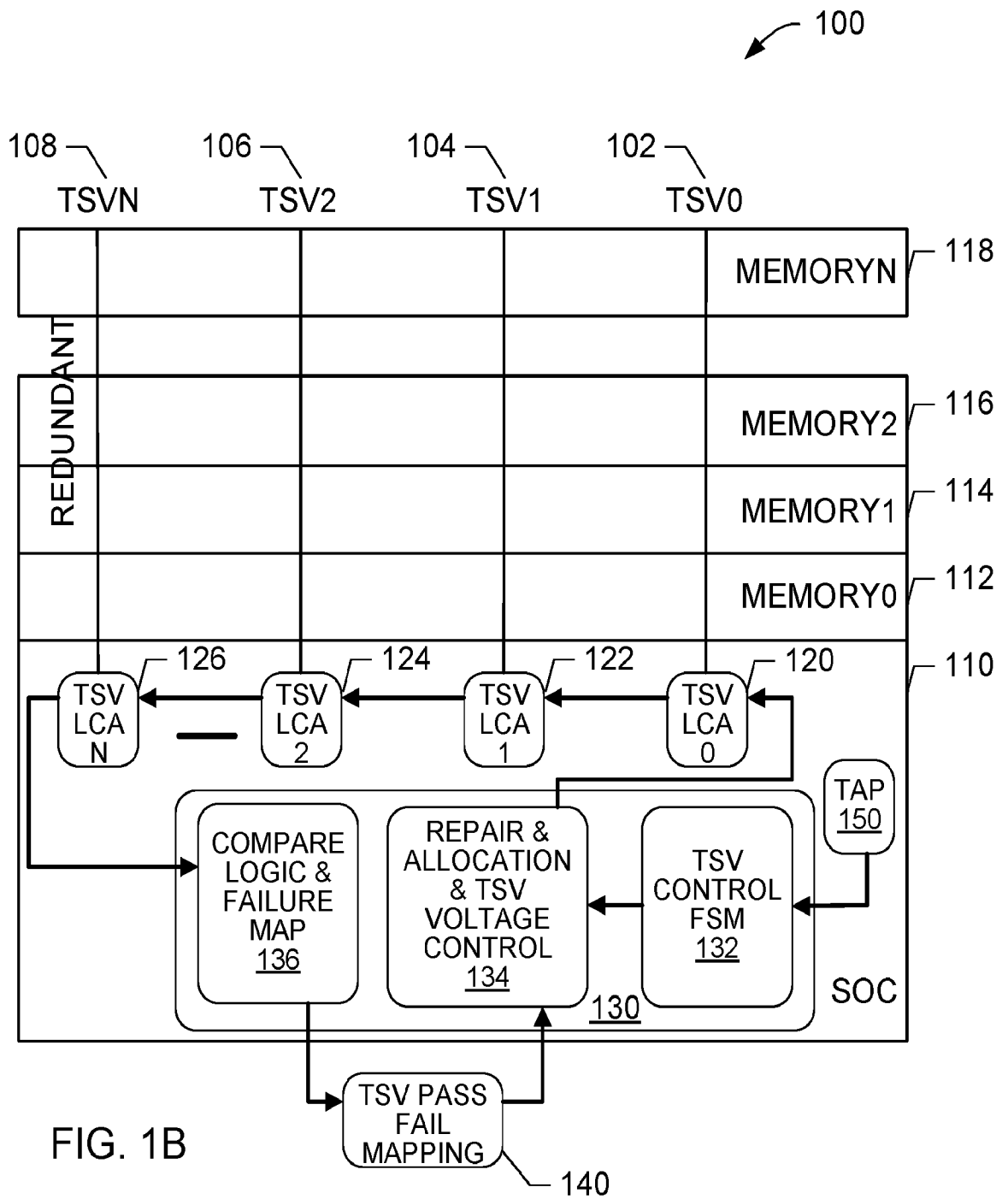


FIG. 1B

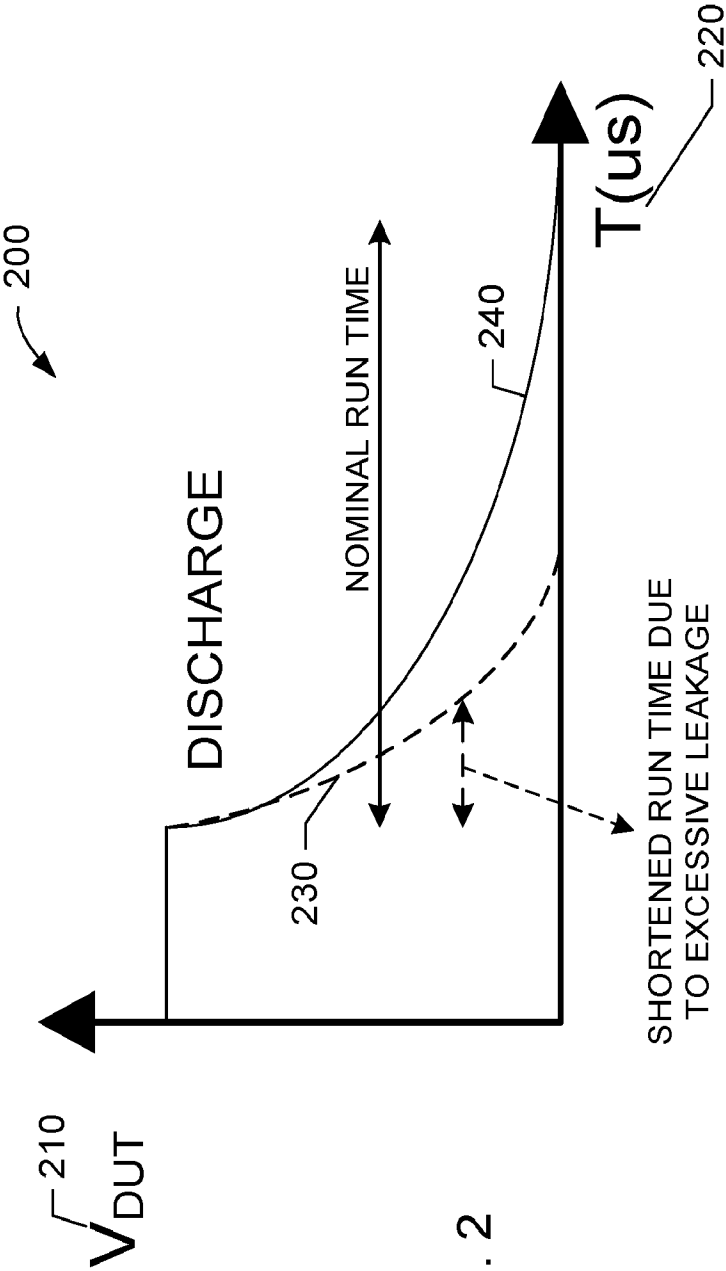
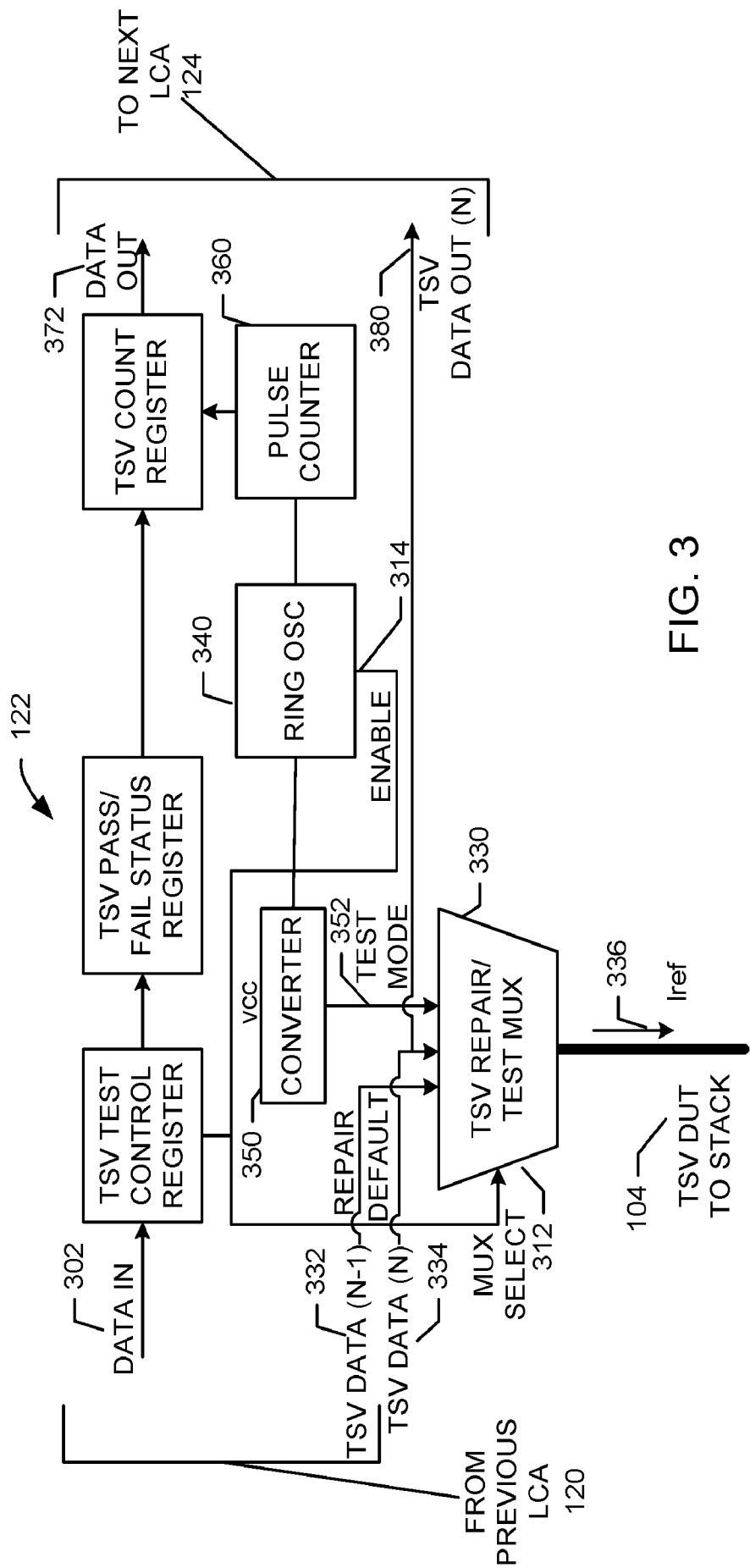


FIG. 2



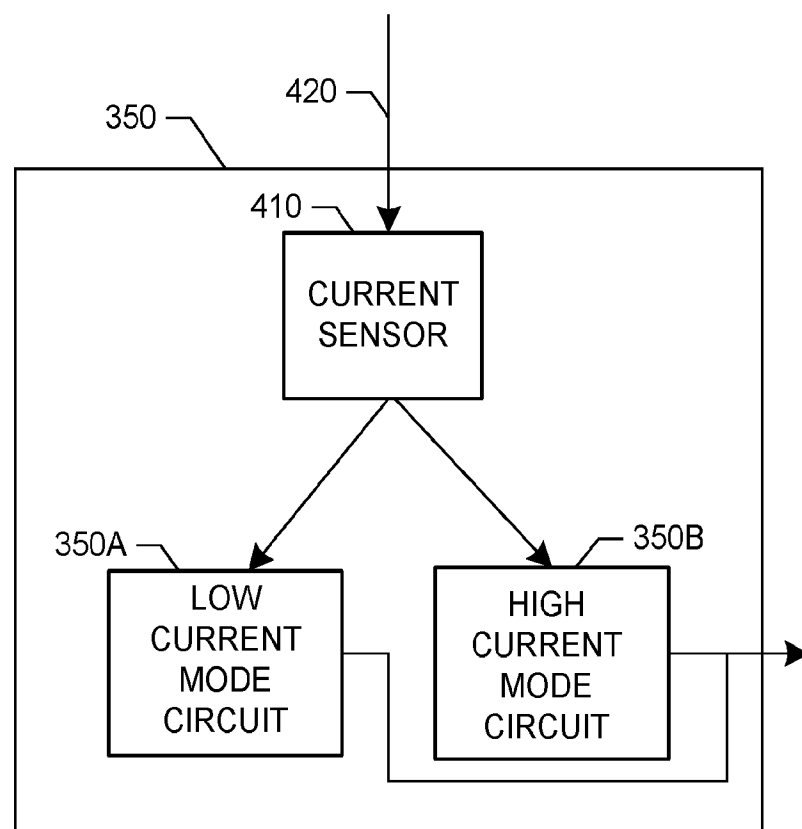


FIG. 4

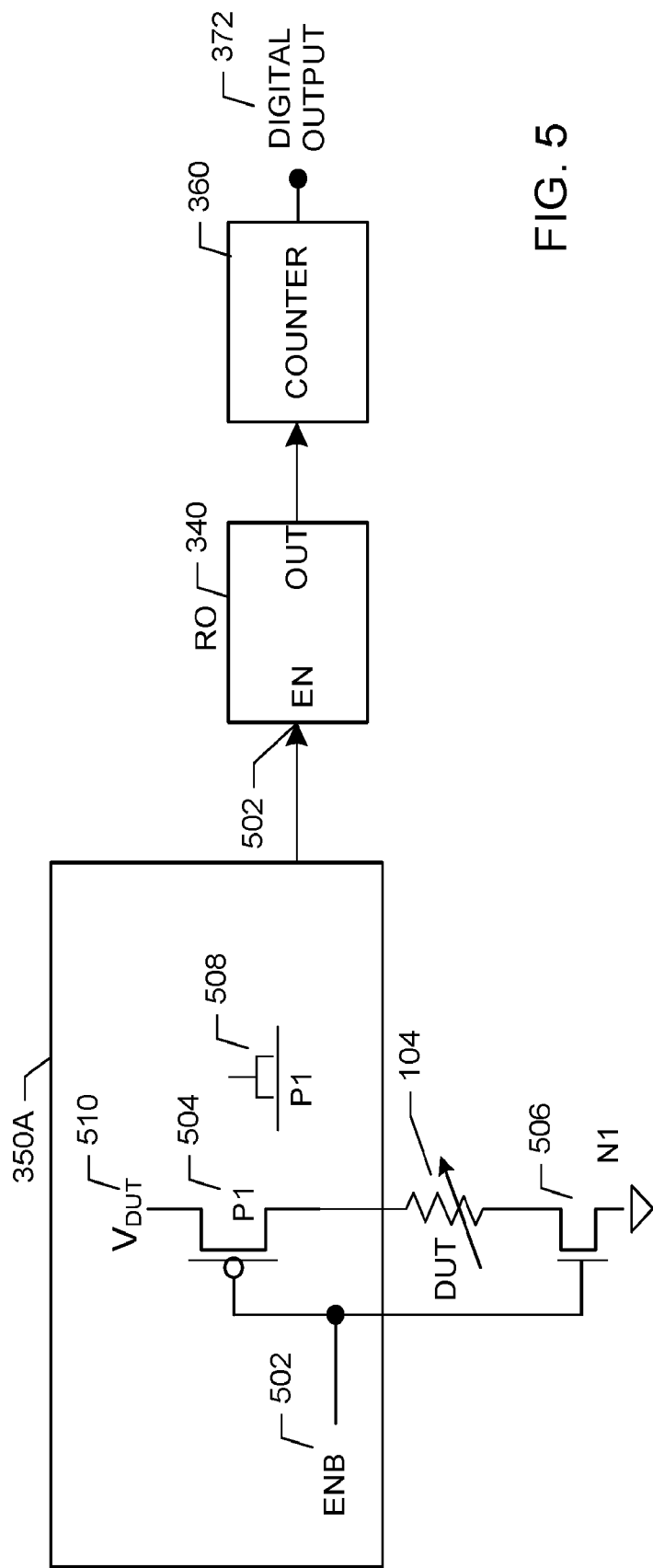


FIG. 5

600

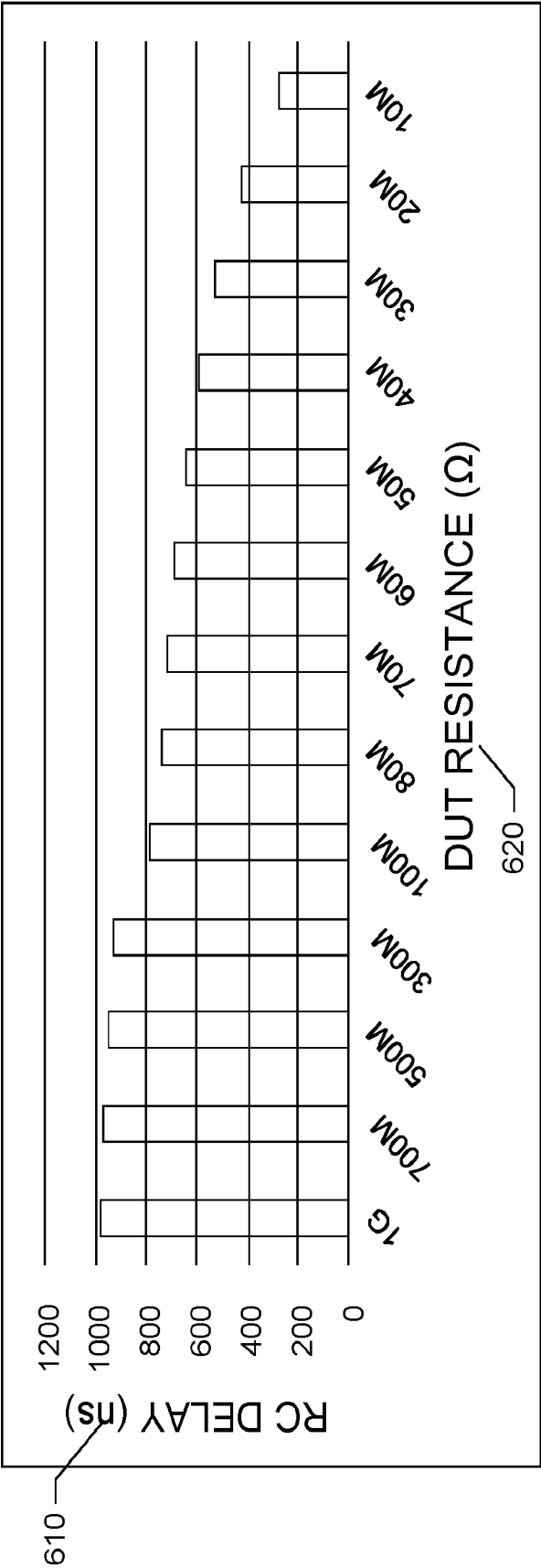


FIG. 6

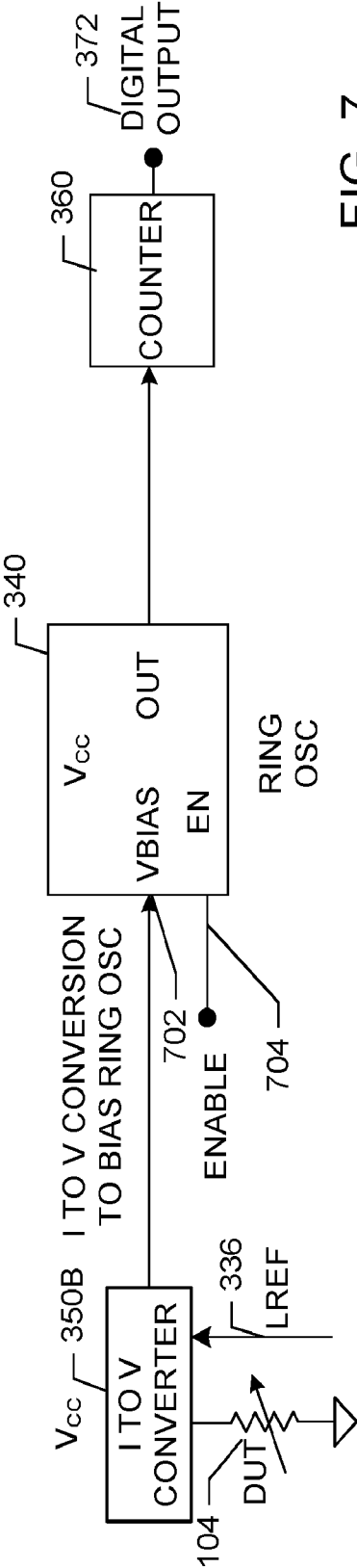


FIG. 7

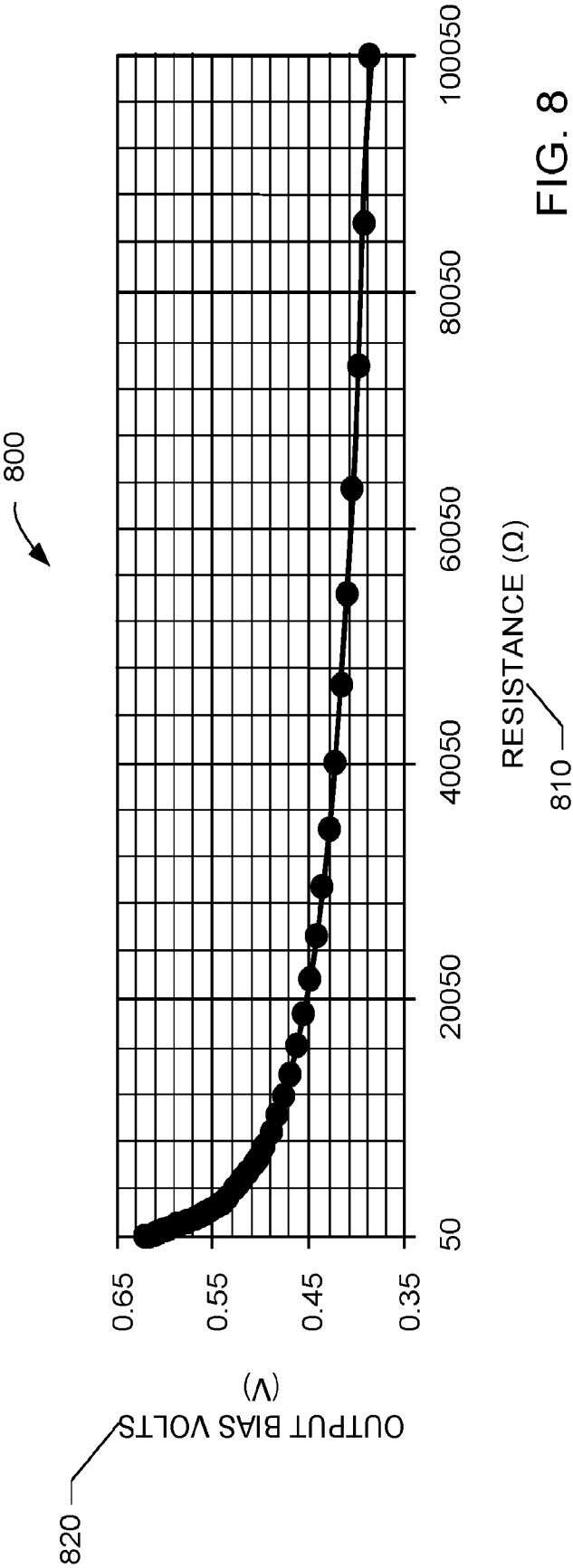


FIG. 8

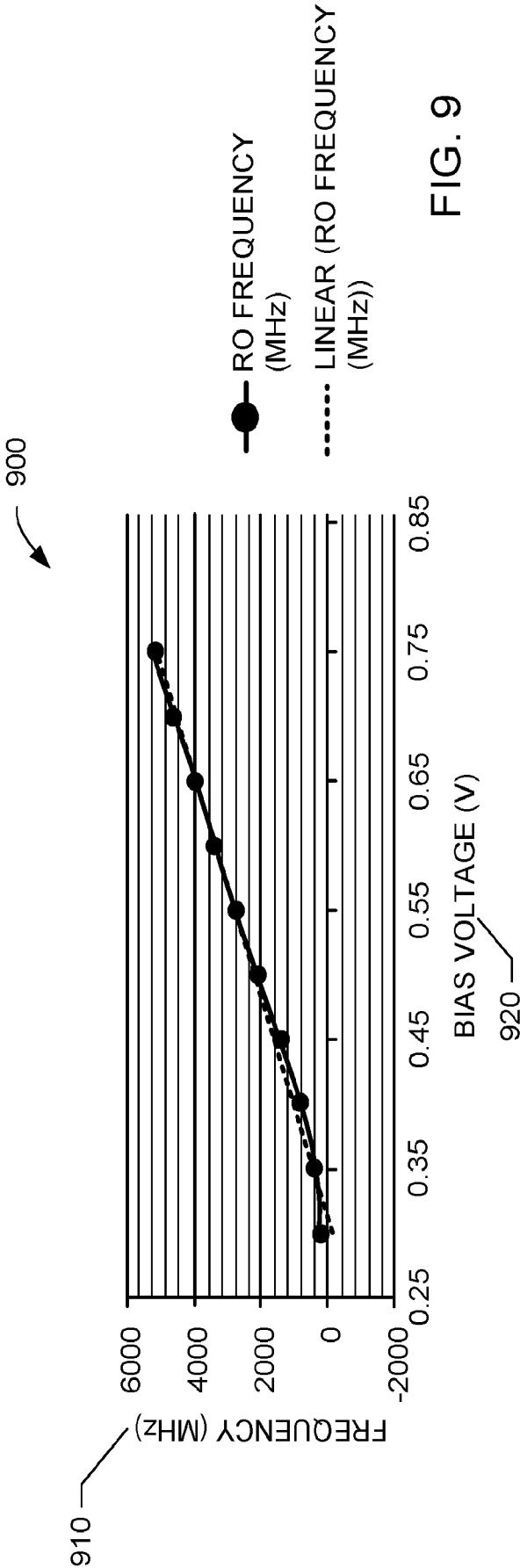


FIG. 9

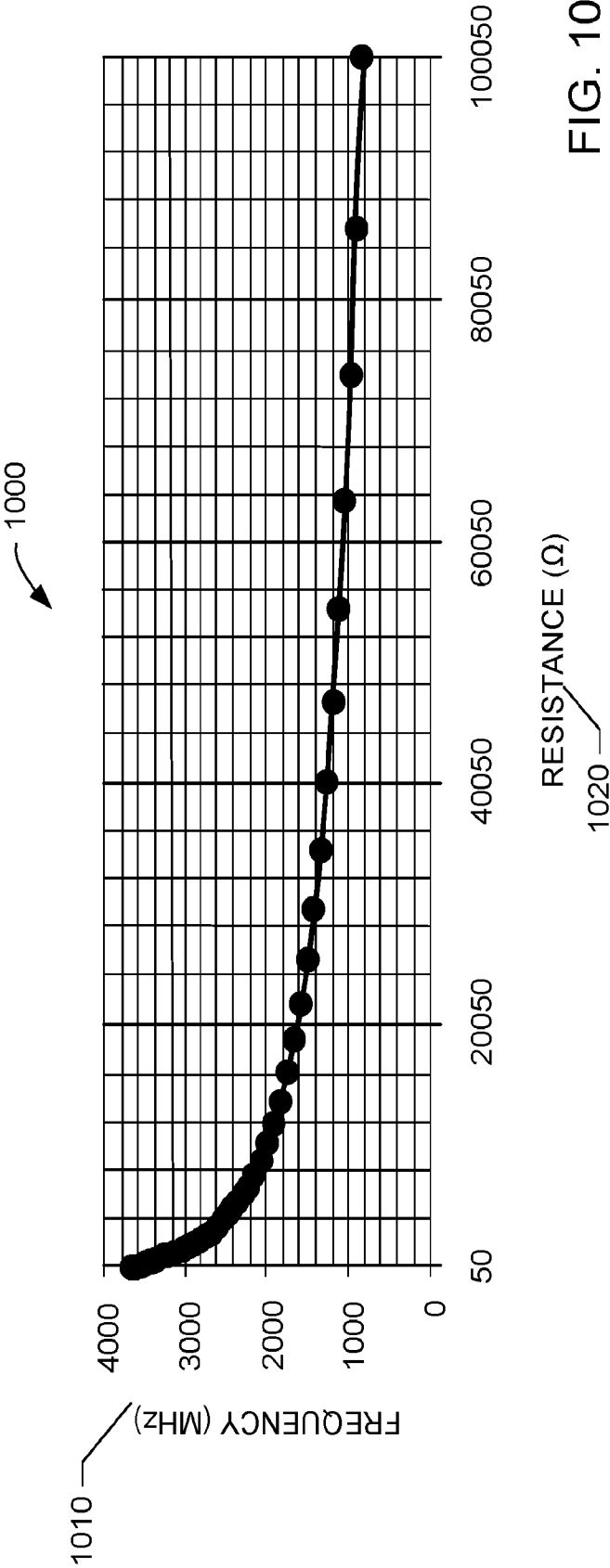


FIG. 10

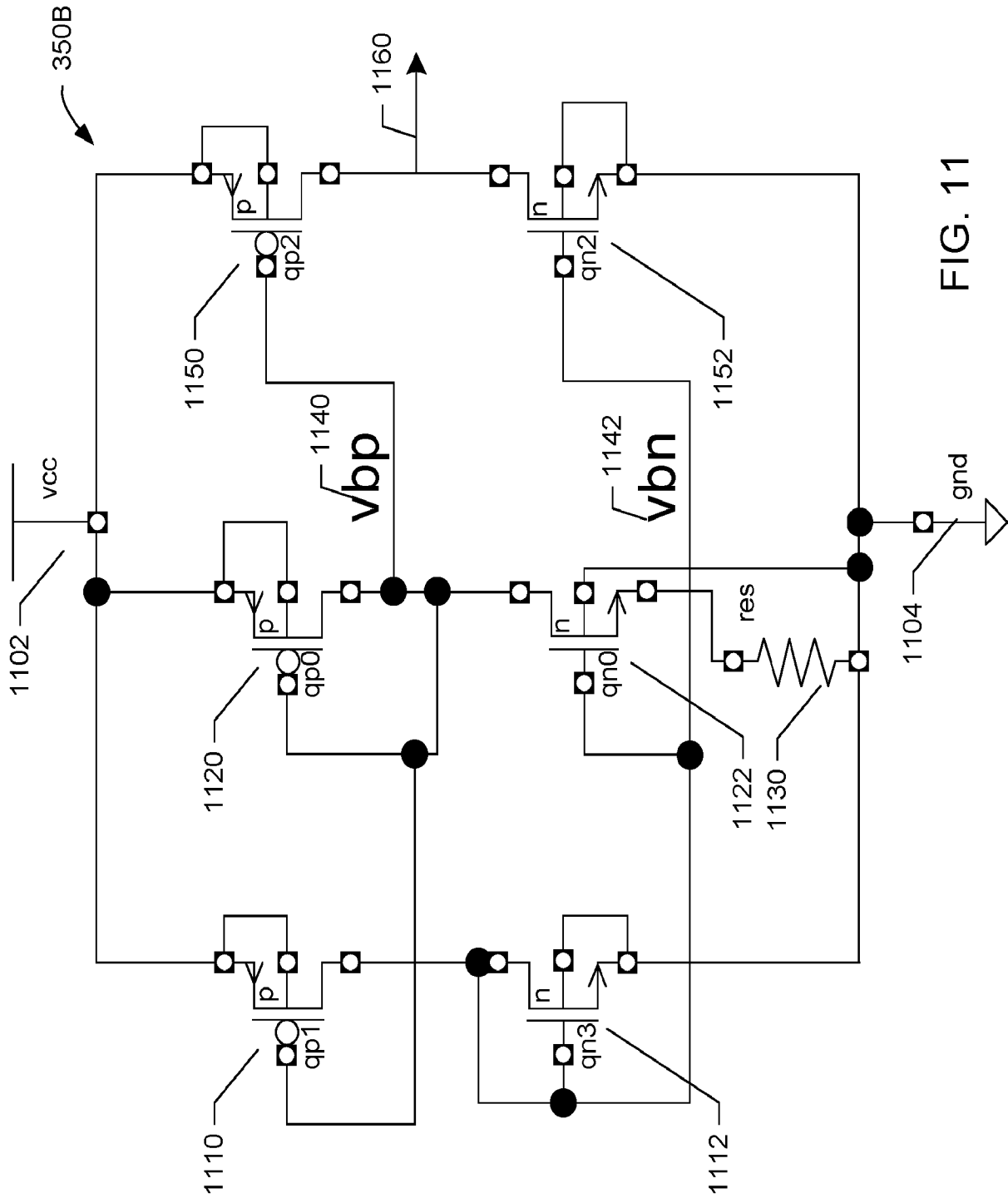


FIG. 11

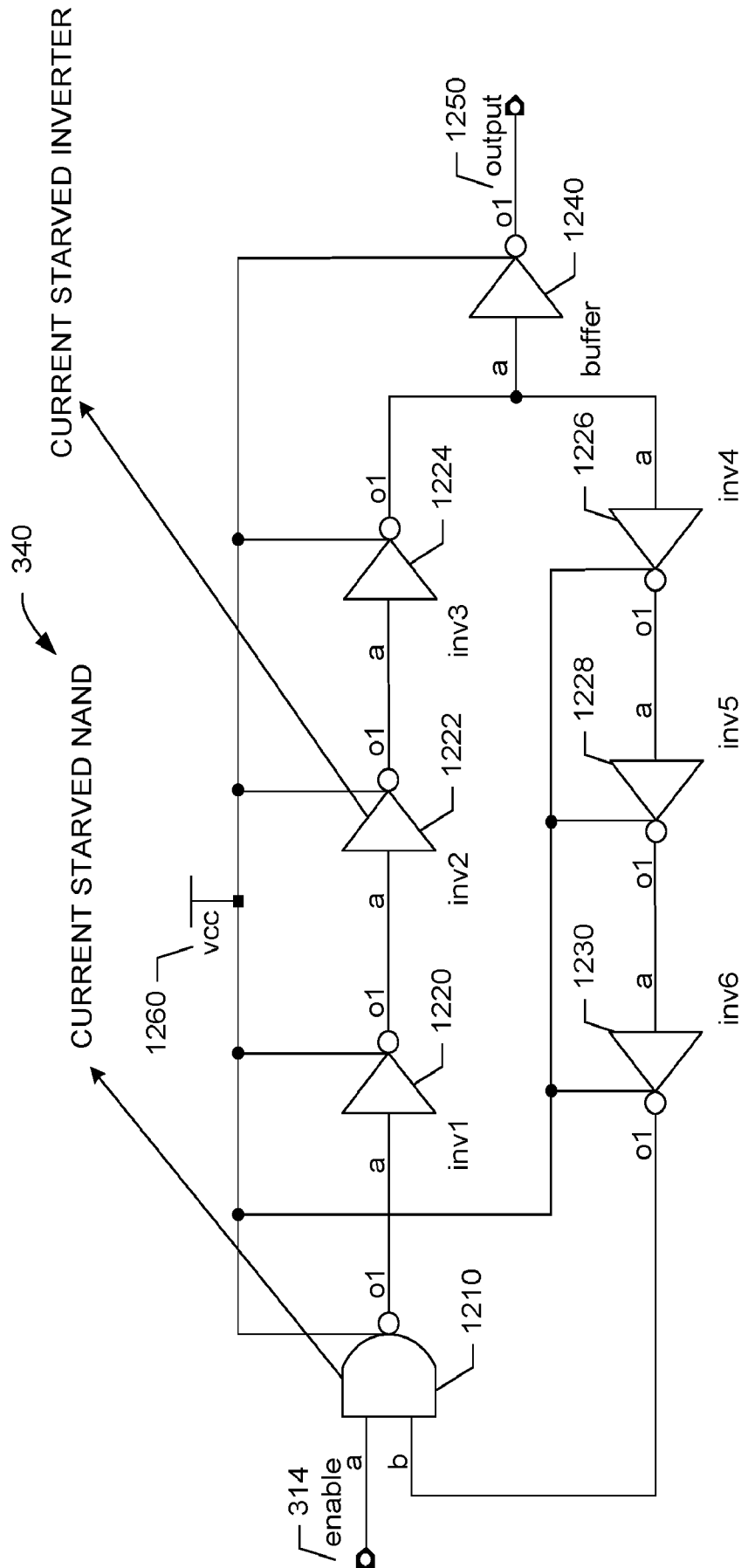


FIG. 12

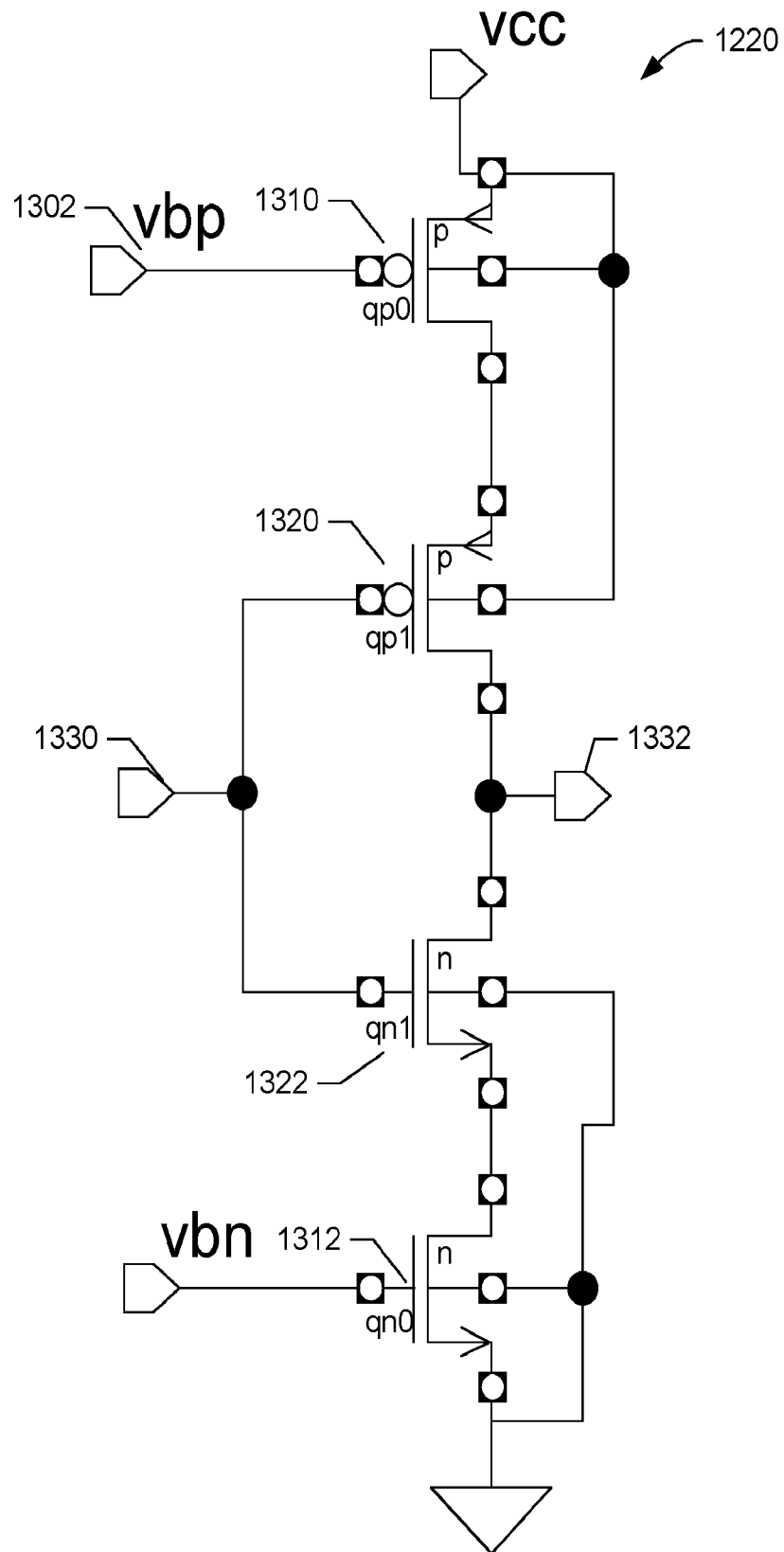
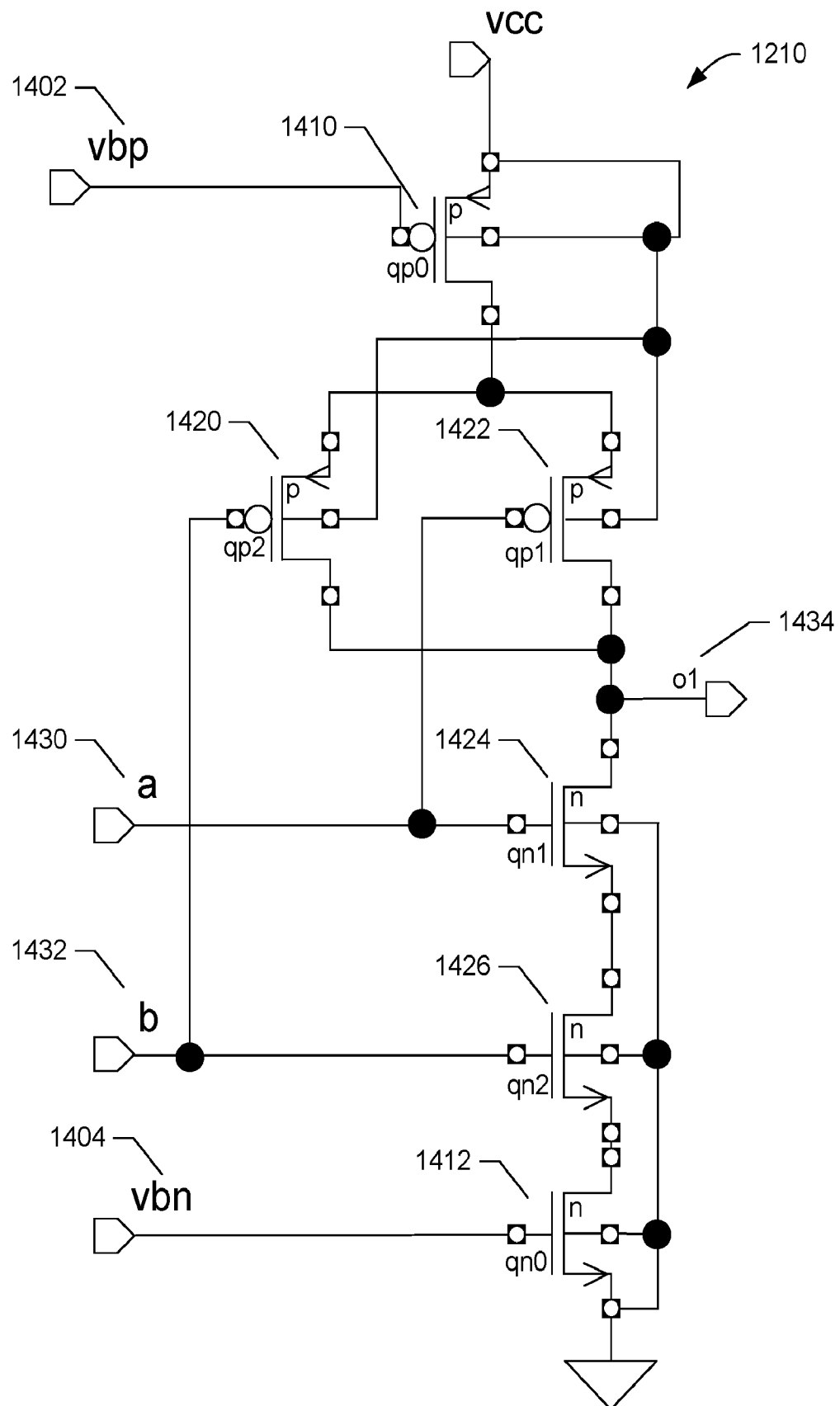


FIG. 13



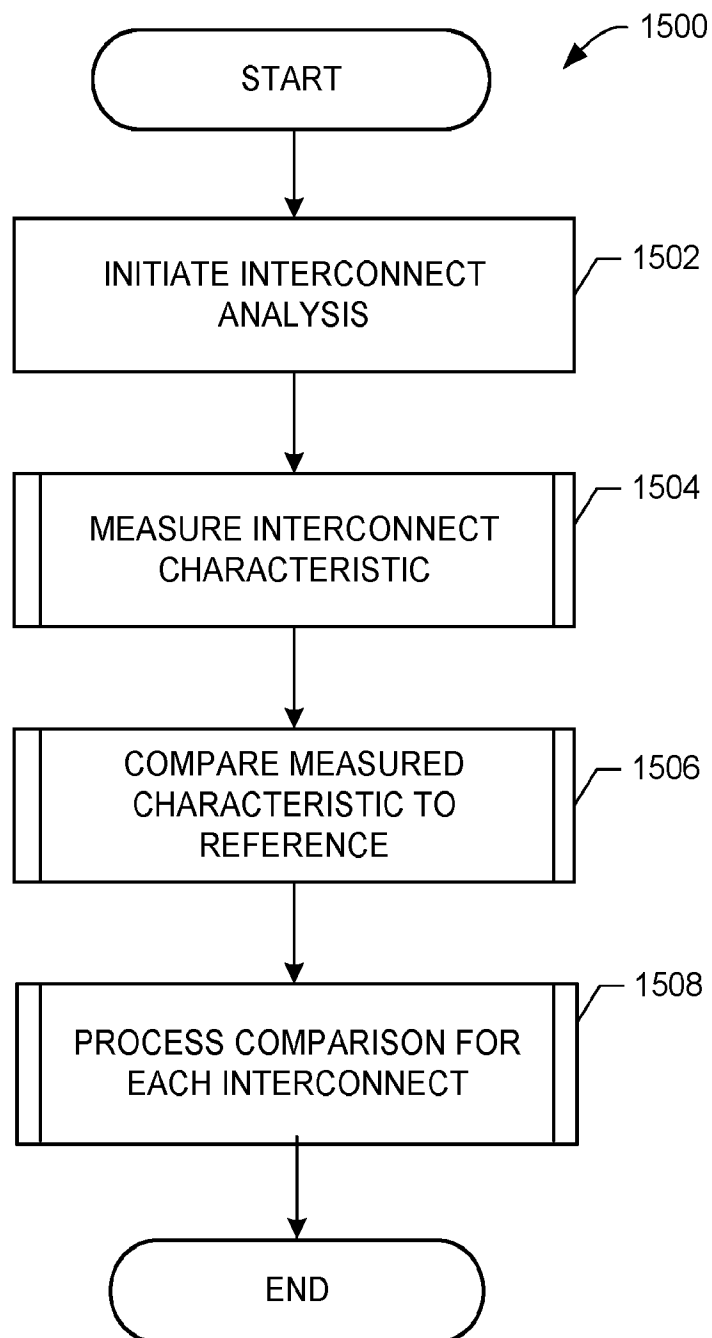


FIG. 15

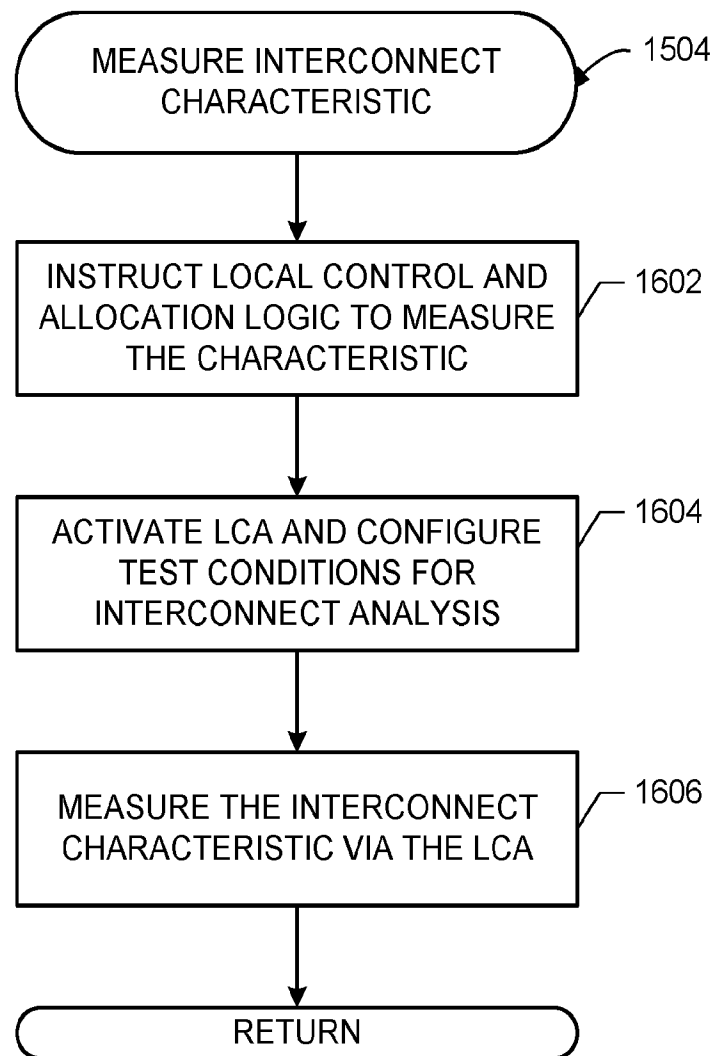


FIG. 16

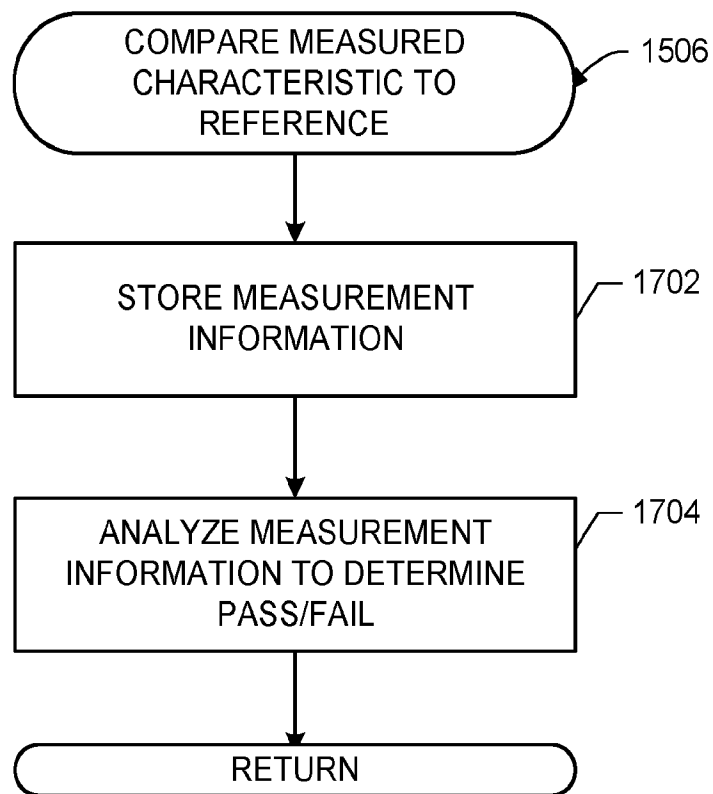


FIG. 17

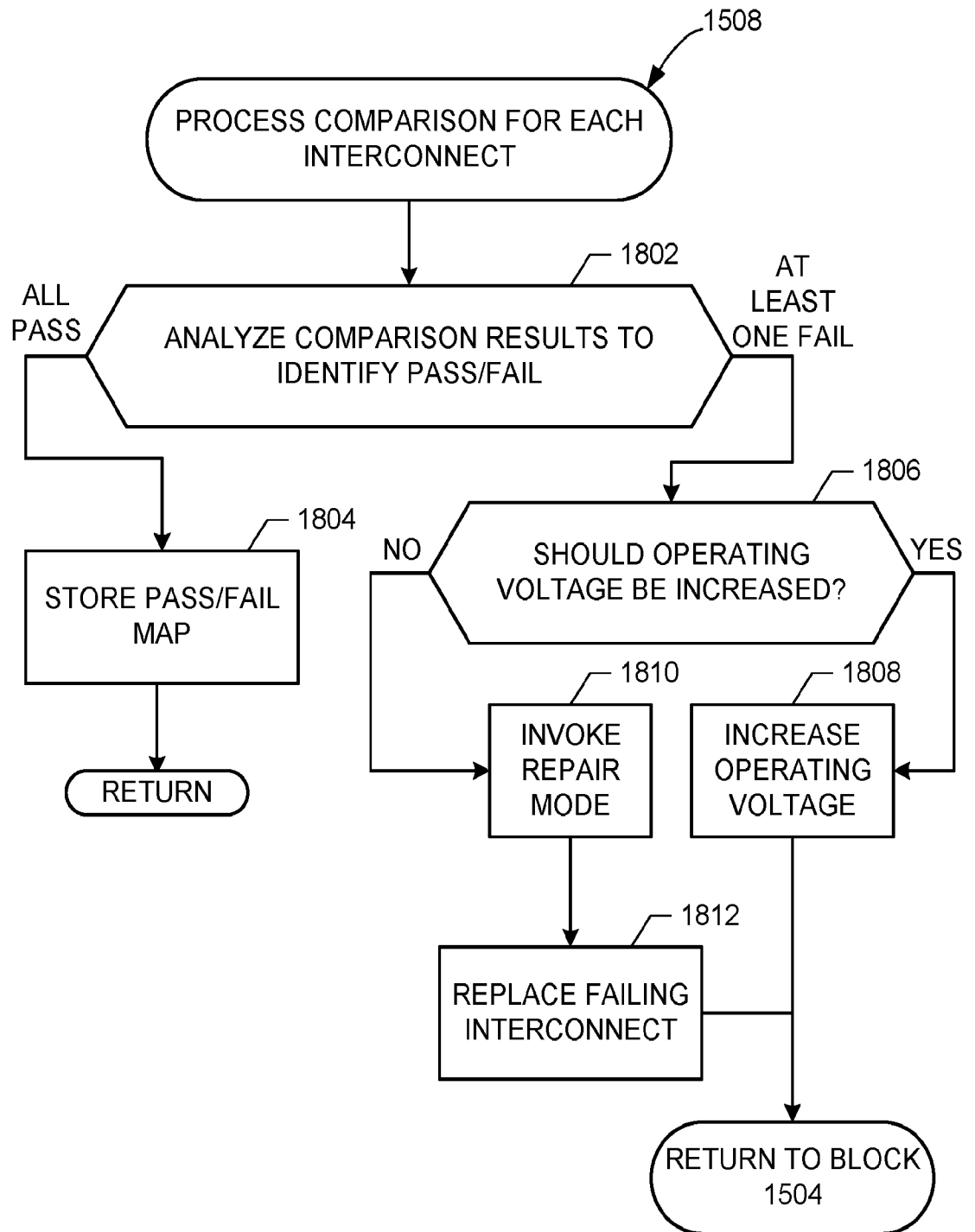


FIG. 18

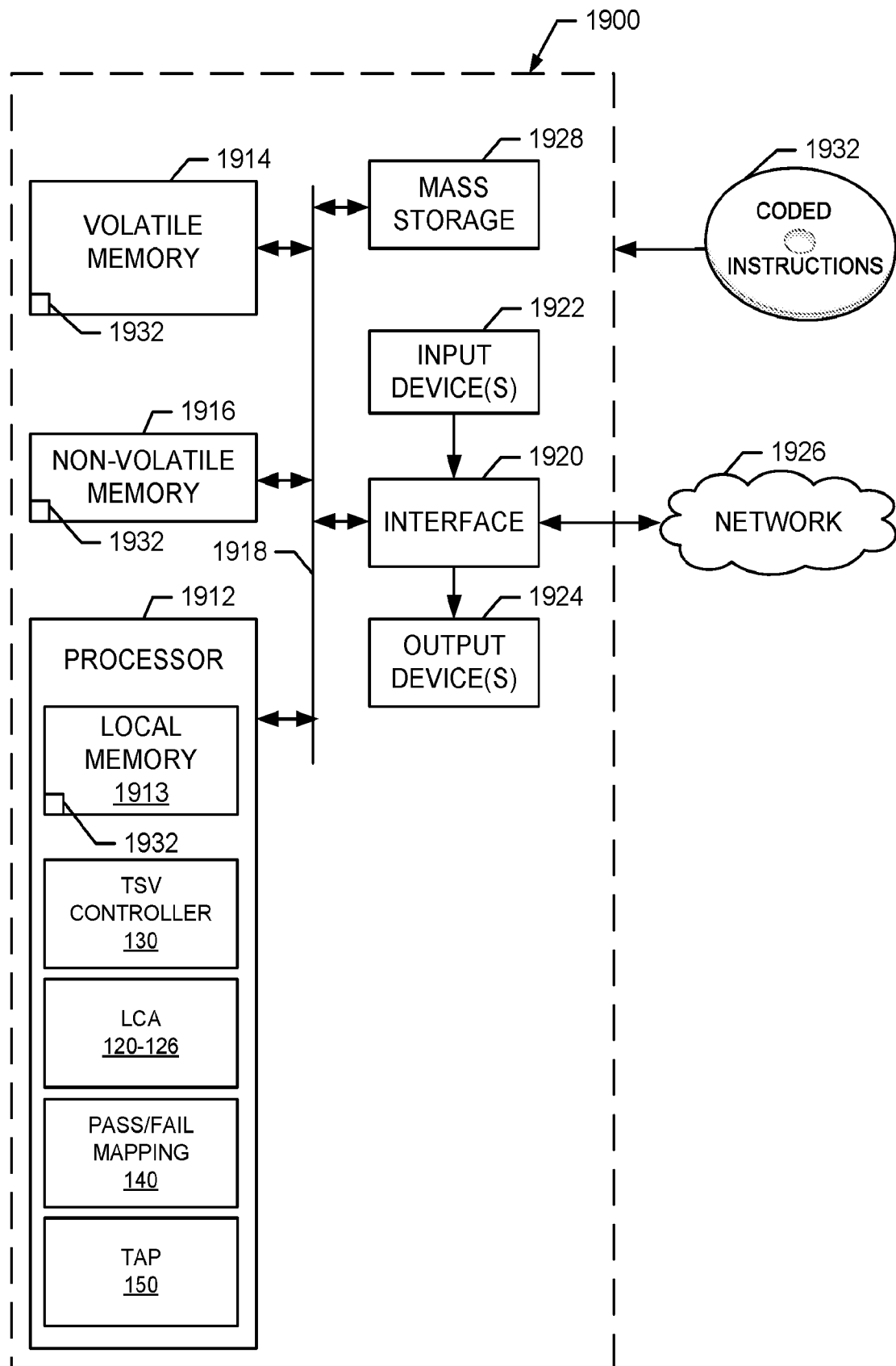


FIG. 19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/040394**A. CLASSIFICATION OF SUBJECT MATTER****G01R 31/28(2006.01)i, G01R 31/26(2006.01)i, G01R 31/27(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R 31/28; G01R 31/3185; G01R 31/26; H01L 21/66; G01R 31/27

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: through, silicon, via, TSV, interconnect, repair, ring, oscillator, controller

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 9157960 B2 (BRINGIVIJAYARAGHAVAN et al.) 13 October 2015 See abstract, column 3, lines 51-59, claim 3 and figure 3.	1-22
A	US 2014-0266291 A1 (COMMISSARIAT A L'ENERGIE ATOMIQUE ET AUX ENE ALT) 18 September 2014 See abstract, claims 3-8 and figures 1-3.	1-22
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Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

23 March 2017 (23.03.2017)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040394

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