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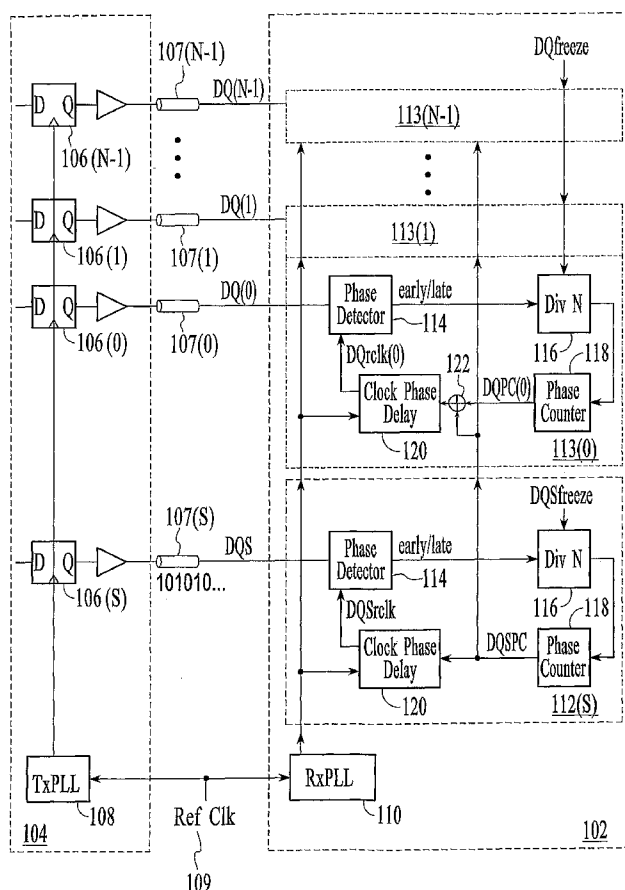
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(54) Title: BIT-DESKEWING IO METHOD AND SYSTEM



(57) Abstract: An IO method and system for bit-deskewing are described. Embodiment includes a computer system with multiple components that transfer data among them. In one embodiment, a system component receives a forward strobe signal and multiple data bit signals from a transmitting component. The receiving component includes a forward strobe clock recovery circuit configurable to align a forward strobe sampling clock so as to improve sampling accuracy. The receiving component further includes at least one data bit clock recovery circuit configurable to align a data bit sampling clock so as to improve sampling accuracy, and to receive a signal from the forward strobe clock recovery circuit that causes the data bit sampling clock to track the forward strobe sampling clock during system operation.



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BIT-DESKEWING IO METHOD AND SYSTEM

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TECHNICAL FIELD

The invention is in the field of data transfer in computer and other digital systems.

BACKGROUND

25

As computer and other digital systems become more complex and more capable, methods and hardware to enhance the transfer of data between system components or elements typical continually evolve. Data to be transferred include signals representing data, commands, or any other signals. System components or elements can include different functional hardware blocks on a single integrated circuit (IC), or on different ICs. The different ICs may or may not be on the same printed circuit board (PCB). System components typically include an input/output (I/O) interface specifically designed to receive data from other system components and to transmit data to other system components. Generally speaking, existing I/O interfaces can be categorized into serial and parallel “links”. Regardless of the type of I/O interface, transferred data must be synchronized between system components for proper operation. Synchronization includes accounting for or compensating for several phenomena that potentially cause errors, including signal jitter and signal skew. The phenomena include differences between component clocks, and physical attributes of the data paths that create noise and affect the integrity of the transferred

signal. Current approaches to handling serial I/O and parallel I/O interfaces deal with these data synchronization issues, but have limitations.

5 A typical serial link embeds clock information within the data stream and extracts the clock information at the receiver using a clock recovery scheme. Such schemes are also known as per-line closed-loop timing. Guaranteeing transition density requires encoding the data, typically using 8B/10B codes. A disadvantage of this approach is that it adds bandwidth overhead and increases complexity, which hurts performance and increases cost.

10 A typical parallel link sends a clock signal, or strobe, with a group of N data signals (for example, N may be 8 in a double data rate dynamic random access memory (DDR DRAM)). Depending on the data rate and the level of sophistication required, one of the following “source-synchronous timing” methods is used: the receiver simply samples the data with the strobe directly if the strobe has already been shifted by half a bit time relative to the data sent by the transmitter; or if the
15 strobe is aligned with the edge of the data sent by the transmitter, the receiver delays the strobe by the same fixed amount across the group of data to sample the data eye at the nominal center.

Each of the two parallel link approaches require very tight matching of the trace impedance and trace length across the group of data and the strobe to achieve
20 high data rates. To alleviate this, each bit receiver can delay the strobe by a different amount to place its own clock at the center of its own data. This is sometimes called per-bit de-skew. A disadvantage of this parallel scheme is that the strobe (which is usually sent across a circuit board and distributed to the group of data) is noisy, thus reducing the system timing budget. In addition, the receiver simply uses or delays
25 the strobe, which adds jitter rather than filtering jitter. In some implementations, a strobe is transmitted for each data bit rather than for a group of bits, which increases pin counts and cost.

BRIEF DESCRIPTION OF THE DRAWINGS

30 **Figure 1** is a block diagram of portions of a system including a receiver interface according to an embodiment.

Figure 2 is a flow diagram of a method performed by circuitry of Figure 1 according to an embodiment.

DETAILED DESCRIPTION

Embodiments of a bit-deskewing IO method and system are described herein. A method and system for bit-deskewing are described. In one embodiment, a system component receives a forward strobe signal and multiple data bit signals
5 from a transmitting component. The receiving component includes a forward strobe clock recovery circuit configurable to align a forward strobe sampling clock so as to improve sampling accuracy. The receiving component further includes at least one data bit clock recovery circuit configurable to align a data bit sampling clock so as to improve sampling accuracy, and to receive a signal from the forward strobe clock
10 recovery circuit that causes the data bit sampling clock to track the forward strobe sampling clock during system operation.

Embodiments achieve data rates similar to a serial link with per-line closed-loop timing, but without the typically associated complexity and encoding bandwidth overhead. In one embodiment these advantages are provided in an
15 interface that includes improved performance over existing source-synchronous parallel links, but does not include the complexity and overhead (e.g., as a result of encoding a clock in a serial data stream) associated with current serial links.

Figure 1 is a block diagram of portions of a system 100 according to an embodiment. System 100 includes a transmitter 104 and a receiver interface 102.
20 System 100 may be any computer system or sub-system thereof, digital system, component or combination of components that transmits data among components. The components may be blocks of circuitry on an integrated circuit, different integrated circuits on the same printed circuit board, or components that communicate via a network. In various embodiments, the components communicate
25 at high speeds and high data rates. For example, system 100 may be a computer system with graphics processing or video processing unit communicating with double data rate (DDR) DRAMs, but embodiments are not so limited.

Relevant portions of the transmitter 104 are shown, including latches or flip-flops 106(0) – 106(N-1) and associated output buffers. In one embodiment, the
30 transmitter 104 transmits a strobe signal, or forward clock (labeled DQS) that is associated with data bits DQ(0) – DQ(N-1). The data bits and the forward strobe are transmitted on transmission medium 107. Transmission medium 107 in various embodiments can be one or more of a cable, a PCB trace, or any other known transmission medium. The data bits DQ are transmitted according to the

communication taking place between the transmitter 104 and a receiving component that includes the receiver interface 102. The forward strobe DQS, in contrast, is continually transmitted as a toggling logic value (101010...) as shown. The transmitter 104 further includes a transmit phase lock loop (TxPLL) 108, which is a well known circuit. For example, PLLs are used as a control mechanism in most frequency synthesizers. TxPLL 108 operates in a known manner.

The receiver interface 102 includes a receive PLL (RxPLL) 110 that operates in a known manner. TxPLL 108 and RxPLL 110 both receive a reference clock signal, Ref Clk 109. The output of TxPLL 108 provides a clock signal for latches 106. The output of RxPLL 110 is input to a clock phase delay circuit 120 for each of the data bits DQ and for the forward strobe signal DQS, as described in more detail below.

The forward strobe signal DQS is received by a clock recovery circuit 112(S) of the receiver interface 102. Receiver interface 102 also includes a separate clock recovery circuit 113 for each of the data bits DQ (clock recovery circuit 113(0) for DQ(0), clock recovery circuit 113(1) for DQ(1), etc.).

In order to help ensure that received signals, including the strobe and the data signals, are correctly sampled by the receiver interface 102, the sampling clock signal is aligned so as to optimally sample the received signals. For example, in one embodiment, the sampling clock signal is aligned to sample close to the center of the received data valid window (also referred to as the data eye). This maximizes setup and hold times and reduces the probability of sampling error. The forward strobe signal and the data bits DQ are transmitted edge-aligned. One function of the clock recovery circuits 112 and 113 in the receiver interface 102 is to adjust the phase of the received RxPLL 110 output signal so that the sample point is close to the center of the data eye. In other embodiments, the phase of the received RxPLL 110 output signal may be adjusted or aligned according to other criteria in order to improve sampling accuracy appropriately to the design of the system embodiment.

Referring to clock recovery circuit 112(S), the forward strobe DQS is received by a phase detector 114. The phase detector 114 is a known circuit, such as a comparator for example, that compares the phase of the received signal to that of the sampling clock signal and determines whether it is early or late with respect to the sampling clock signal. As further explained below, the sampling clock signal is the output of the RxPLL 110 after its phase relationship to the received signal is

adjusted to be aligned with the center of the forward strobe DQS through the clock phase delay circuit 120. The output of the phase detector 114 is an early/late indication for each clock cycle. The early/late indications are input to a divider 116. The divider 116 is adjustable to reduce the number of detected early/late indications by some ratio. The output of the divider 116 is an adjusted number of early/late indications that are received by a phase counter 118. The number of early/late indications is adjusted because it may not be desirable to react to every early or late indication by adjusting the phase of the RxPLL 110 output. For example, adjusting the phase of the RxPLL 110 output in reaction to each early/late indication could cause clock dither. Therefore the early/late indications are divided by a number, for example 32, such that the phase of the RxPLL 110 output is moved for every 32 indications.

The output of the phase counter 118 is a signal DQSPC which is input to a clock phase delay circuit 120 that adjusts the delay of the RxPLL 110 output to place the RxPLL 110 output at the center of DQS. In one embodiment, the clock phase delay circuit 120 is a phase interpolator, but embodiments are not so limited. The clock phase delay circuit 120 outputs a recovered forward clock signal DQSrclk that is fed back to the phase detector circuit 114. In the present embodiments, DQSrclk will be adjusted until it is at the center of the received DQS signal to maximize the setup/hold time window. In this way the DQSrclk is compared to the received DQS signal for continual adjustment while the clock recovery circuit 112(S) is enabled or active.

According to an embodiment, the clock recovery circuit 112(S) is run in an initial "training" phase to train the circuit 112(S) in the appropriate number of delays required to center the recovered forward clock signal DQSrclk on the data eye of DQS (the received strobe signal). This number of delays is represented by the DQSPC signal. Once the clock recovery circuit 112(S) has been trained and a DQSPC signal has been obtained, the clock recovery circuit 112(S) is disabled by a DQS freeze signal input to the divider circuit 116. The DQS freeze signal has the affect of maintaining the DQSPC signal at a stable value.

The receiver interface 102 further includes data bit clock recovery circuits 113(0), 113(1), and so on, through 113(N-1) for each of the data bits DQ. In an embodiment, the data bit clock recovery circuits 113 are disabled during the training phase of the clock recovery circuit 112(S) by a common DQfreeze signal. After the

clock recovery circuit 112(S) is trained and disabled, the clock recovery circuits 113 are enabled for a data clock recovery circuit training phase. In the data clock recovery circuit training phase, each of the data clock recovery circuits 113 operates to detect any phase difference between the output of the RxPLL 110 and the data eye of the respective received data signal. In one embodiment, the phase adjustment established during the training phase of the strobe clock recovery circuit 112(S), as represented by the DQSPC signal, is added to a phase adjustment determined by each clock recovery circuit 113.

With reference to the clock recovery circuit 133(0), the data signal DQ(0) is received by a phase detector circuit 114. As explained with reference to the clock recovery circuit 112(S), the output of the phase detector circuit 114 is received by an adjustable divider circuit 116. The output of the divider circuit 116 is received by a phase counter 118, which outputs a signal DQPC(0) to an adder 122. The adder 122 also receives the DQSPC signal from the strobe clock recovery circuit 112(S), and adds the received signals to generate an input to a phase delay circuit 120. The DQPC signal is an intermediate clock offset that is added to the DQSPC clock offset to generate the data clock offset signal that is input to the clock phase delay circuit 120. The input from the adder 122 to the clock phase delay circuit 120 indicates an amount by which the RxPLL 110 output should be delayed. The output of the clock phase delay circuit 120 is a recovered clock signal for data bit DQ(0), or DQrclk(0).

Each of the data clock recovery circuits 113 goes through a similar training phase to arrive at a DQPC signal and a DQrclk signal. The training phases for the different clock recovery circuits 113 can occur simultaneously or at different times. When all of the data clock recovery circuits 113 are trained, they are all disabled with the DQfreeze signal. Disabling the data clock recovery circuits 113 prevents the DQPC signals of respective circuits 113 from changing.

During normal system operation, the strobe clock recovery circuit 112(S) is enabled once again and runs freely while the component containing the receiver interface 102 is operational. Thus, the circuit 112(S) will adjust DQSPC as required to keep the DQSrclk in the center of the received forward strobe (DQS). The data clock recovery circuits, on the other hand, remain disabled during normal system operation. Because each of the data clock recovery circuits receive DQSPC, however, the phase adjustment or offset of the signal that clocks each of the data bits (DQ(0) through DQ(N-1)) will be adjusted to track any DQSPC change. The data

thus “tracks” the forward strobe. That is, the data and the forward strobe move together because their respective sampling clocks move together. This is effective because the relationship of each data signal to the forward strobe (or the relationship between the respective sampling clocks of each data signal and the forward strobe) was established during the training phases and should not vary greatly, given that they each should see similar environment changes.

Figure 2 is a flow diagram illustrating a bit-deskewing method 200 that can be performed by the system of Figure 1 according to an embodiment. The system initializes at 202. As part of the initialization process, the forward strobe clock recovery circuit is enabled and the data clock recovery circuit is disabled as shown at 204. At 206, the forward strobe clock recovery circuit is allowed to run in order to establish DQSPC. As previously described, the DQSPC is established when the value of DQSPC is appropriate to cause a clock phase delay circuit to place the forward strobe sampling clock DQSrclk in the center of the received forward strobe data eye. In one embodiment, the forward strobe sampling clock DQSrclk is the delayed output of a transmit PLL, RxPLL, that receives a reference clock. In one embodiment, the forward strobe clock recovery circuit is run for a predetermined amount of time (for example, one millisecond) that has been determined to be sufficient to establish DQSPC. In other embodiments additional circuitry (not shown) determines when DQSPC is established.

When DQSPC has been established, the forward strobe clock recovery circuit is disabled and the data clock recovery circuits are enabled, as shown at 208. The data clock recovery circuits are run to establish respective DQPCs at 210. As previously described with reference to Figure 1, DQSPC is added to each DQPC phase counter output during this data clock recovery training phase.

When the DQPCs have been established, the forward strobe clock recovery circuit is enabled again and the data clock recovery circuits are disabled, as shown at 212. Normal system operation then proceeds at 214.

In various embodiments, clock recovery events during normal operation may cause one or more of the clock recovery circuits to complete another training phase during system operation. For example, in one embodiment, if one or more of the DQPC values have not changed for a predetermined number of clock cycles (for example one thousand cycles), the training processes starting at 208 are repeated. In another embodiment, the system components that contain the receiver interface

experience idle periods or power saving periods during which no “useful” work is done by the component. Idle periods are also clock recovery events in such embodiments. An example of such a component is a double data rate dynamic random access memory (DDR DRAM) for which a refresh cycle can be used as a
5 clock recovery event.

In various embodiments, the control of the described circuitry is performed by a high-level system protocol. Some of the behavior of the circuitry can be specified for a particular component such that a user of the component can tailor the behavior of the circuitry through the protocol. Examples of specified behavior are
10 values for the divider circuit, predetermined amounts of time for performing clock recovery circuit training, and which events, if any, are clock recovery events.

Embodiment of the bit-deskewing IO method and system disclosed herein include a system comprising: at least one component configurable to transmit a plurality of data bits and a forward strobe associated with the plurality of data bits; at
15 least one component configurable to receive the plurality of signals. In an embodiment, the at least one component configurable to receive comprises: a forward strobe clock recovery circuit configurable to align a forward strobe sampling clock so as to improve sampling accuracy; and at least one data bit clock recovery circuit configurable to align a data bit sampling clock so as to improve
20 sampling accuracy, and to receive a signal from the forward strobe clock recovery circuit that causes the data bit sampling clock to track the forward strobe sampling clock during operation of the at least one component configurable to receive.

In an embodiment, the signal received from the forward strobe clock recovery circuit comprises a forward strobe clock offset, and wherein the forward
25 strobe clock offset is combined with an intermediate data bit clock offset to generate a data bit clock offset.

In an embodiment, the data bit sampling clock is aligned by generating a data bit clock offset in a training phase during which the at least one data bit clock recovery circuit is active, and wherein the data bit clock offset includes an
30 intermediate data bit clock offset combined with the signal from the forward strobe clock recovery circuit, wherein the signal comprises a forward strobe clock offset.

In an embodiment, during operation of the at least one component configurable to receive, the at least one data bit clock recovery circuit is inactive, the

intermediate data bit clock offset is fixed, and the data bit clock offset varies with the forward strobe clock offset.

In an embodiment, the forward strobe clock recovery circuit aligns the forward strobe sampling clock during a forward strobe training phase, including
5 generating a forward strobe clock offset, and the at least one data bit clock recovery circuit aligns the data bit sampling clock during a data bit training phase in which the forward strobe clock recovery circuit is inactive, wherein the signal received from the forward strobe clock is the forward strobe offset, which is combined with an intermediate data clock offset to generate a data bit clock offset.

10 In an embodiment, the at least one data bit clock recovery circuit comprises a data bit clock recover circuit for each of the plurality of data bits.

In an embodiment, wherein the at least one data bit clock recovery circuit includes a phase detector that receives a respective data bit and a recovered data clock signal and outputs an early/late indication that represents a phase difference.

15 In an embodiment, the at least one data bit clock recovery circuit further includes a phase counter that receives the early/late indication and outputs an intermediate data bit clock offset.

In an embodiment, the early/late indication is divided by a predetermined number before it is received by the phase counter.

20 In an embodiment, the at least one data bit clock recovery circuit further includes an adder that adds the intermediate data bit clock offset to the signal received from the forward strobe clock recovery circuit, wherein the signal comprises a forward strobe clock offset.

In an embodiment, the at least one data bit clock recovery circuit further
25 includes a clock phase delay circuit that receives an output of the adder and generates the recovered data clock signal.

Embodiments further include a computer readable medium having instruction stored thereon which, when operated in a system, cause the system to implement a method of data transfer, the method comprising: training a forward
30 strobe clock recovery circuit to determine a forward strobe sampling clock offset to be used to improve sampling accuracy; and training at least one data bit clock recovery circuit to determine a data bit sampling clock offset to be used to improve sampling accuracy, wherein the data bit sampling clock offset includes the forward strobe sampling clock offset and an intermediate data bit sampling clock offset.

In an embodiment, the method implemented by the system further comprises enabling the forward strobe clock recovery circuit and disabling the data clock recovery circuit while training the forward strobe clock recovery circuit.

5 In an embodiment, the method implemented by the system further comprises disabling the forward strobe clock recovery circuit and enabling the data clock recovery circuit while training the data clock recovery circuit.

10 In an embodiment, the method implemented by the system further comprises enabling the forward strobe clock recovery circuit and disabling the data clock recovery circuit during system operation such that the data bit sampling clock offset tracks the forward strobe sampling clock offset.

In an embodiment, the method implemented by the system further comprises: detecting at least one clock recovery event during operation of the system; and repeating training at least one data bit clock recovery circuit.

15 In an embodiment, the at least one clock recovery event comprises: passage of a predetermined amount of time since a last training of the at least one data clock recovery circuit; an idle state of a system component that includes the at least one data clock recovery circuit; and a low power state of a system component that includes the at least one data clock recovery circuit.

20 Embodiments further include a method for transferring data in a system, the method comprising: training a forward strobe clock recovery circuit to determine a forward strobe sampling clock offset to be used to improve sampling accuracy; and training at least one data bit clock recovery circuit to determine a data bit sampling clock offset to be used to improve sampling accuracy, wherein the data bit sampling clock offset includes the forward strobe sampling clock offset and an intermediate
25 data bit sampling clock offset.

An embodiment includes enabling the forward strobe clock recovery circuit and disabling the data clock recovery circuit while training the forward strobe clock recovery circuit.

30 An embodiment includes disabling the forward strobe clock recovery circuit and enabling the data clock recovery circuit while training the data clock recovery circuit.

An embodiment includes enabling the forward strobe clock recovery circuit and disabling the data clock recovery circuit during system operation such that the data bit sampling clock offset tracks the forward strobe sampling clock offset.

An embodiment includes detecting at least one clock recovery event during operation of the system, and repeating training at least one data bit clock recovery circuit.

5 In an embodiment, the at least one clock recovery event comprises: passage of a predetermined amount of time since a last training of the at least one data clock recovery circuit; an idle state of a system component that includes the at least one data clock recovery circuit; and a low power state of the at least one data clock recovery circuit.

10 Embodiments further include an apparatus for transmitting data comprising: a strobe signal transmitter for transmitting a strobe signal on a transmission medium; and at least one data transmitter for transmitting at least one data signal on a transmission medium, wherein a receiver strobe sampling clock is aligned for sampling the strobe signal, and wherein at least one receiver data sampling clock is aligned to track the aligned receiver strobe sampling clock.

15 In an embodiment, the strobe signal is continually transmitted on the transmission medium.

In an embodiment, the continually transmitted strobe signal is toggled between a logical high value and a logical low value.

20 Embodiments further include a method of transmitting data comprising: transmitting a strobe signal on a transmission medium; and transmitting at least one data signal on a transmission medium, wherein a strobe sampling clock that samples the transmitted strobe signal is adjusted by an adjustment value that is used to align the strobe sampling clock, and wherein the adjustment value is further used to align at least one data sampling clock that samples the at least one data signal.

25 In an embodiment, transmitting the strobe signal comprises continually transmitting the strobe signal on the transmission medium.

In an embodiment, continually transmitting the strobe signal comprises toggling the continually transmitted strobe signal between a logical high value and a logical low value.

30 Embodiments further include a receiver for receiving data comprising: a forward strobe clock recovery circuit configurable to align a forward strobe sampling clock; and at least one data bit clock recovery circuit configurable to align a data bit sampling clock and to receive a signal from the forward strobe clock

recovery circuit, the at least one data bit recovery circuit configuring the data bit sampling clock to track the forward strobe sampling clock during operation.

In an embodiment, the signal received from the forward strobe clock recovery circuit comprises a forward strobe clock offset, and wherein the forward
5 strobe clock offset is combined with an intermediate data bit clock offset to generate a data bit clock offset.

In an embodiment, the data bit sampling clock is aligned by generating a data bit clock offset in a training phase during which the at least one data bit clock
10 recovery circuit is active, and wherein the data bit clock offset includes an intermediate data bit clock offset combined with the signal from the forward strobe clock recovery circuit, wherein the signal comprises a forward strobe clock offset.

In an embodiment, during operation of the at least one component configurable to receive, the at least one data bit clock recovery circuit is inactive, the intermediate data bit clock offset is fixed, and the data bit clock offset varies with
15 the forward strobe clock offset.

In an embodiment, the forward strobe clock recovery circuit aligns the forward strobe sampling clock during a forward strobe training phase, including generating a forward strobe clock offset, and the at least one data bit clock recovery circuit aligns the data bit sampling clock during a data bit training phase in which
20 the forward strobe clock recovery circuit is inactive, wherein the signal received from the forward strobe clock is the forward strobe offset, which is combined with an intermediate data clock offset to generate a data bit clock offset.

In an embodiment, the at least one data bit clock recovery circuit comprises a data bit clock recover circuit for each of the plurality of data bits.

25 In an embodiment, the at least one data bit clock recovery circuit includes a phase detector that receives a respective data bit and a recovered data clock signal and outputs an early/late indication that represents a phase difference.

In an embodiment, the at least one data bit clock recovery circuit further includes a phase counter that receives the early/late indication outputs an
30 intermediate data bit clock offset.

In an embodiment, the early/late indication is divided by a predetermined number before it is received by the phase counter.

In an embodiment, the at least one data bit clock recovery circuit further includes an adder that adds the intermediate data bit clock offset to the signal

received from the forward strobe clock recovery circuit, wherein the signal comprises a forward strobe clock offset.

In an embodiment, the at least one data bit clock recovery circuit further includes a clock phase delay circuit that received an output of the adder and
5 generates the recovered data clock signal.

Embodiments further include a method for receiving data comprising: responsive to receiving a forward strobe, a forward strobe clock recovery circuit aligning a forward strobe sampling clock; and aligning a data bit sampling clock to track the forward strobe sampling clock during operation.

10 In an embodiment, the signal received from the forward strobe clock recovery circuit comprises a forward strobe clock offset, and wherein the forward strobe clock offset is combined with an intermediate data bit clock offset to generate a data bit clock offset.

In an embodiment, the data bit sampling clock is aligned by generating a data
15 bit clock offset in a training phase during which the at least one data bit clock recovery circuit is active, and wherein the data bit clock offset includes an intermediate data bit clock offset combined with the signal from the forward strobe clock recovery circuit, wherein the signal comprises a forward strobe clock offset.

In an embodiment, during operation of the at least one component
20 configurable to receive, the at least one data bit clock recovery circuit is inactive, the intermediate data bit clock offset is fixed, and the data bit clock offset varies with the forward strobe clock offset.

In an embodiment, the forward strobe clock recovery circuit aligns the forward strobe sampling clock during a forward strobe training phase, including
25 generating a forward strobe clock offset, and the at least one data bit clock recovery circuit aligns the data bit sampling clock during a data bit training phase in which the forward strobe clock recovery circuit is inactive, wherein the signal received from the forward strobe clock is the forward strobe offset, which is combined with an intermediate data clock offset to generate a data bit clock offset.

30 In an embodiment, the at least one data bit clock recovery circuit comprises a data bit clock recover circuit for each of the plurality of data bits.

In an embodiment, the at least one data bit clock recovery circuit includes a phase detector that receives a respective data bit and a recovered data clock signal and outputs an early/late indication that represents a phase difference.

In an embodiment, the at least one data bit clock recovery circuit further includes a phase counter that receives the early/late indication outputs an intermediate data bit clock offset.

5 In an embodiment, the early/late indication is divided by a predetermined number before it is received by the phase counter.

In an embodiment, the at least one data bit clock recovery circuit further includes an adder that adds the intermediate data bit clock offset to the signal received from the forward strobe clock recovery circuit, wherein the signal comprises a forward strobe clock offset.

10 In an embodiment, the at least one data bit clock recovery circuit further includes a clock phase delay circuit that received an output of the adder and generates the recovered data clock signal.

Aspects of the invention described above may be implemented as functionality programmed into any of a variety of circuitry, including but not limited to programmable logic devices (PLDs), such as field programmable gate arrays (FPGAs), programmable array logic (PAL) devices, electrically programmable logic and memory devices and standard cell-based devices, as well as application specific integrated circuits (ASICs) and fully custom integrated circuits. Some other possibilities for implementing aspects of the invention include: microcontrollers with memory (such as electronically erasable programmable read only memory (EEPROM)), embedded microprocessors, firmware, software, etc. Furthermore, aspects of the invention may be embodied in microprocessors having software-based circuit emulation, discrete logic (sequential and combinatorial), custom devices, fuzzy (neural) logic, quantum devices, and hybrids of any of the above device types. Of course the underlying device technologies may be provided in a variety of component types, e.g., metal-oxide semiconductor field-effect transistor (MOSFET) technologies like complementary metal-oxide semiconductor (CMOS), bipolar technologies like emitter-coupled logic (ECL), polymer technologies (e.g., silicon-conjugated polymer and metal-conjugated polymer-metal structures), mixed analog and digital, etc.

Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in a sense of “including, but not limited to.” Words using the singular or plural number

also include the plural or singular number respectively. Additionally, the words “herein,” “hereunder,” “above,” “below,” and words of similar import, when used in this application, refer to this application as a whole and not to any particular portions of this application. When the word “or” is used in reference to a list of two or more
5 items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

The above description of illustrated embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed.
10 While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. The teachings of the invention provided herein can be applied to other systems, not only for the system including graphics processing or video processing or DDR DRAMs
15 as described above. The various operations described may be performed in a very wide variety of architectures and distributed differently than described. In addition, though many configurations are described herein, none are intended to be limiting or exclusive.

In other embodiments, some or all of the hardware and software capability
20 described herein may exist in a printer, a camera, television, handheld device, mobile telephone or some other device. The elements and acts of the various embodiments described above can be combined to provide further embodiments. These and other changes can be made to the invention in light of the above detailed description.

25 In general, in the following claims, the terms used should not be construed to limit the video processing method and system to the specific embodiments disclosed in the specification and the claims, but should be construed to include any processing systems that operate under the claims to provide video processing. Accordingly, the method and system is not limited by the disclosure, but instead the
30 scope of the method and system for bit-deskewing is to be determined entirely by the claims.

While certain aspects of the method and apparatus for video processing are presented below in certain claim forms, the inventors contemplate the various aspects of the method and apparatus in any number of claim forms. For example,

while only one aspect of the method and apparatus may be recited as embodied in computer-readable medium, other aspects may likewise be embodied in computer-readable medium. Accordingly, the inventors reserve the right to add additional claims after filing the application to pursue such additional claim forms for other
5 aspects of the method and apparatus for bit-deskewing.

CLAIMS

What is claimed is:

1 1. A system, comprising:
2 at least one component configurable to transmit a plurality of data bits and a
3 forward strobe associated with the plurality of data bits;
4 at least one component configurable to receive the plurality of signals,
5 wherein the at least one component configurable to receive comprises,
6 a forward strobe clock recovery circuit configurable to align a
7 forward strobe sampling clock so as to improve sampling accuracy; and
8 at least one data bit clock recovery circuit configurable to align a data
9 bit sampling clock so as to improve sampling accuracy, and to receive a signal from
10 the forward strobe clock recovery circuit that causes the data bit sampling clock to
11 track the forward strobe sampling clock during operation of the at least one
12 component configurable to receive.
13

1 2. The system of claim 1, wherein the signal received from the forward
2 strobe clock recovery circuit comprises a forward strobe clock offset, and wherein
3 the forward strobe clock offset is combined with an intermediate data bit clock offset
4 to generate a data bit clock offset.

1 3. The system of claim 1, wherein the data bit sampling clock is aligned
2 by generating a data bit clock offset in a training phase during which the at least one
3 data bit clock recovery circuit is active, and wherein the data bit clock offset
4 includes an intermediate data bit clock offset combined with the signal from the
5 forward strobe clock recovery circuit, wherein the signal comprises a forward strobe
6 clock offset.

1 4. The system of claim 3, wherein during operation of the at least one
2 component configurable to receive, the at least one data bit clock recovery circuit is
3 inactive, the intermediate data bit clock offset is fixed, and the data bit clock offset
4 varies with the forward strobe clock offset.

1 5. The system of claim 1, wherein:
2 the forward strobe clock recovery circuit aligns the forward strobe sampling
3 clock during a forward strobe training phase, including generating a forward strobe
4 clock offset; and
5 the at least one data bit clock recovery circuit aligns the data bit sampling
6 clock during a data bit training phase in which the forward strobe clock recovery
7 circuit is inactive, wherein the signal received from the forward strobe clock is the
8 forward strobe offset, which is combined with an intermediate data clock offset to
9 generate a data bit clock offset.

1 6. The system of claim 1, wherein the at least one data bit clock
2 recovery circuit comprises a data bit clock recover circuit for each of the plurality of
3 data bits.

1 7. The system of claim 6, wherein the at least one data bit clock
2 recovery circuit includes a phase detector that receives a respective data bit and a
3 recovered data clock signal and outputs an early/late indication that represents a
4 phase difference.

1 8. The system of claim 7, wherein the at least one data bit clock
2 recovery circuit further includes a phase counter that receives the early/late
3 indication outputs an intermediate data bit clock offset.

1 9. The system of claim 8, wherein the early/late indication is divided by
2 a predetermined number before it is received by the phase counter.

1 10. The system of claim 8, wherein the at least one data bit clock
2 recovery circuit further includes an adder that adds the intermediate data bit clock
3 offset to the signal received from the forward strobe clock recovery circuit, wherein
4 the signal comprises a forward strobe clock offset.

1 11. The system of claim 10, wherein the at least one data bit clock
2 recovery circuit further includes a clock phase delay circuit that received an output
3 of the adder and generates the recovered data clock signal.

1 12. A computer readable medium having instruction stored thereon
2 which, when operated in a system, cause the system to implement a method of data
3 transfer, the method comprising:
4 training a forward strobe clock recovery circuit to determine a forward strobe
5 sampling clock offset to be used to improve sampling accuracy; and
6 training at least one data bit clock recovery circuit to determine a data bit
7 sampling clock offset to be used to improve sampling accuracy, wherein the data bit
8 sampling clock offset includes the forward strobe sampling clock offset and an
9 intermediate data bit sampling clock offset.

1 13. The medium of claim 12, wherein the method implemented by the
2 system further comprises enabling the forward strobe clock recovery circuit and
3 disabling the data clock recovery circuit while training the forward strobe clock
4 recovery circuit.

1 14. The medium of claim 12, wherein the method implemented by the
2 system further comprises disabling the forward strobe clock recovery circuit and
3 enabling the data clock recovery circuit while training the data clock recovery
4 circuit.

1 15. The medium of claim 12, wherein the method implemented by the
2 system further comprises enabling the forward strobe clock recovery circuit and
3 disabling the data clock recovery circuit during system operation such that the data
4 bit sampling clock offset tracks the forward strobe sampling clock offset.

1 16. The medium of claim 12, wherein the method implemented by the
2 system further comprises:
3 detecting at least one clock recovery event during operation of the system;
4 and
5 repeating training at least one data bit clock recovery circuit.

1 17. The medium of claim 16, wherein the at least one clock recovery
2 event comprises:

3 passage of a predetermined amount of time since a last training of the at least
4 one data clock recovery circuit;
5 an idle state of a system component that includes the at least one data clock
6 recovery circuit; and
7 a low power state of a system component that includes the at least one data
8 clock recovery circuit.

1 18. A method for transferring data in a system, the method comprising:
2 training a forward strobe clock recovery circuit to determine a forward strobe
3 sampling clock offset to be used to improve sampling accuracy; and
4 training at least one data bit clock recovery circuit to determine a data bit
5 sampling clock offset to be used to improve sampling accuracy, wherein the data bit
6 sampling clock offset includes the forward strobe sampling clock offset and an
7 intermediate data bit sampling clock offset.

1 19. The method of claim 18, further comprising enabling the forward
2 strobe clock recovery circuit and disabling the data clock recovery circuit while
3 training the forward strobe clock recovery circuit.

1 20. The method of claim 18, further comprising disabling the forward
2 strobe clock recovery circuit and enabling the data clock recovery circuit while
3 training the data clock recovery circuit.

1 21. The method of claim 18, further comprising enabling the forward
2 strobe clock recovery circuit and disabling the data clock recovery circuit during
3 system operation such that the data bit sampling clock offset tracks the forward
4 strobe sampling clock offset.

1 22. The method of claim 18, further comprising:
2 detecting at least one clock recovery event during operation of the system;
3 and
4 repeating training at least one data bit clock recovery circuit.

1 23. The method of claim 22, wherein the at least one clock recovery
2 event comprises:
3 passage of a predetermined amount of time since a last training of the at least
4 one data clock recovery circuit;
5 an idle state of a system component that includes the at least one data clock
6 recovery circuit; and
7 a low power state of the at least one data clock recovery circuit.

1 24. An apparatus for transmitting data comprising:
2 a strobe signal transmitter for transmitting a strobe signal on a
3 transmission medium; and
4 at least one data transmitter for transmitting at least one data signal on a
5 transmission medium, wherein a receiver strobe sampling clock is aligned for
6 sampling the strobe signal, and wherein at least one receiver data sampling clock is
7 aligned to track the aligned receiver strobe sampling clock.

1 25. The apparatus of claim 24 wherein the strobe signal is continually
2 transmitted on the transmission medium.

1 26. The apparatus of claim 25 wherein the continually transmitted strobe
2 signal is toggled between a logical high value and a logical low value.

1 27. A method of transmitting data comprising:
2 transmitting a strobe signal on a transmission medium; and
3 transmitting at least one data signal on a transmission medium, wherein a
4 strobe sampling clock that samples the transmitted strobe signal is adjusted by an
5 adjustment value that is used to align the strobe sampling clock, and wherein the
6 adjustment value is further used to align at least one data sampling clock that
7 samples the at least one data signal.

1 28. The method of claim 27 wherein transmitting the strobe signal
2 comprises continually transmitting the strobe signal on the transmission medium.

1 29. The method of claim 28, wherein continually transmitting the strobe
2 signal comprises toggling the continually transmitted strobe signal between a logical
3 high value and a logical low value.

1 30. A receiver for receiving data comprising:
2 a forward strobe clock recovery circuit configurable to align a forward strobe
3 sampling clock; and
4 at least one data bit clock recovery circuit configurable to align a data bit
5 sampling clock and to receive a signal from the forward strobe clock recovery
6 circuit, the at least one data bit recovery circuit configuring the data bit sampling
7 clock to track the forward strobe sampling clock during operation.

1 31. The receiver of claim 30 wherein the signal received from the
2 forward strobe clock recovery circuit comprises a forward strobe clock offset, and
3 wherein the forward strobe clock offset is combined with an intermediate data bit
4 clock offset to generate a data bit clock offset.

1 32. The receiver of claim 30, wherein the data bit sampling clock is
2 aligned by generating a data bit clock offset in a training phase during which the at
3 least one data bit clock recovery circuit is active, and wherein the data bit clock
4 offset includes an intermediate data bit clock offset combined with the signal from
5 the forward strobe clock recovery circuit, wherein the signal comprises a forward
6 strobe clock offset.

1 33. The receiver of claim 32, wherein during operation of the at least one
2 component configurable to receive, the at least one data bit clock recovery circuit is
3 inactive, the intermediate data bit clock offset is fixed, and the data bit clock offset
4 varies with the forward strobe clock offset.

1 34. The receiver of claim 30, wherein:
2 the forward strobe clock recovery circuit aligns the forward strobe sampling
3 clock during a forward strobe training phase, including generating a forward strobe
4 clock offset; and

5 the at least one data bit clock recovery circuit aligns the data bit sampling
6 clock during a data bit training phase in which the forward strobe clock recovery
7 circuit is inactive, wherein the signal received from the forward strobe clock is the
8 forward strobe offset, which is combined with an intermediate data clock offset to
9 generate a data bit clock offset.

1 35. The receiver of claim 30, wherein the at least one data bit clock
2 recovery circuit comprises a data bit clock recover circuit for each of the plurality of
3 data bits.

1 36. The receiver of claim 35, wherein the at least one data bit clock
2 recovery circuit includes a phase detector that receives a respective data bit and a
3 recovered data clock signal and outputs an early/late indication that represents a
4 phase difference.

1 37. The receiver of claim 36, wherein the at least one data bit clock
2 recovery circuit further includes a phase counter that receives the early/late
3 indication outputs an intermediate data bit clock offset.

1 38. The receiver of claim 37, wherein the early/late indication is divided
2 by a predetermined number before it is received by the phase counter.

1 39. The receiver of claim 37, wherein the at least one data bit clock
2 recovery circuit further includes an adder that adds the intermediate data bit clock
3 offset to the signal received from the forward strobe clock recovery circuit, wherein
4 the signal comprises a forward strobe clock offset.

1 40. The receiver of claim 39, wherein the at least one data bit clock
2 recovery circuit further includes a clock phase delay circuit that received an output
3 of the adder and generates the recovered data clock signal.

1 41. A method for receiving data comprising:
2 responsive to receiving a forward strobe, a forward strobe clock recovery
3 circuit aligning a forward strobe sampling clock; and

4 aligning a data bit sampling clock to track the forward strobe sampling clock
5 during operation.

1 42. The method of claim 41 wherein the signal received from the forward
2 strobe clock recovery circuit comprises a forward strobe clock offset, and wherein
3 the forward strobe clock offset is combined with an intermediate data bit clock offset
4 to generate a data bit clock offset.

1 43. The method of claim 41, wherein the data bit sampling clock is
2 aligned by generating a data bit clock offset in a training phase during which the at
3 least one data bit clock recovery circuit is active, and wherein the data bit clock
4 offset includes an intermediate data bit clock offset combined with the signal from
5 the forward strobe clock recovery circuit, wherein the signal comprises a forward
6 strobe clock offset.

1 44. The method of claim 43, wherein during operation of the at least one
2 component configurable to receive, the at least one data bit clock recovery circuit is
3 inactive, the intermediate data bit clock offset is fixed, and the data bit clock offset
4 varies with the forward strobe clock offset.

1 45. The method of claim 41, wherein:
2 the forward strobe clock recovery circuit aligns the forward strobe sampling
3 clock during a forward strobe training phase, including generating a forward strobe
4 clock offset; and
5 the at least one data bit clock recovery circuit aligns the data bit sampling
6 clock during a data bit training phase in which the forward strobe clock recovery
7 circuit is inactive, wherein the signal received from the forward strobe clock is the
8 forward strobe offset, which is combined with an intermediate data clock offset to
9 generate a data bit clock offset.

1 46. The method of claim 41, wherein the at least one data bit clock
2 recovery circuit comprises a data bit clock recover circuit for each of the plurality of
3 data bits.

1 47. The method of claim 46, wherein the at least one data bit clock
2 recovery circuit includes a phase detector that receives a respective data bit and a
3 recovered data clock signal and outputs an early/late indication that represents a
4 phase difference.

1 48. The method of claim 47, wherein the at least one data bit clock
2 recovery circuit further includes a phase counter that receives the early/late
3 indication outputs an intermediate data bit clock offset.

1 49. The method of claim 48, wherein the early/late indication is divided
2 by a predetermined number before it is received by the phase counter.

1 50. The method of claim 48, wherein the at least one data bit clock
2 recovery circuit further includes an adder that adds the intermediate data bit clock
3 offset to the signal received from the forward strobe clock recovery circuit, wherein
4 the signal comprises a forward strobe clock offset.

1 51. The method of claim 50, wherein the at least one data bit clock
2 recovery circuit further includes a clock phase delay circuit that received an output
3 of the adder and generates the recovered data clock signal.

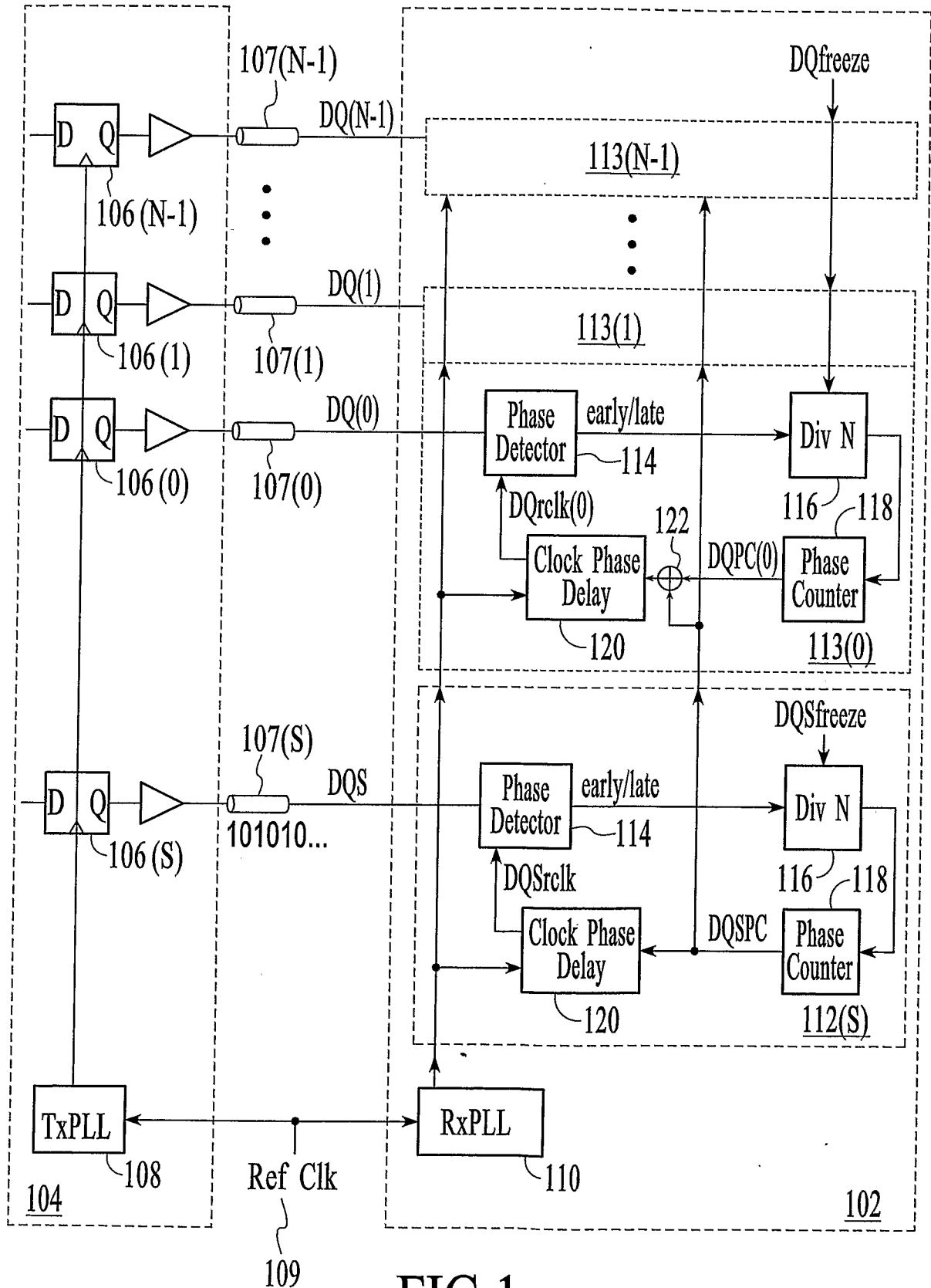


FIG.1

SHEET 2/2

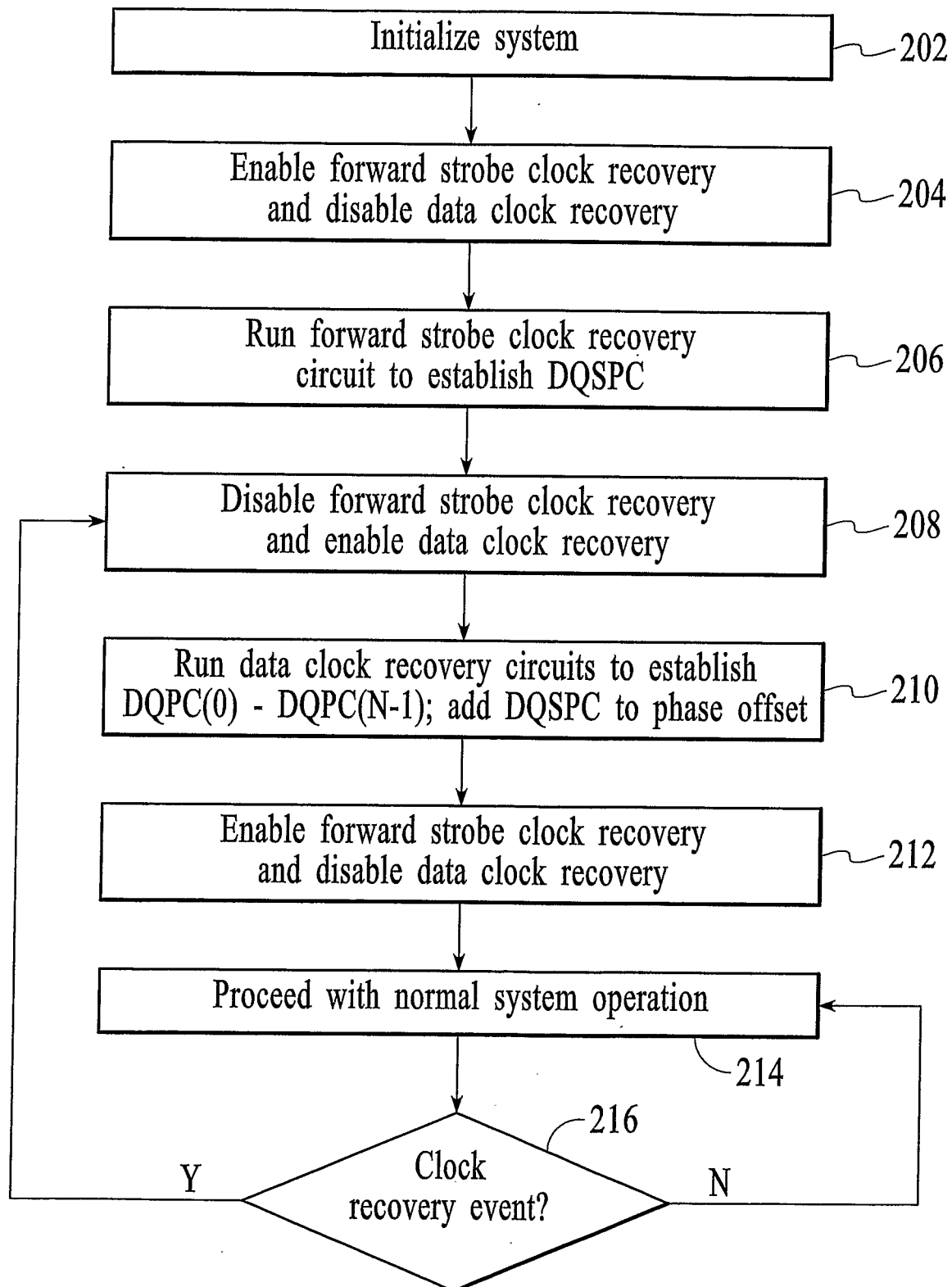


FIG.2

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/028092

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04L7/033
ADD. H03L7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2004/213067 A1 (BEST SCOTT C [US] ET AL) 28 October 2004 (2004-10-28) abstract figures 1,3-7,9 page 1, paragraph 3 page 1, paragraph 5 page 2, paragraph 17 page 2, paragraph 19 page 3, paragraph 28 - page 4, paragraph 34 page 4, paragraph 37 page 5, paragraph 48 page 6, paragraph 62 page 7, paragraph 63	1,2, 6-12, 16-18, 22-51 3-5, 13-15, 19-21



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

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Information on patent family members

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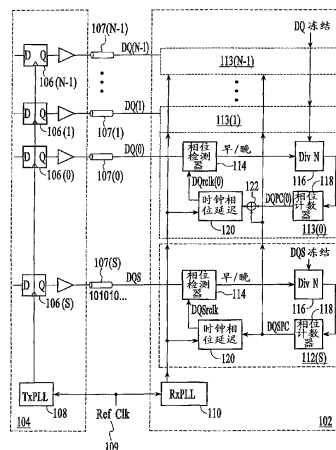
权利要求书 7 页 说明书 13 页 附图 2 页

[54] 发明名称

位去偏斜 IO 方法和系统

[57] 摘要

描述了一种用于位去偏斜的 IO 方法和系统。实施例包括具有多个部件的计算机系统，所述多个部件在相互之间传输数据。 在一个实施例中，系统部件从发送部件接收前向选通脉冲信号和多个数据位信号。 接收部件包括前向选通脉冲时钟恢复电路，该前向选通脉冲时钟恢复电路可配置用于对齐前向选通脉冲采样时钟以提高采样精确度。 接收部件还包括至少一个数据位时钟恢复电路，该至少一个数据位时钟恢复电路可配置用于对齐数据位采样时钟以提高采样精确度，以及从前向选通脉冲时钟恢复电路接收信号，其在系统运行期间使得数据位采样时钟跟踪前向选通脉冲采样时钟。



1. 一种系统, 包括:

至少一个可配置用于发送多个数据位和与所述多个数据位相关联的前向选通脉冲的部件;

至少一个可配置用于接收所述多个信号的部件, 其中所述至少一个可配置用于接收的部件包括:

前向选通脉冲时钟恢复电路, 可配置用于对齐前向选通脉冲采样时钟以提高采样精确度; 以及

至少一个数据位时钟恢复电路, 可配置用于对齐数据位采样时钟以提高采样精确度, 以及在所述至少一个可配置用于接收的部件的运行期间从所述前向选通脉冲时钟恢复电路接收信号, 其使得所述数据位采样时钟跟踪所述前向选通脉冲采样时钟。

2. 权利要求 1 所述的系统, 其中从所述前向选通脉冲时钟恢复电路接收的所述信号包括前向选通脉冲时钟偏移, 并且其中所述前向选通脉冲时钟偏移与中间数据位时钟偏移相结合以产生数据位时钟偏移。

3. 权利要求 1 所述的系统, 其中在训练阶段, 所述数据位采样时钟通过产生数据位时钟偏移来对齐, 所述至少一个数据位时钟恢复电路在所述训练阶段是激活的, 并且其中所述数据位时钟偏移包括与来自所述前向选通脉冲时钟恢复电路的所述信号相结合的中间数据位时钟偏移, 其中所述信号包括前向选通脉冲时钟偏移。

4. 权利要求 3 所述的系统, 其中在所述至少一个可配置用于接收的部件的运行期间, 所述至少一个数据位时钟恢复电路是非激活的, 所述中间数据位时钟偏移是固定的, 并且所述数据位时钟偏移随所述前向选通脉冲时钟偏移而变化。

5. 权利要求 1 所述的系统, 其中:

在前向选通脉冲训练阶段, 所述前向选通脉冲时钟恢复电路对齐所述前向选通脉冲采样时钟, 包括产生前向选通脉冲时钟偏移; 以及

在数据位训练阶段, 所述至少一个数据位时钟恢复电路对齐所述数据位采样时钟, 所述前向选通脉冲时钟恢复电路在所述数据位训练阶段是非激活的, 其中从所述前向选通脉冲时钟接收的所述信号是所述前向选通脉冲偏移, 其与中间数据时钟偏移相结合以产生数据位时钟偏移。

6. 权利要求 1 所述的系统, 其中针对所述多个数据位中的每一个, 所述至少一个数据位时钟恢复电路包括数据位时钟恢复电路。

7. 权利要求 6 所述的系统, 其中所述至少一个数据位时钟恢复电路包括相位检测器, 所述相位检测器接收相应的数据位和经恢复的数据时钟信号并且输出表示相位差的早/晚指示。

8. 权利要求 7 所述的系统, 其中所述至少一个数据位时钟恢复电路还包括相位计数器, 所述相位计数器接收所述早/晚指示, 输出中间数据位时钟偏移。

9. 权利要求 8 所述的系统, 其中所述早/晚指示在由所述相位计数器接收前被除以预定的数。

10. 权利要求 8 所述的系统, 其中所述至少一个数据位时钟恢复电路还包括加法器, 所述加法器将所述中间数据位时钟偏移加到从所述前向选通脉冲时钟恢复电路接收的所述信号上, 其中所述信号包括前向选通脉冲时钟偏移。

11. 权利要求 10 所述的系统, 其中所述至少一个数据位时钟恢复电路还包括时钟相位延迟电路, 所述时钟相位延迟电路接收所述加法器的输出并且产生所述经恢复的数据时钟信号。

12. 一种计算机可读介质, 其上存储有指令, 当在系统中运行时, 其使得所述系统实施一种数据传输的方法, 所述方法包括:

训练前向选通脉冲时钟恢复电路以确定用于提高采样精确度的前向选通脉冲采样时钟偏移; 以及

训练至少一个数据位时钟恢复电路以确定用于提高采样精确度的数据位采样时钟偏移, 其中所述数据位采样时钟偏移包括所述前向选通脉冲采样时钟偏移和中间数据位采样时钟偏移。

13. 权利要求 12 所述的介质, 其中由所述系统实施的所述方法还包括: 当训练所述前向选通脉冲时钟恢复电路时, 使能所述前向选通脉冲时钟恢复电路并且禁止所述数据时钟恢复电路。

14. 权利要求 12 所述的介质, 其中由所述系统实施的所述方法还包括: 当训练所述数据时钟恢复电路时, 禁止所述前向选通脉冲时钟恢复电路并且使能所述数据时钟恢复电路。

15. 权利要求 12 所述的介质, 其中由所述系统实施的所述方法还包

括：在系统运行期间，使能所述前向选通脉冲时钟恢复电路并且禁止所述数据时钟恢复电路，使得所述数据位采样时钟偏移跟踪所述前向选通脉冲采样时钟偏移。

16. 权利要求 12 所述的介质，其中由所述系统实施的所述方法还包括：

在所述系统的运行期间检测至少一个时钟恢复事件；以及
重复训练至少一个数据位时钟恢复电路。

17. 权利要求 16 所述的介质，其中所述至少一个时钟恢复事件包括：
自所述至少一个数据时钟恢复电路的上一次训练起经过了预定量的时间；

包括所述至少一个数据时钟恢复电路的系统部件的空闲状态；以及
包括所述至少一个数据时钟恢复电路的系统部件的低功率状态。

18. 一种在系统中传输数据的方法，所述方法包括：

训练前向选通脉冲时钟恢复电路以确定用于提高采样精确度的前向选通脉冲时钟偏移；

训练至少一个数据位时钟恢复电路以确定用于提高采样精确度的数据位采样时钟偏移，其中所述数据位采样时钟偏移包括所述前向选通脉冲采样时钟偏移和中间数据位采样时钟偏移。

19. 权利要求 18 所述的方法，还包括：当训练所述前向选通脉冲时钟恢复电路时，使能所述前向选通脉冲时钟恢复电路并且禁止所述数据时钟恢复电路。

20. 权利要求 18 所述的方法，还包括：当训练所述数据时钟恢复电路时，禁止所述前向选通脉冲时钟恢复电路并且使能所述数据时钟恢复电路。

21. 权利要求 18 所述的方法，还包括：在系统运行期间，使能所述前向选通脉冲时钟恢复电路并且禁止所述数据时钟恢复电路，使得所述数据位采样时钟偏移跟踪所述前向选通脉冲采样时钟偏移。

22. 权利要求 18 所述的方法，还包括：

在所述系统的运行期间检测至少一个时钟恢复事件；以及
重复训练至少一个数据位时钟恢复电路。

23. 权利要求 22 所述的方法, 其中所述至少一个时钟恢复事件包括:

自所述至少一个数据时钟恢复电路的上一次训练起经过了预定量的时间;

包括所述至少一个数据时钟恢复电路的系统部件的空闲状态; 以及
所述至少一个数据时钟恢复电路的低功率状态。

24. 一种用于发送数据的装置, 包括:

选通脉冲信号发送器, 用于在传输介质上发送选通脉冲信号; 以及

至少一个数据发送器, 用于在传输介质上发送至少一个数据信号, 其中接收器选通脉冲采样时钟被对齐以便采样所述选通脉冲信号, 并且其中至少一个接收器数据采样时钟被对齐以便跟踪所述对齐的接收器选通脉冲采样时钟。

25. 权利要求 24 所述的装置, 其中所述选通脉冲信号在所述传输介质上连续地被发送。

26. 权利要求 25 所述的装置, 其中所述连续地被发送的选通脉冲信号在逻辑高值和逻辑低值之间转换。

27. 一种发送数据的方法, 包括:

在传输介质上发送选通脉冲信号; 以及

在传输介质上发送至少一个数据信号, 其中采样所发送的选通脉冲信号的选通脉冲采样时钟被调节一个用来对齐所述选通脉冲采样时钟的调节值, 并且其中所述调节值还用来对齐对所述至少一个数据信号进行采样的至少一个数据采样时钟。

28. 权利要求 27 所述的方法, 其中发送所述选通脉冲信号包括在所述传输介质上连续地发送所述选通脉冲信号。

29. 权利要求 28 所述的方法, 其中连续地发送所述选通脉冲信号包括使所述连续地被发送的选通脉冲信号在逻辑高值和逻辑低值之间转换。

30. 一种用于接收数据的接收器, 包括:

前向选通脉冲时钟恢复电路, 可配置用于对齐前向选通脉冲采样时钟; 以及

至少一个数据位时钟恢复电路, 可配置用于对齐数据位采样时钟以及从所述前向选通脉冲时钟恢复电路接收信号, 所述至少一个数据位恢复电

路将所述数据位采样时钟配置成在运行期间跟踪所述前向选通脉冲采样时钟。

31. 权利要求 30 所述的接收器，其中从所述前向选通脉冲时钟恢复电路接收的所述信号包括前向选通脉冲时钟偏移，并且其中所述前向选通脉冲时钟偏移与中间数据位时钟偏移相结合以产生数据位时钟偏移。

32. 权利要求 30 所述的接收器，其中在训练阶段，所述数据位采样时钟通过产生数据位时钟偏移来对齐，所述至少一个数据位时钟恢复电路在所述训练阶段是激活的，并且其中所述数据位时钟偏移包括与来自所述前向选通脉冲时钟恢复电路的所述信号相结合的中间数据位时钟偏移，其中所述信号包括前向选通脉冲时钟偏移。

33. 权利要求 32 所述的接收器，其中在所述至少一个可配置用于接收的部件的运行期间，所述至少一个数据位时钟恢复电路是非激活的，所述中间数据位时钟偏移是固定的，并且所述数据位时钟偏移随所述前向选通脉冲时钟偏移而变化。

34. 权利要求 30 所述的接收器，其中：

在前向选通脉冲训练阶段，所述前向选通脉冲时钟恢复电路对齐所述前向选通脉冲采样时钟，包括产生前向选通脉冲时钟偏移；以及

在数据位训练阶段，所述至少一个数据位时钟恢复电路对齐所述数据位采样时钟，所述前向选通脉冲时钟恢复电路在所述数据位训练阶段是非激活的，其中从所述前向选通脉冲时钟接收的所述信号是所述前向选通脉冲偏移，其与中间数据时钟偏移相结合以产生数据位时钟偏移。

35. 权利要求 30 所述的接收器，其中针对所述多个数据位中的每一个，所述至少一个数据位时钟恢复电路包括数据位时钟恢复电路。

36. 权利要求 35 所述的接收器，其中所述至少一个数据位时钟恢复电路包括相位检测器，所述相位检测器接收相应的数据位和经恢复的数据时钟信号并且输出表示相位差的早/晚指示。

37. 权利要求 36 所述的接收器，其中所述至少一个数据位时钟恢复电路还包括相位计数器，所述相位计数器接收所述早/晚指示，输出中间数据位时钟偏移。

38. 权利要求 37 所述的接收器，其中所述早/晚指示在由所述相位计数器接收前被除以预定的数。

39. 权利要求 37 所述的接收器, 其中所述至少一个数据位时钟恢复电路还包括加法器, 所述加法器将所述中间数据位时钟偏移加到从所述前向选通脉冲时钟恢复电路接收的所述信号上, 其中所述信号包括前向选通脉冲时钟偏移。

40. 权利要求 39 所述的接收器, 其中所述至少一个数据位时钟恢复电路还包括时钟相位延迟电路, 所述时钟相位延迟电路接收所述加法器的输出并且产生所述经恢复的数据时钟信号。

41. 一种用于接收数据的方法, 包括:

响应于接收到前向选通脉冲, 选通脉冲时钟恢复电路对齐前向选通脉冲采样时钟; 以及

在运行期间对齐数据位采样时钟以跟踪所述前向选通脉冲采样时钟。

42. 权利要求 41 所述的方法, 其中从所述前向选通脉冲时钟恢复电路接收的所述信号包括前向选通脉冲时钟偏移, 并且其中所述前向选通脉冲时钟偏移与中间数据位时钟偏移相结合以产生数据位时钟偏移。

43. 权利要求 41 所述的方法, 其中在训练阶段, 所述数据位采样时钟通过产生数据位时钟偏移来对齐, 所述至少一个数据位时钟恢复电路在所述训练阶段是激活的, 并且其中所述数据位时钟偏移包括与来自所述前向选通脉冲时钟恢复电路的所述信号相结合的中间数据位时钟偏移, 其中所述信号包括前向选通脉冲时钟偏移。

44. 权利要求 43 所述的方法, 其中在所述至少一个可配置用于接收的部件的运行期间, 所述至少一个数据位时钟恢复电路是非激活的, 所述中间数据位时钟偏移是固定的, 并且所述数据位时钟偏移随所述前向选通脉冲时钟偏移而变化。

45. 权利要求 41 所述的方法, 其中:

在前向选通脉冲训练阶段, 所述前向选通脉冲时钟恢复电路对齐所述前向选通脉冲采样时钟, 包括产生前向选通脉冲时钟偏移; 以及

在数据位训练阶段, 所述至少一个数据位时钟恢复电路对齐所述数据位采样时钟, 所述前向选通脉冲时钟恢复电路在所述数据位训练阶段是非激活的, 其中从所述前向选通脉冲时钟接收的所述信号是所述前向选通脉冲偏移, 其与中间数据时钟偏移相结合以产生数据位时钟偏移。

46. 权利要求 41 所述的方法, 其中针对所述多个数据位中的每一个,

所述至少一个数据位时钟恢复电路包括数据位时钟恢复电路。

47. 权利要求 46 所述的方法，其中所述至少一个数据位时钟恢复电路包括相位检测器，所述相位检测器接收相应的数据位和经恢复的数据时钟信号并且输出表示相位差的早/晚指示。

48. 权利要求 47 所述的方法，其中所述至少一个数据位时钟恢复电路还包括相位计数器，所述相位计数器接收所述早/晚指示，输出中间数据位时钟偏移。

49. 权利要求 48 所述的方法，其中所述早/晚指示在由所述相位计数器接收前被除以预定的数。

50. 权利要求 48 所述的方法，其中所述至少一个数据位时钟恢复电路还包括加法器，所述加法器将所述中间数据位时钟偏移加到从所述前向选通脉冲时钟恢复电路接收到的所述信号上，其中所述信号包括前向选通脉冲时钟偏移。

51. 权利要求 50 所述的方法，其中所述至少一个数据位时钟恢复电路还包括时钟相位延迟电路，所述时钟相位延迟电路接收所述加法器的输出并且产生所述经恢复的数据时钟信号。

位去偏斜 IO 方法和系统

技术领域

本发明涉及在计算机和其他数字系统中进行数据传输的领域。

背景技术

随着计算机和其他数字系统变得越来越复杂和功能强大,用以增强在系统部件或元件之间传输数据的方法和硬件通常也不断地发展。待传输的数据包括表示数据、命令的信号或任何其他信号。系统部件或元件可以包括位于单个集成电路(IC)或位于不同集成电路上的不同功能的硬件块。所述不同集成电路可以在或不在同一印刷电路板(PCB)上。系统部件通常包括专门设计用来从其他系统部件接收数据以及将数据发送到其他系统部件的输入/输出(I/O)接口。一般来说,现有的 I/O 接口可以被分类为串行“链接”和并行“链接”。不管是哪种 I/O 接口类型,所传输的数据必须在系统部件之间同步,以便进行正确的操作。同步包括考虑或补偿潜在地引起误差的多个现象,所述现象包括信号抖动和信号偏斜。所述现象包括部件时钟之间的差和数据路径的物理属性,所述物理属性引起噪声并且影响所传输信号的完整性。当前用来操纵串行 I/O 接口和并行 I/O 接口的方法处理这些数据同步问题,但是有局限性。

典型的串行链接将时钟信息嵌入数据流中并且在接收器中使用一种时钟恢复方案来提取该时钟信息。这样的方案也被称为每线闭环定时(per-line closed-loop timing)。保证转换密度需要对数据进行编码,通常利用 8B/10B 码对数据进行编码。这种方法的缺点是增加了带宽开销并且提高了复杂性,这损害了性能并且提高了成本。

典型的并行链接在发送一组 N 个数据信号(例如,在双数据率动态随机存取存储器(DDR DRAM)中, N 可以是 8)的同时还发送时钟信号或选通脉冲(strobe)。依赖于数据率和需要的精密水平,使用以下的“源同步定时”方法之一:如果选通脉冲相对于发送器所发送的数据移动了半个比特时间,则接收器只是直接用该选通脉冲对数据进行采样;或者如果采样脉冲与发送器所发送的数据的边沿是对齐的,则接收器在整组数据上

将该选通脉冲延迟同一固定量，以在标称中心对数据眼进行采样。

上述两种并行链接方法中每个都需要对整组数据和选通脉冲进行非常严格的迹线阻抗和迹线长度匹配，以达到高数据率。为了减轻这种情况，每个位接收器可以将选通脉冲延迟不同的量以将其自己的时钟置于其自己的数据的中心。有时这叫做每位去偏斜。这种并行方案的缺点是选通脉冲（其通常在整個电路板上发送并且分布到整组数据）是有噪声的，因而减小了系统的定时预算。另外，接收器只是使用或延迟选通脉冲，其增加了抖动而不对抖动进行滤波。在一些实施方式中，为每个数据位而不是一组数据位发送一个选通脉冲，这增加了管脚数量和成本。

附图说明

图 1 是根据一个实施例的包括接收器接口的系统的一部分的框图。

图 2 是根据一个实施例的由图 1 的电路执行的方法的流程图。

具体实施方式

在此描述位去偏斜 IO 方法和系统的实施例。描述了一种用于位去偏斜的方法和系统。在一个实施例中，系统部件从发送部件接收前向选通脉冲信号和多个数据位信号。所述接收部件包括前向选通脉冲时钟恢复电路，该前向选通脉冲时钟恢复电路可配置成对齐前向选通脉冲采样时钟以提高采样精确度。所述接收部件还包括至少一个数据位时钟恢复电路，该数据位时钟恢复电路可配置成对齐数据位采样时钟以提高采样精确度，并且从前向选通脉冲时钟恢复电路接收信号，其在系统操作期间使得数据数据位采样时钟跟踪前向选通脉冲时钟。

实施例达到的数据率与使用每线闭环定时的串行链接类似，但是没有通常相关联的复杂性和编码带宽开销。在一个实施例中，在接口中提供了这些优点，所述接口包括相对于现有的源同步并行链接改进了的性能，但是（例如由于将时钟编码到串行数据流中）不包括与当前串行链接相关联的复杂性和开销。

图 1 是根据一个实施例的系统 100 的一部分的框图。系统 100 包括发送器 104 和接收器接口 102。系统 100 可以是任何计算机系统或其子系统、数字系统、在部件之间传输数据的部件或部件的组合。部件可以是集成电

路上的电路块、同一印刷电路板上的不同集成电路或者通过网络进行通信的部件。在各个实施例中，所述部件以高速和高数据率进行通信。例如，系统 100 可以是计算机系统，具有与双数据率(DDR) DRAM 通信的图形处理或视频处理单元，但实施例不限于此。

示出了发送器 104 的相关部分，包括锁存器或触发器 106(0)-106(N-1) 和相关的输出缓冲器。在一个实施例中，发送器 104 发送与数据位 DQ(0)-DQ(N-1)相关联的选通脉冲信号或前向时钟（标记为 DQS）。数据位和前向选通脉冲在传输介质 107 上发送。在不同的实施例中，传输介质 107 可以是一个或多个线缆、PCB 迹线或任何其他已知传输介质。数据位 DQ 根据发生在发送器 104 和包括接收器接口 102 的接收部件之间的通信而被发送。相对照的，如图所示，前向选通脉冲 DQS 作为触发逻辑值（toggling logic value）（101010...）连续地被发送。发送器 104 还包括发送锁相环（TxPLL）108，其是公知电路。例如，在大部分频率合成器中使用 PLL 作为控制机构。TxPLL108 以已知方式工作。

接收器接口 102 包括以已知方式工作的接收 PLL（RxPLL）110。TxPLL 108 和 RxPLL 110 都接收参考时钟信号 Ref Clk 109。TxPLL 108 的输出为锁存器 106 提供时钟信号。RxPLL 110 的输出被输入到针对每个数据位 DQ 以及针对前向选通脉冲信号 DQS 的时钟相位延迟电路 120，其在以下更详细地描述。

前向选通脉冲信号 DQS 由接收器接口 102 的时钟恢复电路 112（S）接收。针对数据位 DQ 中的每一个，接收器接口 102 还包括单独的时钟恢复电路 113（时钟恢复电路 113（0）针对 DQ(0)，时钟恢复电路 113（1）针对 DQ(1)等等）。

为了帮助确保包括选通脉冲和数据信号的所接收信号被接收器接口 102 正确地采样，采样时钟信号被对齐，以便最优地采样所接收信号。例如，在一个实施例中，采样时钟信号被对齐，以便在所接收数据的有效窗口（也称为数据眼）的中心附近进行采样。这使建立和保持时间最大化，并且减小了采样误差的可能性。前向选通脉冲信号和数据位 DQ 以边沿对齐的方式被发送。接收器接口 102 中的时钟恢复电路 112 和 113 的功能是对所接收的 RxPLL 110 输出信号的相位进行调节，以使采样点接近数据眼的中心。在另一个实施例中，可以根据其他准则来调节或对齐所接收的 RxPLL 110 输出信号的相位，以提高适合于系统实施例的设计的采样精确度。

参考时钟恢复电路 112 (S), 前向选通脉冲 DQS 由相位检测器 114 接收。相位检测器 114 是已知电路, 例如比较器, 其将所接收信号的相位和采样时钟信号的相位相比较, 并确定所接收信号相对于采样时钟信号是早还是晚。如在以下进一步解释的, 采样时钟信号是 RxPLL 110 的输出, 之后, 其与所接收信号的相位关系通过时钟相位延迟电路 120 被调节成与前向选通脉冲 DQS 的中心对齐。相位检测器 114 的输出是针对每个时钟周期的早/晚指示。早/晚指示被输入到除法器 116。除法器 116 可调节用于使得检测到的早/晚指示的数量以一定的比率减少。除法器 116 的输出是经调节的由相位计数器 118 所接收的早/晚指示的数量。之所以对早/晚指示的数量进行调节, 是因为可能不希望通过调节 RxPLL 110 输出的相位来对每个早或晚指示做出反应。例如, 响应于每个早/晚指示而调节 RxPLL 110 输出的相位可能导致时钟抖动。因此, 早/晚指示被除以一个数, 例如 32, 使得 RxPLL 110 输出的相位每 32 个指示移动一次。

相位计数器 118 的输出是信号 DQSPC, 其被输入到时钟相位延迟电路 120, 该时钟相位延迟电路 120 调节 RxPLL 110 输出的延迟以将 RxPLL 110 输出置于 DQS 的中心。在一个实施例中, 时钟相位延迟电路 120 是相位内插器, 但实施例不限于此。时钟相位延迟电路 120 输出恢复的前向时钟信号 DQSclk, 该恢复的前向时钟信号 DQSclk 被反馈到相位检测器电路 114。在当前的实施例中, DQSclk 将被调节, 直到其位于所接收 DQS 信号的中心以最大化建立/保持时间窗。这样, 当时钟恢复电路 112 (S) 被使能或激活时, DQSclk 与所接收 DQS 信号相比较以便不断地进行调节。

根据一个实施例, 时钟恢复电路 112 (S) 运行在初始“训练”阶段, 以便适当数量的延迟来训练电路 112 (S), 所述适当数量的延迟是将恢复的前向时钟信号 DQSclk 置于 DQS (所接收的选通脉冲信号) 的数据眼的中心所需的。该数量的延迟由 DQSPC 信号表示。一旦时钟恢复电路 112 (S) 被训练完并且获得了 DQSPC 信号, 时钟恢复电路 112 (S) 就由输入到除法器电路 116 的 DQS 冻结信号禁止。DQS 冻结信号具有使 DQSPC 信号保持在稳定值的作用。

针对数据位 DQ 中的每一个, 接收器接口 102 还包括数据位时钟恢复电路 113 (0)、113 (1) 等等, 直到 113 (N-1)。在一个实施例中, 数据位时钟恢复电路 113 在时钟恢复电路 112 (S) 的训练阶段由公共 DQ 冻结信号禁止。在时钟恢复电路 112 (S) 被训练并被禁止之后, 时钟恢复

电路 113 在数据时钟恢复电路训练阶段被使能。在数据时钟恢复电路训练阶段, 数据时钟恢复电路 113 中的每一个都进行操作以检测 RxPLL 110 的输出和各自所接收的数据信号的数据眼之间的相位差。在一个实施例中, 在时钟恢复电路 112(S) 的训练阶段所确定的相位调节(其由 DQSPC 信号表示)被加到由每个时钟恢复电路 113 所确定的相位调节上。

参考时钟恢复电路 133(0), 数据信号 DQ(0) 由相位检测器电路 114 接收。如参考时钟恢复电路 112(S) 所解释的, 相位检测器电路 114 的输出由可调节的除法器电路 116 接收。除法器电路 116 的输出由相位计数器 118 接收, 相位计数器 118 将信号 DQPC(0) 输出到加法器 122。加法器 122 还接收来自选通脉冲时钟恢复电路 112(S) 的 DQSPC 信号, 并且将所接收的信号相加以产生到相位延迟电路 120 的输入。DQPC 信号是中间时钟偏移, 其被加到 DQSPC 时钟偏移上以产生数据时钟偏移信号, 该数据时钟偏移信号被输入到时钟相位延迟电路 120。从加法器 122 到时钟相位延迟电路 120 的输入指示了 RxPLL 110 的输出应该被延迟的量。时钟相位延迟电路 120 的输出是用于数据位 DQ(0) 的经恢复时钟信号, 或 DQrclk(0)。

每个数据时钟恢复电路 113 都经过类似的训练阶段以得到 DQPC 信号和 DQrclk 信号。针对不同时钟恢复电路 113 的训练阶段可以同时发生或在不同时间发生。当所有的数据时钟恢复电路 113 被训练完, 它们都由 DQ 冻结信号禁止。禁止数据时钟恢复电路 113 防止了各个电路 113 的 DQPC 信号发生改变。

在正常的系统操作中, 当包含接收器接口 102 的部件在运行时, 选通脉冲时钟恢复电路 112(S) 再次被使能并且自由运行。因而, 电路 112(S) 将根据需要来调节 DQSPC, 以使 DQSrcclk 保持在所接收的前向选通脉冲(DQS)的中心。另一方面, 数据时钟恢复电路在正常的系统操作期间保持禁止。但是, 因为每个数据时钟恢复电路都接收 DQSPC, 为每个数据位(从 DQ(0) 到 DQ(N-1))提供时钟的信号的相位调节或偏移将被调节以跟踪任何 DQSPC 改变。数据因而“跟踪”前向选通脉冲。亦即, 由于数据和前向选通脉冲各自的采样时钟一起移动, 数据和前向选通脉冲也一起移动。这是有效的, 因为每个数据信号和前向选通脉冲的关系(或每个数据信号和前向选通脉冲各自的采样时钟之间的关系)是在训练阶段建立的, 并且如果它们每一个遇到的是类似的环境变化, 那么该它们的关系就没有大的变化。

图 2 是根据一个实施例的说明位去偏斜方法 200 的流程图,该位去偏斜方法可以由图 1 的系统执行。在 202,系统初始化。作为初始化过程的一部分,使能前向选通脉冲时钟恢复电路,并禁止数据时钟恢复电路,如在 204 所示。在 206,允许前向选通脉冲时钟恢复电路运行以确定 DQSPC。如先前所述,当 DQSPC 的值适于使时钟相位延迟电路将前向选通脉冲采样时钟 DQSrclk 置于所接收的前向选通脉冲数据眼的中心时,确定 DQSPC。在一个实施例中,前向选通脉冲采样时钟 DQSrclk 是发送 PLL、RxPLL 的延迟输出,该 RxPLL 接收参考时钟。在一个实施例中,前向选通脉冲时钟恢复电路运行预定量的时间(例如,一毫秒),该预定量的时间被确定成足以确定 DQSPC。在另一个实施例中,附加的电路(未示出)确定何时确定 DQSPC。

当确定了 DQSPC,禁止前向选通脉冲时钟恢复电路,并使能数据时钟恢复电路,如在 208 所示。在 210,运行数据时钟恢复电路以确定各个 DQPC。如先前参考图 1 所述,在该数据时钟恢复训练阶段,DQSPC 被加到每个 DQPC 相位计数器输出上。

当确定了 DQPC,再次使能前向选通脉冲时钟恢复电路,并禁止数据时钟恢复电路,如在 212 所示。然后在 214 进行正常的系统操作。

在不同的实施例中,在正常操作期间的时钟恢复事件可能引起一个或多个时钟恢复电路在系统运行期间完成另一训练阶段。例如,在一个实施例中,如果一个或多个 DQPC 值在预定数量的时钟周期(例如一千个周期)内没有改变,则将重复在 208 开始的训练过程。在另一个实施例中,包含接收器接口 102 的系统部件经历空闲时段或功率节省时段,在此期间,系统部件不做“有用的”工作。在这样的实施例中,空闲时段也是时钟恢复事件。这样的部件的一个例子是双数据率动态随机存取存储器(DDR DRAM),对于 DDR DRAM 来说,刷新周期可以被用作时钟恢复事件。

在不同的实施例中,通过高层系统协议来执行对所述电路的控制。可以针对特定部件指定电路的某种性状(behavior),使得部件的用户可以通过协议来调整电路的性状。所指定的性状的例子是用于除法器电路的值、用于执行时钟恢复电路训练的预定量时间以及哪些事件(如果有的话)是时钟恢复事件。

在这里公开的去偏斜 IO 方法和系统的实施例包括一种系统,该系统包括:至少一个可配置用于发送多个数据位和与多个数据位相关联的前向选通脉冲的部件;至少一个可配置用于接收多个信号的部件。在一个实施

例中,所述至少一个可配置用于接收的部件包括:前向选通脉冲时钟恢复电路,可配置用于对齐前向选通脉冲采样时钟以提高采样精确度;以及至少一个数据位时钟恢复电路,可配置用于对齐数据位采样时钟以提高采样精确度,并且在所述至少一个可配置用于接收的部件的运行期间从前向选通脉冲时钟恢复电路接收信号,其使得数据位采样时钟跟踪前向选通脉冲采样时钟。

在一个实施例中,从前向选通脉冲时钟恢复电路接收的信号包括前向选通脉冲时钟偏移,并且其中前向选通脉冲时钟偏移与中间数据位时钟偏移相结合以产生数据位时钟偏移。

在一个实施例中,在训练阶段,所述数据位采样时钟通过产生数据位时钟偏移来对齐,所述至少一个数据位时钟恢复电路在所述训练阶段是激活的,并且其中所述数据位时钟偏移包括与来自所述前向选通脉冲时钟恢复电路的所述信号相结合的中间数据位时钟偏移,其中所述信号包括前向选通脉冲时钟偏移。

在一个实施例中,在所述至少一个可配置用于接收的部件的运行期间,所述至少一个数据位时钟恢复电路是非激活的,所述中间数据位时钟偏移是固定的,并且所述数据位时钟偏移随所述前向选通脉冲时钟偏移而变化。

在一个实施例中,在前向选通脉冲训练阶段,所述前向选通脉冲时钟恢复电路对齐所述前向选通脉冲采样时钟,包括产生前向选通脉冲时钟偏移;以及在数据位训练阶段,所述至少一个数据位时钟恢复电路对齐所述数据位采样时钟,所述前向选通脉冲时钟恢复电路在所述数据位训练阶段是非激活的,其中从所述前向选通脉冲时钟接收的所述信号是所述前向选通脉冲偏移,其与中间数据时钟偏移相结合以产生数据位时钟偏移。

在一个实施例中,针对多个数据位中的每一个,所述至少一个数据位时钟恢复电路包括数据位时钟恢复电路。

在一个实施例中,其中所述至少一个数据位时钟恢复电路包括相位检测器,该相位检测器接收相应的数据位和经恢复的数据时钟信号并且输出表示相位差的早/晚指示。

在一个实施例中,所述至少一个数据位时钟恢复电路还包括相位计数器,该相位计数器接收早/晚指示,输出中间数据位时钟偏移。

在一个实施例中,早/晚指示在由相位计数器接收前被除以预定的数。

在一个实施例中，所述至少一个数据位时钟恢复电路还包括加法器，该加法器将中间数据位时钟偏移加到从前向选通脉冲时钟恢复电路接收的信号上，其中所述信号包括前向选通脉冲时钟偏移。

在一个实施例中，所述至少一个数据位时钟恢复电路还包括时钟相位延迟电路，该时钟相位延迟电路接收加法器的输出并且产生经恢复的数据时钟信号。

实施例还包括一种计算机可读介质，其上存储有指令，当在系统中运行时，其使得所述系统实施一种数据传输的方法，所述方法包括：训练前向选通脉冲时钟恢复电路以确定用于提高采样精确度的前向选通脉冲采样时钟偏移；以及训练至少一个数据位时钟恢复电路以确定用于提高采样精确度的数据位采样时钟偏移，其中所述数据位采样时钟偏移包括所述前向选通脉冲采样时钟偏移和中间数据位采样时钟偏移。

在一个实施例中，由所述系统实施的所述方法还包括：当训练所述前向选通脉冲时钟恢复电路时，使能所述前向选通脉冲时钟恢复电路并且禁止所述数据时钟恢复电路。

在一个实施例中，由所述系统实施的所述方法还包括：当训练所述数据时钟恢复电路时，禁止所述前向选通脉冲时钟恢复电路并且使能所述数据时钟恢复电路。

在一个实施例中，由所述系统实施的所述方法还包括：在系统运行期间，使能所述前向选通脉冲时钟恢复电路并且禁止所述数据时钟恢复电路，使得所述数据位采样时钟偏移跟踪所述前向选通脉冲采样时钟偏移。

在一个实施例中，由所述系统实施的所述方法还包括：在所述系统的运行期间检测至少一个时钟恢复事件；以及重复训练至少一个数据位时钟恢复电路。

在一个实施例中，所述至少一个时钟恢复事件包括：自所述至少一个数据时钟恢复电路的上一次训练起经过了预定量的时间；包括所述至少一个数据时钟恢复电路的系统部件的空闲状态；以及包括所述至少一个数据时钟恢复电路的系统部件的低功率状态。

实施例还包括一种在系统中传输数据的方法，所述方法包括：训练前向选通脉冲时钟恢复电路以确定用于提高采样精确度的前向选通脉冲时钟偏移；训练至少一个数据位时钟恢复电路以确定用于提高采样精确度的数据位采样时钟偏移，其中所述数据位采样时钟偏移包括所述前向选通脉

冲采样时钟偏移和中间数据位采样时钟偏移。

一个实施例包括：当训练所述前向选通脉冲时钟恢复电路时，使能所述前向选通脉冲时钟恢复电路并且禁止所述数据时钟恢复电路。

一个实施例包括：当训练所述数据时钟恢复电路时，禁止所述前向选通脉冲时钟恢复电路并且使能所述数据时钟恢复电路。

一个实施例包括在系统运行期间，使能所述前向选通脉冲时钟恢复电路并且禁止所述数据时钟恢复电路，使得所述数据位采样时钟偏移跟踪所述前向选通脉冲采样时钟偏移。

一个实施例包括：在所述系统的运行期间检测至少一个时钟恢复事件；以及重复训练至少一个数据位时钟恢复电路。

在一个实施例中，所述至少一个时钟恢复事件包括：自所述至少一个数据时钟恢复电路的上一次训练起经过了预定量的时间；包括所述至少一个数据时钟恢复电路的系统部件的空闲状态；以及所述至少一个数据时钟恢复电路的低功率状态。

实施例还包括一种发送数据的装置，包括：选通脉冲信号发送器，用于在传输介质上发送选通脉冲信号；以及至少一个数据发送器，用于在传输介质上发送至少一个数据信号，其中接收器选通脉冲采样时钟被对齐以便采样所述选通脉冲信号，并且其中至少一个接收器数据采样时钟被对齐以便跟踪所述对齐的接收器选通脉冲采样时钟。

在一个实施例中，选通脉冲信号在传输介质上连续地被发送。

在一个实施例中，连续地被发送的选通脉冲信号在逻辑高值和逻辑低值之间转换。

实施例还包括一种发送数据的方法，包括：在传输介质上发送选通脉冲信号；以及在传输介质上发送至少一个数据信号，其中采样所发送的选通脉冲信号的选通脉冲采样时钟被调节一个用来对齐所述选通采样脉冲时钟的调节值，并且其中所述调节值还用来对齐对所述至少一个数据信号进行采样的至少一个数据采样时钟。

在一个实施例中，发送选通脉冲信号包括在传输介质上连续地发送选通脉冲信号。

在一个实施例中，连续地发送所述选通脉冲信号包括使所述连续地被发送的选通脉冲信号在逻辑高值和逻辑低值之间转换。

实施例还包括一种用来接收数据的接收器，包括：前向选通脉冲时钟恢复电路，可配置用于对齐前向选通脉冲采样时钟；以及至少一个数据位时钟恢复电路，可配置用于对齐数据位采样时钟以及从所述前向选通脉冲时钟恢复电路接收信号，所述至少一个数据位恢复电路将所述数据位采样时钟配置成在运行期间跟踪所述前向选通脉冲采样时钟。

在一个实施例中，从所述前向选通脉冲时钟恢复电路接收的所述信号包括前向选通脉冲时钟偏移，并且其中所述前向选通脉冲时钟偏移与中间数据位时钟偏移相结合以产生数据位时钟偏移。

在一个实施例中，在训练阶段，所述数据位采样时钟通过产生数据位时钟偏移来对齐，所述至少一个数据位时钟恢复电路在所述训练阶段是激活的，并且其中所述数据位时钟偏移包括与来自所述前向选通脉冲时钟恢复电路的所述信号相结合的中间数据位时钟偏移，其中所述信号包括前向选通脉冲时钟偏移。

在一个实施例中，在所述至少一个可配置用于接收的部件的运行期间，所述至少一个数据位时钟恢复电路是非激活的，所述中间数据位时钟偏移是固定的，并且所述数据位时钟偏移随所述前向选通脉冲时钟偏移而变化。

在一个实施例中，在前向选通脉冲训练阶段，所述前向选通脉冲时钟恢复电路对齐所述前向选通脉冲采样时钟，包括产生前向选通脉冲时钟偏移；以及在数据位训练阶段，所述至少一个数据位时钟恢复电路对齐所述数据位采样时钟，所述前向选通脉冲时钟恢复电路在所述数据位训练阶段是非激活的，其中从所述前向选通脉冲时钟接收的所述信号是所述前向选通脉冲偏移，其与中间数据时钟偏移相结合以产生数据位时钟偏移。

在一个实施例中，针对所述多个数据位中的每一个，所述至少一个数据位时钟恢复电路包括数据位时钟恢复电路。

在一个实施例中，所述至少一个数据位时钟恢复电路包括相位检测器，所述相位检测器接收相应的数据位和经恢复的数据时钟信号并且输出表示相位差的早/晚指示。

在一个实施例中，所述至少一个数据位时钟恢复电路还包括相位计数器，所述相位计数器接收所述早/晚指示，输出中间数据位时钟偏移。

在一个实施例中，所述早/晚指示在由所述相位计数器接收前被除以预定的数。

在一个实施例中，所述至少一个数据位时钟恢复电路还包括加法器，所述加法器将所述中间数据位时钟偏移加到从所述前向选通脉冲时钟恢复电路接收的所述信号上，其中所述信号包括前向选通脉冲时钟偏移。

在一个实施例中，所述至少一个数据位时钟恢复电路还包括时钟相位延迟电路，所述时钟相位延迟电路接收所述加法器的输出并且产生所述经恢复的数据时钟信号。

实施例还包括一种用于接收数据的方法，包括：响应于接收到前向选通脉冲，选通脉冲时钟恢复电路对齐前向选通脉冲采样时钟；以及在运行期间对齐数据位采样时钟以跟踪所述前向选通脉冲采样时钟。

在一个实施例中，从所述前向选通脉冲时钟恢复电路接收的所述信号包括前向选通脉冲时钟偏移，并且其中所述前向选通脉冲时钟偏移与中间数据位时钟偏移相结合以产生数据位时钟偏移。

在一个实施例中，在训练阶段，所述数据位采样时钟通过产生数据位时钟偏移来对齐，所述至少一个数据位时钟恢复电路在所述训练阶段是激活的，并且其中所述数据位时钟偏移包括与来自所述前向选通脉冲时钟恢复电路的所述信号相结合的中间数据位时钟偏移，其中所述信号包括前向选通脉冲时钟偏移。

在一个实施例中，在所述至少一个可配置用于接收的部件的运行期间，所述至少一个数据位时钟恢复电路是非激活的，所述中间数据位时钟偏移是固定的，并且所述数据位时钟偏移随所述前向选通脉冲时钟偏移而变化。

在一个实施例中，在前向选通脉冲训练阶段，所述前向选通脉冲时钟恢复电路对齐所述前向选通脉冲采样时钟，包括产生前向选通脉冲时钟偏移；以及在数据位训练阶段，所述至少一个数据位时钟恢复电路对齐所述数据位采样时钟，所述前向选通脉冲时钟恢复电路在所述数据位训练阶段是非激活的，其中从所述前向选通脉冲时钟接收的所述信号是所述前向选通脉冲偏移，其与中间数据时钟偏移相结合以产生数据位时钟偏移。

在一个实施例中，针对所述多个数据位中的每一个，所述至少一个数据位时钟恢复电路包括数据位时钟恢复电路。

在一个实施例中，所述至少一个数据位时钟恢复电路包括相位检测器，所述相位检测器接收相应的数据位和经恢复的数据时钟信号并且输出表示相位差的早/晚指示。

在一个实施例中,所述至少一个数据位时钟恢复电路还包括相位计数器,所述相位计数器接收所述早/晚指示,输出中间数据位时钟偏移。

在一个实施例中,所述早/晚指示在由所述相位计数器接收前被除以预定的数。

在一个实施例中,所述至少一个数据位时钟恢复电路还包括加法器,所述加法器将所述中间数据位时钟偏移加到从所述前向选通脉冲时钟恢复电路接收到的所述信号上,其中所述信号包括前向选通脉冲时钟偏移。

在一个实施例中,所述至少一个数据位时钟恢复电路还包括时钟相位延迟电路,所述时钟相位延迟电路接收所述加法器的输出并且产生所述经恢复的数据时钟信号。

以上描述的本发明的方面可以作为编程到各种电路中任何一种中的功能来实现,所述电路包括但不限于可编程器件(PLD),比如现场可编程门阵列(FPGA)、可编程阵列逻辑(PAL)器件、电可编程逻辑和存储器件和基于标准单元的器件,以及专用集成电路(ASIC)和全定制集成电路。实现本发明的方面的一些其它可能性包括:带有存储器(如电可擦除可编程只读存储器(EEPROM))的微控制器、嵌入式微处理器、固件、软件等。此外,本发明的方面可以以具有基于软件的电路模拟的微处理器、分立逻辑(顺序的和组合的)、定制器件、模糊(神经)逻辑、量子器件以及任何以上器件类型的混合来实施。当然,基本的器件技术可以以各种部件类型来提供,例如金属氧化物半导体场效应晶体管(MOSFET)技术如互补金属氧化物半导体(CMOS)、双极技术如发射极耦合逻辑(ECL)、聚合物技术(例如硅共轭聚合物和金属共轭聚合物金属结构)、数模混合技术等。

除非上下文明确地另有要求,否则,在整个说明书和权利要求书中,词“包括”等应被解释为包含的意思而不是排除的或穷尽的意思。也就是说,是“包括但不限于”的意思。使用单数或复数的词也分别包括复数或单数的情况。另外,词“在此”、“在下文中”、“以上”、“以下”和含有类似意思的词,当用于本申请时,指的是整个本申请而不是本申请的任何特定部分。当词“或”用于两个或更多项的罗列时,该词覆盖了该词的所有以下解释:罗列中各项的任何一个、罗列中各项的全部以及罗列中各项的任何组合。

以上对所图示的本发明的实施例的说明不是为了穷举或将本发明限

制到所公开的精确形式。尽管为了说明的目的，在此描述了本发明的特定实施例和例子，但是本领域技术人员将认识到，在本发明的范围内进行各种等同修改是可能的。在此提供的本发明的教导可以应用于其它系统，而不只用于如以上所述的包括图形处理或视频处理或 DDR DRAM 的系统。所描述的各种操作可以在各种各样的体系结构中实施，并且可以以不同于所描述的方式分布。另外，虽然在此描述了很多配置，但是没有一个是意图用于限制或排他的。

在另外的实施例中，在此描述的硬件或软件能力的一些或全部可以存在于打印机、照相机、电视、手持设备、移动电话或一些其它设备中。以上描述的不同实施例的部件和行为可以被组合以提供另外的实施例。可以根据以上详细描述对本发明进行这些或其它的改变。

通常，在以下的权利要求中，所使用的术语不应被解释为将所述视频处理方法和系统限制为在说明书和权利要求中所公开的特定实施例，而应被解释为包括根据权利要求来运行以便提供视频处理的任何处理系统。因此，所述方法和系统不受所述公开的限制，相反，用于位去偏斜的方法和系统的范围将完全由权利要求所确定。

尽管用于视频处理的方法和装置的某些方面在以下以某些权利要求的形式呈现，但是发明人以任何数量权利要求形式构思了所述方法和装置的各个方面。例如，尽管仅所述方法和装置的一个方面可以被描述为以计算机可读介质实施，但是其他方面也可以类似地以计算机可读介质实施。因此，发明人保留在提交本申请之后增加另外的权利要求的权利，以针对用于位去偏斜的方法和装置的其它方面继续实行这样的另外权利要求的形式。

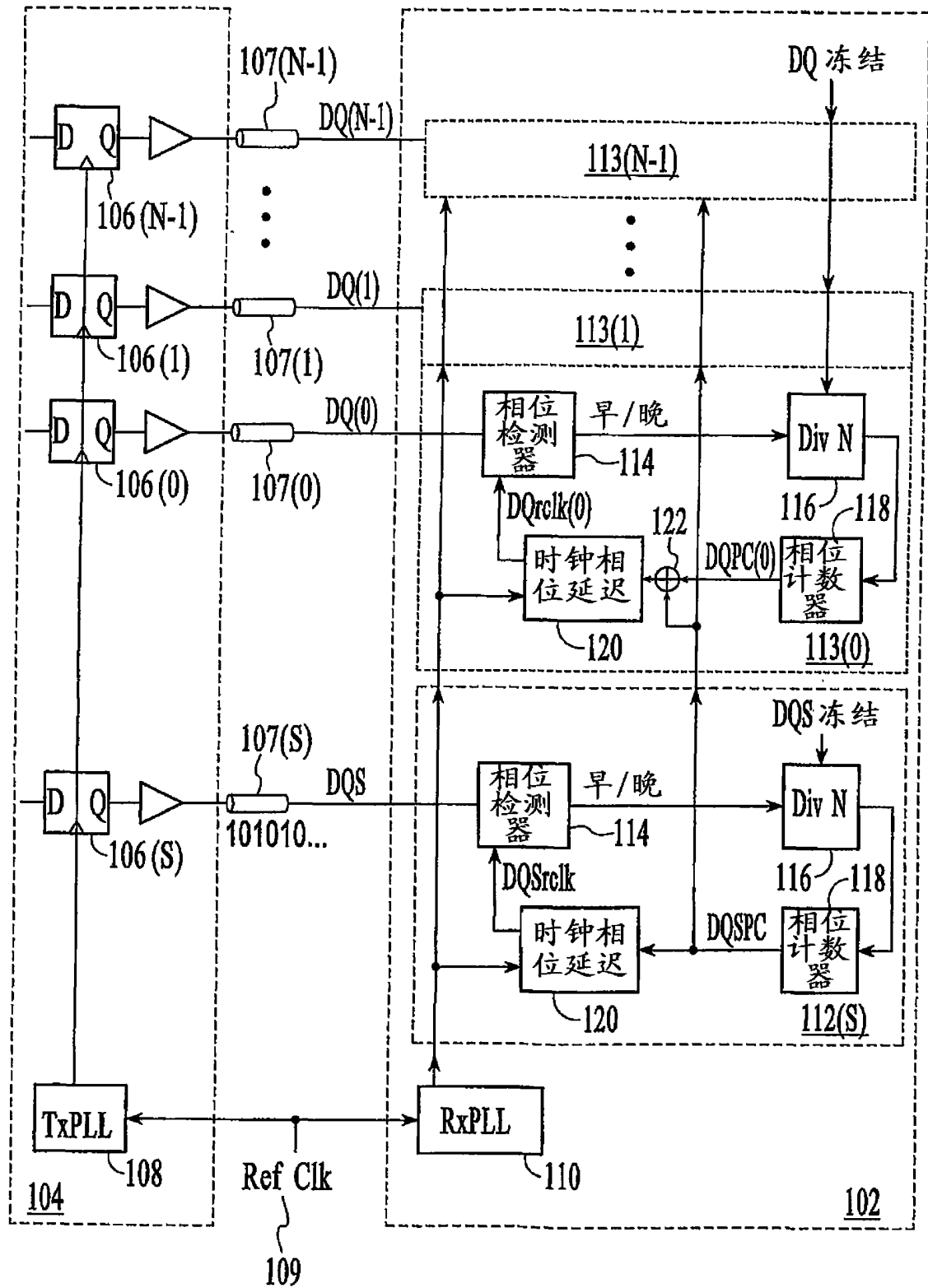


图 1

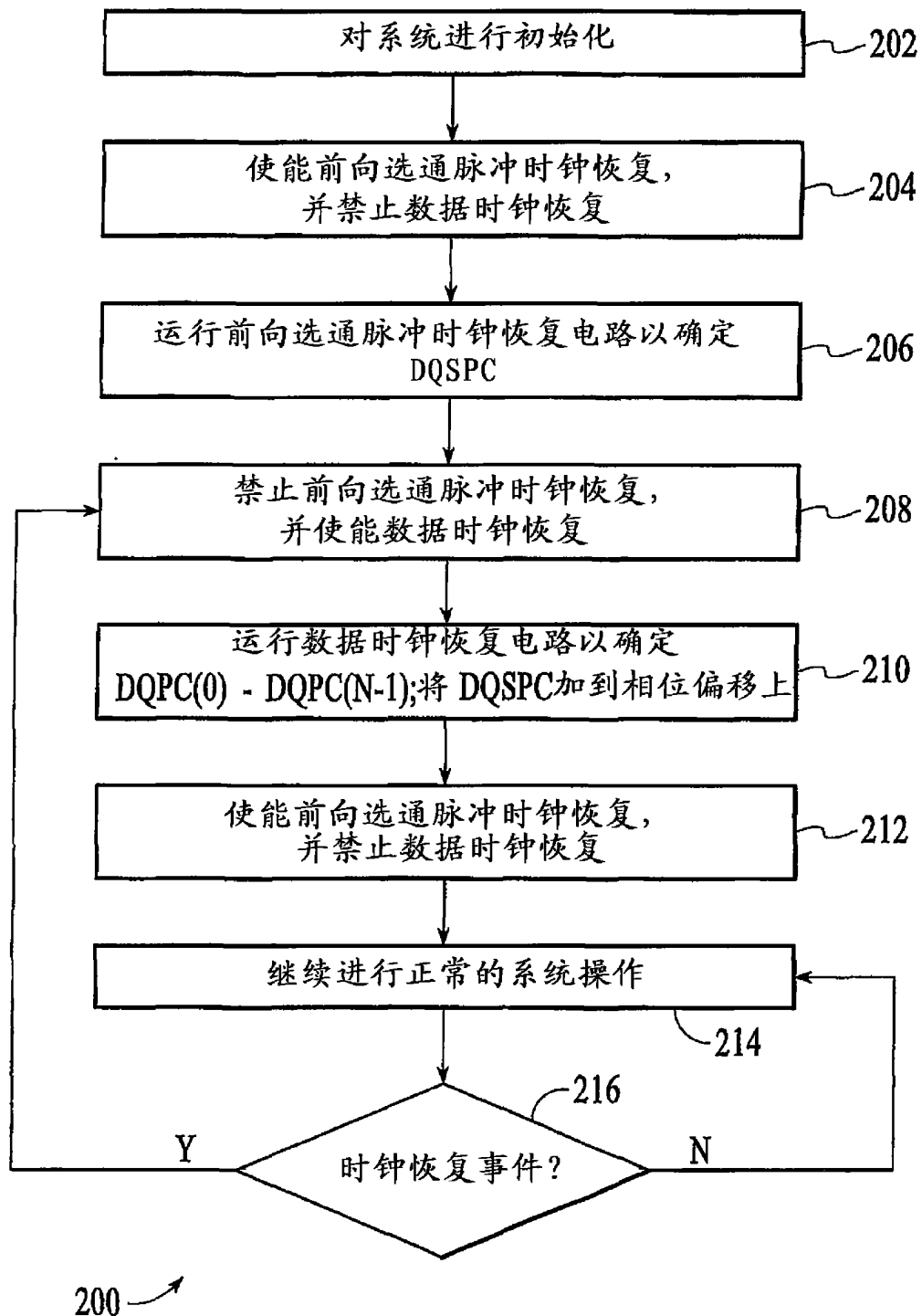


图2