

- [54] OFF-DELAY TIMING APPARATUS
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- [51] Int. Cl. H03k 17/28, H03k 17/66, H03k 17/74
- [58] Field of Search 317/141 S, 148.5 R;
307/242, 252 B, 293

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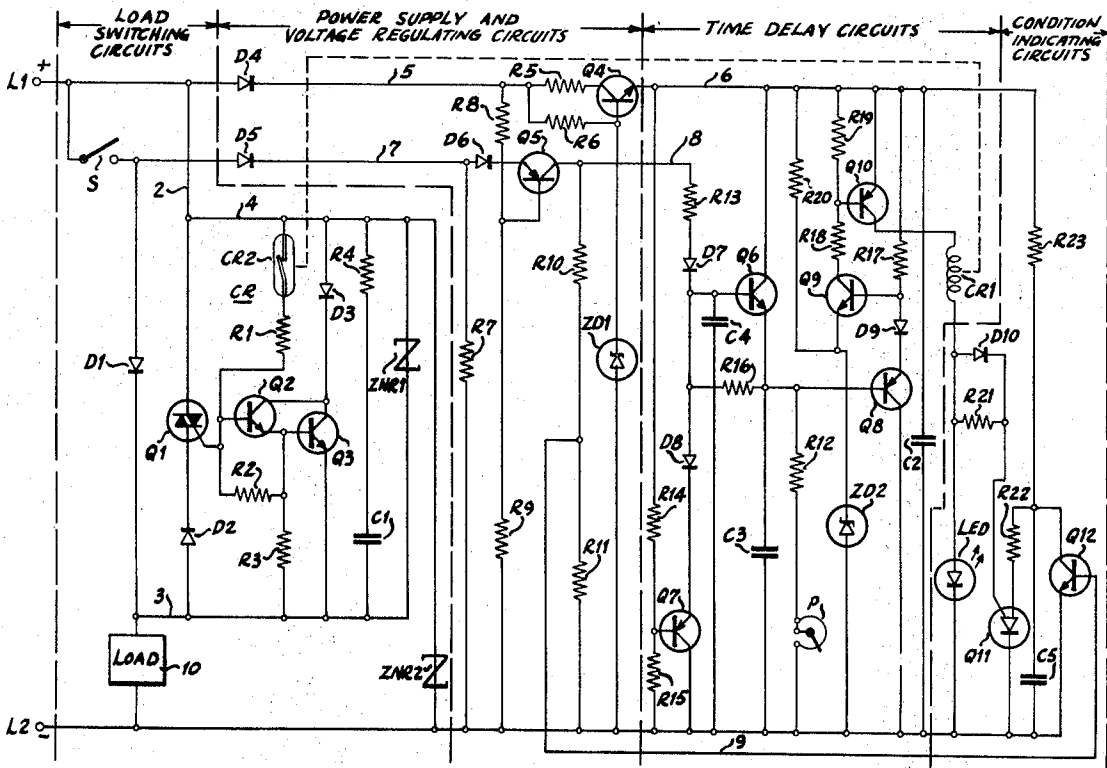
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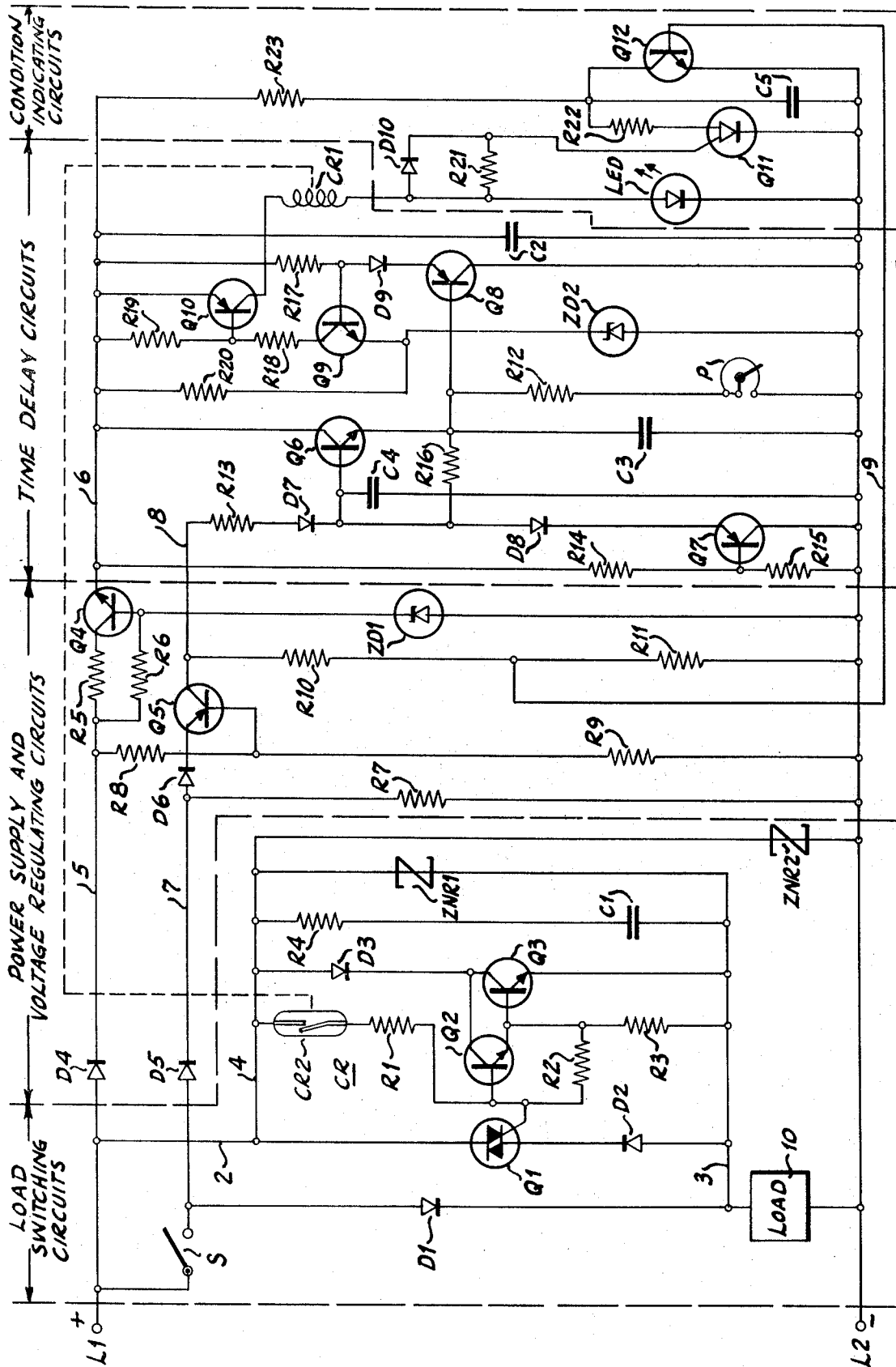
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[57] ABSTRACT

A device for supplying current to a load from a relatively wide range of D.C. and A.C. voltage sources, and affording time delay-OFF mode of deenergization upon opening of a selector switch. An electric illuminous indicating device provides indication of steady state and time delay-OFF modes of operation by steady and blinking illumination conditions. Provision is made to prevent improper operation of the device when the leakage current resistance shunting the open selector switch circuit exceeds, for example, 40,000 ohms. Unwanted operation due to transient voltage and current conditions is provided by extensive use of suppression and blocking devices.

10 Claims, 1 Drawing Figure





OFF-DELAY TIMING APPARATUS

BACKGROUND OF THE INVENTION

This invention relates to apparatus for supplying current to a load and deenergizing the same after a time delay by operation of a selector switch.

The use of solid state or semiconductor devices in timing delay relay apparatus has become quite prevalent. However, such relays have usually been limited to the use of one type of current, either D.C. or A.C. but not both. Normally, their use has also been limited to a rather narrow range of current supply voltages. Further, few if any of such solid state relays have been provided with means to give a visual indication of their existing states or modes of operation.

OBJECTS OF THE INVENTION

A primary object of the present invention is to provide an improved form of an essentially all solid state relay or device for energizing loads instantaneously and deenergizing the same after an adjustable time delay period.

Another object of the invention is to provide a device of the aforementioned kind which is characterized by its ability to work satisfactorily when the current supply is either D.C. or A.C. and with different supply voltages over a substantial range.

A further object of the invention is to provide a device of the aforementioned type which also affords luminous indication of its steady state, OFF-delay and OFF conditions of operation.

A still further object of the invention is to provide a time delay apparatus of the aforementioned kind which is well protected against damage and unwanted operation from transient voltages, and

Still another object is to provide a device of the aforementioned kind which is immune to unwanted or improper operation by leakage current in a selector switch circuit.

SUMMARY OF THE INVENTION

During closed condition of a selector switch, current flow to a load is afforded by a half wave diode or rectifier when the supply current is D.C., and together with a thyristor controlled by contacts of an electromagnetic switch and arranged to conduct on the opposite half cycles when the current supply is A.C. Opening of the selector switch renders the diode ineffective and starts operation of a time delay de-energizing circuit.

Transistors under the control of contacts of the electromagnetic switch are effective when said diode is ineffective to supply either D.C. current to the load or half waves of A.C. current until opening of the contacts of said electromagnetic switch at the end of the time delay period renders them and the thyristor nonconducting.

The diode provides a high current path for positive half cycle currents or D.C. currents when the selector switch is closed, thus enabling the timer apparatus to drive solenoid or lamp loads while at the same time permitting the controlled transistors to be small and economical units.

An electric illuminous indicating device is connected in series with the control winding of the electromagnetic switch and is illuminated steadily whenever the selector switch is closed. A programmable unijunction transistor under the control of a capacitor-transistor

controlled oscillator is cyclically rendered nonconducting and conducting upon opening of said selector switch to correspondingly interrupt and reestablish current flow through said indicating device to cause the latter to blink and indicate the OFF-timing mode of operation.

The power supply is arranged to provide unidirectional energizing potential for the time delay, electromagnetic switch control winding and illuminous indicating circuits from either D.C. or A.C. current sources when the voltage thereof exceeds a given value. A transistor-zener diode regulator maintains said unidirectional potential at a desired value. Provision is also made to insure that the control circuit for the time delay control and indicating circuits cannot be rendered effective by leakage circuits having circuit path resistance in excess of 40,000 ohms from L1 to the selector switch terminal.

A number of protective devices are provided to inhibit unwanted operation to the various semiconductor devices under transient voltage and current conditions.

THE DRAWING

The single FIGURE of the drawing is a schematic diagram of an apparatus constructed in accordance with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to the drawing, it shows the complete time delay apparatus which, for ease of understanding, will be described under sub-headings from right to left set forth at the top of the drawing. The power supply lines L1 and L2 are common to all of the circuits and may be subjected to either A.C. or D.C. supply current. The applied voltage on these lines can be in the range of 20 to 132 volts and if A.C. is used the frequency can be in the 50 to 400 Hz range.

LOAD SWITCHING CIRCUITS

A manual switch S, which can be of any preferred type, is connected at one side to line L1 and at its other side in series with a diode D1 and a load 10 to line L2. A bilateral thyristor Q1 of the type designated "Triac" has one of its main conducting terminals connected to line L1 through a conductor 2 and its other such terminal connected in series with a diode D2, a conductor 3 and load 10 to line L2. With D.C. current applied and line L1 positive, line L2 current will flow continuously from line L1 through switch S, diode D1 and load 10 to line L2. With A.C. applied across lines L1 and L2, the latter path will be conducting on half cycles when L1 is positive with respect to line L2. On the opposite half cycles current will flow from line L2 through load 10, conductor 3, diode D2, triac Q1 and conductor 2 to line L1 whenever Triac Q1 is conducting.

The conduction of Triac Q1 is dependent upon the closure of contacts CR2 of an electromagnetic operated switch CR which in a preferred form is of the sealed reed type. Contacts CR2 are connected at one end through conductor 2 and 4 to line L1 and at the other end in series with resistors R1, R2 and R3, conductor 3 and load 10 to line L2. The gate terminal of Triac Q1 is connected to the point common between resistors R1 and R2. When contacts CR2 are closed, a bias path is provided from conductor 3 through D2 through the cathode to gate of Q1 and then through R1 and CR2 to conductor 4 to provide a bias circuit for Q1

such that it will be rendered conducting only on the half cycles of A.C. current when line L2 is positive with respect to line L1.

A resistor R4 and capacitor C1 are connected in series across conductors 3 and 4 in parallel with the main conducting path of Triac Q1. These provide dv/dt suppression protection to prevent Q1 unwantedly from turning on due to transient voltage having high dv/dt.

A diode D3 is connected through its anode terminal and conductors 2 and 4 to line L1 and through its cathode terminal, and in one branch, in series with the collector-emitter circuit of an N-P-N transistor Q2, resistor R3, conductor 3 and load 10. The cathode of diode D3 is connected in a second branch in series with the collector-emitter circuit of an N-P-N transistor Q3, conductor 3 and load 10 to line L2. Transistor Q2 has its base connected to the point common between the gate terminal of Q1 and resistors R1 and R2, and transistor Q3 has its base connected to the point common between the emitter of Q2 and resistors R2 and R3. It will be apparent that transistors Q2 and Q3 are connected in a Darlington configuration and will both be conducting whenever the contacts CR2 are closed. When the supply voltage is A.C., transistors Q2 and Q3 will only be capable of conducting when line L1 is positive with respect to line L2.

A voltage variable resistor ZNR1 is connected across conductors 3 and 4 to limit the maximum voltage that can be impressed across transistors Q1 and Q3 and its aforescribed biasing circuitry. It thus suppresses transient voltage that might occur because of inductive kick in the load 10 when switch S is opened thereby preventing damage to transistors Q2 or Q3.

From the foregoing it will be apparent that, with A.C. applied across lines L1 and L2 and switch S closed, diode D1 and Triac Q1 will conduct respectively during opposite half cycles and conduct the major portion of the load current. While Q3 will be conducting during the same half cycles, most of the load current will flow through diode D1 due to the lower voltage drop through this path. When D.C. is applied across lines L1 and L2 and the former is positive and the latter negative, current will flow through diode D1 continuously.

Now when switch S is opened, current flow through diode D1 will of course be interrupted. However, as long as contacts CR2 remain closed, current will be conducted continuously by transistor Q3 through load 10 if the supply voltage is D.C., and on half cycles of one polarity of A.C. The Triac Q1 of course will not conduct when the supply voltage is D.C. and when it is A.C. will conduct on the opposite half cycles from that when Q3 conducts.

When contacts CR2 open after a time delay period as will hereinafter be explained in detail, transistors Q2 and Q3 immediately become nonconducting. If the voltage applied across lines L1 and L2 is A.C. and the latter is positive with respect to line L1 upon opening of the switch Triac Q1 will continue conducting until the current through it decreases to zero.

POWER SUPPLY AND REGULATING CIRCUIT

A fixed unidirectional potential is provided for the time delay and indicating circuits by a diode D4 and an N-P-N transistor Q4. Diode D4 is connected at its anode terminal to line L1 and at its cathode terminal in series with a conductor 5, a resistor R5 and the collector-emitter circuit of transistor Q4 to unidirectional

potential bus 6. The base of transistor Q4 is connected in series with a zener diode ZD1 to line L2 and through a resistor R6 to the point common between diode D4 and resistor R5. Diode D4 serves to rectify A.C. voltage when applied across lines L1 and L2. Resistors R5 serves to limit the peak current when supply voltage is first applied across lines L1 and L2, and R6 serves as a base bias resistor.

A diode D5 is connected at its anode terminal in series with switch S to line L1 and at its cathode terminal in series with a conductor 7, a diode D6 and the emitter-collector circuit of a P-N-P transistor Q5 to a conductor 8. Resistor R7 connected between conductor 7 and line L2 causes a current to be supplied through switch S and diode D5 before a voltage potential can be established at the anode of diode D6. The base of transistor Q5 is connected to the point common between voltage divider resistors R8 and R9 which are connected in series across conductor 5 and line L2. Voltage divider resistors R10 and R11 are connected in series across conductor 8 and line L2.

Zener diode ZD1 is selected so that with the supply voltage across lines L1 and L2 in excess of 20 volts, the transistor Q4 will be regulated to provide a unidirectional and constant potential across conductor 6 and line L2 of 15 volts. A capacitor C2 connected across conductor 6 and line L2 to provide filtering of the unidirectional potential thereacross when the supply voltage is A.C. Diode D6 serves to block reverse current through transistor Q5 from resistors R8 to 7 whenever switch S is open.

When voltage is applied across lines L1 and L2 and switch S is closed, transistor Q5 will not turn on unless the potential at the emitter of Q5 is greater than the voltage at the base of Q5 set by voltage divider R8 and R9. If switch S is closed, but has a series resistance, the timer apparatus will turn on if the voltage divider formed by the switch S and the load, shunted by R7, has a lower division ratio than that established by R8 and R9. If switch S is open, but shunted by a leakage resistance, the timer apparatus will not turn on so long as the voltage divider formed by the switch shunt leakage and the load shunted by R7 has a higher division ratio than that established by R8 and R9. Since this apparatus is implemented by the use of voltage divider ratios, it will function properly independent of the absolute value of applied line voltage, L1 to L2, over a wide range, for example, 20V to 120V in the preferred embodiment. While the leakage resistance shunting switch S which will cause the timer apparatus to turn on improperly is dependent on the load driven by the timer apparatus, the worst case value (occurring with no load) is defined by R7 together with the voltage divider ratio established by R8 and R9 and is, for example, 40,000 ohms in the preferred embodiment.

TIME Delay CIRCUITS

The basic timing means affording off delay opening of contacts CR2 is afforded by a capacitor C3, which is charged through an N-P-N transistor Q6, and a discharge circuit comprising a fixed resistor 12 and a variable resistor P. Transistor Q6 has its collector connected to bus 6 and its emitter in series with timing capacitor C3 to line L2. Conductor 8 is connected in series with a resistor R13, diodes D7 and D8 and the emitter-collector circuit of a P-N-P transistor Q7. The base of transistor Q6 is connected to the point common be-

tween diodes D7 and D8, and with 15 volts potential between conductor 8 and line L2, will be biased to turn Q6 on to permit flow of charging current therethrough into timing capacitor C3.

A transistor Q7 has its base connected to the point common between voltage divider resistors R14 and R15, and a resistor R16 is connected to the point common between diodes D7 and D8 and to the point common between timing capacitor C3 and the emitter of transistor Q6. The peak voltage that capacitor C3 will charge to when transistor Q6 is conducting is slightly less as determined by the potential afforded at the base of transistor Q7. The latter potential is of course determined by the resistance values of resistors R14 and R15 and may be adjusted in accordance with the maximum of the timing range desired.

Diode D7 serves to block possible current flow from timing capacitor C3 back through the emitter to base circuit of transistor Q6 and then through R13, R10 and R11. Diode D8 serves to block reverse current flow from conductor 6 through resistor 14 and the base to emitter circuit of transistor Q7 and thus prevents unwanted turn-on of transistor Q6. A capacitor C4 connected between the base of transistor Q6 and line L2 serves to absorb transient voltages that might otherwise turn on Q6 and thereby charge timing capacitor C3 even though switch S is open.

The point common between the emitter of Q6, resistor R16, capacitor C3 and resistor R12 is connected to the base of P-N-P transistor Q8. The emitter of Q8 is connected to the cathode of a diode D9 which has its anode connected in series with a resistor R17 to bus 6. The collector of Q8 is connected directly to line L2. When timing capacitor C3 is charged to peak voltage which occurs almost immediately following closure of switch S, transistor Q8 will be biased to its nonconducting state.

Now let it be assumed that switch S is opened following charging of timing capacitor C3 to its peak voltage. Immediately transistor Q6 is rendered nonconducting preventing further charging current flow into capacitor C3. The latter then discharges through resistor R12 and P. At the end of the desired timing interval, as determined by the setting of resistor P, the potential on the base of transistor Q8 decreases to a value rendering the latter conducting.

When transistor Q8 is made nonconducting, it in turn renders an N-P-N transistor Q9 and a P-N-P transistor Q10 conducting, and the latter in turn energizes the electromagnetic winding CR1 of relay CR1. Transistor Q9 has its collector connected in series with voltage divider resistors R18 and R19 to bus 6, and its emitter is connected in series with a zener diode ZD2 to line L2 and also in series with a resistor R20 to bus 6. The base of Q9 is connected to the point common between resistor R17 and diode D9. Transistor Q10 has its emitter connected to bus 6, its collector to the upper end of winding CR1, and its base to the point common between resistors R18 and R19.

It will be observed that with Q8 rendered nonconducting (switch S closed), the base of Q9 will be biased sufficiently above zener ZD2 voltage for base current to flow into Q9, thereby causing Q9 to turn on. When Q9 turns on, the potential at the base of Q10 will bias Q10 on thereby causing current flow through Q10 and winding CR1. When Q8 again becomes conducting, which occurs as aforescribed at the end of the de-

sired time delay period, transistors Q9 and Q10 of course turn off to deenergize winding CR1.

INDICATING CIRCUITS

The lower end of winding CR1 of relay CR is connected in series with a light emitting diode LED to line L2. Whenever transistor Q10 is conducting, current flows therethrough and winding CR1 and diode LED to line L2. With switch S closed, diode LED will illuminate steadily to indicate that the relay is in its closed steady state condition.

A programmable unijunction transistor Q11, popularly called a "PUT," and a capacitor C5 are connected in circuit with diode LED to cause the latter to intermittently illuminate or "blink" during the aforementioned time delay discharge of timing capacitor C3 to afford an indication that the relay is then in its timing operating mode.

PUT Q11 has its gate terminal connected in series with a resistor 21, and also in series with a diode D10 parallel to resistor 21, to the point common between winding CR1 and diode LED. The anode terminal of Q11 is connected in series with resistors R22 and R23 to bus 6. The capacitor C5 is connected at its upper terminal to the point common between resistors R22 and R23 and is connected at its lower terminal to line L2. An N-P-N transistor Q12 has its collector connected to the point common between resistors R22 and R23 and capacitor C5, and its emitter is connected to line 12. The base of Q12 is connected through a conductor 9 to the point common between voltage divider resistors R10 and R11.

With switch S closed, transistor Q12 will be biased to its conducting state thereby effectively connecting the upper terminal of C5 and the anode of PUT Q11 to the potential of line L2. Consequently, capacitor C5 cannot charge and PUT Q11 is prevented from conducting. Thus, when switch S is closed and winding CR1 is energized, all current flowing through the latter flows through the diode LED continuously and its illumination is corresponding continuous. When switch S is opened, the bias on the base of Q12 is reduced to essentially the potential of line L2 and it turns off. Charging current will then flow from bus 6 and resistor R23 into capacitor C5. When capacitor C5 charges up the potential at the anode of PUT Q11 correspondingly increases, and when this potential exceeds the potential at the gate terminal of Q11, turns on discharging capacitor C5 through resistor R22 and its anode-cathode circuit. Turn on of Q11 also shunts current flowing through winding CR1 through diode D10 and resistor 21 and the gate-cathode circuit of Q11 to line L2 and thus away from diode LED. During such shunt-away of current from diode LED, the latter extinguishes.

Now as capacitor C5 discharges the current flow into anode of PUT Q11 finally decreases below the "valley" current value, and Q11 then becomes nonconducting, and current then again flows through diode LED to effect illumination of the latter. Thereafter capacitor C5 recharges then discharges to cause turn on of Q11 and extinguishes of diode LED again. This cycle repeats and continues as long as transistor Q10 remains conducting. The blink rate and off periods of diode LED will be determined by the value of capacitor C5 and resistors R22 and R23 and the voltage across LED. Of course when transistors Q9 and Q10 turn off at the end of the timed interval, current flow through winding

CR1 and diode LED ceases and the latter is then in a continuously dark or non-illuminated state to indicate that the timing relay is in its "off" state.

We claim:

1. In an apparatus for energizing a load from sources of A.C. or D.C. voltage supply, and having an OFF time delay deenergizing mode upon re-opening of a control switch, the combination comprising:
 - a. a selectively operable switch for connection to a voltage supply source
 - b. a unidirectional conducting device in circuit with said switch and connectable to a load for supplying the same whenever said switch is closed with D.C. current or half waves of A.C. current of one polarity according to the type of current provided by the voltage supply source
 - c. semiconductor means for connection to the voltage supply source and the load and having control means energizable to provide the same current conduction modes to the load as said unidirectional conducting device
 - d. second semiconductor means for connection to the voltage supply source and having control means energizable to provide half waves of A.C. current flow of opposite polarity when the source of voltage is A.C.
 - e. means including a electromagnetic switch having a control winding which when energized effects closure of contacts to render the first mentioned semiconductor means effective when said supply voltage is D.C. and both of said semiconductor means effective when the supply voltage is A.C.
 - f. means which when connected to an A.C. and D.C. supply source affords a source of unidirectional potential
 - g. means for energizing the control winding of said electromagnetic switch upon closure of said selectively operable switch and for deenergizing said control winding after a time delay period upon re-opening of the latter switch comprising:
 - h. transistor means in circuit with said source of unidirectional potential and said control winding and being controllable to energize and deenergize said control winding
 - i. control means for said transistor means in circuit with said selectively operable switch and said source of unidirectional potential comprising:
 - j. time delay means including capacitor means quickly chargeable to a given level upon closure of said selectively operable switch to render said transistor means operable to correspondingly energize said control winding and further including an adjustable resistance discharge path which is rendered effective upon reopening of said selectively operable switch to discharge said capacitor means during a time delay period to another level which causes said transistor means to deenergize said control winding.
2. The combination according to claim 1 together with luminous indicating means in circuit with said control winding and said source of unidirectional current and affording luminous indication of the energized state of said control winding whenever said selectively operable switch is closed, and together with means which operates upon reopening of said selectively operable switch to cyclically shunt the current flowing through said control winding around said indicating

means to afford corresponding cyclic off-and-on energization of said indicating means during the aforementioned time delay period.

3. The combination according to claim 2 wherein said luminous indicating means is a light emitting diode, and wherein the last specified means comprises a programmable unijunction transistor having its gate-cathode circuit connected in shunt across said light emitting diode, a capacitor connected in shunt across the anode-cathode circuit of said programmable unijunction transistor and an N-P-N transistor having its collector-emitter circuit connected in parallel with the last mentioned capacitor and its base connected in circuit to render such transistor conducting whenever said selectively operable switch is closed.

4. The combination according to claim 1 wherein said first mentioned semiconductor means comprises N-P-N transistor connected as Darlington pair with their collector-emitter circuits connected across the supply voltage with the connected load and having either bases connected in circuit with the contacts of said electromagnetic switch to render their transistors conducting whenever the contacts of such switch are closed.

5. The combination according to claim 4 wherein said second semiconductor means comprises a diode and a bilateral thyristor having its main conducting path connected in circuit with said diode and the load across said supply voltage and its control electrode connected in circuit with said contacts of said electromagnetic switch, said thyristor being rendered conducting whenever said supply voltage is A.C. and said last mentioned contacts are closed to provide half-waves of current flow of said opposite polarity to the load.

6. The combination according to claim 1 wherein said means when connected to an A.C. or D.C. supply source affords a source of unidirectional potential comprises a diode and N-P-N transistor having its collector-emitter circuit connected in series with said diode in one line of the voltage supply, and a zener diode connected between the base of the last mentioned transistor and another line of said supply source.

7. The combination according to claim 1 together with leaky switch detector means comprising a diode, a voltage divider connected across the supply source, and a P-N-P transistor having its emitter-collector circuit connected in series with said diode between said selectively operable switch and said control means.

8. The combination according to claim 2 wherein said transistor means comprises a P-N-P transistor having its emitter-collector circuit connected in series with the control winding of said electromagnetic switch and said indicating means across said unidirectional potential source, a pair of series connected resistors, a zener diode, an N-P-N transistor having its collector-emitter circuit connected in series with said resistors and said zener diode across said unidirectional potential source, a third resistor, and a P-N-P transistor having its emitter-collector circuit connected in series across said unidirectional source, with said third resistor, said first mentioned P-N-P transistor having its base connected to the point common between said series connected resistors and said N-P-N transistor having its base connected to the point between said third resistor and the last specified P-N-P transistor.

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9. The combination according to claim 8 wherein said last specified P-N-P transistor has its base connected in circuit with said selectively operable switch, said capacitor means, and said resistance discharge path and responds to charge of said capacitor means to said given level to be rendered nonconducting to in turn render said N-P-N transistor and said first mentioned P-N-P transistor conducting, said last specified P-N-P transistor upon opening of said selectively operable switch and discharge of said capacitor to said other level being rendered conducting to in turn render said N-P-N transistor and said first mentioned transis-

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tor nonconducting.

10. The combination according to claim 1 wherein the specified elements and means are so arranged that the selectively operable switch will have direct connections to the high potential or hot side of D.C. or A.C. supply sources respectively and so that the controlled load will be connected between the low or neutral sides of D.C. or A.C. supply sources respectively and said unidirectional conducting device and said first mentioned and second semiconductor means.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,784,881 Dated January 8, 1974

Inventor(s) Lawrence E. Van Horn, William H. Elliot,
Russell P. Schuchmann & Herman P. Schutten

It is certified that error appears in the above-identified patent
and that said Letters Patent are hereby corrected as shown below:

Inventors

Add the name of -- Herman P. Schutten,
Elm Grove, Wisconsin --

Column 2, line 62, "12" should be -- L2 --.

Column 6, line 29, "12" should be -- L2 --.

Signed and sealed this 3rd day of December 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

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