



US005841695A

United States Patent [19]

[11] **Patent Number:** **5,841,695**

Wik

[45] **Date of Patent:** **Nov. 24, 1998**

[54] **MEMORY SYSTEM USING MULTIPLE STORAGE MECHANISMS TO ENABLE STORAGE AND RETRIEVAL OF MORE THAN TWO STATES IN A MEMORY CELL**

[57] **ABSTRACT**

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A memory circuit which uses multiple storage mechanisms in each of its memory cells. In one embodiment, the memory circuit comprises a memory cell array and a data sense module. Each cell of the array includes a first, second and third transistors, and a capacitance. The first transistor has a first gate coupled to a first word line, a floating gate which stores a first charge, a first source coupled to a first data line, and a first drain. The second transistor has a second gate coupled to the first drain, a second source coupled to a second word line, and a second drain. The third transistor has a third gate coupled to a third word line, a third source coupled to the second drain, and a third drain coupled to a second data line. The capacitance is coupled between ground and the third source. The capacitance stores a second charge when the second word line is asserted and the third word line is de-asserted. The second gate stores a third charge when the first word line is de-asserted. The data sense module is coupled to the first and second data lines, and configured to sense the second charge if the third word line is asserted while the second word line is asserted. The data sense module is further configured to sense the third charge by detecting a current through the second transistor if the second word line is de-asserted while the third word line is asserted. The data sense module is still further configured to detect the first charge by storing a fourth charge on said second gate if the first word line is asserted while the first data line is de-asserted, the first data line is then asserted, and the first word line is then de-asserted at a predetermined time period after the assertion of the first data line. The fourth charge is then sensed by detecting a current through the second transistor if the second word line is de-asserted while the third word line is asserted. The data sense module determines the state represented by the stored charge quantities. Since additional logic states may be used to represent additional information bits, this memory circuit increases the number of bits that may be stored per memory cell, thereby increasing the storage density and reducing the cost per bit.

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[21] Appl. No.: **865,470**

[22] Filed: **May 29, 1997**

[51] **Int. Cl.**⁶ **G11C 16/02**; G11C 11/56

[52] **U.S. Cl.** **365/185.08**; 365/149; 365/168; 365/185.03

[58] **Field of Search** 365/149, 150, 365/45, 168, 185.03, 185.21, 185.08

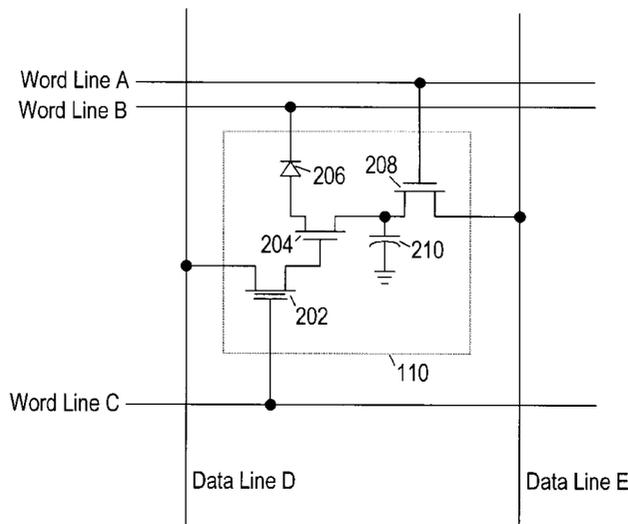
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20 Claims, 3 Drawing Sheets



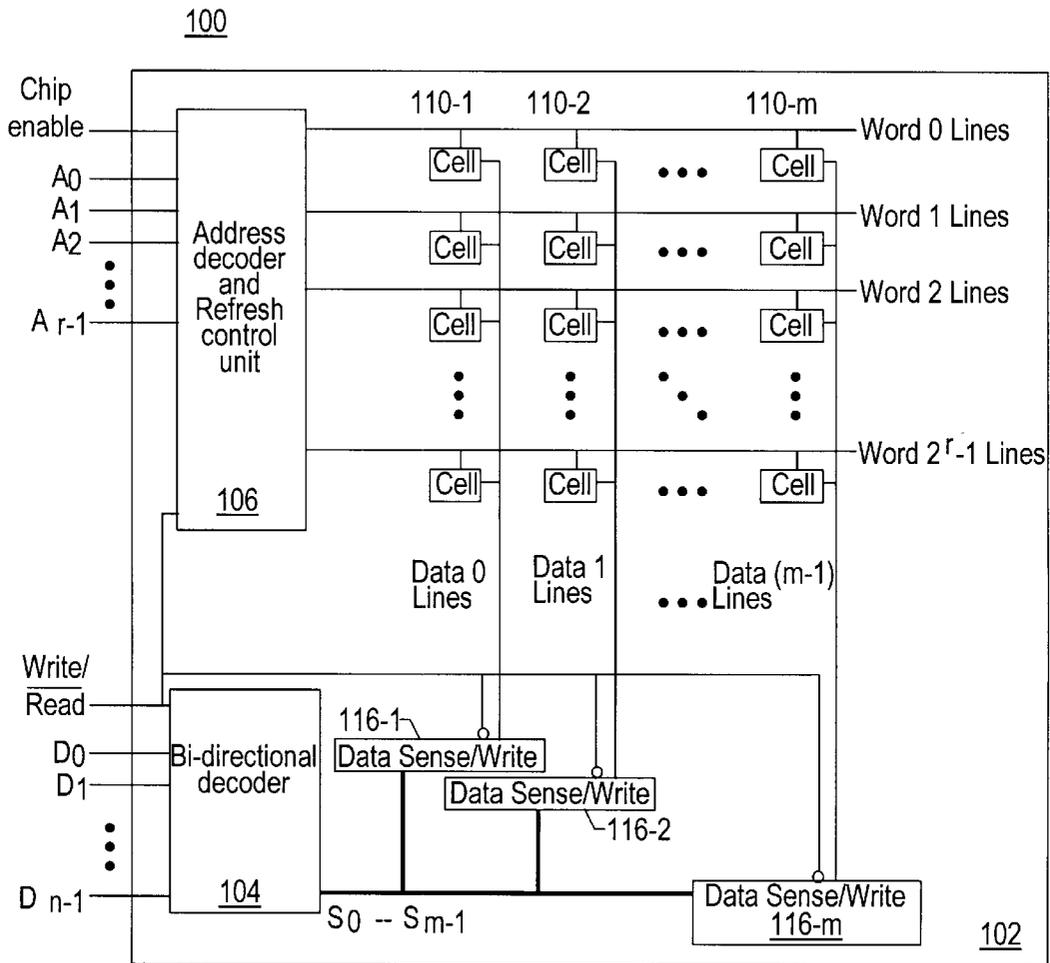


FIG. 1

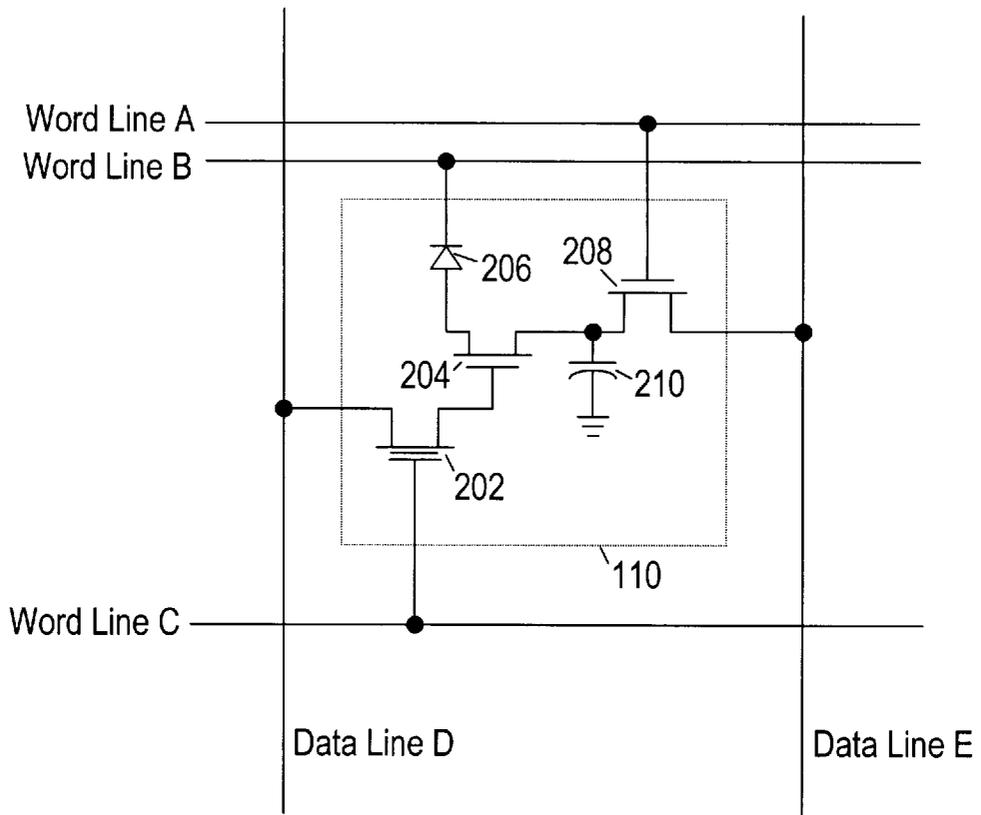


FIG. 2

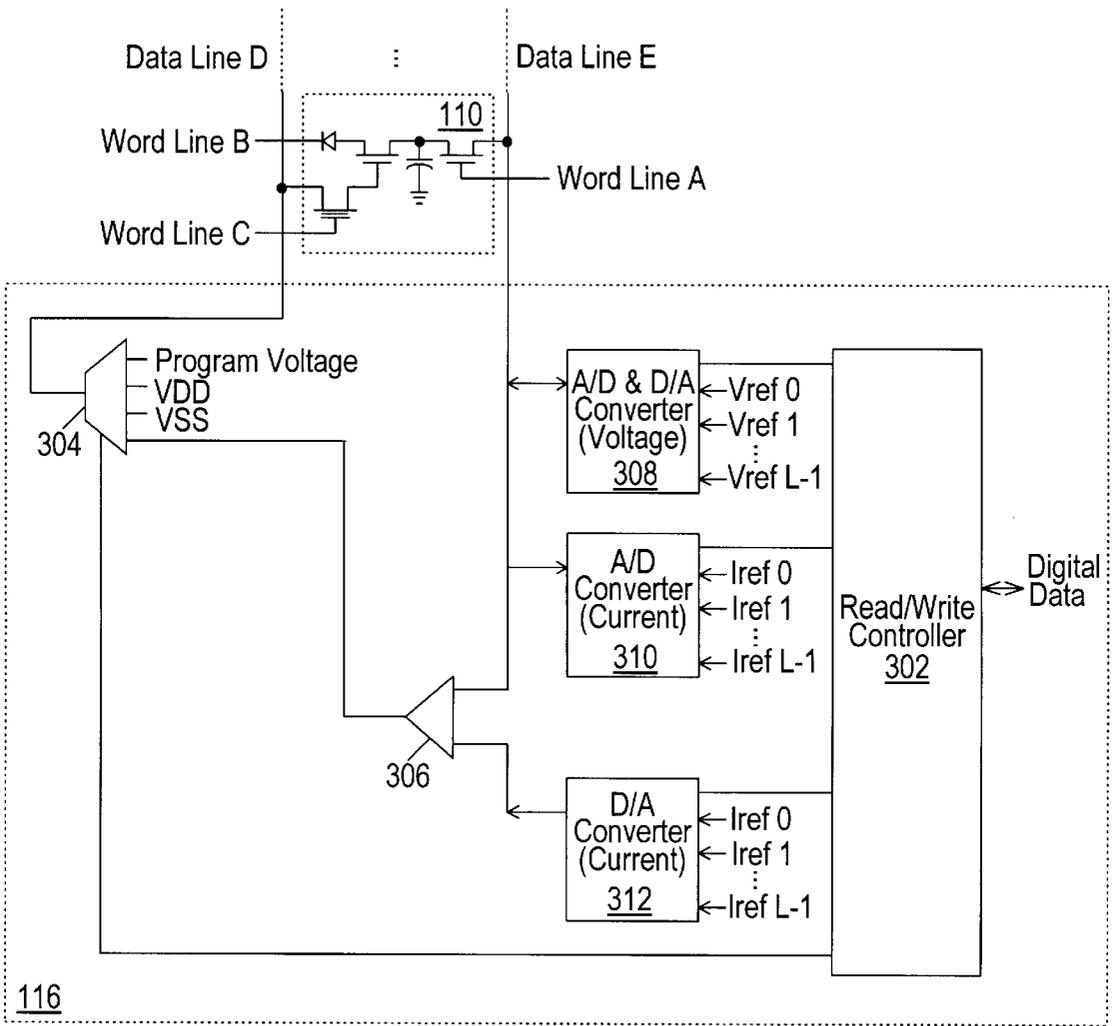


FIG. 3

MEMORY SYSTEM USING MULTIPLE STORAGE MECHANISMS TO ENABLE STORAGE AND RETRIEVAL OF MORE THAN TWO STATES IN A MEMORY CELL

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of solid state devices for information storage, and in particular to a method and structure for storing multilevel logic values in a dynamic random access memory (DRAM).

2. Description of the Related Art

Memory devices store and retrieve large quantities of digital data at electronic speeds. Early digital computers used magnetic cores as the devices in fast-access memories. With the introduction of semiconductor memory chips in the late 1960s, magnetic cores began to be replaced by integrated circuits which implement a much higher-density memory function. This not only increased the performance capabilities of the memory, but also drastically decreased its cost. By the end of the 1970s, magnetic core memories had been completely displaced as high-speed memory devices.

Memory capacities in digital systems are commonly expressed in terms of bits (binary digits), since a separate device or circuit is used to store each bit of data. Each storage element is referred to as a cell. Memory capacities are also sometimes stated in terms of bytes (8 or 9 bits) or words (arbitrarily defined, but commonly 16–80 bits). Every bit, byte, or word is stored in a particular location, identified by a unique numeric address. Only a single bit, byte, or word is stored or retrieved during each cycle of memory operation.

The units of memory storage capacity are typically kilobits and megabits (or kilobytes and megabytes). Since memory addressing is based on binary codes, capacities that are integral powers of 2 are typically used. As a result, a memory device with a 1-kbit capacity can actually store 1024 bits, and a 64-kbyte device can store 65,536 bytes.

In digital computers, the number of memory bits is usually 100 to 1000 times greater than the number of logic gates, which implies that the memory cost per bit must be kept very low. In addition, it is desirable for the memory devices to be as small as possible (since this will allow the highest density of cells on a chip), to operate at a high speed, to have a small power consumption, and to operate reliably. To achieve this end, memory cells are designed to be as simple and compact as possible. Typically, the cell itself is not capable of outputting digital data in an electrical form compatible with the requirements of the remainder of the system. To restore the electrical characteristics of the cell's outputted data to adequate values, properly designed peripheral circuits (e.g. sense amplifiers, memory registers, and output drivers) are necessary. These circuits are designed to be shared by many memory cells. The trade-off thus made is that of a less robust output signal from the cell, in exchange for a simple, compact memory cell design.

The most flexible digital memories are those that allow for data storage (hereafter, writing) as well as data retrieval (hereafter, reading). Memories in which both of these functions can be rapidly and easily performed, and whose cells can be accessed in random order (independent of their physical locations), are referred to as random-access memories (RAMs). Read-only memories (ROMs) are those in which only the read operation can be performed rapidly. Entering data into a ROM is referred to as programming the

ROM. This operation is much slower than the writing operation used in RAMs.

The storage cells in a typical semiconductor memory are arranged in an array consisting of horizontal rows and vertical columns. Each cell shares electrical connections with all the other cells in its row, and column. The horizontal lines connected to all the cells in the row are called word lines, and the vertical lines (along which data flows into and out of the cells) are referred to as data lines. Each cell therefore has a unique memory location, or address, which can be accessed at random through the selection of the appropriate word and data line. Some memories are designed so that all the cells in a row are accessed simultaneously. This array configuration of semiconductor memories lends itself well to the regular structured designs which are favored in VLSI.

There are a number of important circuits on the periphery of the array. One such peripheral circuit is the address decoder. This circuit allows a large number of word and data lines to be accessed with the fewest number of address lines. Address decoders for this purpose have 2^n output lines, with a different one selected for each different n-bit input code. In later generations of memory circuits, address multiplexing was integrated on some memory chips to reduce the number of address pins by half.

Another peripheral circuit is the read/write control circuitry. This circuitry determines whether data is to be written into or read from the memory. Because such circuits also amplify and buffer the data signals retrieved from the cells, one of the important circuits in this subsystem is the sense amplifier. In dynamic memories that need periodic data refreshing, refresh circuitry may also be provided.

Recently, additional peripheral circuits have been added to the basic memory organization structure. These circuits serve mainly to improve the manufacturability and testability of the chips. Those designed to increase manufacturability include redundancy circuits and error-correction circuits. Redundancy circuits allow some defective chips to be salvaged, while self-testing circuits reduce testing time. Error-detection and correction techniques involve the addition of parity bits to allow the system to detect bad data, accomplish parity checking, and in some cases provide correction of the data errors.

Most RAMs have only one input-data lead and one output-data lead (or a single combined input/output lead). Writing into and reading from such RAMs is done one bit at a time. Other RAMs have a number of input- and output-data leads, with the number determined by the word length of the system's data bus. ROMs, on the other hand, are typically organized so that the number of output-data leads is the same as the number of lines on the data bus. ROMs are programmed word by word and are read from in the same manner.

In semiconductor RAMs, information is stored on each cell either through the charging of a capacitor or the setting of the state of a bi-stable flip-flop circuit. With either method, the information on the cell is destroyed if the power is interrupted. Such memories are therefore referred to as volatile memories. When the charge on a capacitor is used to store data in a semiconductor-RAM cell, the charge needs to be periodically refreshed, since leakage currents will remove it in a few milliseconds. Hence, volatile memories based on this storage mechanism are known as dynamic RAMs, or DRAMs.

If the data is stored (written) by setting the state of a flip-flop, it will be retained as long as power is connected to

the cell (and flip-flop is not reset by another write signal). RAMs fabricated with such cells are known as static RAMs, or SRAMs. Volatile RAMs can be treated as non-volatile if they are provided with a battery backup. Some DRAM and SRAM chips are even packaged together with a battery to facilitate implementation of this approach.

It is often desirable to use memory devices that will retain information even when the power is interrupted. Magnetic media offer such nonvolatile-memory storage. In addition, a variety of semiconductor memories have been developed with this characteristic. At present, virtually all such non-volatile memories are ROMs. While data can be entered into these memories, the programming procedure varies from one type of ROM to the other.

The first group of nonvolatile memories consists of those ROMs in which data is entered during manufacturing, and cannot be subsequently altered by the user. These devices are known as masked ROMs (or simply ROMs). The next category consists of memories whose data can be entered by the user (user-programmable ROMs). In the first example of this type, known as a programmable ROM, or PROM, data can be entered into the device only once. In the remaining ROM types, data can be erased as well as entered. In one class of erasable ROMs, the cells must be exposed to a strong ultraviolet light in order for the data to be erased. These ROMs are called erasable-programmable ROMs, or EPROMs. In the final type, data can be electrically erased as well as entered into the device; these are referred to as EEPROMs. The time needed to enter data into both EPROMs and EEPROMs is much longer than the time required for the write operation in a RAM. As a result, none of the ROM types can at present be classified as fully functional RAM devices.

Many variations on the basic memory organization architecture have been developed, including video RAMs and multiport RAMs. Architectures which combine memory and logic circuits on the same chip are becoming increasingly popular. However, the primary trends in semiconductor memory development are to increase the storage density and to reduce the cost per bit. It would therefore be desirable to have a method and structure for further increasing the bit storage density and reducing the cost per bit.

SUMMARY OF THE INVENTION

The problems outlined above are in large part solved by a memory circuit which uses multiple storage mechanisms in each of its memory cells. In one embodiment, the memory circuit comprises a memory cell array and a data sense module. The memory cell array has a first, second, and third word lines for each row of the array, and a first and second data lines for each column of the array. Each cell is coupled to the word and data lines of the associated row and column. Each cell includes a first, second and third transistors, and a capacitance. The first transistor has a first gate coupled to the first word line, a floating gate with a first stored charge, a first source coupled to the first data line, and a first drain. The second transistor has a second gate coupled to the first drain, a second source coupled to the second word line, and a second drain. The third transistor has a third gate coupled to the third word line, a third source coupled to the second drain, and a third drain coupled to the second data line. The capacitance is coupled between ground and the third source. The capacitance has a second stored charge when the second word line is asserted and the third word line is de-asserted. The second gate has a third stored charge when the first word line is de-asserted.

The data sense module is coupled to the first and second data lines, and configured to sense the second charge if the third word line is asserted while the second word line is asserted. The data sense module is further configured to sense the third charge by detecting a current through the second transistor if the second word line is de-asserted while the third word line is asserted. The data sense module is still further configured to detect the first charge by storing a fourth charge on said second gate if the first word line is asserted while the first data line is de-asserted, the first data line is then asserted, and the first word line is then de-asserted at a predetermined time period after the assertion of the first data line. The fourth charge is then sensed by detecting a current through the second transistor if the second word line is de-asserted while the third word line is asserted. The data sense module determines the state represented by the stored charge quantities. Since additional logic states may be used to represent additional information bits, this memory circuit increases the number of bits that may be stored per memory cell, thereby increasing the storage density and reducing the cost per bit.

Broadly speaking, the present invention contemplates a memory cell which uses multiple storage mechanisms. The memory cell comprises a first, second and third transistors, and a capacitance. The first transistor has a first gate, a floating gate, a first source, and a first drain. The floating gate stores a first charge. The first gate is coupled to a first word line, and the first source is coupled to a first data line. The second transistor has a second gate, a second source, and a second drain. The second gate is coupled to the first drain, and the second source is coupled to a second word line. The third transistor has a third gate, a third source, and a third drain. The third gate is coupled to a third word line, the third source is coupled to the second drain, and the third drain is coupled to a second data line. The capacitance is coupled between a predetermined potential and the third source. The memory cell may further comprise a diode coupled between the second source and the second word line to block current flow if the second word line has a higher potential than the second source.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

FIG. 1 is a block diagram of a semiconductor memory architecture using multiple storage mechanisms according to the present invention;

FIG. 2 is a block diagram illustrating the function of a memory cell according to present invention; and

FIG. 3 is a block diagram illustrating an embodiment of the data sense/write module.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows an exemplary memory architecture using memory cells with multiple storage mechanisms. In this

embodiment, memory **100** has a ground plane **102** surrounding the chip circuitry which shields the circuitry from electromagnetic noise. Memory **100** receives a chip enable signal, a read/write signal, and r address bit signals at an address decoder and refresh unit **106**. During operation when the chip enable signal is asserted with the read/write signal indicating a read, address decoder and refresh unit **106** controls the word lines associated with one of 2^r rows of memory cells. When the word lines are controlled in a manner which is described further below, the corresponding row of memory cells may be read and refreshed. In a similar fashion, the corresponding row of memory cells may be written to.

Memory **100** also has n bi-directional binary data lines (D_0 - D_{n-1}) connected to a bi-directional decoder **104**. Bi-directional decoder **104** is coupled to receive the read/write signal and is further coupled to m data paths which carry multi-value logic signals (S_0 - S_{m-1}). Each of the data paths can be driven by either bi-directional decoder **104** or one of a set of data sense/write modules **116-1** through **116-m** (referred to collectively as modules **116**). Each of the modules **116** is coupled to a pair of data lines. Each pair of data lines is coupled to a column of the memory cells.

An exemplary memory read operation is now described. Consider a situation in which the address bits are all zero, the write/read control line indicates a read operation, and the chip enable signal is asserted. Upon occurrence of this situation, address decoder and refresh unit **106** manipulates the word lines for word **0** (i.e. "Word 0 Lines"). This allows modules **116** to sense charges stored in cells **110-1** through **110-m** via the data lines. Subsequent to the sense operation, modules **116** convert the sensed charges into m multi-value logic signals (S_0 - S_{m-1}) which are coupled to bi-directional decoder **104**. Bi-directional decoder **104** converts the m multi-value logic signals (S_0 - S_{m-1}) to n binary digital signals, and drives the n bits on data lines D_0 - D_{n-1} . In this manner, a multi-value logic state stored in each cell may be read.

In one specific implementation, the cells being read are refreshed concurrent with the read operation. For the implementation of FIG. 1, modules **116** convert the m multi-value logic signals (S_0 - S_{m-1}) into multi-level voltage signals and drive them on the data lines which are coupled to cells **110**. If at this time the word 0 lines are manipulated as described further below, cells **110** store the multi-level voltage signals. In this way, the content of cells **110** can be refreshed every time they are read.

The effectuation of memory write operations is similar. For example, if the address bits are all zero and the write/read control line indicates a write operation when the chip enable signal is asserted, then address decoder and refresh unit **106** manipulates the word 0 lines. Bi-directional decoder **104** receives data from the bi-directional binary data lines D_0 - D_{n-1} and converts the data into m multi-value logic signals which are driven onto the m data paths. The modules **116** convert the input m multi-value logic signals into multi-level voltage signals and drive the data lines coupled to the selected cells **110**. Having the word 0 lines manipulated as described further below causes the multi-level signals to be stored in cells **110**.

Address decoder and refresh unit **106** further includes refresh circuitry to read and refresh the contents of each memory cell within a given time interval. The refresh cycles can be implemented in many ways, one of which is to have them happening continuously while the chip is not enabled. In this implementation method, bi-directional decoder **104** is

disabled and the modules **116** are enabled during refresh cycles. Address decoder and refresh unit **106** may employ a counter which sequentially manipulates each group of word lines, causing a read and refresh operation similar to that described previously. In order to assure that each memory cell is refreshed, the chip must spend a specified fraction of a given time interval in the disabled mode.

Turning now to FIG. 2, portions of memory circuit **100** are shown in greater detail. Circuit portions that correspond to those of FIG. 1 are numbered identically for simplicity and clarity. FIG. 2 illustrates a memory cell **110** which is exemplary of each of the cells of FIG. 1. Memory cell **110** includes a floating gate transistor **202**, a storage transistor **204**, a read transistor **208**, and a capacitance **210**. The preferred embodiment also includes a diode **206**. Memory cell **110** is coupled to word lines A, B, and C, and to data lines D and E. When word lines A and C are low and word line B is high (or high impedance), memory cell **110** is in the storage mode. A first charge may be stored on the floating gate of transistor **202**, a second charge may be stored on the gate of transistor **204**, and a third charge may be stored on capacitance **210**.

The process of sensing the three stored charges begins by driving word line A high, thereby causing transistor **208** to conduct, and consequently allowing the third charge on capacitance **210** to be sensed by module **116** via data line E. After the third charge has been sensed, word line B is driven low, thereby allowing diode **206** (if present) to conduct, and consequently allowing the conductivity of transistor **204** to be sensed by module **116** via data line E. Since the conductivity of transistor **204** is determined by the stored second charge, module **116** is able to determine the second charge.

Subsequent to the determination of the second charge, word line C is driven high while data line D is driven low, thereby causing transistor **202** to conduct, and consequently discharging the gate of transistor **204**. The conductivity of transistor **202** is dependent on the stored first charge on the floating gate. To determine this first charge, data line D is driven high and allowed to charge the gate of transistor **204** for a fixed time interval. The end of this interval may be marked by driving word line C low, thereby causing transistor **202** to stop conducting. This results in a fourth charge being stored on the gate of transistor **204**. The fourth charge is directly related to the size of the first charge, and may be sensed in the same fashion as the second charge, i.e. by measuring the conductivity of transistor **204** via data line E. In this fashion, module **116** is able to sense the first, second and third charges stored in memory cell **110**.

Module **116** determines a digital representation of the sensed first, second and third charges, and for a read operation, module **116** drives a multilevel digital signal representation of the sensed values to bi-directional decoder **104**. After each read operation, and during refresh operations, the second and third charges must be re-stored in memory cell **110**. To achieve this, word lines A and C are driven high while word line B is driven low, and module **116** drives a voltage on data line D while measuring the conductivity of transistor **204** via data line E. The voltage level on data line D is adjusted until the desired second charge quantity is stored on the gate of transistor **204** (as determined by the measured conductivity). Word line C is then driven low and word line B is driven high. Module **116** then charges capacitance **210** to the potential necessary to store the desired third charge on capacitance **210**, after which word line A is driven low. Thus memory cell **110** has been returned to the storage mode with the second and third charges refreshed.

The process of writing the three stored charges begins with the storage of the first charge. Word line C is driven to a high voltage and data line D is driven low to create a high electric field across a tunneling oxide in transistor 202. This causes the floating gate to become negatively charged. Once an equilibrium has been reached, word line C is driven low and data line D is driven to a high voltage to reverse the electric field across the tunneling oxide for a predetermined amount of time. This allows the charge on the floating gate to be discharged the amount necessary to leave the desired charge quantity on the floating gate. The storage of the second and third charges may then occur as described above. Specifically, word lines A and C are driven high while word line B is driven low, and module 116 drives a voltage on data line D while measuring the conductivity of transistor 204 via data line E. The voltage level on data line D is adjusted until the desired second charge quantity is stored on the gate of transistor 204 (as determined by the measured conductivity). Word line C is then driven low and word line B is driven high. Module 116 then charges capacitance 210 to the potential necessary to store the desired third charge on capacitance 210, after which word line A is driven low. Thus memory cell 110 has been placed in storage mode with the desired first, second and third charges.

Turning now to FIG. 3, one embodiment of module 116 is illustrated. Module 116 includes a read/write controller 302, a data line multiplexer 304, a feedback circuit 306, a bi-directional analog to digital (A/D) and digital to analog (D/A) converter 308, and an A/D converter 310, and a D/A converter 312. During a read cycle, word line A is driven high to allow bi-directional converter 308 to sense the charge on capacitor 210. Bi-directional converter 308 receives reference voltages V_{ref_0} – $V_{ref_{L-1}}$ to determine a digital representation of the logic state represented by the charge on capacitance 210. In this embodiment, L possible logic states are allowed. The digital representation is sent to Read/Write controller 302. Word line B is then driven low to allow the A/D converter 310 to sense the current through transistor 204. A/D converter 310 receives reference currents I_{ref_0} – $I_{ref_{L-1}}$ to determine a digital representation of the logic state represented by the charge on the gate of transistor 204. In this embodiment, L possible logic states are allowed, although a different number may also be realized. The digital representation is sent to Read/Write controller 302. Read/Write controller 302 then drives data line D low by switching multiplexer 304 to V_{ss} while word line C driven high. This is followed by Read/Write controller 302 driving data line D high with multiplexer 304 switched to V_{DD} for a fixed amount of time before word line C is driven low. This causes the charge on the gate of transistor 204 to be discharged and replaced by a charge determined by the charge on the floating gate of transistor 202. A/D converter 310 then re-determines the digital representation of the charge on the gate of transistor 204 and sends the determination to Read/Write controller 302. Each of the digital representations are latched and an overall logical state for memory cell 110 is determined and output to bi-directional decoder 104.

During a write cycle, Read/Write controller 302 receives an overall logical state for memory cell 110. This overall logical state is decomposed into desired first, second, and third charges for the floating gate of transistor 202, the gate of transistor 204, and capacitance 210. When word line C is driven to a high programming voltage, Read/Write controller 302 uses multiplexer 304 to drive data line D low (V_{ss}) to allow a negative charge to accumulate on the floating gate. Word line C is then driven low while Read/Write controller

302 switches multiplexer 304 to the program voltage for an amount of time necessary to cause the charge on the floating gate to equal the desired first charge. Word lines A and C are then driven high with word line B driven low. Read/Write controller 302 switches multiplexer 304 to the output signal from feedback circuit 306. The D/A converter 312 sets a desired current, and feedback circuit 306 begins charging the gate of transistor 204 until the desired second charge is reached. Word line C is driven low and word line B is driven high. Bi-directional converter 308 then charges capacitance 210 to the desired third charge, and word line A is driven low.

Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. For example, the channel conductivities which represent the multi-level logic states may be chosen to maximize the detection margin, or be adjustable to permit a range of refresh time to be used. It is intended that the following claims be interpreted to embrace all such variations and modifications.

What is claimed is:

1. A memory cell which uses multiple storage mechanisms, wherein said memory cell comprises:

a first transistor having a first gate, a floating gate, a first source, and a first drain, wherein said first gate is coupled to a first word line, wherein said floating gate is configured to store a first charge, and wherein said first source is coupled to a first data line;

a second transistor having a second gate, a second source, and a second drain, wherein said second gate is coupled to said first drain, and wherein said second source is coupled to a second word line;

a third transistor having a third gate, a third source, and a third drain, wherein said third gate is coupled to a third word line, wherein said third source is coupled to said second drain, and wherein said third drain is coupled to a second data line; and

a capacitance coupled between a predetermined potential and said third source.

2. The memory cell of claim 1, further comprising:

a diode coupled between said second source and said second word line, wherein said diode is oriented to block current flow if said second word line has a higher potential than said second source.

3. The memory cell of claim 1, wherein said capacitance is configured to store a second charge if said third word line is de-asserted and while said second word line is asserted.

4. The memory cell of claim 3, wherein said second gate is configured to store a third charge if said first word line is de-asserted.

5. The memory cell of claim 4, wherein said second gate is configured to store a fourth charge if said first word line is asserted while said first data line is de-asserted, said first data line is then asserted, and said first word line is then de-asserted at a predetermined time interval after said assertion of the first data line.

6. The memory cell of claim 4, wherein said second charge is sensed via said second data line if said third word line is asserted while said second word line is asserted.

7. The memory cell of claim 4, wherein said third charge is sensed by detecting a current through said second transistor if said second word line is de-asserted while said third word line is asserted.

8. The memory cell of claim 5, wherein said first charge is sensed by sensing said fourth charge, wherein said fourth charge is sensed by detecting a current through said second

transistor if said second word line is de-asserted while said third word line is asserted.

9. A memory circuit comprising:

a memory cell array having a first word line, a second word line, a third word line for each row of the array, and a first data line and a second data line for each column of the array, wherein each cell of the array has an associated row and column and includes:

a first transistor having a first gate, a floating gate, a first source, and a first drain, wherein said first gate is coupled to said first word line, wherein said floating gate is configured to store a first charge, and wherein said first source is coupled to said first data line;

a second transistor having a second gate, a second source, and a second drain, wherein said second gate is coupled to said first drain, and wherein said second source is coupled to said second word line;

a third transistor having a third gate, a third source, and a third drain, wherein said third gate is coupled to said third word line, wherein said third source is coupled to said second drain, and wherein said third drain is coupled to said second data line; and

a capacitance coupled between a predetermined potential and said third source, wherein said capacitance is configured to store a second charge when said second word line is asserted and said third word line is de-asserted, and wherein said second gate is configured to store a third charge when said first word line is de-asserted; and

a data sense module coupled to said first and second data lines, wherein said module is configured to sense said second charge if said third word line is asserted while said second word line is asserted, wherein said module is further configured to sense said third charge by detecting a current through said second transistor if said second word line is de-asserted while said third word line is asserted, wherein said module is still further configured to detect said first charge by storing a fourth charge on said second gate if said first word line is asserted while said first data line is de-asserted, said first data line is then asserted, and said first word line is then de-asserted at a predetermined time interval after said assertion of the first data line, wherein said fourth charge is then sensed by detecting a current through said second transistor if said second word line is de-asserted while said third word line is asserted.

10. The memory circuit of claim 9, wherein said data sense module is further configured to determine a digital signal represented by said first, second, and third charges.

11. The memory circuit of claim 10, wherein said data sense module is configured to refresh said third charge by applying a potential to said first data line while said first word line is asserted.

12. The memory circuit of claim 10, wherein said data sense module is configured to refresh said second charge by

applying a potential to said second data line while said second word line is asserted and said third word line is asserted.

13. The memory circuit of claim 9, further comprising an address decoder configured to assert and de-assert said first, second, and third word lines in response to receiving an address signal, thereby allowing said data sense module to sense said first, second, and third charges.

14. The memory circuit of claim 9, further comprising an address decoder configured to assert and de-assert said first, second, and third word lines in response to receiving an address signal, thereby allowing said data sense module to sense and refresh said second and third charges.

15. The memory circuit of claim 9, further comprising a bi-directional decoder configured to convert n binary data bits into m logic signals during a write operation, wherein each of said logic signals has one of a plurality of distinct digital values, said bidirectional gate further configured to convert m logic signals, each having one of said distinct digital values, into n binary data bits during a read operation.

16. The memory circuit of claim 15, wherein the data sense module includes:

a read/write controller coupled to receive one of said logic signals from the bi-directional decoder; and

a bi-directional A/D converter coupled to said read/write controller and configured to drive said second data line during a write operation and to sense said third charge during a read operation.

17. The memory circuit of claim 16, wherein the data sense module further includes a multiplexer coupled to said read/write controller and configured to responsively drive said first data line with a program voltage, a high voltage, and a low voltage.

18. The memory circuit of claim 17, wherein the data sense module further includes a feedback circuit coupled to receive a desired current value and to sense said current through said second transistor, wherein said feedback circuit is configured to responsively provide a feedback signal to said multiplexer, and wherein said multiplexer is further configured to responsively drive said first data line with said feedback signal.

19. The memory circuit of claim 15, wherein the data sense module includes:

a read/write controller coupled to receive one of said logic signals from the bi-directional decoder; and

an A/D converter coupled to said read/write controller and configured to sense said current through said second transistor during a read operation.

20. The memory circuit of claim 18, wherein the data sense module further includes a D/A converter coupled to provide said desired current value to said feedback circuit.

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