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(71) Applicant: NORTH CAROLINA STATE UNIVERSITY [US/US]; 103 Holladay Hall, Campus Box 7003, Raleigh, NC 27695-7003 (US).

(72) Inventors: MEHROTRA, Manoj; Apartment #2, 1621 Crest Road, Raleigh, NC 27606 (US). BALIGA, Bantval, Jayant; 2612 Bembridge Drive, Raleigh, NC 27613 (US).

(74) Agents: BIGEL, Mitchell, S. et al.; Bell, Seltzer, Park & Gibson, P.O. Drawer 34009, Charlotte, NC 28234 (US).

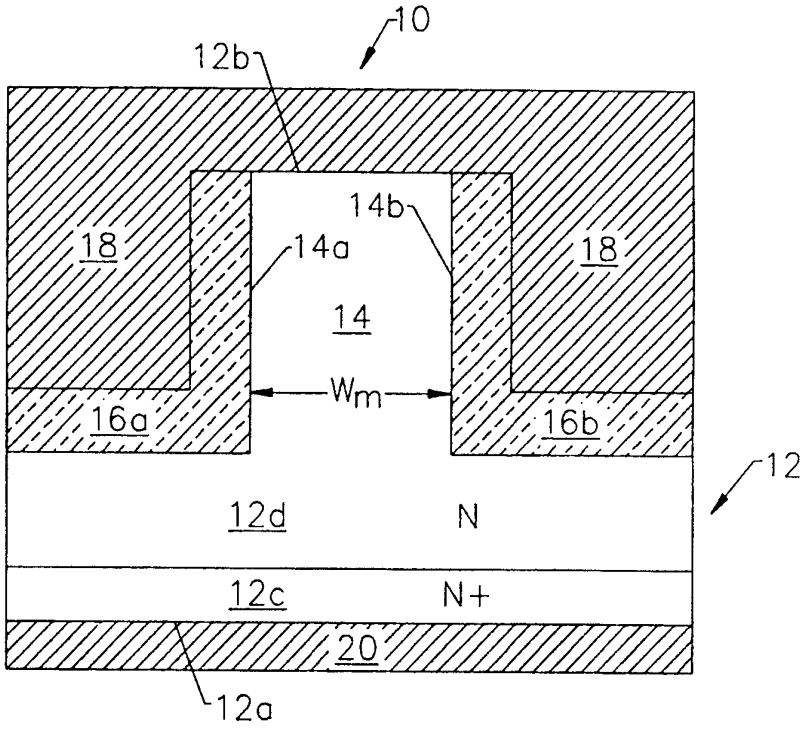
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(54) Title: SCHOTTKY BARRIER RECTIFIER WITH MOS TRENCH

(57) Abstract

A trench MOS Schottky barrier rectifier includes a semiconductor substrate having first and second faces, a cathode region of first conductivity type at the first face and a drift region of first conductivity type on the cathode region, extending to the second face. First and second trenches are formed in the drift region at the second face and define a mesa of first conductivity type therebetween. The mesa can be rectangular or circular in shape or of stripe geometry. Insulating regions are defined on the sidewalls of the trenches, adjacent the mesa, and an anode electrode is formed on the insulating regions, and on the top of the mesa at the second face. The anode electrode forms a Schottky rectifying contact with the mesa. The magnitude of reverse-biased leakage currents in the mesa and the susceptibility to reverse breakdown are limited not only by the potential barrier formed by the rectifying contact but also by the potential difference between the mesa and the portion of anode electrode extending along the insulating regions.Moreover, by properly choosing the width of the mesa, and by doping the mesa to a concentration greater than about $1x10^{16}$ per cubic centimeters, reverse blocking voltages greater than those of a corresponding parallel-plane P-N junction rectifier can be achieved.



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SCHOTTKY BARRIER RECTIFIER WITH MOS TRENCH

Field of the Invention

This invention relates to rectifiers and more particularly to metal-semiconductor rectifying devices, and methods of fabricating these devices.

Background of the Invention

Schottky barrier rectifiers are used extensively as output rectifiers in switching-mode power supplies and in other high-speed power switching applications such as motor drives, for carrying large forward currents and supporting high reverse blocking voltages. As is well known to those having skill in the art, a two-terminal rectifier exhibits a very low resistance to current flow in a forward direction and a very high resistance to current flow in a reverse direction. As is also well known to those having skill in the art, a Schottky barrier rectifier produces unipolar rectification as a result of nonlinear current transport across a metal-semiconductor contact.

There are basically four distinct processes for the transport of predominantly unipolar charge carriers across a metal/N-type semiconductor contact. The four processes are (1) transport of electrons from the semiconductor over a metal/semiconductor potential barrier and into the metal (thermionic emission), (2) quantum-mechanical tunneling (field emission) of electrons through the barrier, (3) recombination in the

space-charge region and (4) hole injection from the metal to the semiconductor. In addition, edge leakage currents, caused by high electric fields at the metal contact periphery, as well as interface currents, caused by the presence of traps at the metal-semiconductor interface, may also be present.

Current flow by means of thermionic emission (1) is the dominant process for a Schottky power rectifier with a moderately doped semiconductor region (e.g., Si with doping concentration $\leq 1x10^{16}$ cm^{-3}), operated at moderate temperatures (e.g., 300K). Moderate doping of the semiconductor region also produces a relatively wide potential barrier between the metal and semiconductor regions and thereby limits the proportion of current caused by tunneling (2). Space-charge recombination current (3) is similar to that observed in a P-N junction diode and is significant only at very low forward current densities. Finally, current transport due to minority carrier injection (4) is significant only at large forward current densities.

As the voltages of modern power supplies continue to decrease in response to need for reduced power consumption and increased energy efficiency, it becomes more advantageous to decrease the on-state voltage drop across a power rectifier, while still maintaining high forward-biased density levels. As well known to those skilled in the art, the on-state voltage drop is dependent on the forward voltage drop across the metal/semiconductor junction and the series resistance of the semiconductor region and cathode contact.

The need for reduced power consumption also requires minimizing the reverse-biased leakage current. The reverse-biased leakage current is the current in the rectifier during a reverse-biased blocking mode of operation. To sustain high reverse-biased blocking

voltages and minimize reverse-biased leakage currents, the semiconductor portion of the rectifier is typically lightly doped and made relatively thick so that the reverse-biased electric field at the metal/semiconductor interface does not become excessive. The magnitude of the reverse-biased leakage current for a given reverse-biased voltage is also inversely dependent on the Schottky barrier height (potential barrier) between the metal and semiconductor regions. Accordingly, to achieve reduced power consumption, both the forward-biased voltage drop and reverse-biased leakage current should be minimized and the reverse blocking voltage should be maximized.

Unfortunately, there is a tradeoff between the forward-biased voltage drop and the reverse-biased leakage current in a Schottky barrier rectifier, so that it is difficult to minimize both characteristics simultaneously. In particular, as the Schottky barrier height is reduced, the forward voltage drop decreases but the reverse-biased leakage current increases. Conversely, as the barrier height is increased, the forward voltage drop increases but the leakage current decreases. The doping level in the semiconductor region also plays a significant role. The higher the doping level, the lower the forward-biased voltage drop but reverse-biased breakdown is reduced by impact-ionization.

Therefore, in designing Schottky barrier rectifiers, design parameters such as barrier heights and semiconductor doping levels are selected to meet the requirements of a particular application because all device parasitics cannot be simultaneously minimized. Low barrier heights are typically used for Schottky rectifiers intended for high current operation with large duty cycles, where the power losses during forward conduction are dominant. High barrier heights are typically used for Schottky rectifiers intended for

applications with higher ambient temperatures or requiring high reverse blocking capability.

The height of the Schottky barrier formed by the metal/semiconductor junction is related to the work function potential difference between the metal contact and the semiconductor substrate. A graphical illustration of the relationship between metal work function and Schottky barrier height may be found in Chapter 5, Figure 3 of the textbook by S. M. Sze entitled *Semiconductor Devices, Physics and Technology*, John Wiley & Sons, 1985, at page 163. A detailed and comprehensive discussion of the design of Schottky barrier power rectifiers may be found in Section 8.2 of the textbook entitled *Modern Power Devices* by coinventor Baliga, published by John Wiley and Sons, Inc., 1987, the disclosure of which is hereby incorporated herein by reference.

In particular, sections 8.2.1 and 8.2.2 of the Baliga textbook disclose the semiconductor physics associated with both forward conduction and reverse blocking in a parallel-plane Schottky rectifier, having the structure of Figure 8.13 of the Baliga textbook. As set forth in Equation 8.14, the forward voltage drop is dependent on the drift region, substrate and contact resistances (R_D, R_S and R_C) and the forward current density (J_F), as well as the saturation current (J_S) which is a function of the Schottky barrier height (ϕ_{Bn}). The maximum reverse blocking voltage (i.e., breakdown voltage) of a Schottky rectifier (BV_{pp}) is also disclosed as ideally being equal to that of a one-sided abrupt P-N junction rectifier (e.g., P^+-N or N^+-P), having the structure of Figure 3.3 of the Baliga textbook. The breakdown voltage (BV_{pp}) is dependent on the doping concentration of the drift region (N_D), as described by Equation (1) below.

$$N_D = 2 \times 10^{18} (BV_{pp})^{-4/3} \quad (1)$$

Equation (1) is a reproduction of Equation 8.18 from the aforementioned Baliga textbook. A graphical representation of breakdown voltage and depletion layer width (W_{pp}) at breakdown versus drift region doping (N_D) for an abrupt P-N junction rectifier is shown by Figure 1. Figure 1 is a reproduction of Figure 3.4 from the aforementioned Baliga textbook.

In reality, however, the actual breakdown voltage of a Schottky rectifier is about one-third (⅓) that for the abrupt parallel-plane P-N junction described by Equation (1) and graphically illustrated by Figure 1. As will be understood by those skilled in the art, the reduction in breakdown voltage below the parallel plane value is caused, in part, by image-force-induced lowering of the potential barrier between the metal and the semiconductor regions, which occurs at reverse-biased conditions.

One attempt to optimize the on-state voltage drop/reverse blocking voltage tradeoff associated with the Schottky barrier rectifier is the Junction Barrier controlled Schottky (JBS) rectifier. The JBS rectifier is a Schottky rectifier having an array of Schottky contacts at the face of a semiconductor substrate with corresponding semiconductor channel regions beneath the contacts. The JBS rectifier also includes a P-N junction grid interspersed between the Schottky contacts. This device is also referred to as a "pinch" rectifier, based on the operation of the P-N junction grid. The P-N junction grid is designed so that the depletion layers extending from the grid into the substrate will not pinch-off the channel regions to forward-biased currents, but will pinch-off the channel regions to reverse-biased leakage currents.

As will be understood by those skilled in the art, under reverse bias conditions, the depletion layers formed at the P-N junctions spread into the channel regions, beneath the Schottky barrier contacts. The dimensions of the grid and doping levels of the P-type regions are designed so that the depletion layers intersect under the array of Schottky contacts, when the reverse bias exceeds a few volts, and cause pinch-off. Pinch-off of the channels by the depletion layers causes the formation of a potential barrier in the substrate and further increases in the reverse-biased voltage are supported by the depletion layer, which then extends into the substrate, away from the Schottky barrier contacts. Accordingly, once a threshold reverse-biased voltage is achieved, the depletion layers shield the Schottky barrier contacts from further increases in reverse-biased voltage. This shielding effect prevents the lowering of the Schottky barrier potential at the interface between the metal contacts and semiconductor substrate and inhibits the formation of large reverse leakage currents.

The design and operation of the JBS rectifier is described in Section 8.4 of the above cited textbook and in U.S. Patent No. 4,641,174 to coinventor Baliga, entitled *Pinch Rectifier*, the disclosures of which are hereby incorporated herein by reference. For example, as shown by Figure 6 of the '174 patent, reproduced herein as Figure 2, an embodiment of a pinch rectifier **200** comprises a plurality of Schottky rectifying contacts **232** formed by metal layer **230** and substrate **204** and a P-N junction grid formed by regions **234** and substrate **204**. Unfortunately, the JBS rectifier typically possesses a relatively large series resistance and a relatively large forward voltage drop caused by the reduction in overall Schottky contact area dedicated to forward conduction. This reduction in area is necessarily caused by the presence of the P-

N junction grid at the face of the substrate. In addition, large forward currents can cause large forward voltage drops and can lead to the onset of minority carrier conduction (i.e., bipolar), which limit the JBS's performance at high switching rates. Finally, although the reverse blocking voltage for the JBS may be somewhat higher than the reverse blocking voltage for a Schottky rectifier having an equivalent drift region doping (N_D), it does not achieve the level of reverse blocking capability obtainable with a parallel-plane P-N junction, as shown by Figure 1.

Another attempt to optimize the forward voltage drop/reverse blocking voltage tradeoff is disclosed in U.S. Patent No. 4,982,260 to Chang, coinventor Baliga and Tong, entitled *Power Rectifier with Trenches*, the disclosure of which is hereby incorporated by reference. For example, as shown by Figures 10B and 14B, reproduced herein as Figures 3 and 4, respectively, conventional P-i-N rectifiers (P^+-N^--N^+) are modified to include an interspersed array of Schottky contacts on a face of an N-type semiconductor substrate. As shown by Figure 3, the Schottky contact regions **550A-C** are separated from the P^+ portions **510A-D** (of the P-i-N rectifier) by MOS trench regions **522A-522F**. In another embodiment shown by Figure 4, the Schottky contact regions **718A-E** are interspersed adjacent the P^+ portions **720A-F**, which are formed at the bottom of trenches **710A-F**. As will be understood by those skilled in the art, these modified P-i-N rectifiers also typically possess an unnecessarily large series resistance in the drift region (N^- regions **506, 706**). Moreover, only a relatively small percentage of forward-conduction area is dedicated to the Schottky contacts, which dominate the forward bias characteristics by turning on at lower forward voltages than the parallel connected P^+-N junctions. Finally, although the forward leakage

current for these P-i-N type rectifiers is substantially lower than corresponding forward leakage current for a Schottky rectifier, like the JBS, they do not achieve the level of reverse blocking capability associated with an abrupt parallel-plane P-N junction.

A MOS barrier Schottky (MBS) rectifier has also been proposed to allow for unipolar conduction at forward voltage drops greater than 0.5 Volts and at forward unipolar current densities greater than those obtainable using the JBS rectifier, described above. In particular, this MBS rectifier was described in an article entitled *New Concepts in Rectifiers*, Proceedings of the Third International Workshop on the Physics of Semiconductor Devices, November 27-December 2, World Scientific Publications, Madras, India, 1985, by coinventor Baliga. As shown by the performance simulation curves of Figure 5 of that article, ideal reverse blocking voltages on the order of 150-1200 volts represent the theoretical limit for an MBS rectifier having a relatively high forward voltage drop greater than about 0.5 volts. The simulation curves of Figure 5 were based on Equations 8.14 and 8.18 of the aforementioned Baliga textbook. Accordingly, the curves of Figure 5 assume ideal Schottky rectifier behavior and, as noted above, do not take into account effects such as image-force-induced lowering of the potential barrier between the metal and the drift region.

Thus, notwithstanding these developments, there continues to be a need for a Schottky rectifier having low forward voltage drop and high reverse blocking capability, and preferably a Schottky rectifier having an ideal or near ideal parallel-plane blocking voltage.

Summary of the Invention

It is therefore an object of the present invention to provide a Schottky rectifier for low power supply applications.

It is also an object of the present invention to provide a Schottky rectifier capable of sustaining high forward biased current densities with low forward voltage drop.

It is another object of the present invention to provide a Schottky rectifier capable of sustaining high reverse blocking voltages.

It is still another object of the present invention to provide a Schottky rectifier capable of sustaining ideal or higher than ideal parallel-plane reverse blocking voltages.

These and other objects are provided according to the present invention, by a Schottky rectifier having a cathode region and a drift region thereon, in a semiconductor substrate such as silicon. The drift region is relatively highly doped in order to reduce the forward voltage drop at high forward biased current densities. However, in order to provide a rectifier which also has high blocking voltages, the present invention includes means, in the drift region, for increasing the reverse blocking voltage of the Schottky rectifier above the reverse blocking voltage of a corresponding ideal parallel-plane abrupt P-N junction rectifier.

In particular, the present invention provides a Schottky rectifier having a plurality of spaced apart trenches in the drift region. The trenches define at least one mesa, having a predetermined mesa width and predetermined mesa doping concentration. According to the invention, high reverse blocking voltages can be achieved using a mesa having a doping concentration greater than $1x10^{16}$ cm^{-3}, and wherein the product of the mesa doping concentration and mesa width is less than

or equal to $5x10^{12}$ cm^{-2}. Unexpectedly, the geometry of the rectifier in combination with the doping level can be manipulated to provide better performance than conventional devices. Thus, while providing a Schottky rectifier with a relatively high drift region doping concentration would typically cause a relatively low reverse blocking voltage, the present invention includes means for increasing the reverse-blocking voltage to ideal or higher than ideal values, even for doping concentrations greater than about $1x10^{16}$ cm^{-3}.

One embodiment of the present invention comprises a semiconductor substrate having first and second opposing faces. The substrate includes a cathode region of first conductivity type extending to the first face and a drift region of first conductivity type on the cathode region. The drift region extends to the second face and first and second trenches are formed in the drift region, at the second face. The trenches, which typically include sidewalls extending parallel to each other, define a mesa in the drift region. The mesa is preferably of stripe, rectangular or circular shape. First and second insulating regions are also formed on the trench sidewalls.

In addition, an anode electrode is formed on the second face and on the first and second insulating regions. The anode electrode forms a Schottky rectifying contact with the mesa at the second face. Since the anode electrode is also formed on the insulating regions and extends into the adjacent trenches, the application of a potential bias to the anode electrode not only effects conduction at the anode electrode/mesa interface on the second face, but also effects the electric field profile in the mesa, beneath the interface. While not wishing to be bound by any theory, it is believed that the unexpected shape of the electric field distribution in the mesa causes the rectifier to be less susceptible to reverse biased

breakdown and, in fact, causes the reverse blocking voltage to exceed the corresponding ideal parallel-plane reverse blocking voltage. For example, a Schottky rectifier according to the present invention, having a drift region doping of $1x10^{17}$ cm^{-3}, was fabricated and tested and showed a reverse blocking voltage of greater than fifteen (15) volts. The expected blocking voltage for a similarly doped parallel-plane abrupt P-N junction was only 9.5 volts.

Finally, instead of forming trenches in the drift region to define a mesa therebetween, the mesa may also be formed as extensions of the drift region using conventional techniques such as selective epitaxial growth (SEG). In this embodiment, insulating regions such as SiO_2 can be formed on the sides of the mesa using conventional growth or deposition techniques.

Brief Description of the Drawings

Figure 1 is a graphical illustration of breakdown voltage and depletion layer width versus doping concentration for a parallel-plane abrupt P-N junction.

Figure 2 illustrates a cross-sectional representation of a prior art pinch rectifier, according to Figure 6 of U.S. Patent No. 4,641,174.

Figure 3 illustrates a cross-sectional representation of a prior art P-i-N rectifier, according to Figure 10B of U.S. Patent No. 4,982,260.

Figure 4 illustrates a cross-sectional representation of a prior art P-i-N rectifier, according to Figure 14B of U.S. Patent No. 4,982,260.

Figure 5 illustrates a cross-sectional view of a first embodiment of a trench MOS Schottky barrier rectifier (TMBR) according to the present invention.

Figures 6A-6F are cross-sectional views of the structure of Figure 5 during intermediate fabrication steps.

Figure 7 is a graphical illustration of experimental results comparing reverse leakage current versus reverse bias for a parallel-plane Schottky rectifier and a trench MOS Schottky barrier rectifier according to the present invention.

Figure 8 is a graphical illustration of experimental results comparing forward current versus forward bias for a parallel-plane Schottky rectifier and a trench MOS Schottky rectifier according to the present invention.

Figure 9 is a graphical illustration of simulation results showing reverse breakdown voltage versus trench depth for a trench MOS Schottky rectifier according to the present invention.

Detailed Description of a Preferred Embodiment

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which a preferred embodiment of the invention is shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiment set forth herein; rather, this embodiment is provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

Referring now to Figure 5, a cross-sectional illustration of a trench MOS Schottky barrier rectifier (TMBR) according to the present invention is shown. The rectifier **10** includes a semiconductor substrate **12** of first conductivity type, typically N-type conductivity, having a first face **12a** and a second opposing face **12b**. The substrate **12** preferably comprises a relatively highly doped cathode region **12c** (shown as N^+) adjacent the first face **12a**. A drift region **12d** of first conductivity type (shown as N) preferably extends from the cathode region **12c** to the

second face **12b**. Accordingly, the doping concentration of the cathode region is preferably greater than the drift region. A mesa **14** having a cross-sectional width "W_m", defined by opposing sides **14a** and **14b**, is preferably formed in the drift region **12d**. The mesa can be of stripe, rectangular, cylindrical or other similar geometry. Insulating regions **16a** and **16b** (shown as SiO_2) are also provided on the mesa sides. The rectifier also includes an anode electrode **18** on the insulating regions **16a**, **16b**. The anode electrode **18** forms a Schottky rectifying contact with the mesa **14**. The height of the Schottky barrier formed at the anode electrode/mesa interface is dependent not only on the type of electrode metal and semiconductor (e.g., Si, Ge, GaAs, and SiC) used, but is also dependent on the doping concentration in the mesa **14**. Finally, a cathode electrode **20** is provided adjacent the cathode region **12c** at the first face **12a**. The cathode electrode **20** ohmically contacts the cathode region **12c**.

As will be understood by one skilled in the art, because the anode electrode **18** is formed on the insulating regions **16a**, **16b** adjacent the mesa sides **14a**, **14b**, the application of a potential bias to the anode electrode not only effects conduction at the anode electrode/mesa interface on the second face **12b**, but also renders the rectifier **10** less susceptible to reverse-biased breakdown, and has been shown to cause the reverse blocking voltage of the present invention to exceed the corresponding ideal parallel-plane blocking voltage for an abrupt P-N junction. Based on experimental testing, as shown by Figure 7, a trench MOS Schottky barrier rectifier having a drift region doping concentration of $1x10^{17}$ cm^{-3} showed a reverse blocking voltage of greater than fifteen (15) volts, compared to 9.5 volts for a corresponding parallel-plane abrupt P-N junction.

Relatively high reverse blocking voltages are achieved even with drift region doping concentrations of greater than $1x10^{16}$ cm^{-3}. Furthermore, by selecting the mesa width "W_m" so that the product of the drift region doping concentration and the mesa width is less than or equal to $5x10^{12}$ cm^{-2}, better than ideal reverse blocking voltages are obtained for rectifiers according to the present invention with drift region doping concentrations greater than $1x10^{16}$ cm^{-3}.

Referring now to Figures 6A-6F, a technique for fabricating the rectifier **10** of Figure 5 will be described. Referring first to Figure 6A, a substrate **12** having first and second opposing faces **12a** and **12b** is provided with a relatively highly doped cathode region **12c** at face **12a**, and a drift region **12d** on the cathode region, extending to the second face **12b**. As will be understood by one skilled in the art, the drift region **12d** having thickness "T_d", may be provided by epitaxial growth using conventional techniques. A plurality of adjacent mesas **14** can be formed in the drift region **12d** by initially providing a multilayered stack of oxide (SiO_2), nitride (Si_3N_4) and photoresist (regions **13**, **15**, and **17**, respectively) on the second face **12b**. Although the formation of the oxide regions **13** is not necessary, the oxide regions **13** are preferably made relatively thin, approximately 100Å, to relieve interlayer stress between the semiconductor **12** and the nitride regions **15**. Then, conventional lithographic patterning and etching steps can be performed to form discrete mesas **14** having thermal oxidation resistant nitride regions **15**, as shown by Figure 6b. Regions **15** are also chosen to be removable by an etch that does not etch SiO_2.

As will be understood by one skilled in the art, the etching step defines a plurality of first, second, third and fourth adjacent trenches **22**, having respective trench widths "W_t" and trench depths "d", in

the drift region **12d**. If mesas **14** of stripe geometry are to be formed, the respective first, second, third and fourth trench sidewalls **22a** will extend parallel to each other in a third direction (not shown), which is orthogonal to the cross-sectional view. Alternatively, the patterning and etching steps can be performed to define rectangular, cylindrical or other similar geometries. However, because rectangular or cylindrical mesas occupy a comparatively smaller percentage of total forward conduction area for a given size substrate than mesa stripes of identical width, the forward voltage drop for rectifiers with rectangular or cylindrical mesas will likely be higher for a given forward current.

Referring now to Figure 6C, respective first, second, third and fourth insulating regions **16** such as SiO_2 (approx. 1000Å) can be formed on the trench sidewalls **22a** and on the trench bottoms **22b**, using conventional thermal oxide growth, but not on the face **12b** because of the presence of the nitride regions **15**. Next, the nitride regions **15** and stress relief oxide regions **13** (if present) are removed and top metallization **23** and metal patterning steps are performed to define the anode electrode **18** as shown by Figures 6D-6E. Finally, a backside metallization step is performed to define the cathode electrode **20** at the first face **12a** as shown by Figure 6F. Accordingly, for high current applications, a trench MOS Schottky barrier rectifier according to the present invention can be formed having a plurality of adjacent mesa regions **14** connected in parallel to a single anode electrode metallization layer **18** and cathode metallization layer **20**.

As will be understood by one skilled in the art, although the above described process for forming a plurality of mesas with stripe geometry is preferred, other processes can also be used. For example, instead

of forming trenches **22** to define the mesas **14**, the mesas can be extensions of the drift region using conventional growth techniques such as selective epitaxial growth (SEG). In addition, the doping profiles of the mesas can be controlled in-situ in order to optimize the tradeoff between forward voltage drop and reverse blocking voltage for a particular rectifier application.

Accordingly, a semiconductor rectifier having low forward voltage drop and high reverse blocking voltage includes a semiconductor substrate **12** having first and second opposing faces **12a**, **12b**, a cathode region **12c** of first conductivity type and drift region **12d** of first conductivity type thereon. The rectifier also includes means, in the drift region, for increasing the reverse blocking voltage of the rectifier above the reverse blocking voltage of a corresponding ideal parallel-plane abrupt P-N junction rectifier. As described in reference to Figures 5 and 6A-6F, means for increasing the reverse blocking voltage preferably includes a plurality of trenches **22** in the drift region **12d**, insulating regions **16** on the trench sidewalls **22a** and an anode electrode **18** contacting a mesa(s) **14**, defined between adjacent sidewalls. By setting the mesa doping concentration to a level above $1x10^{16}$ cm^{-3} and by setting the product of the mesa(s) width "W_m" and mesa doping concentration to a value less than or equal to $5x10^{12}$ cm^{-2}, higher than expected blocking voltages can be obtained.

Referring now to Figure 7, a graphical illustration of experimental results showing reverse leakage current versus reverse bias for a parallel-plane Schottky rectifier and for a trench MOS Schottky barrier rectifier (TMBR) according to the present invention, is provided. Both devices had drift region doping concentrations (N_{drift}) of $1x10^{17}$ cm^{-3}. For the TMBR, the mesa was of stripe geometry and had a mesa

width "W_m" of 0.5 μm, trench width "W_t" of 0.5 μm and trench depth "d" of 2.0 μm. Accordingly, the pitch between adjacent trenches was 1.0μm or twice the mesa width and the product of the doping concentration in the mesa and mesa width equaled $5x10^{12}$ cm^{-2}. As shown by Figure 7, the TMBR achieved a breakdown voltage of greater than 15 volts, which was substantially greater than that for the parallel-plane Schottky rectifier (less than 5 volts) and corresponding parallel-plane abrupt P-N junction rectifier (9.5 volts). Referring now to Figure 8, a graphical illustration of forward current versus forward bias voltage for the parallel-plane Schottky rectifier and for the trench MOS Schottky barrier rectifier (TMBR) of Figure 7, is provided. Each of the TMBR curves corresponds to a rectifier having a mesa width and a doping concentration set to a predetermined value, so that the product of mesa width and doping concentration is less than $5x10^{12}$ cm^{-2}.

Referring now to Figure 9, a graphical illustration of simulated breakdown voltage versus trench depth "d" is provided, showing breakdown voltages of greater than twenty (20) volts for TMBR devices having trench depths greater than 0.5μm. The simulated curve for the TMBR according to the present invention was based on a device having mesa width "W_m" of 0.5μm, trench width of W_t=0.5μm, insulating region thickness of 500 Å, drift region thickness of T_d=3.0μm, drift region doping of $1x10^{17}$ cm^{-3} and anode electrode work function potential of 4.77eV.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED:

1. A rectifier comprising:

a semiconductor substrate having first and second faces, a cathode region of first conductivity type therein, adjacent the first face, and a drift region of first conductivity type therein, on said cathode region;

a cathode electrode contacting said cathode region;

a first trench at the second face and having a first sidewall in said drift region;

a second trench at the second face and having a second sidewall in said drift region, and wherein the first and second sidewalls define a mesa therebetween which has a predetermined mesa width and a predetermined mesa doping concentration;

first and second insulating regions on the first sidewall and on the second sidewall, respectively; and

an anode electrode on the second face and on said first and second insulating regions, said anode electrode forming a Schottky rectifying junction with the mesa at the second face; and

wherein the predetermined mesa doping concentration is greater than $1x10^{16}$ dopants per cubic centimeter.

2. The rectifier of Claim 1, wherein a product of the predetermined mesa doping concentration and the predetermined mesa width is less than or equal to $5x10^{12}$ per square centimeter.

3. The rectifier of Claim 1, wherein a product of the predetermined mesa doping concentration and the predetermined mesa width is less than or equal to $5x10^{12}$ per square centimeter in the entire mesa.

4. The rectifier of Claim 2, wherein said drift region is uniformly doped.

5. The rectifier of Claim 2, wherein the predetermined mesa doping concentration is greater than $1x10^{16}$ dopants per cubic centimeter in the entire mesa.

6. The rectifier of Claim 2, wherein the mesa is uniformly doped.

7. The rectifier of Claim 2, wherein said cathode region has a predetermined cathode region doping concentration and wherein the predetermined mesa doping concentration is less than the predetermined cathode region doping concentration.

8. The rectifier of Claim 2, wherein said first trench has a first width equal to the predetermined mesa width and wherein said second trench has a second width equal to the predetermined mesa width.

9. The rectifier of Claim 2, wherein the distance between a center of said first trench and a center of said second trench is twice the predetermined mesa width.

10. The rectifier of Claim 2, wherein said semiconductor substrate comprises silicon and wherein said first insulating region and said second insulating region comprise silicon dioxide.

11. The rectifier of Claim 2, wherein said first and second insulating regions line said first and second trenches, respectively.

12. The rectifier of Claim 11, wherein said anode electrode extends into said first and second trenches and wherein said first and second insulating regions extend between said drift region and said anode electrode.

13. The rectifier of Claim 2, wherein said first trench has a first trench bottom in said drift region and wherein said second trench has a second trench bottom in said drift region.

14. The rectifier of Claim 13, wherein a depth of said first trench equals a depth of said second trench.

15. The rectifier of Claim 13, wherein a junction between said drift region and said cathode region extends between the first trench bottom and the first face.

16. The rectifier of Claim 15, wherein the first sidewall extends parallel to the second sidewall.

17. A rectifier comprising:

a semiconductor substrate having first and second opposing faces, said substrate having a cathode region of first conductivity type extending to said first face and a drift region of said first conductivity type extending to said second face, said drift region having a predetermined drift region doping concentration;

a cathode electrode on the first face, ohmically contacting said cathode region;

an anode electrode on the second face, said anode electrode forming a Schottky rectifying junction with said drift region at the second face; and

means, in said drift region, for increasing the reverse blocking voltage of said Schottky rectifying junction above the reverse blocking voltage of an ideal parallel-plane abrupt P-N junction rectifier having a region of first conductivity type and a more highly doped region of opposite conductivity type forming a P-N junction with said region of first conductivity type, and wherein the doping concentration of said region of first conductivity type equals said predetermined drift region doping concentration.

18. The rectifier of Claim 17, wherein said means for increasing the reverse blocking voltage of said Schottky rectifying junction comprises:

a first trench in said drift region at the second face; and

a second trench in said drift region at the second face;

wherein said first and second trenches define a mesa therebetween; and

wherein the predetermined drift region doping concentration is greater than $1x10^{16}$ dopants per cubic centimeter.

19. The rectifier of Claim 18, wherein the drift region is uniformly doped.

20. A rectifier comprising:

a semiconductor substrate having first and second faces;

a cathode electrode on the first face;

a first trench in said substrate, at the second face;

a second trench in said substrate, adjacent the first trench, and wherein the first and second trenches define a mesa therebetween which has a

predetermined mesa width and a predetermined mesa doping concentration;

first and second insulating regions in the first and second trenches, respectively; and

an anode electrode on the second face and on said first and second insulating regions, said anode electrode forming a Schottky rectifying junction with the mesa at the second face;

wherein the predetermined mesa doping concentration is greater than $1x10^{16}$ dopants per cubic centimeter; and

wherein a product of the predetermined mesa doping concentration and the predetermined mesa width is less than or equal to $5x10^{12}$ per square centimeter.

21. The rectifier of Claim 20, wherein the product of the predetermined mesa doping concentration and the predetermined mesa width is less than or equal to $5x10^{12}$ per square centimeter in the entire mesa.

22. The rectifier of Claim 20, wherein the mesa is uniformly doped.

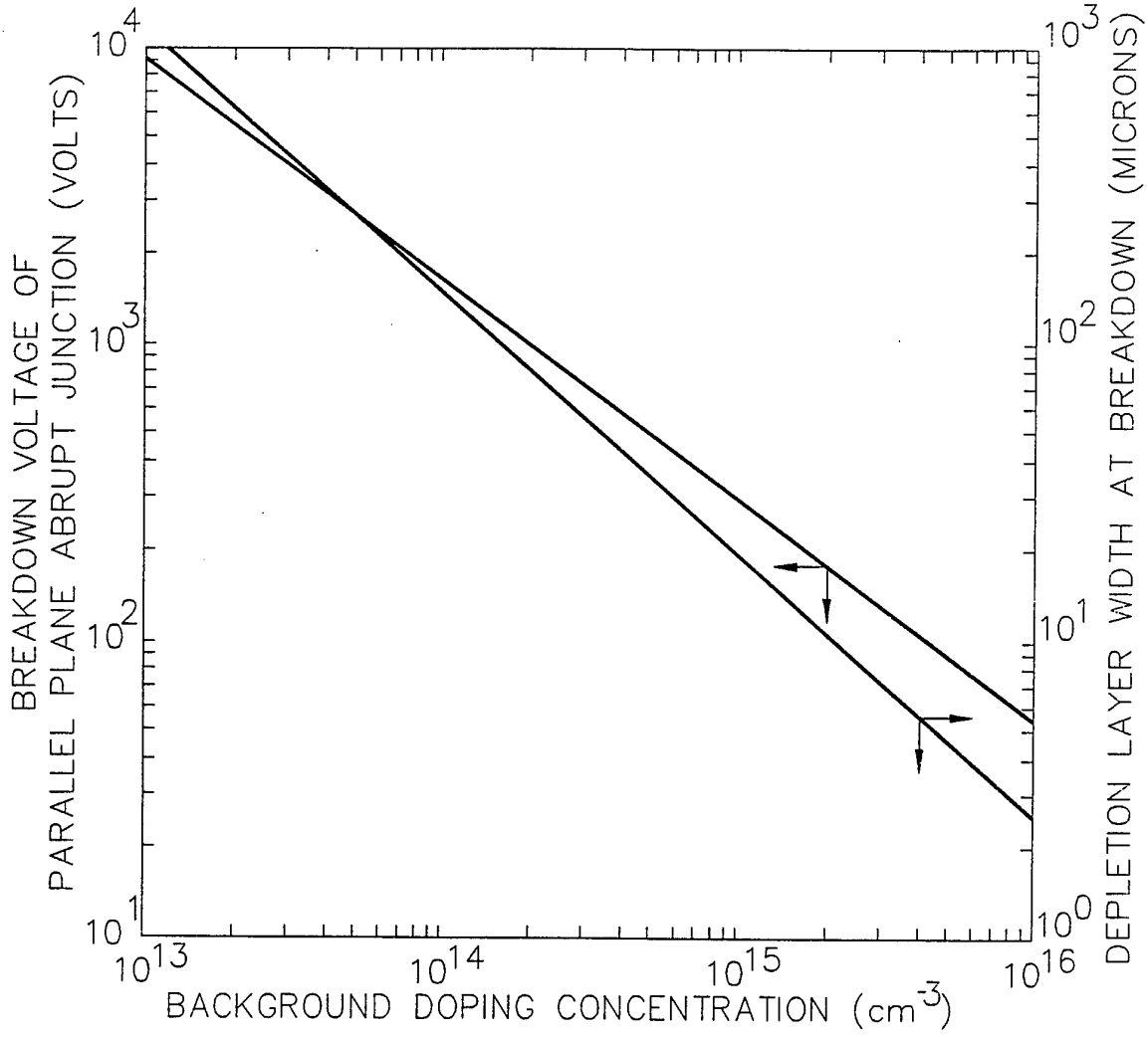


FIG. 1.
(PRIOR ART)

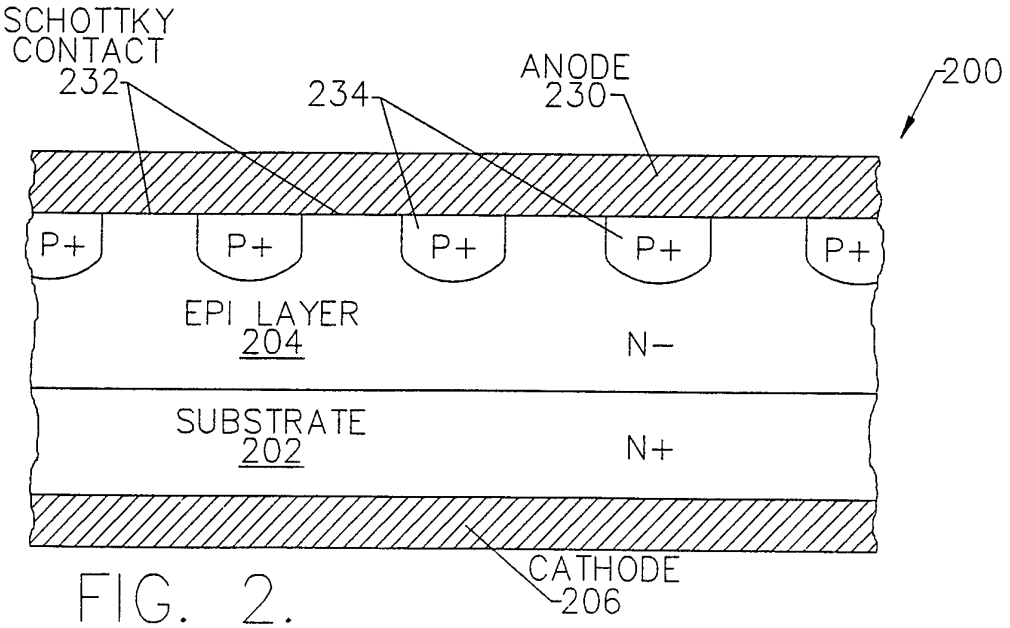


FIG. 2.
(PRIOR ART)

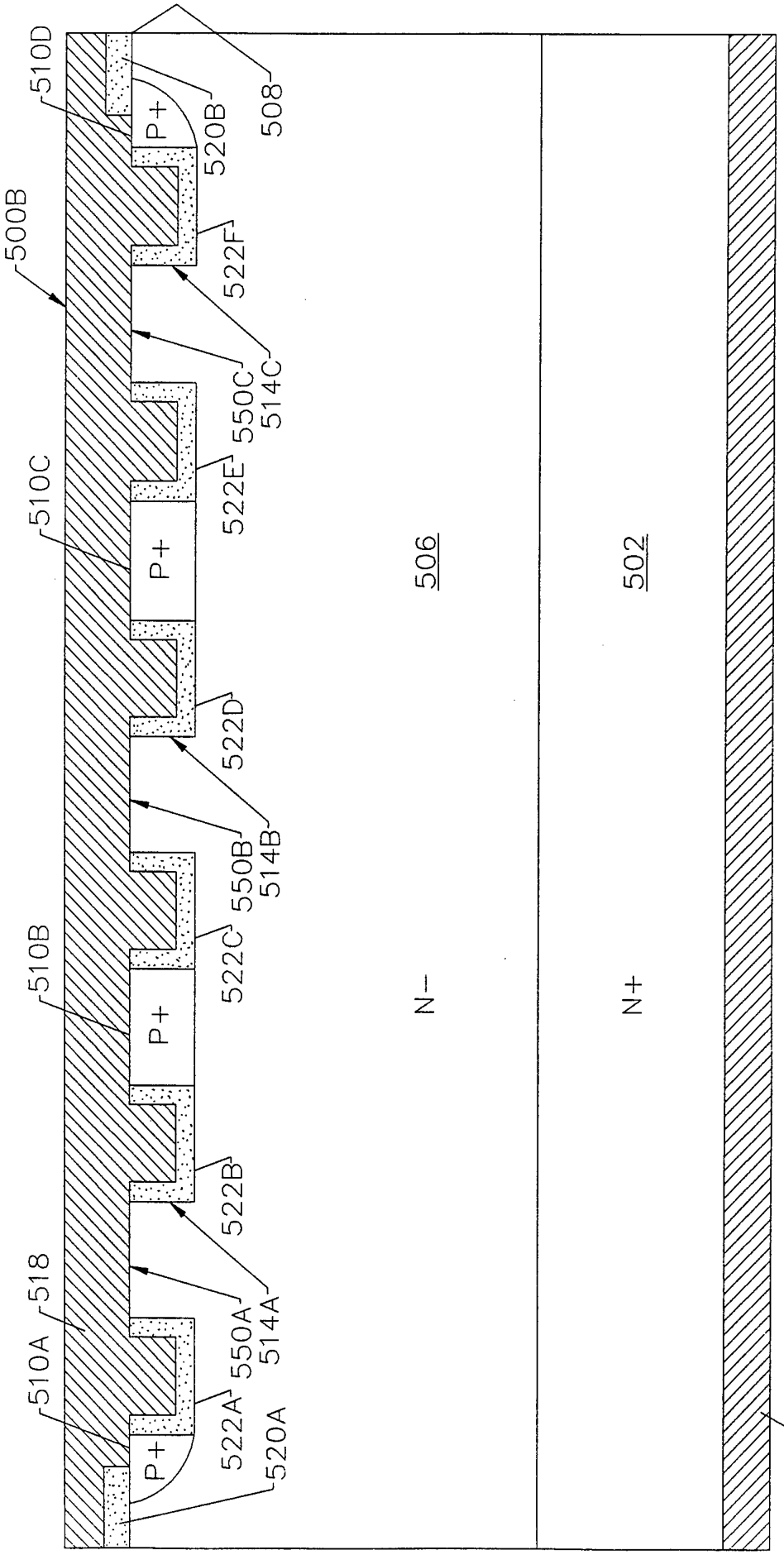


FIG. 3.
(PRIOR ART)

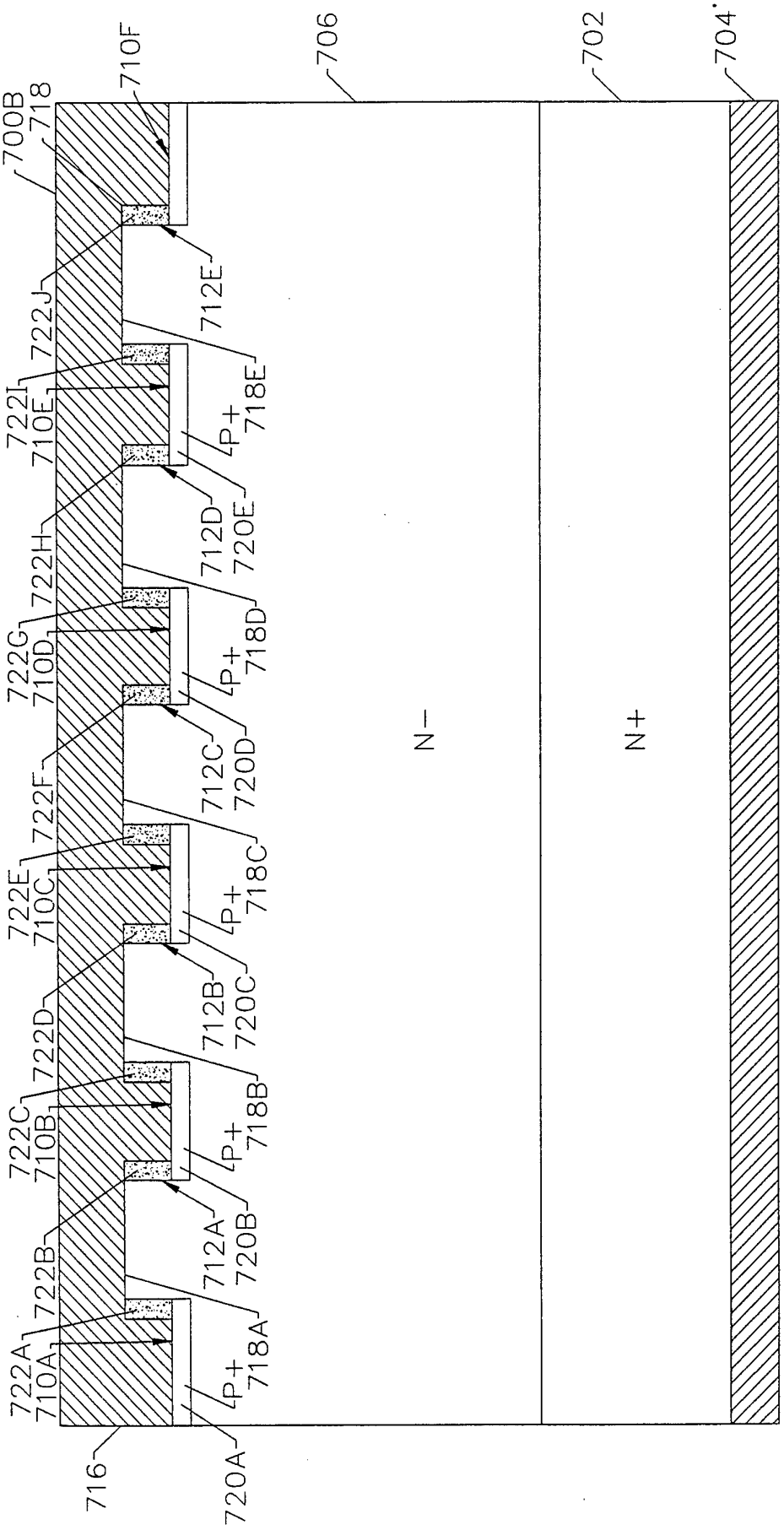


FIG. 4.
(PRIOR ART)

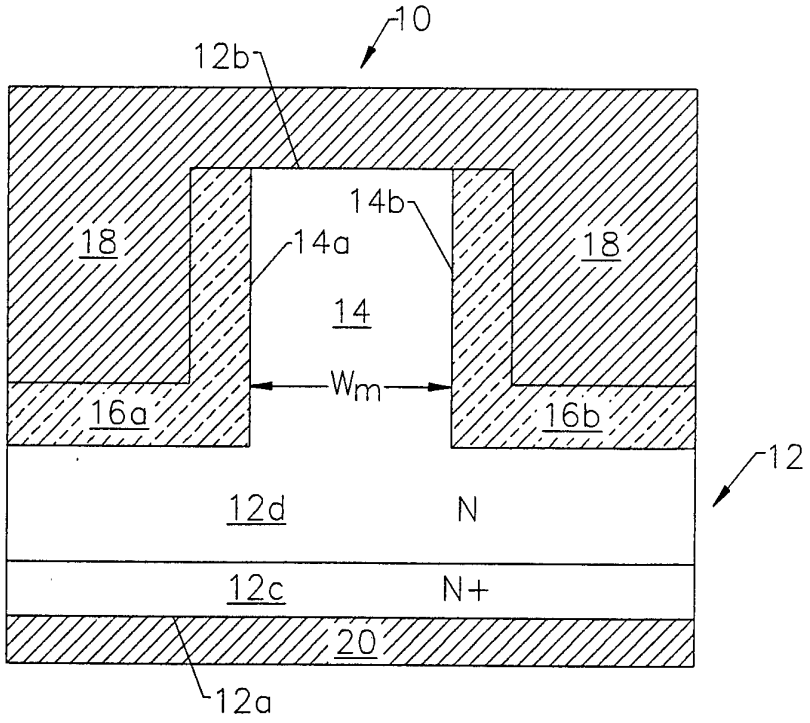


FIG. 5.

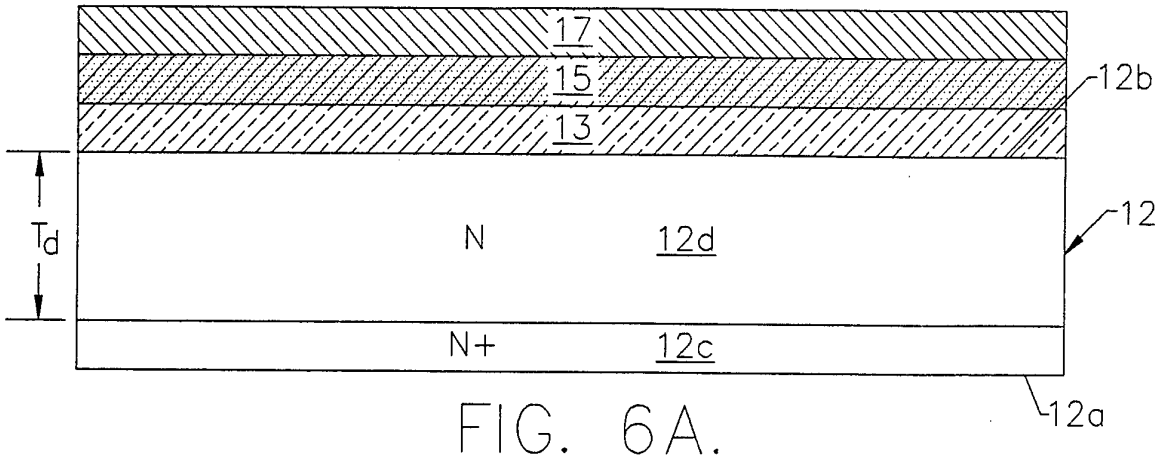


FIG. 6A.

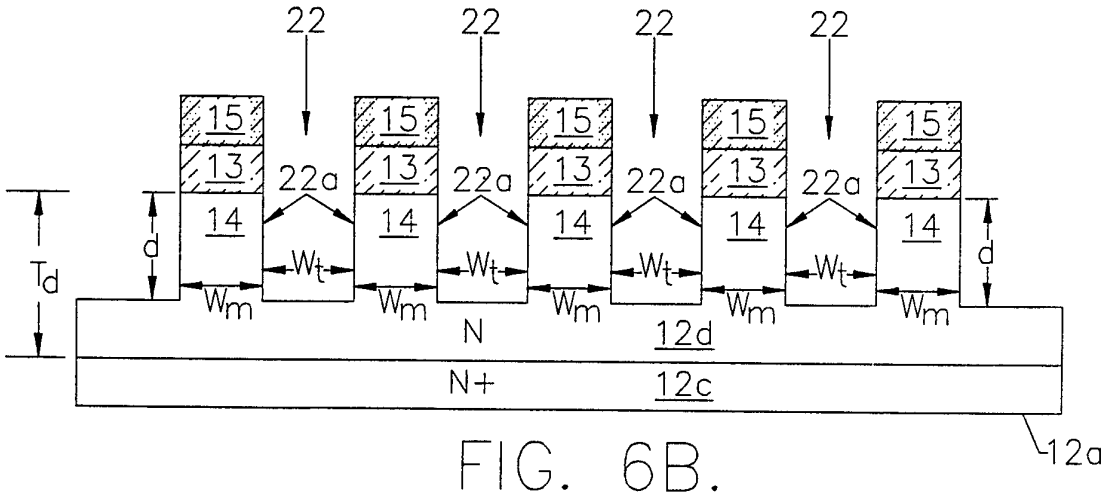


FIG. 6B.

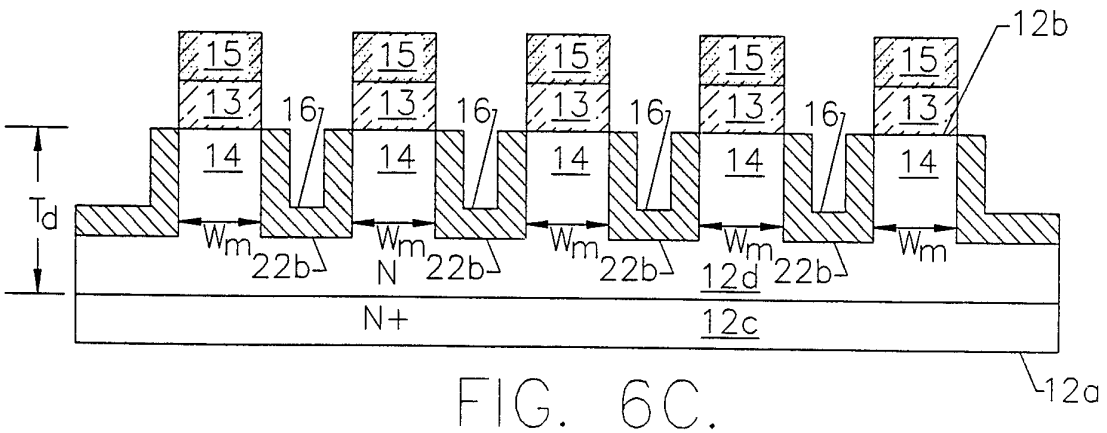


FIG. 6C.

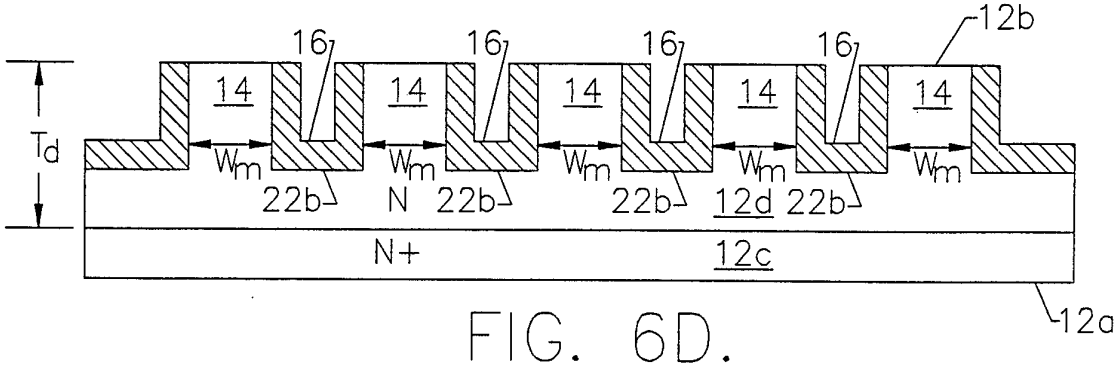


FIG. 6D.

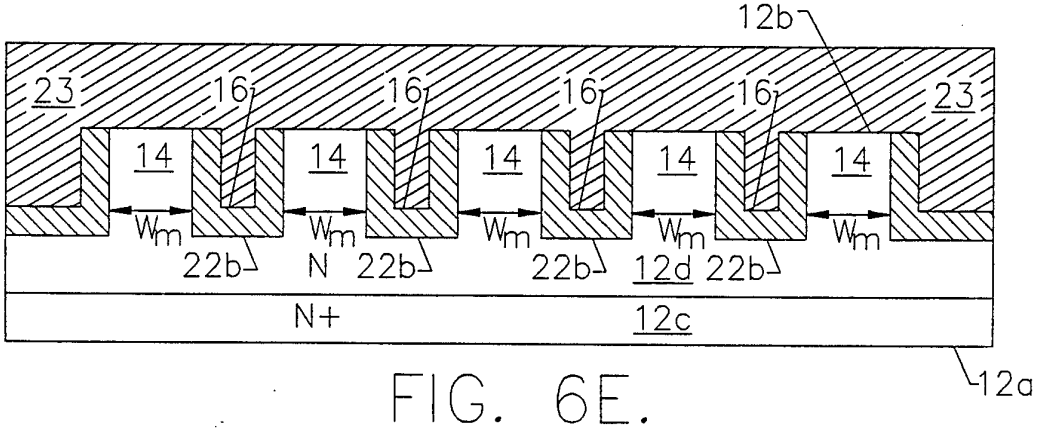


FIG. 6E.

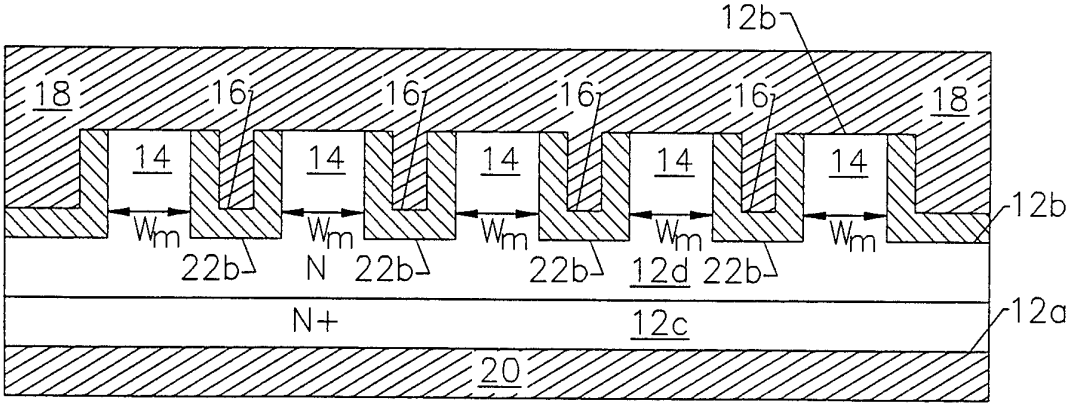


FIG. 6F.

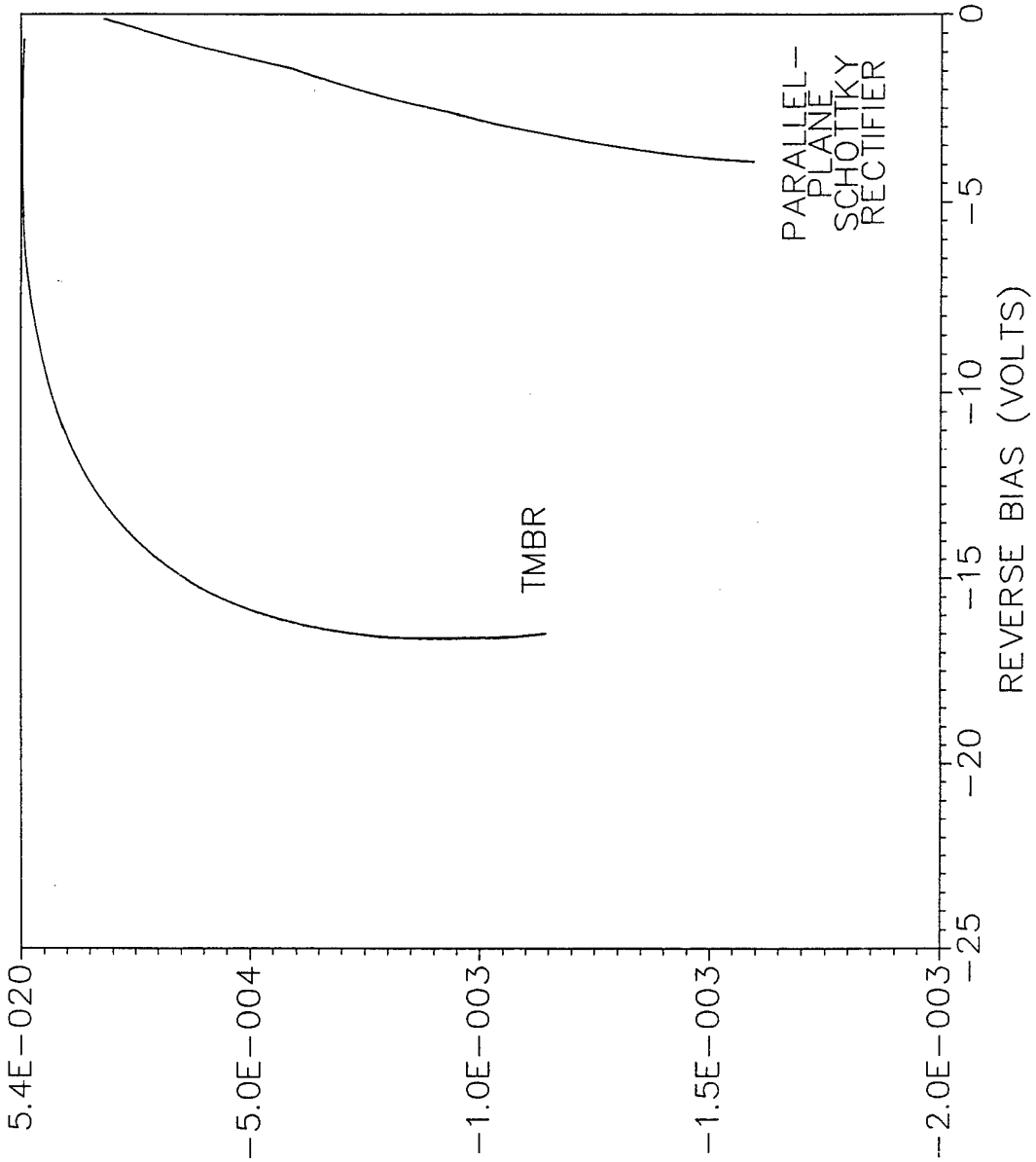

5.4E-020
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-1.0E-003
-1.5E-003
-2.0E-003
REVERSE LEAKAGE CURRENT (A)
0
-5
-10
-15
-20
-25
REVERSE BIAS (VOLTS)
TMBR
PARALLEL-PLANE SCHOTTKY RECTIFIER

FIG. 7.

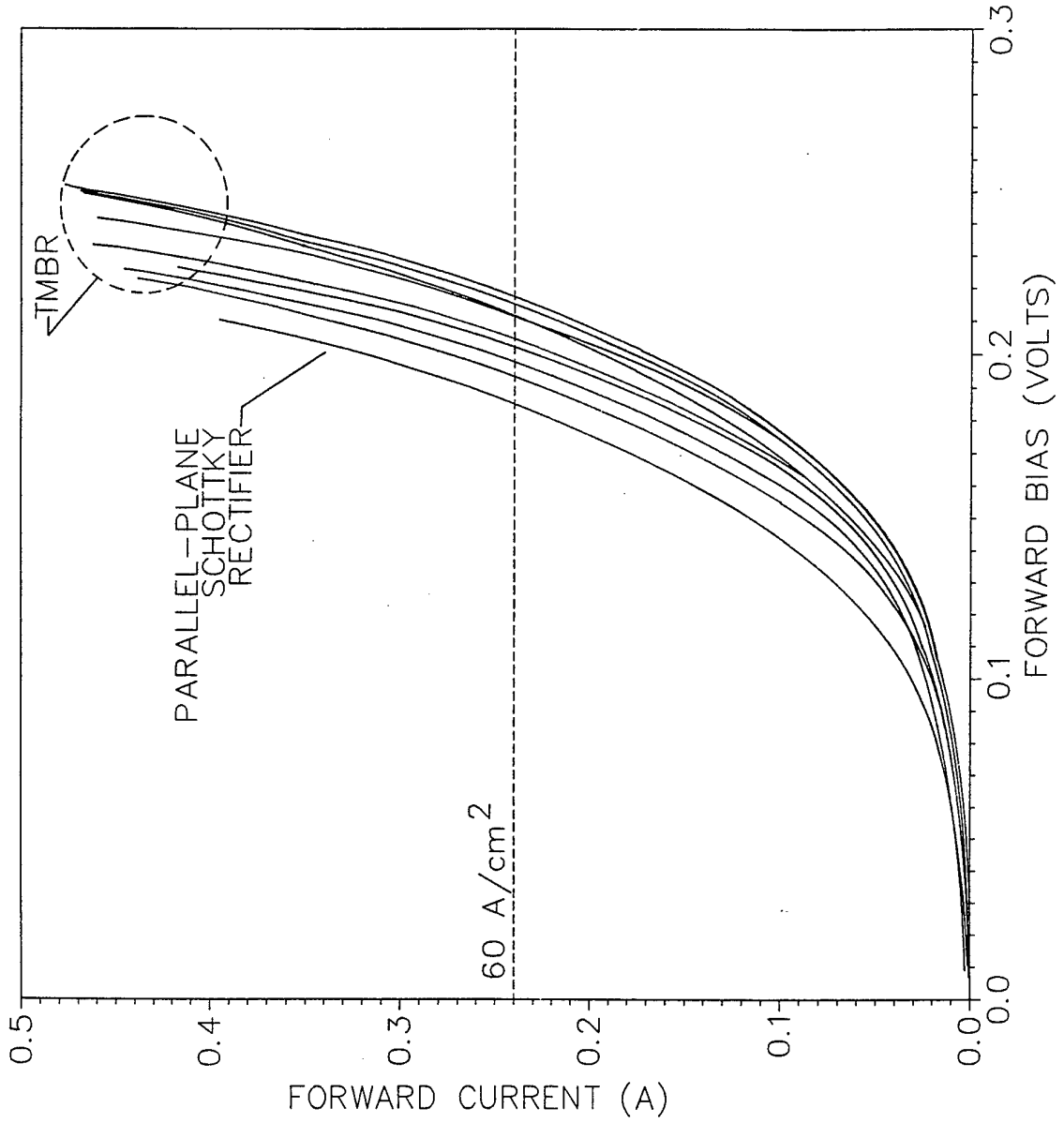

TMBR
PARALLEL-PLANE SCHOTTKY RECTIFIER
60 A/cm2
FORWARD CURRENT (A)
0.5
0.4
0.3
0.2
0.1
0.0
FORWARD BIAS (VOLTS)
0.0
0.1
0.2
0.3

FIG. 8.

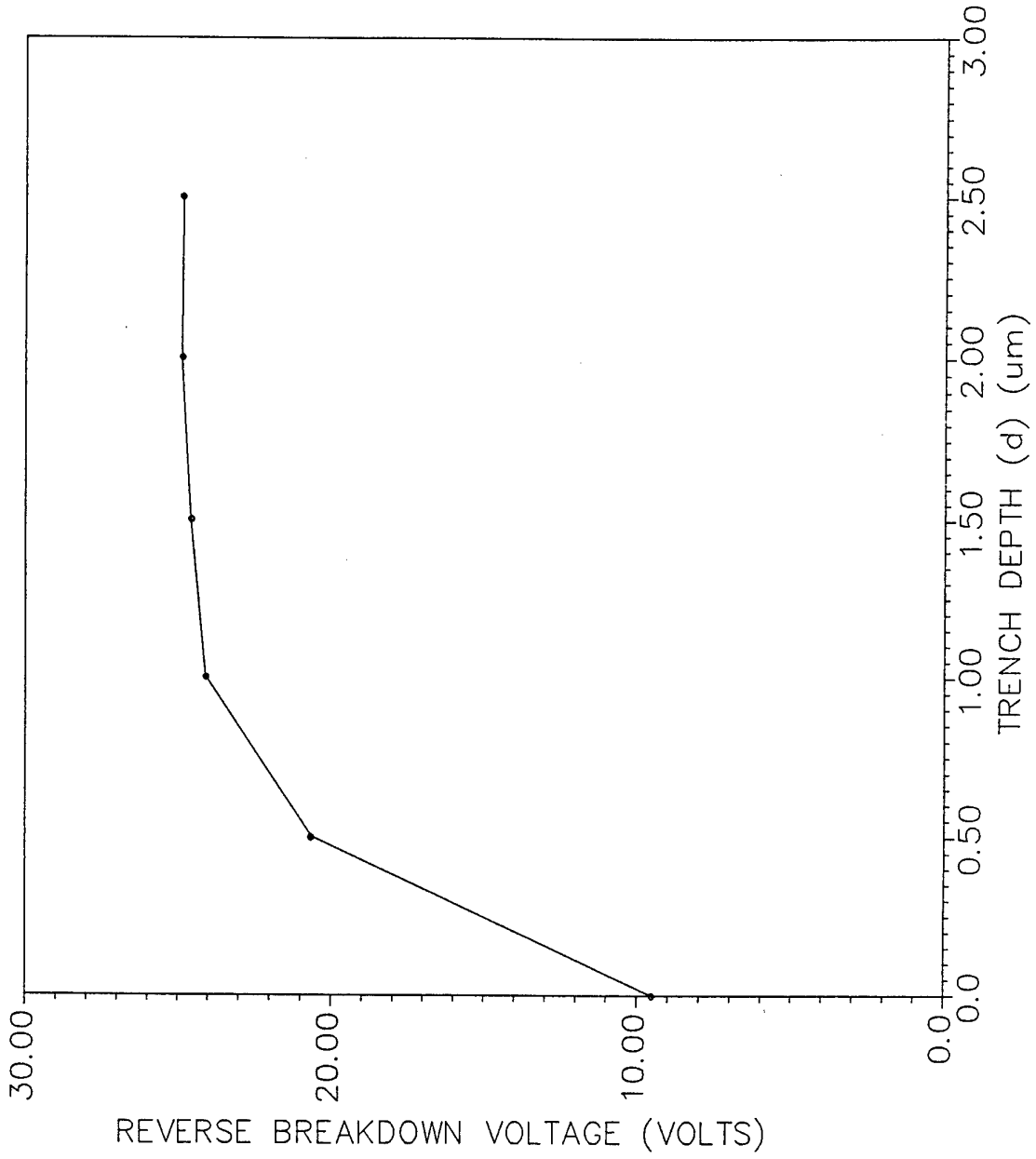

30.00
20.00
10.00
0.0
REVERSE BREAKDOWN VOLTAGE (VOLTS)
0.0
0.50
1.00
1.50
2.00
2.50
3.00
TRENCH DEPTH (d) (um)

FIG. 9.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 94/07348

A. CLASSIFICATION OF SUBJECT MATTER

H 01 L 29/86,H 01 L 29/48

According to International Patent Classification (IPC) or to both national classification and IPC 6

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H 01 L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	B.J. BALIGA "Modern Power Devices", 1987, JOHN WILEY & SONS, New York, pages 444,446; chapter 8.4.3; fig. 8.29 (cited in the application). --	1-22
Y	US, A, 4 903 189 (NGO,STEIGERWALD,WALTEN, BALIGA,KORMAN,CHANG) 20 February 1990 (20.02.90), abstract; fig. 3-6; column 10, line 20 - - column 11, line 54; claims 1-6,12. --	1-22
A	US, A, 4 982 260 (CHANG,BALIGA,TOWG) 01 January 1991 (01.01.91),	1-22

[X] Further documents are listed in the continuation of box C.

[ ] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 October 1994	17. 11. 94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	HEINICH e.h.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 94/07348

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Fig. 10,11,14,15; column 6, line 31 - column 7, line 55; column 8, line 34 - column 9, line 44 (cited in the application). --	
A	US, A, 5 040 034 (MURAKAMI) 13 August 1991 (13.08.91), Fig. 7,8; column 6, line 32 - - column 7, line 33; abstract. --	1-22
A	US, A, 5 202 750 (GOUGH) 13 April 1993 (13.04.93), abstract; fig. 3; column 7, lines 10-68. ----	1,17, 20

ANHANG

zum internationalen Recherchenbericht über die internationale Patentanmeldung Nr.

ANNEX

to the International Search Report to the International Patent Application No.

ANNEXE

au rapport de recherche international relatif á la demande de brevet international n°

PCT/US 94/07348 SAE 93554

In diesem Anhang sind die Mitglieder der Patentfamilien der im obengenannten internationalen Recherchenbericht angeführten Patentdokumente angegeben. Diese Angaben dienen nur zur Unterrichtung und erfolgen ohne Gewähr.

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The Office is in no way liable for these particulars which are given merely for the purpose of information.

La présente annexe indique les membres de la famille de brevets relatifs aux documents de brevets cités dans le rapport de recherche international visée ci-dessus. Les reseignements fournis sont donnés á titre indicatif et n'engagent pas la responsibilité de l'Office.

Im Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
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