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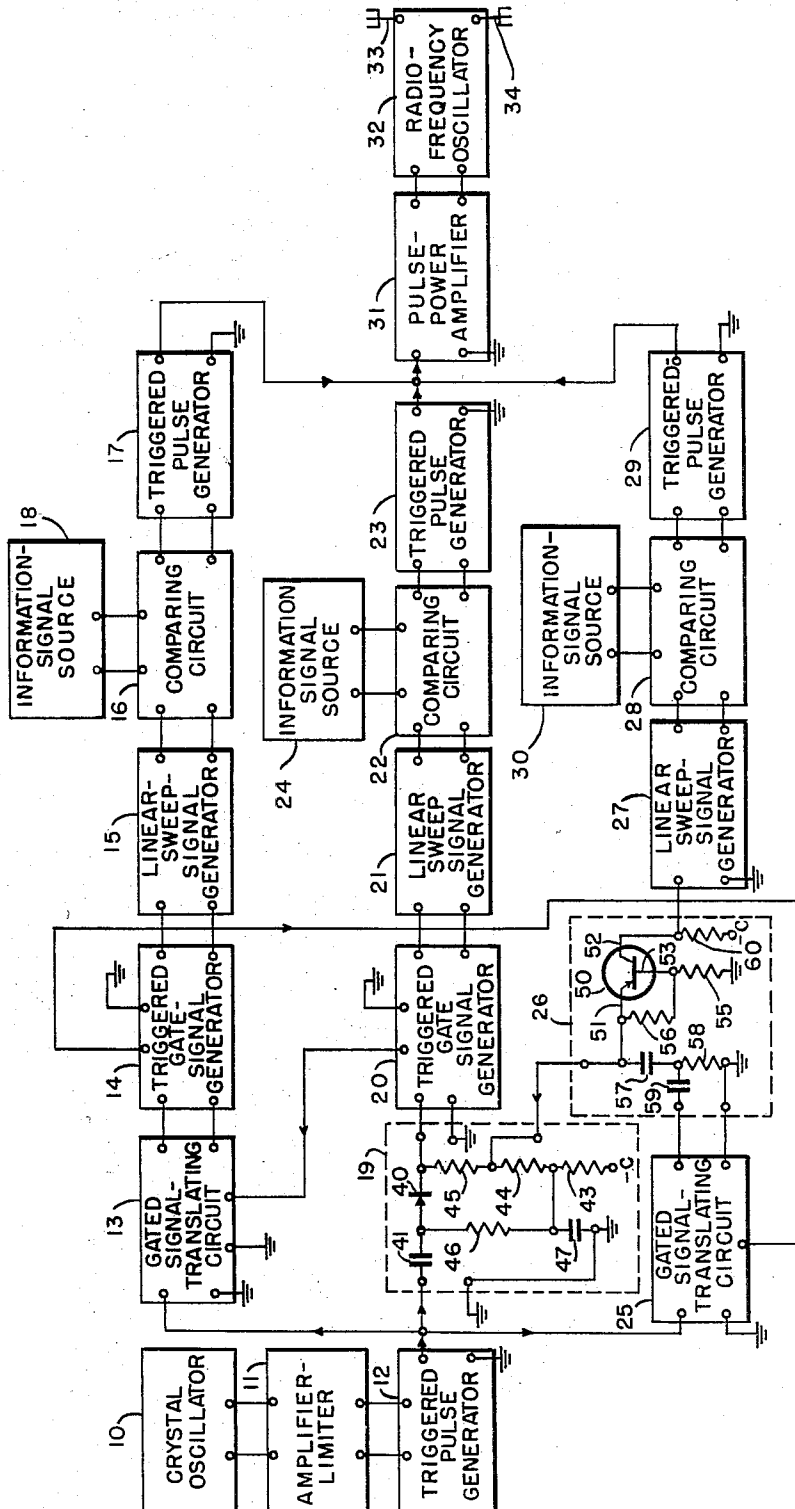
2,857,526

SELECTIVE PULSE-TRANSLATING SYSTEM

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2 Sheets-Sheet 1

FIG. 1



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2 Sheets-Sheet 2

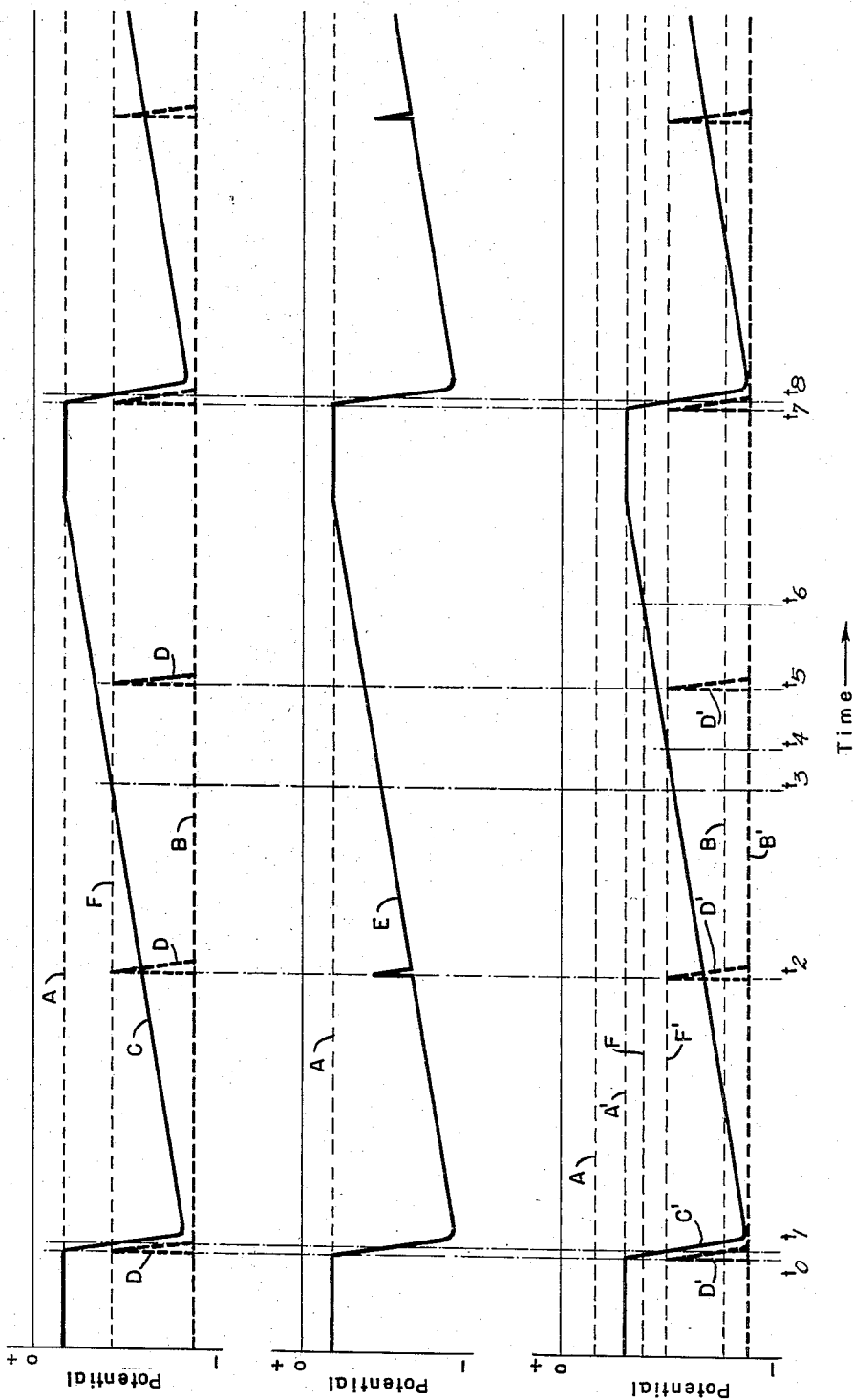


FIG. 2

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SELECTIVE PULSE-TRANSLATING SYSTEM

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GENERAL

This invention relates to selective pulse-translating systems and, particularly, to selective pulse-translating systems of the type gated by signals developed by a generator of the transistor type.

Selective pulse-translating systems are useful in, for example, telemetering equipment which transmits and receives a plurality of distinct and unrelated sets of information by means of a single signal carrier. Such circuits are particularly useful in connection with guided-missile and other applications where it is desired that maximum information be translated by a minimum amount of equipment. Such information, for example, may represent test-measurement data from various testing apparatus aboard the missile.

Telemetering equipment heretofore proposed has employed pulse-time modulation of the transmitter output signal to enable the various sets of information to be transmitted in time multiplex. For this purpose, the transmitting equipment has employed a plurality of gated signal-translating systems in order that the various information sources might individually be effective to control the modulation of the transmitter signal during successive time intervals.

Some selective pulse-translating systems previously proposed employ gated circuits controlled by signals developed by gate-signal generators. Vacuum tubes have heretofore been employed in these circuits of the telemetering equipment, but vacuum-tube circuits are undesirable where size, weight, and power requirements must be held at a minimum. Another system heretofore proposed utilizes a transistor gate-signal generator for supplying gating signals to a gated circuit but requires a coupling condenser of cumbersome physical size to pass satisfactorily to the gated circuit only the pulsating component of a gating signal of long duration, for example, 2000 microseconds. Another previously proposed type of system utilizes a relatively bulky potentiometer to apply an adjustable direct-current signal to the gated circuit to compensate for undesired direct-current variations applied thereto as a result of alterations of transistor parameters. Such alterations may be caused, for example, when commercially obtainable transistors of the same type, which may undesirably have different parameters, are substituted in the gate-signal generator as replacement parts.

It is an object of the invention, therefore, to provide a new and improved selective pulse-translating system which substantially avoids one or more of the foregoing limitations of such systems heretofore proposed.

It is another object of the invention to provide a new and improved relatively simple transistor-type selective pulse-translating system of reduced bulk.

It is a further object of the invention to provide a new and improved transistor-type selective pulse-translating system which automatically compensates for alterations of transistor parameters.

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In accordance with the invention, a selective pulse-translating system comprises a bias-responsive gating device for selectively translating pulses applied thereto and bias-circuit means including a unidirectional-potential source for normally biasing the gating device to a nontranslating condition. The system further includes a gate-signal generator including a transistor having an output electrode directly coupled to the gating device through the bias-circuit means and having a unidirectional-potential level partially determined by the parameters of the transistor for supplying to the gating device recurrent gate signals to condition the gating device for conduction during gating intervals. The system additionally includes potential-variation-attenuating impedance means included in the bias-circuit means and including a potential divider coupled between the unidirectional-potential source and the output electrode and having a tapped portion directly coupled across the gating device for developing and applying to the gating device a bias potential representative of said unidirectional-potential level but having substantially reduced magnitude variations relative thereto automatically to reduce variations in the duration of the gating intervals caused by alterations of the parameters of the transistor.

For a better understanding of the present invention, together with other and further objects thereof, reference is had to the following description taken in connection with the accompanying drawings, and its scope will be pointed out in the appended claims.

Referring to the drawings:

Fig. 1 is a circuit diagram, partly schematic, of a complete telemeter transmitter including a selective pulse-translating system in accordance with the present invention, and

Fig. 2 is a graph representing signals developed at various points of the Fig. 1 system and used in explaining the operation thereof.

Description of Fig. 1 telemeter transmitter

Referring to Fig. 1 of the drawings, the telemeter transmitter there represented comprises a source of precisely spaced periodic pulses including, for example, a crystal oscillator 10, an amplifier-limiter 11, and a triggered pulse generator 12, all of conventional construction and coupled in the order named. The transmitter further includes, for example, three similar time-modulation channels individually including unit groups 13-18, inclusive, 25-30, inclusive, and 19-24, inclusive, for individually controlling the modulation of the transmitter output signal during successive time intervals. Gated signal-translating circuits 13, 25, and 19 of the individual channels, constructed in accordance with the invention in combination with units 14, 26, and 20, respectively, and more fully described hereinafter, are coupled to the triggered pulse generator 12.

In the first channel there are coupled to the gated signal-translating circuit 13, in cascade, and in the order named, a triggered gate-signal generator 14, a linear sweep-signal generator 15, a comparing circuit 16, and a triggered pulse generator 17 which, except for the combination of units 13 and 14, may all be of conventional construction. Also coupled to the comparing circuit 16 is an information-signal source 18.

The second channel comprising units 25-30, inclusive, contains units corresponding to those of the first channel with the triggered gate-signal generator 26 shown in detail. The third channel comprising units 19-24, inclusive, also corresponds to the other channels with the gated signal-translating circuit 19 shown in detail. The output units of the time-modulation channels, namely, the trig-

gered pulse generators 17, 29, and 23 are coupled through a pulse-power amplifier 31 to a radio-frequency oscillator 32 which, in turn, is coupled to an antenna system 33, 34. Units 31 and 32 and the antenna system 33, 34 may also be of conventional construction.

The triggered gate-signal generator of each time-modulation channel is also coupled to the gated signal-translating circuit of the following channel, for example, the generator 14 of the first channel is coupled to the gated signal-translating circuit 25 of the second channel, generator 26 of the second channel is coupled to the gated signal-translating circuit 19 of the third channel, and the generator 20 of the third channel is coupled to the gated signal-translating circuit 13 of the first channel to complete a ring-type system for selectively translating pulses in the various channels.

While three time-modulation channels have been shown for explanatory purposes, it will be understood that a telemeter transmitter may contain any number of such channels. Also, as telemeter transmitters are often used in applications where space and size requirements are critical, it may be desirable that miniaturized circuitry including transistors and contact diodes be employed throughout the transmitter. The units 10-32, inclusive, with the exception of the combinations of gated signal-translating circuits 13, 25, and 19 and the generators 14, 26, and 20, respectively, may be of conventional construction and operation so that a detailed description and explanation of the operation thereof are unnecessary herein. The comparing circuits 16, 22, and 28 may comprise, for example, diode comparators of the type shown on page 338 of the text "Waveforms" by Chance et al., volume 19, MIT Radiation Laboratory Series, McGraw-Hill, 1949.

Operation of Fig. 1 telemeter transmitter

Considering briefly the general operation of the above-described telemeter transmitter as a whole, the crystal oscillator 10 generates a sinusoidal signal having a frequency of, for example, 1400 cycles per second which is supplied to the amplifier-limiter 11 wherein the sinusoidal signal is amplified and shaped to develop a periodic signal of rectangular wave form of corresponding frequency. This signal is supplied to the triggered pulse generator 12 which, in synchronism with the individual waves thereof generates periodic pulses of, for example, one-microsecond duration and occurring at a repetition frequency of, for example, 1400 pulses per second. These precisely timed periodic pulses from the generator 12 are applied to the input units of the three time-modulation channels 13-18, 25-30, and 19-24.

At any given instant, as will be more fully explained, hereinafter, the input unit or gated signal-translating circuit 13, 25, or 19 of one of the three time-modulation channels is in a translating condition while those of the other channels are in a nontranslating condition. The condition of each channel changes with time so that the periodic pulses from the generator 12 are selectively and successively translated by the gated circuits 13, 25, and 19 of the respective channels. In this manner, considering the pulses in arbitrary groups of three, every first pulse is translated by the gated circuit 13 of the first channel, every second pulse is translated by the gated circuit 25 of the second channel, and every third pulse is translated by the gated circuit 19 of the third channel.

Assuming for the present that the gated circuit 13 is maintained in a translating condition by a gate signal supplied thereto from generator 20 while the gated circuits 19 and 25 are in a nontranslating condition, then an initial one of the pulses from the generator 12 will be translated by the gated circuit 13 to the triggered gate-signal generator 14 to cause the generator 14 to generate a gate signal which is supplied to the linear-sweep-signal generator 15. This signal serves to initiate the generation in the sweep-signal generator 15 of a linear-sweep signal

of sawtooth wave form which is supplied to the comparing circuit 16. Also supplied to the comparing circuit 16 is an information signal from the information-signal source 18 representing, for example, information derived from a measuring device, such as a temperature-measuring thermocouple, a strain gauge of an electrical type, etc.

The comparing circuit 16 compares the linear sweep signal with the information signal and when the magnitude of the sweep signal equals the magnitude of the information signal, the comparing circuit 16 supplies a time-modulated short-duration pulse to the triggered pulse generator 17. This pulse is time-modulated in accordance with the information signal because the time at which it occurs relative to the initiation of the sweep signal is controlled by the magnitude of the information signal. In response to this pulse from the comparing circuit 16, the triggered pulse generator 17 generates a pulse of preferred magnitude and duration, for example one-half microsecond, which is supplied to the pulse-power amplifier 31 wherein it is amplified and supplied to the radio-frequency oscillator 32 for controlling the oscillations thereof. In response thereto, the radio-frequency oscillator 32 supplies a burst of radio-frequency energy to the antenna system 33, 34 from which it is radiated.

During the operation of the first time-modulation channel just discussed, the second and third channels remain inactive because the gated circuits 25 and 19, being in a nontranslating condition, prevent translation of the initial pulse by those channels. While generating the signal supplied to the sweep generator 15, the triggered gate-signal generator 14 also generates and supplies to the gated circuit 25 of the second channel another signal suitable for gating that circuit. This gate signal causes the gated circuit 25 to operate in a translating condition during a time interval satisfactory for allowing translation of a second of the crystal-controlled pulses supplied by the generator 12. The gated circuit 13 does not translate this second pulse and is no longer able to translate pulses because the gate signal previously supplied thereto by the pulse generator 20 of the third channel has ceased being effective and the circuit has returned to its nontranslating condition.

The second pulse from the crystal-controlled generator 12, which is translated by the gated circuit 25, is supplied to the triggered gate-signal generator 26 wherein it causes generation of a pulse signal which is supplied to the sweep-signal generator 27 and a gate signal which is supplied to the gated circuit 19 of the third channel. The operation of the remainder of the second channel is analogous to that of the first channel previously explained.

The gate signal from the generator 26 of the second channel enables the gated circuit 19 of the third channel to pass a third pulse from the crystal-controlled pulse generator 12. In the meantime, the gate signal supplied by the generator 14 of the first channel to the gated circuit 25 of the second channel is no longer effective, thereby causing that circuit to become nontranslating. The action of this third pulse from the crystal-controlled pulse generator 12 in the third time-modulation channel is similar to the operation of the other two channels, a gate signal generated by the generator 20 being effective subsequently to enable the gated circuit 13 of the first channel to pass a fourth pulse from the pulse generator 12.

As explained, the crystal-controlled periodic pulses selectively translated by the various time-modulation channels cause the generation of corresponding pulses which are time-modulated in accordance with desired items of information and are supplied to the radio-frequency oscillator 32 through the pulse-power amplifier 31. The radio-frequency oscillator 32, which is successively controlled by pulses from the first, second, and third time-modulation channels, generates a transmitter signal with three sets of interlaced pulses individually

representing the sets of information supplied by the three channels. In order to synchronize a receiver unit, one of the channels may have a fixed-magnitude signal supplied to the comparing circuit thereof by the corresponding information-signal source so that one set of pulses of the transmitted signal may be utilized for time-reference purposes.

Description of selective pulse-translating system of Fig. 1

Referring again to Fig. 1 of the drawings, there is represented in detail a selective pulse-translating system constructed in accordance with the present invention and preferably comprising a gated signal-translating circuit 19 and a triggered gate-signal generator 26. The system comprises a bias-responsive gating device, for example, an electron-discharge contact diode 40 coupled to the crystal-controlled triggered pulse generator 12 by a coupling condenser 41, for selectively translating pulses applied thereto.

The system further includes bias-circuit means for normally biasing the gating device 40 to a nontranslating condition. The bias-circuit means preferably includes a source of unidirectional potential —C connected across a potential divider comprising series-connected resistors 43 and 44 of unit 19 and a transistor emitter-base circuit including resistors 56 and 55 of unit 26. A coupling resistor 45 is connected between the junction of resistors 44 and 56 and the cathode of the gating device 40. The bias-circuit means also includes a coupling resistor 46 connected between a tap of the potential divider at the junction of resistors 43 and 44 and the anode of the gating device 40. A pulsating-signal by-pass condenser 47 is connected across the resistor 43 and the source —C.

The system additionally includes circuit means comprising a coupling condenser 59 and pulse-input resistor 58 of the gate-signal generator 26 for supplying recurrent trigger pulses translated from the crystal-controlled pulse generator 12 by the gated circuit 25.

The gate-signal generator 26 includes a transistor 50 having a first output electrode or emitter 51, a second output electrode or collector 52, and a base electrode 53. The emitter and base serve as trigger-pulse-input electrodes. The generator 26 may comprise, for example, a monostable switching circuit having an emitter-current cutoff operating mode. The emitter 51 is directly coupled to the gating device 40 through the previously mentioned bias-circuit means including resistors 43, 44, 55, 56 and has a unidirectional-potential level partially determined by the parameters of the transistor 50 for supplying to the gating device 40 recurrent gate signals of, for example, saw-tooth wave form and negative polarity relative to the unidirectional-potential level to condition the gating device 40 for conduction during gating intervals which ordinarily have a duration dependent on the magnitude of the saw-tooth gate signals. By the expression "to condition the gating device for conduction" it is meant that the gating device is capable of being conductive upon the application thereto of pulses to be translated. For some applications, the gating device may be rendered conductive by the gate signal alone or it may require the simultaneous application of the gate signal and a pulse to be translated to render the gating device conductive.

The resistor 55 is connected to the base 53 of the transistor 50 and is a preferred form of regenerative feedback impedance means common to both the emitter-base and collector-base circuits while the resistor 56 is directly connected between the emitter 51 and the base 53 for allowing a small emitter-base current to flow while the transistor 50 is in an emitter-current cutoff condition. Also coupled to the emitter 51 are a condenser 57 which, together with the resistors 55 and 56 and a series-connected pulse-input resistor 58, is primarily determinative of the duration of the emitter-gate signal. The collector

52 is coupled to a source of collector potential —C through a load resistor 60.

The selective pulse-translating system 19, 26 additionally comprises potential-variation-attenuating impedance means included in the bias-circuit means for developing and applying to the gating device 40 a bias potential representative of the unidirectional-potential level at the output electrode 51 but having substantially reduced magnitude variations relative thereto automatically to reduce variations in the duration of the gating intervals caused by alterations of the parameters of the transistor 50. This impedance means preferably includes a potential divider comprising the series-connected resistors 43 and 44 and having a tapped portion comprising resistor 44 directly coupled across the gating device 40 for developing and applying thereto a bias potential representative of the collector current during emitter-current cutoff intervals intervening the gating intervals. The resistor 43 preferably has a value greater than the resistor 44 and ordinarily approximately twice the value thereof.

Operation of selective pulse-translating system of Fig. 1

Considering the operation of the selective pulse-translating system 19, 26 just described, as is well known in the art, gate-signal generators comprising transistors may be constructed to have one or more stable operating modes and one or more unstable operating modes including a negative-resistance operating mode. These modes are ordinarily referred to in terms of operating potentials and currents of the transistor electrodes. One stable mode constitutes a low-conduction or emitter-current cutoff operating mode while one unstable mode constitutes a high-conduction emitter-current and collector-current saturation operating mode.

The transistor gate-signal generator 26 preferably has a steady-state operating condition, during intervals between trigger pulses from the gated circuit 25, in the cutoff mode because of the negative emitter-base bias developed across the resistor 56. While the generator 26 is in its steady-state operating condition, the potential-supply source —C causes current to flow through resistors 55 and 56 of the generator circuit 26 and through resistors 43 and 44 of the gated circuit 19. As this current flows through the resistor 44 in the gated circuit 19, it develops a bias-potential component thereacross for maintaining the diode 40 in a normally nontranslating condition. The negative unidirectional-potential reference level at the emitter 51 is represented by curve A of Fig. 2 while the average potential level at the junction of resistors 43 and 44 is represented by curve B of Fig. 2. During the intervals between pulses supplied by the generator 12, the potential represented by curve B is also the potential level at the anode of the gating device 40 and during intervals between gate signals supplied by the generator 26, the potential represented by curve A is also the potential level at the cathode of the gating device 40. The difference between the potentials represented by curves A and B, therefore, represents the reference operating bias of the diode 40.

At a time t_0 , one of the crystal-controlled pulses from the generator 12 is translated by the gated circuit 25 and applied with positive polarity through the coupling condenser 59 to the emitter-base circuit of the transistor 50 overcoming the negative emitter-base cutoff bias. This pulse, therefore, causes increasing emitter-to-base current flow of the transistor 50, thereby causing the generator 26 to switch to its unstable negative-resistance operating mode and, by virtue of current amplification within the transistor 50 and regenerative feed-back action afforded by the base resistor 55, both the emitter-base current flow and base-collector current flow increase rapidly. This results in an almost instantaneous switch of the generator to the saturation operating mode when the trigger pulse from the generator 12 is supplied. As this occurs, both

the emitter 51 and base 53 become more negative, and the condenser 57 in the emitter circuit begins to charge negatively through the emitter-base circuit including resistors 55, 56, and 58 while the emitter-base current flow diminishes as the emitter-base bias becomes more negative until the emitter-base current value is less than that required to maintain operation in the saturation mode. At this point, the generator re-enters the unstable negative-resistance mode and almost instantaneously switches back to the cut-off operating mode. Subsequently, as a consequence of the discharge of the condenser 57 through resistors 55, 56, 58 at a rate greater than the rate at which negative charge is being supplied thereto through resistors 43, 44 by the potential source $-C$, the initial steady-state operating condition is attained.

During the operation just discussed, the emitter potential becomes more negative relatively rapidly as a result of the charging of the condenser 57 through the emitter-base circuit of the transistor 50. After the generator 26 returns to its cutoff operating mode, the emitter potential slowly becomes less negative as the condenser 57 discharges through the resistors 55, 56, and 58. There is thus generated at the emitter of the transistor a potential of saw-tooth wave form which serves as the gate signal for the gated circuit 19. This saw-tooth potential is represented by curve C of Fig. 2, commencing at time t_0 and also represents the gate-signal potential variation at the cathode of the diode 40.

The potential at the anode of the diode 40, represented by curve D of Fig. 2, corresponds essentially to the potential level B with the crystal-controlled pulses supplied by the generator 12 through the coupling condenser 41 superimposed thereon. The peak magnitude of the crystal-controlled pulses of curve D represents a potential level as shown by curve F of Fig. 2 which, together with the saw-tooth gate signal represented by curve C, determines the translating or gating intervals. At a time t_1 , when the saw-tooth gate signal represented by Curve C becomes more negative than this peak-pulse potential level F, the diode 40 is conditioned for conduction. When this occurs, the gated circuit 19 is able to translate portions of the positive pulses, represented by curve D, applied thereto by the pulse generator 12. This gating interval during which the saw-tooth gate signal is more negative than the potential level F is of sufficient duration to allow translation of the next pulse supplied by the crystal-controlled pulse generator 12 which occurs at time t_2 . At the time t_3 , the saw-tooth gate signal decreases to a value equal to the potential level F so that the diode 40 is thereafter returned to a nontranslating condition and the gated circuit 19 no longer translates pulses until the occurrence of the next translating interval beginning at a time t_4 .

Curve E of Fig. 2 represents the potential at the cathode of the diode 40 which is applied to the output terminals of the gated circuit 19. This potential corresponds to the saw-tooth gate signal represented by curve C and supplied by the generator 26 with the portions of the pulses represented by curve D which are more positive than the saw-tooth gate signal during gating intervals superimposed thereon. It will be understood, of course, that the triggered gate-signal generator 20 preferably includes an input resistor—coupling condenser network similar to the resistor—condenser network 58, 59 of unit 26 for translating only the short-duration pulses of curve E to the remainder of the generator.

The advantages of the present selective pulse-translating system will be apparent when the effects of alterations in the parameters of the transistor 50 are considered. Alterations in the transistor parameters occurring, for example, when commercially obtainable transistors are substituted as replacement parts, cause variations in the cutoff mode collector current, thus causing variations in the potential developed across the feed-back resistor 55. These potential variations are supplied through the re-

sistor 56 to the gate-signal-output or emitter electrode 51, causing variations in the unidirectional-potential level, as represented by curve A, thereof. As a result, the current flowing through the potential-divider resistors 43 and 44 varies and hence the bias potential of the diode 40 exhibits a small portion of the variation therein.

Assume, for example, that a parameter alteration of the transistor 50 causes the cutoff mode-collector current to increase. This in turn causes the potential level at the base 53 and hence the unidirectional-potential reference level at the emitter 51 to become more negative. The current flowing through the potential-divider resistors consequently decreases. This current decrease shifts both the cathode and anode reference-potential levels of the diode 40, represented by curves A and B of Fig. 2, respectively, to values represented by curves A' and B' of Fig. 2 because of the decreased average potential drops across resistors 43 and 44. The difference in levels represented by curves B and B' is smaller than the difference in levels represented by curves A and A' because any change of emitter-potential level is attenuated by potential-dividing resistors 43 and 44. The shift in the emitter-potential level represented by curve A' causes a corresponding shift in the saw-tooth gate signal, as indicated by curve C' of Fig. 2. The shift in the anode reference-potential level of the diode 40 represented by curve B' causes a corresponding shift in the pulses, as indicated by curve D', and hence the peak-pulse potential level, as represented by curve F' of Fig. 2.

The decreased average operating bias potential developed across the potential-divider resistor 44, represented by the reduced difference between the potential levels, at the emitter 51 and the junction of the resistors 43 and 44 as represented by curves A' and B', causes a slight increase in the translating interval of the diode 40 as represented by the time difference t_3-t_4 of Fig. 2, the leading edge of the gate signal having negligible change in the translating interval associated therewith because of its relatively short rise time. The reduction of the bias potential of the diode 40 and the corresponding time difference t_3-t_4 has been exaggerated in the drawing for the sake of clarity. With proper selection of circuit parameters, this increase in the translating interval is sufficiently slight to prevent translation of an undesired pulse. The increase or change in translating interval is slight because the potential divider 43, 44 has, in effect, attenuated the potential variation supplied to the diode 40 as a result of the cutoff mode-collector current alteration, thereby causing the bias potential to have substantially reduced magnitude variations.

In selective pulse-translating systems of a type heretofore proposed, the reference-potential level supplied to the anode of the gated bias-responsive pulse-translating diode thereof remains at a predetermined value and does not vary in response to cutoff mode-collector current variations. Thus, the translating interval of the diode may increase by an interval, corresponding, for example, to the time difference t_3-t_6 of Fig. 2, sufficiently great to allow translation of an undesired pulse, corresponding, for example, to that occurring at time t_5 of Fig. 2. In a system constructed in accordance with the present invention, however, the anode reference-potential level, represented by curve B', as well as the cathode potential level, represented by A', of the diode 40 becomes more negative in response to the increase in cutoff mode-collector current, thus compensating for any variation thereof and thereby automatically reducing variations in the duration of the gating or translating intervals caused by alterations of the parameters of the transistor.

While applicant does not intend to limit the invention to any particular design constants, the following values have been found suitable for a selective pulse-translating system constructed in accordance with the present invention and particularly useful in a telemeter transmitter

having eight time-modulation channels similar to the three shown in Fig. 1:

Condenser 41	1500 micromicrofarads.
Condenser 47	0.1 microfarad.
Condenser 57	0.1 microfarad.
Condenser 59	1500 micromicrofarads.
Contact diode 40	Type 1N34 crystal diode.
Resistor 43	330,000 ohms.
Resistor 44	150,000 ohms.
Resistor 45	39,000 ohms.
Resistor 46	10,000 ohms.
Resistor 55	4,700 ohms.
Resistor 56	10,000 ohms.
Resistor 58	820 ohms.
Resistor 60	1,600 ohms.
Transistor 50	Type 1698.
Potential source —C	—45 volts.

From the foregoing description, it will be apparent that a selective pulse-translating system constructed in accordance with the present invention is a new and improved transistor-type selective pulse-translating system which automatically compensates for alterations of transistor parameters and avoids use of bulky circuit components, such as potentiometers and large coupling condensers, employed in systems of this type heretofore proposed.

While there has been described what is at present considered to be the preferred embodiment of this invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the invention, and it is, therefore, aimed to cover all such changes and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

1. A selective pulse-translating system comprising: a bias-responsive gating diode for selectively translating pulses applied thereto; bias-circuit means including a unidirectional potential source for normally biasing said diode to a nontranslating condition; circuit means for supplying recurrent trigger signals; a monostable switching circuit coupled to said trigger-signal-supply means and including a transistor having an emitter, a base, and a collector and including emitter-base and collector-base circuits having a common feed-back impedance means directly coupled to said emitter, said transistor having an emitter-current cutoff operating mode and said emitter being directly coupled to one side of said diode through said bias-circuit means and having a unidirectional-potential level partially determined by the parameters of said transistor for supplying to said diode recurrent gate signals of saw-tooth wave form and negative polarity relative to said unidirectional-potential level to condition said diode for conduction during gating intervals of duration dependent on the magnitude of said saw-tooth gate signals; and potential-variation-attenuating impedance means included in said bias-circuit means and including a potential divider coupled between said unidirectional-potential source and said emitter and having a tapped portion directly coupled across said diode for developing and applying thereto a bias potential representative of said collector current during emitter-current cutoff intervals intervening said gating intervals and representative of said unidirectional-potential level but having substantially reduced magnitude variations relative thereto automatically to reduce variations in the duration of said gating intervals caused by alterations of the parameters of said transistor.

2. A selective pulse-translating system comprising: a bias-responsive gating device for selectively translating pulses applied thereto; bias-circuit means including a unidirectional-potential source for normally biasing said gating device to a nontranslating condition; a gate-signal generator including a transistor having an output electrode directly coupled to said gating device through said bias-circuit means and having a unidirectional-potential level

partially determined by the parameters of said transistor for supplying to said gating device recurrent gate signals to condition said gating device for conduction during gating intervals; and potential-variation-attenuating impedance means included in said bias-circuit means and including a potential divider coupled between said unidirectional-potential source and said output electrode and having a tapped portion directly coupled across said gating device for developing and applying to said gating device a bias potential representative of said unidirectional-potential level but having substantially reduced magnitude variations relative thereto automatically to reduce variations in the duration of said gating intervals caused by alterations of the parameters of said transistor.

3. A selective pulse-translating system comprising: a bias-responsive gating device for selectively translating pulses applied thereto; bias-circuit means including a unidirectional-potential source for normally biasing said gating device to a nontranslating condition; circuit means for supplying recurrent trigger signals; a monostable switching circuit coupled to said trigger-signal-supply means and including a transistor having an output electrode directly coupled to said gating device through said bias-circuit means and having a unidirectional-potential level partially determined by the parameters of said transistor for supplying to said gating device recurrent gate signals to condition said gating device for conduction during gating intervals; and potential-variation-attenuating impedance means included in said bias-circuit means and including a potential divider coupled between said unidirectional-potential source and said output electrode and having a tapped portion directly coupled across said gating device for developing and applying to said gating device a bias potential representative of said unidirectional-potential level but having substantially reduced magnitude variations relative thereto automatically to reduce variations in the duration of said gating intervals caused by alterations of the parameters of said transistor.

4. A selective pulse-translating system comprising: a bias-responsive gating device for selectively translating pulses applied thereto; bias-circuit means including a unidirectional-potential source for normally biasing said gating device to a nontranslating condition; a saw-tooth gate-signal generator including a transistor having an output electrode directly coupled to said gating device through said bias-circuit means and having a unidirectional-potential level partially determined by the parameters of said transistor for supplying to said gating device recurrent gate signals of saw-tooth wave form and negative polarity relative to said unidirectional-potential level to condition said gating device for conduction during gating intervals of duration dependent on the magnitude of said saw-tooth gate signals; and potential-variation-attenuating impedance means included in said bias-circuit means and including a potential divider coupled between said unidirectional-potential source and said output electrode and having a tapped portion directly coupled across said gating device for developing and applying to said gating device a bias potential representative of said unidirectional-potential level but having substantially reduced magnitude variations relative thereto automatically to reduce variations in the duration of said gating intervals caused by alterations of the parameters of said transistor.

5. A selective pulse-translating system comprising: a bias-responsive gating diode for selectively translating pulses applied thereto; bias-circuit means including a unidirectional-potential source for normally biasing said diode to a nontranslating condition; a gate-signal generator including a transistor having an output electrode directly coupled to one electrode of said diode through said bias-circuit means and having a unidirectional-potential level partially determined by the parameters of said transistor for supplying to said diode recurrent gate signals to condition said diode for conduction during gating intervals; and potential-variation-attenuating impedance means

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included in said bias-circuit means and including a potential divider coupled between said unidirectional-potential source and said output electrode and having a tapped portion directly coupled across said gating diode for supplying thereto a potential representative of said unidirectional-potential level automatically to reduce variations in the duration of said gating intervals caused by alterations of the parameters of said transistor.

6. A selective pulse-translating system comprising: a bias-responsive gating device for selectively translating pulses applied thereto; bias-circuit means including a unidirectional-potential source for normally biasing said gating device to a nontranslating condition; a gate-signal generator including a transistor having an emitter, a base, and a collector and including emitter-base and collector-base circuits having a common feed-back impedance means directly coupled to said emitter, said transistor having an emitter-current cutoff operating mode and said emitter being directly coupled to said gating device through said bias-circuit means and having a unidirectional-potential level partially determined by the parameters of said transistor for supplying to said gating device recurrent gate signals to condition said gating device for conduction dur-

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ing gating intervals; and potential-variation-attenuating impedance means included in said bias-circuit means and including a potential divider coupled between said unidirectional-potential source and said emitter and having a tapped portion directly coupled across said gating device for developing and applying to said gating device a bias potential representative of said collector current during emitter-current cutoff intervals intervening said gating intervals and representative of said unidirectional-potential level but having substantially reduced magnitude variations relative thereto automatically to reduce variations in the duration of said gating intervals caused by alterations of the parameters of said transistor.

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