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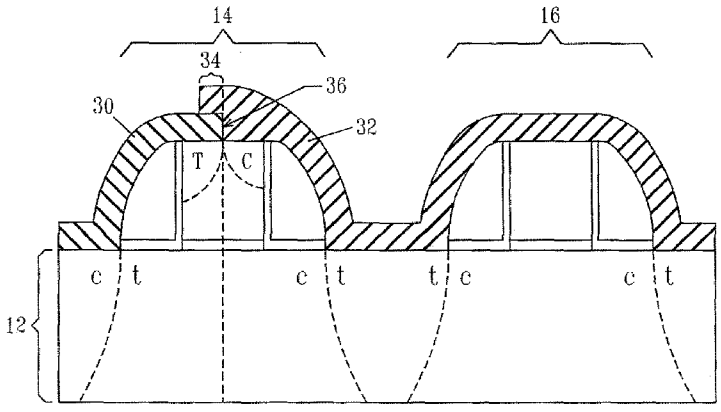
(54) **Title:** METHOD AND STRUCTURE FOR IMPROVING DEVICE PERFORMANCE VARIATION IN DUAL STRESS LINER TECHNOLOGY



(57) **Abstract:** A method and semiconductor structure that overcome the dual stress liner boundary problem, without significantly increasing the overall size of the integrated circuit, are provided. In accordance with the present invention, the dual stress liner boundary (36) or gap therebetween is forced to land on a neighboring dummy gate region (14). By forcing the dual stress liner boundary or gap between the liners (30, 32) to land on the dummy gate region, the large stresses associated with the dual stress liner boundary (36) or gap are transferred to the dummy gate region, not the semiconductor substrate (12). Thus, the impact of the dual stress liner boundary on the nearest neighboring FET (16) is reduced. Additionally, benefits of device variability and packing density are achieved utilizing the present invention.

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METHOD AND STRUCTURE FOR IMPROVING DEVICE PERFORMANCE VARIATION IN DUAL STRESS LINER TECHNOLOGY

DESCRIPTION

Field of the Invention

The present invention relates to a semiconductor structure and a method of fabricating the same. More particularly, the present invention relates to a complementary metal oxide semiconductor (CMOS) structure that has improved device performance, which is obtained by using a modified dual stress liner technology. The present invention also provides a method of fabricating such a CMOS structure using the modified dual stress liner technology.

Background of the Invention

For more than three decades, the continued miniaturization of silicon metal oxide semiconductor field effect transistors (MOSFETs) has driven the worldwide semiconductor industry. Various showstoppers to continued scaling have been predicated for decades, but a history of innovation has sustained Moore's Law in spite of many challenges. However, there are growing signs today that metal oxide semiconductor transistors are beginning to reach their traditional scaling limits.

Since it has become increasingly difficult to improve MOSFETs and therefore CMOS performance through continued scaling, methods for improving performance without scaling have become critical. One approach for doing this is to increase carrier (electron and/or hole) mobilities. Increased carrier mobility can be obtained, for example, by introducing the appropriate stress/strain into the semiconductor lattice.

The application of stress changes the lattice dimensions of the semiconductor substrate. By changing the lattice dimensions, the electronic band structure of the material is changed as well. This results in changes in carrier transport properties such as carrier scattering rates and effective mass, which can be dramatic in certain cases. The application of physical

stress (tensile or compressive) can be further used to enhance the performance of devices fabricated on the semiconductor substrates.

Compressive strain along the device channel increases drive current in p-type field effect transistors (pFETs) and decreases drive current in n-type field effect transistors (nFETs). Tensile strain along the device channel increases drive current in nFETs and decreases drive current in pFETs.

Stress can be introduced into a single crystal oriented substrate by several methods including, for example, forming a stress liner on top of the substrate and around the gate region. Depending on the conductivity type of the FET (i.e., p or n), the stress liner is optimally under tensile stress (preferred for nFETs) or compressive stress (preferred for pFETs). When nFETs and pFETs are integrated onto the same semiconductor substrate, dual stress liner technology is typically used in which a first stress liner under tensile stress is formed around each nFET, while a second stress liner under compressive stress is formed around each pFET. It is noted that the order of forming the stress liners may be variable. For example, the compressive stress liner may be formed prior to the tensile stress liner or visa versa.

However, the boundary between tensile and compressive stress liners in dual stress liner (DSL) technology also induces stress in the substrate, which can influence transistor performance as well. When the DSL boundary is in close proximity (with a lateral distance of about 5 microns or less) from an FET, and oriented parallel to the gate region, a degradation of the devices in proximity to the boundary has been observed. Degradation of 25% pFET and 18% nFET (saturation current at a fixed overdrive) have been demonstrated on recent CMOS structures, which is solely attributed to the DSL boundary influence mentioned above.

Reference is now made to FIGS. 1A-1D which illustrates the DSL boundary influence in greater detail for the case in which the tensile stress liner is formed prior to the formation of the compressive stress liner; in this case the compressive stress liner overlaps a portion of the tensile stress liner. FIG. 1A illustrates a portion of a non-stressed semiconductor substrate 100 that has a tensile stress liner 102 formed on a surface thereof. It is noted that no FET

structures are shown in FIG. 1A since they lay to the periphery of the portion of the substrate 100 shown in FIG. 1A. The FETs are formed prior to disposing the tensile stress liner 102 on the substrate.

FIG. 1B illustrates the structure of FIG. 1A after patterning the tensile stress liner 102 by lithography and etching. As shown, an edge force 106 is created on the substrate 100. Moreover, the tensile stress liner 102 creates local stress in the substrate that decays with distance from the etched edge of the liner 102. In FIG. 1B, reference numeral 108 denotes a region of the substrate 100 under compression, while reference numeral 110 denotes a region of the substrate under tension. The dotted line (designated as 112) denotes a zero stress line.

FIG. 1C illustrates the structure of FIG. 1B after forming a compressive stress liner 114 thereon. The overlap region (i.e., boundary) 119 of the dual liners magnifies the edge force 106. Depending on the relative strengths of the tensile and compressive liners, the zero stress contour can take the form of 112, or either of the two other contours indicated by 112'.

FIG. 1D is an expanded view of FIG. 1C showing the presence of an FET 120 on a surface of the substrate 100. In this drawing, the substrate is under the following stresses (i) compression (c) under the FET 120 (from left spacer outer edge to right spacer outer edge), (ii) tension (t) beneath the compressive liner 114, and (iii) compression (c) under the tensile liner 102.

The problem with such a structure is that the dual stress liner boundary 119 is in longitudinal proximity to the FET 120 which results in substantial degradation of the performance of the FET. The term "longitudinal proximity" is used in the present application to denote that the dual stress liner boundary 119 is located at a distance lengthwise from the FET that is about 5 microns or less. This degradation is observed for both nFETs and pFETs. In particular, it was been found that the longitudinal stress, which is related to the dual stress liner boundary 119, reduces the stress in the FET channel.

One solution to this dual stress liner boundary problem is to design an integrated circuit in which the longitudinal boundaries are placed far away (a longitudinal distance of greater

than 5 microns) from the FET devices. Although such a solution is feasible, it does come with an area penalty that increases the overall size of the integrated circuit. Such an increase in size contradicts the current trend in shrinking integrated circuits.

As such, a method is needed which addresses the dual stress liner boundary problem without significantly increasing the overall size of the integrated circuit.

Summary of the Invention

The present invention aims to provide a method and semiconductor structure that overcomes the dual stress liner boundary problem, without significantly increasing the overall size of the integrated circuit. In accordance with a first embodiment of the present invention, the dual stress liner boundary or gap is forced to land on a neighboring dummy gate region. By forcing the dual stress liner boundary or gap to land on the neighboring dummy gate region, the large stresses associated with the dual stress liner boundary are transferred to the dummy gate material, not the semiconductor substrate. The dummy gate region may be located within an active area of the FET or it may be present atop an isolation region such as a trench isolation region. Thus, the impact of the dual stress liner boundary on the nearest neighboring FET is reduced. Additionally, benefits of device variability and packing density are achieved utilizing the present invention.

In general terms, the present invention provides, in a first embodiment, a semiconductor structure that includes:

a semiconductor substrate having at least one dummy gate region in proximity to at least one active gate region; and

a tensile stress liner and a compressive stress liner located on said substrate, wherein said tensile stress liner and said compressive stress liner are present at least in part over said at least one dummy gate region such that a boundary or gap that exists between the stress liners lays on top of said at least one dummy gate region.

The at least one active gate region may comprise an FET, such as at least one pFET or at least one nFET. Combinations of nFETs and pFETs are also contemplated. In accordance with the presence invention, the boundary or gap between the compressive stress liner and the tensile stress liner is such that it falls atop a dummy gate region that is in close proximity to each FET present on the substrate.

In accordance with the present invention, the compressive stress liner and the tensile stress liner may overlap each other, perfectly abut each other, or a gap may be present between the two liners. In accordance with the present invention the 'boundary' is created by the overlap or perfect abutment of the two stress liners, while the 'gap' is created by an underlap of the two stress liners.

In one preferred embodiment of the present invention, the inventive structure comprises:

a semiconductor substrate having at least one dummy gate region in proximity to at least one pFET; and

a tensile stress liner and a compressive stress liner located on said substrate, wherein said compressive stress liner covers the at least one pFET and is present at least in part over said at least one dummy gate region such that a boundary or gap exists between the stress liners that lands on top of said at least one dummy gate region.

In another preferred embodiment of the present invention, the inventive structure comprises:

a semiconductor substrate having at least one dummy gate region in proximity to at least one nFET; and

a tensile stress liner and a compressive stress liner located on said substrate, wherein said tensile stress liner covers the at least one nFET and is present at least in part over said at least one dummy gate region such that a boundary or gap exists between the stress liners that lands on top of said at least one dummy gate region.

In addition to the semiconductor structure described above, the present invention also provides a method of fabricating the same. In general terms, the method of the present invention includes:

providing a semiconductor substrate having at least one dummy gate region in proximity to at least one active gate region; and

disposing, in any order, a tensile stress liner and a compressive stress liner on said substrate, wherein said tensile stress liner and said compressive stress liner are present at least in part over said at least one dummy gate region such that a boundary or gap between the stress liners lands on top of said at least one dummy gate region.

In addition to using dual stress liners, the present application can also be applied to a semiconductor structure in which a single stress liner is present. In such an instance, the etched edge of the single stress liner is forced to land atop the dummy gate region of the structure.

Brief Description of the Drawings

FIGS. 1A-1D are pictorial representations (through cross sectional views) depicting prior art dual stress liner technology.

FIGS. 2A-2C are pictorial representations (through cross sectional views) depicting the modified dual stress liner technology according to an embodiment of the present invention.

FIG. 3 is a pictorial representation (through a cross sectional view) depicting an alternative embodiment of the present invention.

FIG. 4 is a pictorial representation (through a cross sectional view) depicting another alternative embodiment of the present invention.

FIG. 5 is a pictorial representation (through a cross sectional view) depicting yet another alternative embodiment of the present invention.

Detailed Description of the Invention

Preferred embodiments which provide a method and structure for improving device performance utilizing a variation in the conventional dual stress liner technology, will now be described in greater detail by referring to the following discussion and drawings that accompany the present application. It is noted that the drawings of the present application are provided for illustrative purposes and, as such, they are not drawn to scale.

In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, in order to provide a thorough understanding of the present invention. However, it will be appreciated by one of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well-known structures or processing steps have not been described in detail in order to avoid obscuring the invention.

The present invention provides a method and structure in which a modified dual stress liner process is employed. The modified dual stress liner process of the present invention forces the dual stress liner boundary or gap to land on a dummy gate region that is in close proximity to an active gate region. By "dummy gate region", it is meant a non-active gate region that is typically not a functional transistor, and is typically formed to minimize the variability of nearby active gates. The term "active gate region" denotes a functional transistor gate. By close proximity" it is meant that the boundary between the dual stress liners is from about 5 microns or less from the active gate region.

Reference is first made to FIG. 2A which illustrates an initial structure 10 that is employed in the present invention. As shown, the initial structure 10 includes a semiconductor substrate 12 having at least one dummy gate region 14 and at least one active gate region 16 in close proximity to each other. In accordance with the present invention, the dummy gate region 14 may be located atop an active region of the substrate as is shown in this drawing,

or alternatively, the dummy gate may be located atop an isolation region present within or on the substrate.

The at least one active gate region 16 may be an nFET or a pFET. Combinations of pFETs and nFETs are also contemplated in the present invention.

Each dummy gate region 14 and each active gate 16 present on the substrate 12 includes a gate dielectric 18 located on a surface of the substrate 12 and a gate electrode 20 located on the gate dielectric 20. Each active gate region 16 includes a channel region (not shown) located within the substrate 12 and beneath the gate dielectric/gate electrode stack. Source/drain regions (not shown) are located adjacent to the channel region in each of the active gate regions. Each dummy gate region 14 and active gate region 16 may also include at least one sidewall spacer. In FIG. 1A, a pair of sidewall spacers including an inner L-shaped spacer 26 and an outer spacer 28 is shown. The at least one sidewall spacer is optional, and need not be used in all instances.

The at least one dummy gate region 14 and the at least one active gate region 16 are fabricated using conventional complementary metal oxide semiconductor processing techniques well known to those skilled in the art. For example, deposition of various material layers, lithography, etching, ion implantation and annealing can be used in forming the active gate regions. The same processing steps can be used in forming the at least one dummy gate region 14. Each gate region (active and non-active) can also be formed utilizing a replacement gate process.

The semiconductor substrate 12 includes any semiconductor material including, for example, Si, SiC, SiGeC, Ge, SiGe, Ga, GaAs, InAs, InP as well as other III/V or II/VI compound semiconductors. Layered semiconductors such as, for example, Si/SiGe and semiconductor-on-insulators (SOIs) are also contemplated herein. Typically, the semiconductor substrate 12 is a Si-containing semiconductor such as, for example, Si, SiC, SiGe, SiGeC, or a silicon-on-insulator. The substrate 12 may be unstrained, strained or include regions of strain and unstrain therein. The substrate 12 may be intrinsic or it may be doped with, for example, but not limited to: B, As or P.

When SOI substrates are employed, those substrates include top and bottom semiconductor, e.g., Si, layers that are separated at least in part by a buried insulating layer. The buried insulating layer includes, for example, a crystalline or non-crystalline oxide, nitride or any combination thereof. Preferably, the buried insulating layer is an oxide. Typically, the buried insulating layer is formed during initial stages of a layer transfer process or during an ion implantation and annealing process, such as, for example, SIMOX (separation by ion implantation of oxygen).

The substrate 12 may have a single crystal orientation or alternatively hybrid semiconductor substrates having surface regions of different crystal orientations can also be employed. The hybrid substrate allows for fabricating a FET upon a specific crystal orientation that enhances the performance of each FET formed. For example, the hybrid substrate allows for providing a structure in which a pFET can be formed on a (110) crystal orientation, while the nFET can be formed on a (100) crystal orientation. When a hybrid substrate is used, it may have SOI-like properties, bulk-like properties or a combination of SOI- and bulk-like properties.

In some embodiments of the present invention, at least one isolation region (not shown) is formed into the substrate 12. The at least one isolation region may include a trench isolation region, a field oxide isolation region or combinations thereof. The isolation regions are formed utilizing processing techniques well known to those skilled in the art.

The gate dielectric 18 present in each of the gate regions can comprise the same or different insulating material. For example, the gate dielectric 18 can be comprised of an oxide, nitride, oxynitride, high k material (i.e., a dielectric material having a dielectric constant that is greater than silicon dioxide) or any combination thereof including multilayers. Preferably, the gate dielectric 18 is comprised of an oxide such as, for example, SiO_2.

The gate electrode 20 of each of the gate regions (active and dummy) can be comprised of the same or different conductive material, including, for example, polySi, SiGe, a metal, a metal alloy, a metal silicide, a metal nitride or combinations including multilayers thereof. When multilayers are present, a diffusion barrier (not shown), such as TiN or TaN, can be

positioned between each of the conductive layers. A capping layer (also not shown), such as an oxide, or nitride, can be located atop the gate electrode of each of the gate regions the presence of the capping layer can be used to prevent subsequent formation of a silicide contact on said gate electrode. The silicide contact on said gate electrode is typically formed when the gate electrode includes a Si-containing material and no capping layer is present. Preferably, the gate electrode within each of the gate regions comprises polySi or polySiGe.

The at least one spacer that is optionally present is typically comprised of an oxide, nitride or oxynitride including combinations and multilayers thereof. Although optional, typically one spacer is present in the inventive structure. In the illustrated example, a pair of spacers is shown. Typically, the inner L-shaped spacer 26 is comprised on an oxide, while the outer spacer 28 is comprised of a nitride.

As indicated above, each active gate region 16 also includes S/D regions which typically include extension regions and deep S/D diffusion regions. The source/drain regions together with the gate electrode 20 define the length of the channel in the active gate region 16. It is noted that S/D extensions and S/D diffusion regions are comprised of an upper portion of the semiconductor substrate 12 that has been doped with either n- or p-type dopants by ion implantation. The S/D extensions are typically shallower in depth than the S/D diffusion regions.

Next, and as shown in FIG. 2B, a first stress liner 30 is formed on a portion of the substrate 12 as well as covering a portion of the dummy gate region 14. The terms "first and second stress liner" are used throughout this application to denote stress inducing materials that have been deposited and patterned by lithography and etching. In accordance with the method of the present invention, the first stress liner may be a tensile stress liner or a compressive stress liner. In a preferred embodiment, and for the drawings illustrated in the present application, the first stress liner 30 is a tensile stress liner. This configuration assumes that the active gate region 16 is a pFET. A compressive stress liner would be used for the first stress liner 30 when the active gate region 16 is an nFET.

The presence of the stress liner results in stresses being introduced into the substrate 12. In the drawing, the lower case 't' denotes the tensile stress induced into the substrate by the presence of the tensile stress liner, while the lower case 'c' denotes the compressive stress induced by the presence of the tensile stress liner on the substrate 12. The dotted lines represent the zero stress lines present in the substrate. It is noted that when the first stress liner 30 is a compressive stress liner, the position of the lower case c and t would be reversed from that shown in FIG. 2B.

The first stress liner 30 is comprised of any stress inducing material such as a nitride or a high density plasma (HDP) oxide, or a combination thereof. The stress liner can formed by various chemical vapor deposition (CVD) processes such as low pressure CVD (LPCVD), plasma enhanced CVD (PECVD), rapid thermal CVD (RTCVD) or BTBAS-based ($C_8H_{22}N_2Si$ reacted with ammonia) CVD, where BTBAS is a modern metalorganic precursor for CVD application. The later process provides a low temperature nitride film having high stress. Following deposition of the stress liner material, lithography and etching are used in forming the first stress liner 30.

Preferably, the first stress liner 30 comprises a nitride, such as Si_3N_4, wherein the process conditions of the deposition process are selected to provide an intrinsic tensile strain within the deposited layer. For example, plasma enhanced chemical vapor deposition (PECVD) can provide nitride stress liners having an intrinsic tensile strain. The stress state (tensile or compressive) of the stress liners deposited by PECVD can be controlled by changing the deposition conditions to alter the reaction rate within the deposition chamber. More specifically, the stress state of a deposited nitride stress liner may be set by changing the deposition conditions such as: SiH_4/N_2/He gas flow rate, pressure, RF power, and electrode gap.

In another example, rapid thermal chemical vapor deposition (RTCVD) can provide nitride tensile stress liners having an internal tensile strain. The magnitude of the internal tensile strain produced within the nitride tensile stress liner deposited by RTCVD can be controlled by changing the deposition conditions. More specifically, the magnitude of the tensile strain

within the nitride stress liner may be set by changing deposition conditions such as: precursor composition, precursor flow rate and temperature.

FIG. 2C illustrates the structure of FIG. 2B after a second stress liner 32 is formed thereon. In accordance with the present invention, the second stress liner 32 covers a portion of the substrate 12 and the entire active gate region 16 as well as a portion of the dummy gate region 14. As shown, the second stress liner 32 extends atop a small segment of the patterned stress liner 30 such that an overlap 34 of the first and second stress liners is created atop the dummy gate region 14. In one embodiment, a compressive stress liner overlaps a segment of the tensile stress liner atop the dummy gate region 14. In another embodiment, a tensile stress liner overlaps a segment of a compressive stress liner. Additional embodiments have compressive stress liner and tensile stress liner in close proximity (within approximately 200 nm), but not directly overlapping.

Due to the location of the overlap 34, the dual stress liner boundary (surfaces of the stress liners that abut each other but do not overlap) is present atop the dummy gate region 14 as is shown in FIG. 2C. The large stress forces (represented by upper case 'T' for tensile, and by upper case "C" for compressive) generated by the dual stress liner boundary 36 are located within the dummy gate region 14, not the substrate 12 as well the case with prior art dual stress liner technology. The dotted lines in the drawing again refer to the zero stress lines.

In accordance with the method of the present invention, the second stress liner 32 may be a tensile stress liner or a compressive stress liner with the proviso that it has opposite stress sign as compared to the first stress liner 30. In a preferred embodiment, and for the drawings illustrated in the present application, the second stress liner 32 is a compressive stress liner. This configuration assumes that the active gate region 16 is pFET. A tensile stress liner would be used when the active device region 16 is an nFET.

The presence of the second stress liner 32 results in stress being introduced into the substrate 12. In the drawing, the upper case 'C' denotes the compressive stress induced by the presence of the second compressive stress liner on the substrate 12. The dotted lines in the drawing again refer to the zero stress lines.

The second stress liner 32 is formed utilizing the same basic processing steps as the first stress liner 30. Hence, deposition, lithography and etching are used in forming the second stress liner 32. The second stress liner is comprised of the same or different stress inducing materials as mentioned above for the first stress liner 30.

FIG. 3 shows an alternative structure that can be formed by modifying the basic description provided above for FIGS. 2A-2C. In the structure illustrated in FIG. 3 the dummy gate is formed atop an isolation region 50 such as a trench isolation region. The isolation region 50 is formed into the substrate 12 utilizing techniques that are well known to those skilled in the art. For example, a trench isolation region can be formed by first providing a trench into the substrate by lithograpy and etching, the trench is then filled with a trench dielectric material, typically a trench oxide, and a planariziation process is then performed. It is noted that although this structure includes overlapped stress liners atop the dummy gate region, neither the invention nor this embodiment is limited to the same. Instead, the stress liners may be perfectly abutted to each other over the dummy gate region (as shown in FIG. 4) or a gap 52 may be present between the stress liners atop the dummy gate region (as shown in FIG. 5). These alternative structures can of course be used in conjugation with the embodiment depicted in FIGS. 2A-2C.

In addition to the above embodiments and alternative structures, the present invention also contemplates an embodiment wherein one of the stress liners is removed from the structure such that a single stress liner is present in which the single stress liner has an edge that lands atop the dummy gate region. For example, a system in which a tensile stress liner is deposited but removed from a pFET; no compressive liner is used.

As indicated above, the present invention provides a method and semiconductor structure that overcomes the dual stress liner boundary problem, without significantly increasing the overall size of the integrated circuit. This is achieved in the present invention by ensuring that the dual stress liner boundary between tensile and compressive stress liners is forced to land on a neighboring dummy gate region. By forcing the dual stress liner boundary to land on the dummy gate region, the large stresses associated with the dual stress liner boundary are transferred to the dummy gate region, not directly to the semiconductor substrate. Thus,

the impact of the dual stress liner boundary on the nearest neighboring FET is reduced. Additionally, benefits of device variability and packing density are achieved utilizing the present invention.

While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

For the avoidance of doubt, the term "comprising", as used herein throughout the description and claims is not to be construed as meaning "consisting only of".

CLAIMS

1. A semiconductor structure comprising:

a semiconductor substrate having at least one dummy gate region in proximity to at least one active gate region; and

a tensile stress liner and a compressive stress liner located on said substrate, wherein said tensile stress liner and said compressive stress liner are present in part over said at least one dummy gate region such that a boundary or gap exists between the stress liners that lands on top of said at least one dummy gate region.

2. The semiconductor structure of Claim 1, wherein said semiconductor substrate comprises a Si-containing substrate having a single crystal orientation.

3. The semiconductor structure of Claim 1 or 2, wherein said semiconductor substrate is a hybrid substrate including surface regions of different crystal orientations, wherein each active gate region is disposed on a crystal orientation that provides optimal device performance.

4. The semiconductor structure of Claim 1, 2 or 3, wherein said compressive stress liner covers said at least one active gate region and overlaps a segment of the tensile stress liner atop said dummy gate region.

5. The semiconductor structure of Claim 4, wherein said at least one active gate region is a pFET.

6. The semiconductor structure of any preceding Claim, wherein said tensile stress liner covers said at least one active gate region and overlaps a segment of the compressive stress liner atop said dummy gate region.

7. The semiconductor structure of Claim 6 wherein said at least one active gate region is an nFET.

8. The semiconductor structure of any preceding Claim, wherein said stress liners abut each other, over said dummy gate region or a space is present there between.

9. The semiconductor structure of any preceding Claim, wherein said dummy gate region is located atop an isolation region that is located within or on said semiconductor substrate.

10. A semiconductor structure comprising:

a semiconductor substrate having at least one dummy gate region in proximity to at least one pFET; and

a tensile stress liner and a compressive stress liner located on said substrate, wherein said compressive stress liner covers the at least one pFET and is present in part over said at least one dummy gate region such that a boundary or gap exists between the stress liners that lands on top of said at least one dummy gate region.

11. The semiconductor structure of Claim 10, wherein stress liners overlap each other atop the dummy gate region.

12. The semiconductor structure of Claim 10 or 11, wherein stress liners abut each other atop the dummy gate region or a space is located between the two stress liners atop the dummy gate region.

13. The semiconductor structure of Claim 10, 11 or 12, wherein said dummy gate region is located atop an isolation region that is located within or on said semiconductor substrate.

14. A semiconductor structure comprising:

a semiconductor substrate having at least one dummy gate region in proximity to at least one nFET; and

a tensile stress liner and a compressive stress liner located on said substrate, wherein said tensile stress liner covers the at least one nFET and is present in part over said at least one dummy gate region such that an boundary or gap exists between the stress liners that lands on top of said at least one dummy gate region.

15. The semiconductor structure of Claim 14, wherein stress liners overlap each other atop the dummy gate region.

16. The semiconductor structure of Claim 14 or 15, wherein stress liners abut each other atop the dummy gate region or a space is located between the two stress liners atop the dummy gate region.

17. The semiconductor structure of Claim 14, 15 or 16, wherein said dummy gate region is located atop an isolation region that is located within or on said semiconductor substrate.

18. A semiconductor structure comprising:

a semiconductor substrate having at least one dummy gate region in proximity to at least one FET; and

a tensile stress liner or a compressive stress liner located on said substrate, wherein said stress liner covers the at least one FET and is present in part over said at least one dummy gate region such that an etched edge of the stress liner lands on top of said at least one dummy gate region.

19. A method of forming a semiconductor structure comprising:

providing a semiconductor substrate having at least one dummy gate region in proximity to at least one active gate region; and

disposing, in any order, a tensile stress liner and a compressive stress liner on said substrate, wherein said tensile stress liner and said compressive stress liner are present in part over said at least one dummy gate region such that a boundary or gap exists between the stress liners that lands on top of said at least one dummy gate region.

20. The method of Claim 19, wherein said tensile stress liner is disposed first followed by said compressive stress liner thereby said compressive stress liner covers said at least one active gate region and overlaps a segment of the tensile stress liner atop said dummy gate region.

21. The method of Claim 19 or 20, wherein said compressive stress liner is disposed first followed by said tensile stress liner thereby said tensile stress liner covers said at least one active gate region and overlaps a segment of the compressive stress liner atop said dummy gate region.

22. The method of Claim 19, 20 or 21, wherein said disposing comprises deposition, lithography and etching.

23. The method of any of Claims 19 to 22, wherein disposing comprises a chemical vapor deposition process selected from the group consisting of low pressure chemical vapor deposition, plasma enhanced chemical vapor deposition, rapid thermal chemical vapor deposition, and BTBAS-based chemical vapor deposition.

24. The method of any of Claims 19 to 23, wherein semiconductor substrate is a hybrid substrate including surface regions of different crystal orientations, wherein each active gate region is disposed on a crystal orientation that provides optimal device performance.

25. The method of any of Claims 19 to 24, wherein each dummy gate region comprises a stack including, from bottom to top, a gate dielectric and a gate electrode.

26. The method of Claim 19 to 25, wherein each active gate region comprises a stack including, from bottom to top, gate dielectric and a gate electrode, a channel region between said stack and adjoining source/drain regions.

27. The method of any of Claims 19 to 26, wherein stress liners abut each other atop the dummy gate region or a space is located between the two stress liners atop the dummy gate region.

28. The method of any of Claims 19 to 27, wherein said dummy gate region is located atop an isolation region that is located within or on said semiconductor substrate.

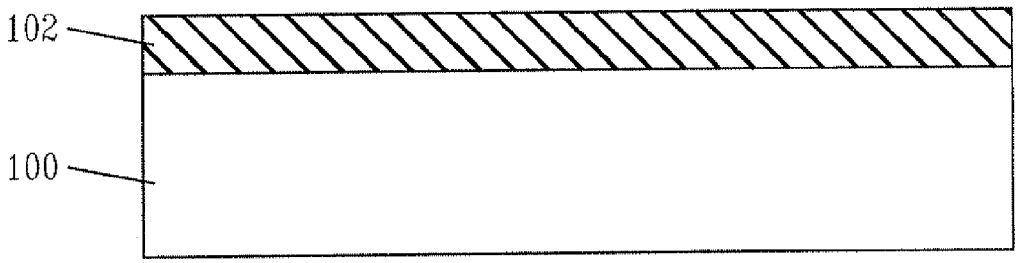

FIG. 1A (Prior Art)

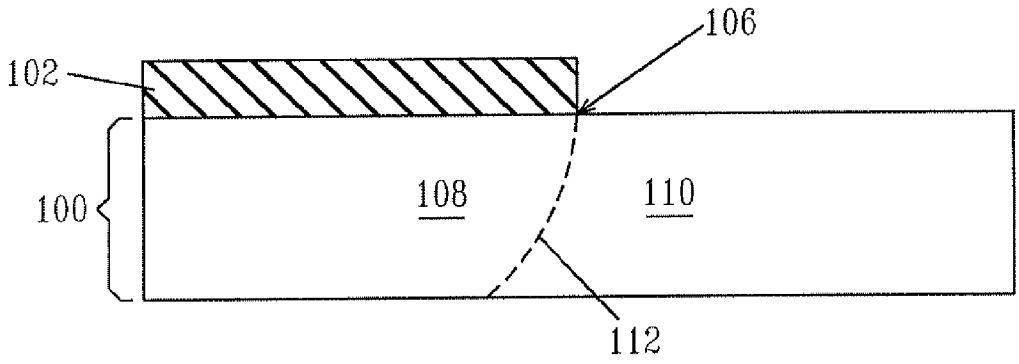

FIG. 1B (Prior Art)

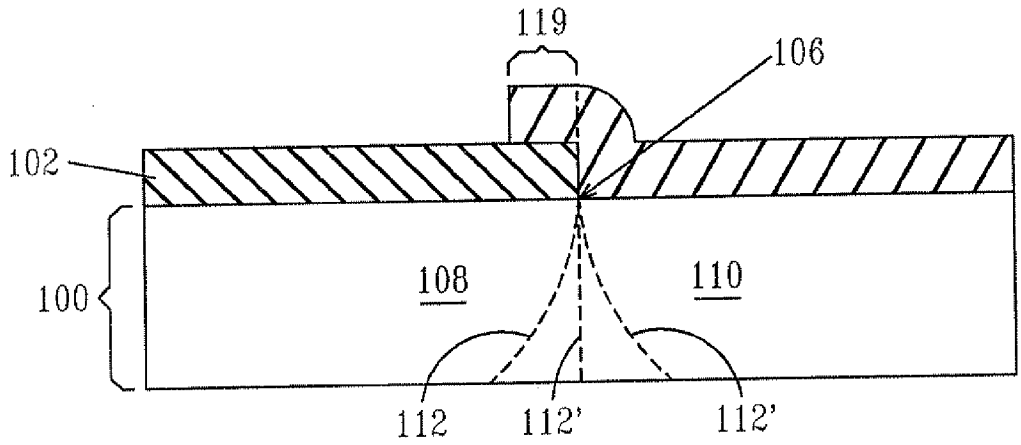

FIG.1C (Prior Art)

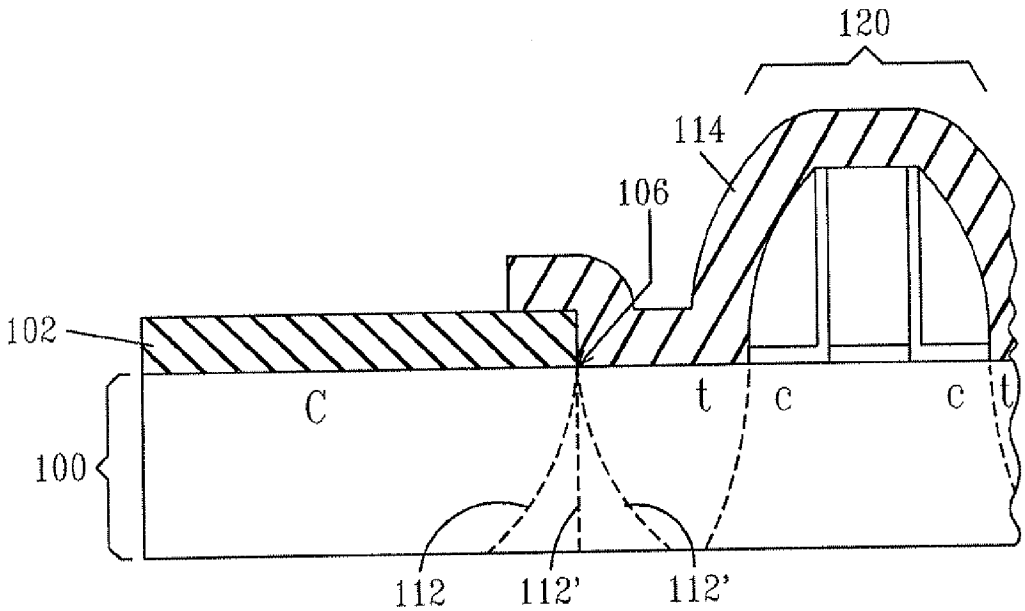

FIG.1D (Prior Art)

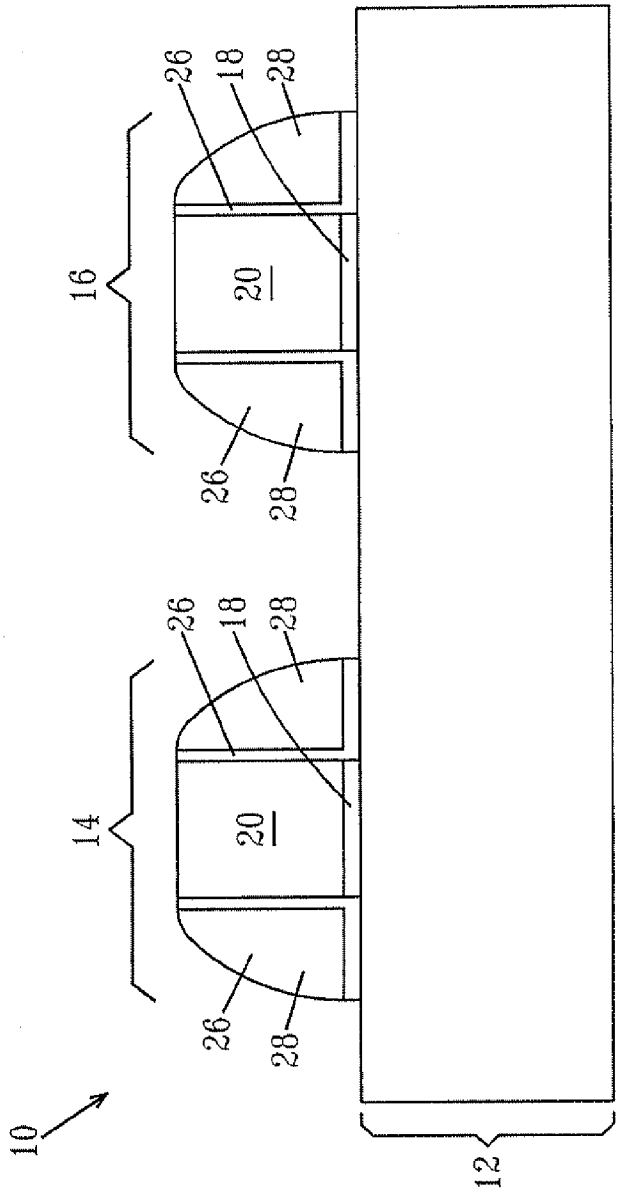

FIG.2A

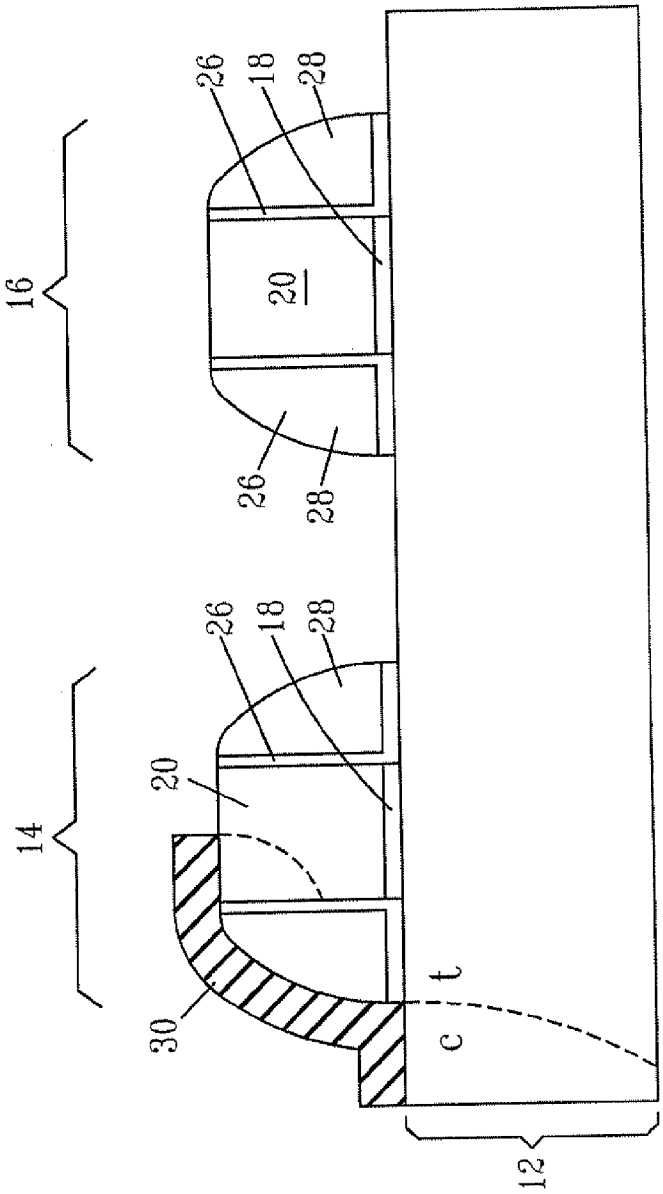

FIG.2B

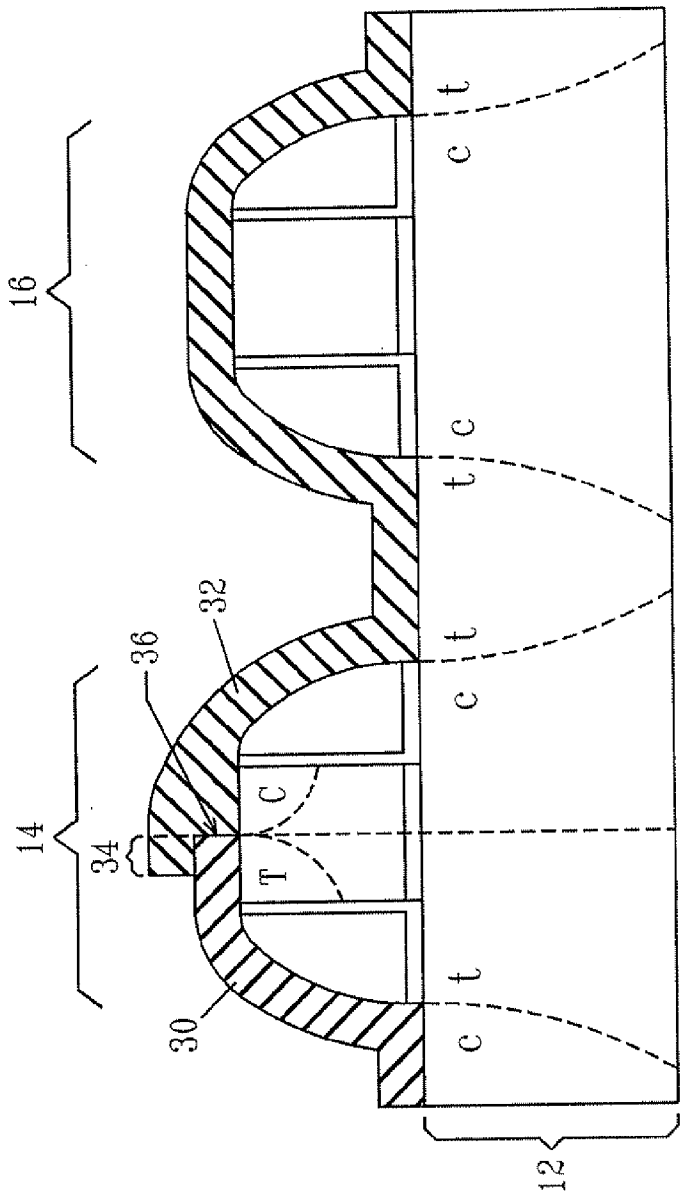

FIG.2C

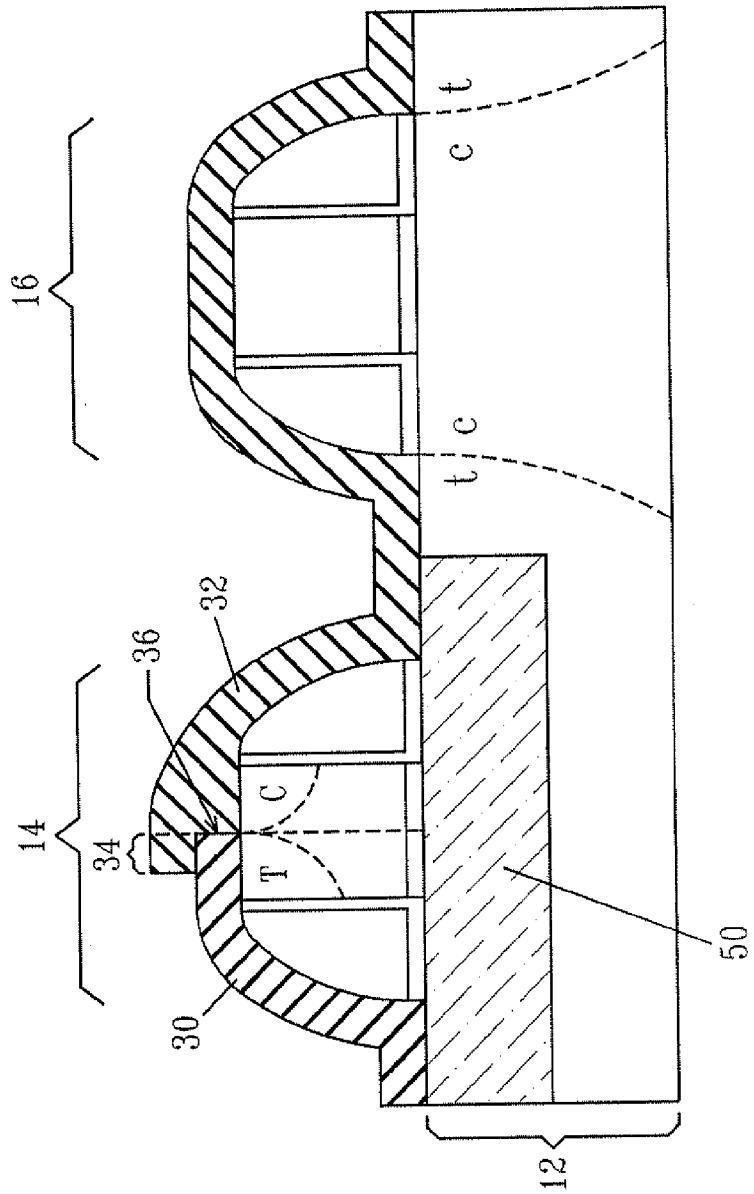

FIG.3

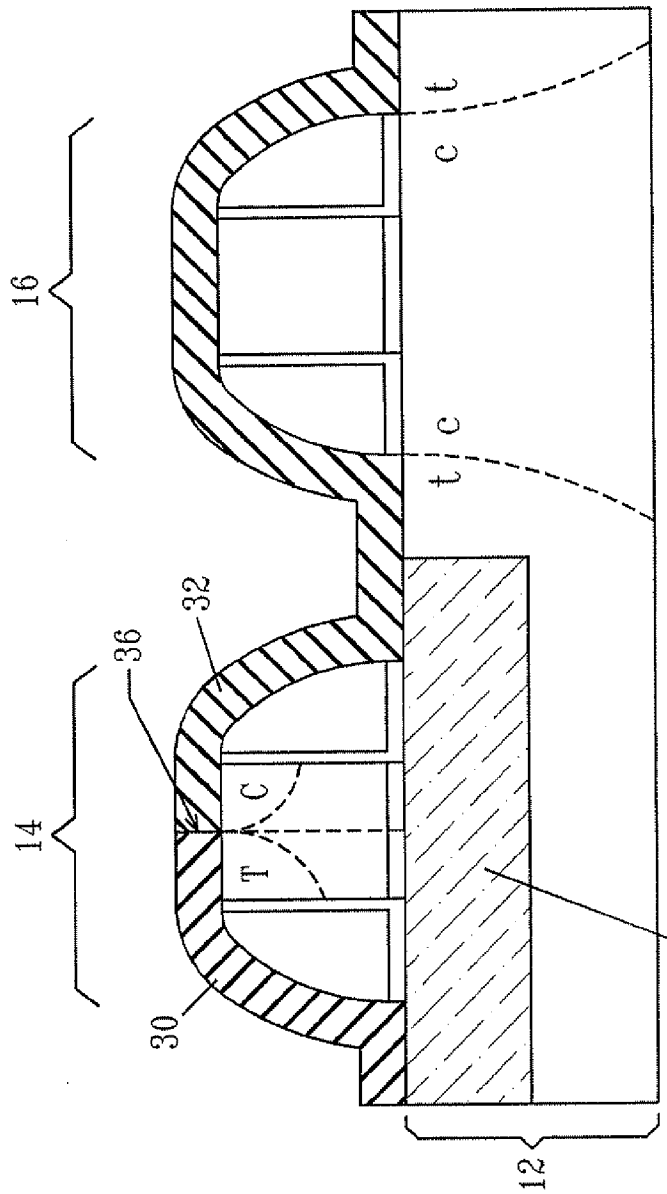

FIG. 4

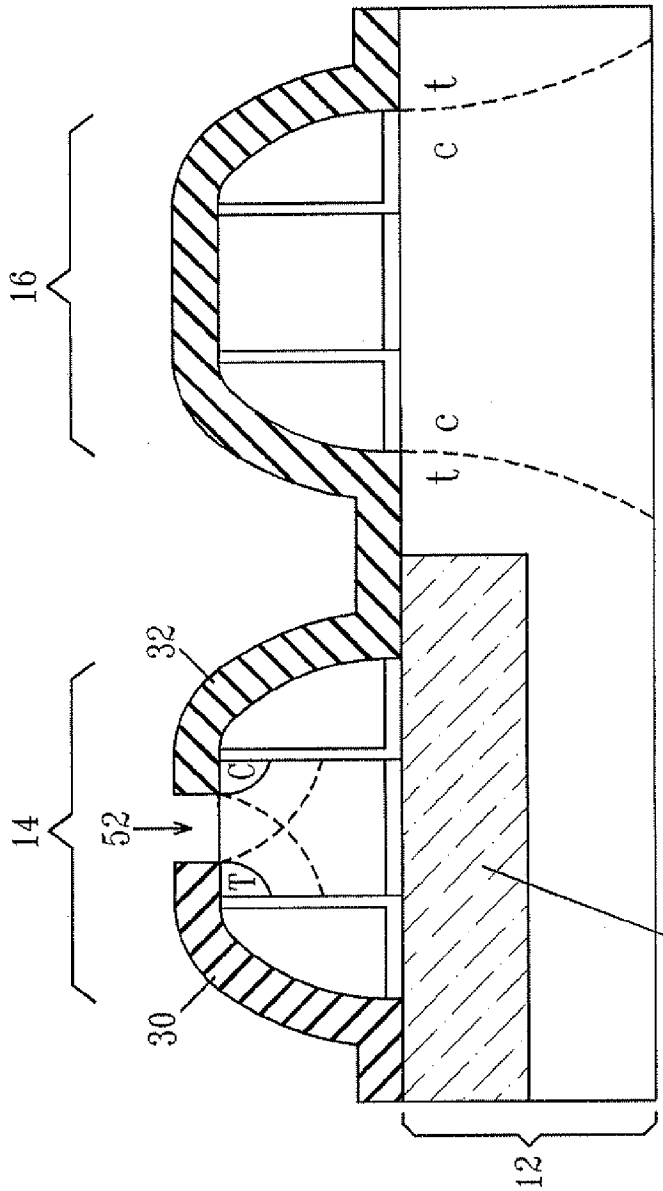

FIG.5

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2007/058273

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/088 H01L27/092 H01L21/8234 H01L21/8238

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/094193 A1 (HORSTMANN MANFRED [DE] ET AL) 4 May 2006 (2006-05-04) paragraphs [0006], [0028] - [0033]; figure 1d	1,2,4,6, 19-23
Y	US 2001/004122 A1 (ITO KAZUYUKI [JP]) 21 June 2001 (2001-06-21) paragraphs [0065] - [0067]; figures 7,8K,10	1-28
Y	US 2004/029323 A1 (SHIMIZU AKIHIRO [JP] ET AL) 12 February 2004 (2004-02-12) paragraphs [0008], [0009], [0013], [0016], [0066], [0094], [0098], [0100]; figures 1-4	1-28

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 November 2007	03/12/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Seck, Martin

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2007/058273

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2005/285137 A1 (SATOH SHIGEO [JP]) 29 December 2005 (2005-12-29) paragraphs [0017], [0018], [0080] - [0088]; figure 7	1-28
Y	SHERAW C D ET AL: "Dual stress liner enhancement in hybrid orientation technology" VLSI TECHNOLOGY, 2005. DIGEST OF TECHNICAL PAPERS. 2005 SYMPOSIUM ON KYOTO, JAPAN JUNE 14-16, 2005, PISCATAWAY, NJ, USA,IEEE, 14 June 2005 (2005-06-14), pages 12-13, XP010818152 ISBN: 4-900784-00-1 the whole document	3
Y	US 2006/046400 A1 (BURBACH GERT [DE] ET AL) 2 March 2006 (2006-03-02) paragraph [0026]; figures 1,2	8,12,16, 27
E	US 2007/252230 A1 (ZHU HUILONG [US] ET AL) 1 November 2007 (2007-11-01) paragraphs [0009], [0073], [0099]; figures 12-16	1-28
A	YANG H S ET AL: "Dual stress liner for high performance sub-45nm gate length SOI CMOS manufacturing" ELECTRON DEVICES MEETING, 2004. IEDM TECHNICAL DIGEST. IEEE INTERNATIONAL SAN FRANCISCO, CA, USA DEC. 13-15, 2004, PISCATAWAY, NJ, USA,IEEE, 13 December 2004 (2004-12-13), pages 1075-1077, XP010789003 ISBN: 0-7803-8684-1 the whole document	1-28

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2007/058273

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