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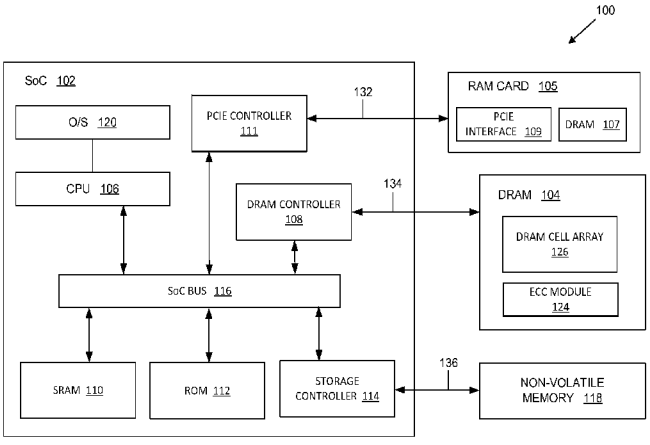

FIG. 1

(57) Abstract: Systems and methods are disclosed for expanding memory for a system on chip (SoC). A memory card is loaded in an expandable memory socket electrically and is coupled to a system on chip (SoC) via an expansion bus. The memory card comprises a first volatile memory device. In response to detecting the memory card, an expanded virtual memory map is configured. The expanded virtual memory map comprises a first virtual memory space associated the first volatile memory device and a second virtual memory space associated with a second volatile memory device electrically coupled to the SoC via a memory bus. One or more peripheral images associated with the second virtual memory space are relocated to a first portion of the first virtual memory space. A second portion of the first virtual memory space is configured as a block device for performing swap operations associated with the second virtual memory space.

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SYSTEMS AND METHODS FOR EXPANDING MEMORY FOR A SYSTEM ON CHIP

DESCRIPTION OF THE RELATED ART

[0001] Portable computing devices (*e.g.*, cellular telephones, smart phones, tablet computers, portable digital assistants (PDAs), and portable game consoles) continue to offer an ever-expanding array of features and services, and provide users with unprecedented levels of access to information, resources, and communications. To keep pace with these service enhancements, such devices have become more powerful and more complex. Portable computing devices now commonly include a system on chip (SoC) comprising one or more chip components embedded on a single substrate (*e.g.*, one or more central processing units (CPUs), a graphics processing unit (GPU), digital signal processors, *etc.*).

[0002] System memory in such portable computing devices typically comprises dynamic random access memory (DRAM). One or more DRAM devices may be electrically coupled to the SoC via a high-performance memory bus. DRAM process technology continues to scale down to accommodate increasing demands for greater memory capacity in smaller chips. While denser DRAM chips provide desirable performance and design advantages, the costs of increasing DRAM capacity combined with downward price pressures due to consumer expectations, can adversely impact profit margins for original equipment manufacturers.

[0003] Accordingly, there is a need for improved systems and methods for expanding DRAM in these and other portable computing devices.

SUMMARY OF THE DISCLOSURE

[0004] Systems, methods, and computer programs are disclosed for expanding memory for a system on chip (SoC). One such method involves detecting a memory card loaded in an expandable memory socket electrically coupled to a system on chip (SoC) via an expansion bus. The memory card comprises a first volatile memory device. In response to detecting the memory card, an expanded virtual memory map is configured. The expanded virtual memory map comprises a first virtual memory space associated the first volatile memory device and a second virtual memory space associated with a second volatile memory device electrically coupled to the SoC via a high-performance memory bus. One or more peripheral images associated with the second virtual

memory space are relocated to a first portion of the first virtual memory space. A second portion of the first virtual memory space is configured as a block device for performing swap operations associated with the second virtual memory space.

[0005] Another embodiment is a system comprising a system on chip (SoC) electrically coupled to a first volatile memory device via a high-performance memory bus. An expandable memory socket is electrically coupled to the SoC via an expansion bus. The SoC comprises a processor configured to: detect a memory card loaded in the expandable memory socket, the memory card comprising a second volatile memory device; in response to detecting the memory card, configure an expanded virtual memory map comprising a first virtual memory space associated the first volatile memory device and a second virtual memory space associated with the second volatile memory device; relocate one or more peripheral images in the first virtual memory space to a first portion of the second virtual memory space; and configure a second portion of the second virtual memory space as a block device for performing swap operations associated with the first virtual memory space.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] In the Figures, like reference numerals refer to like parts throughout the various views unless otherwise indicated. For reference numerals with letter character designations such as "102A" or "102B", the letter character designations may differentiate two like parts or elements present in the same Figure. Letter character designations for reference numerals may be omitted when it is intended that a reference numeral to encompass all parts having the same reference numeral in all Figures.

[0007] FIG. 1 is a block diagram of an embodiment of a system for expanding memory in an exemplary portable communication device.

[0008] FIG. 2 is an overhead schematic view of a package/substrate of the portable communication device of FIG. 1.

[0009] FIG. 3 is a cross-sectional view of the expandable RAM card/socket and SoC in FIG. 2.

[0010] FIG. 4 is a flowchart illustrating an embodiment of a method for expanding system memory for the SoC in FIGS. 1 – 3.

[0011] FIG. 5 is a block diagram illustrating an embodiment of an expanded virtual memory map.

[0012] FIG. 6 is a block diagram of another embodiment of a portable communication device that may incorporate a RAM card/socket for expanding system memory.

[0013] FIG. 7 is a schematic diagram illustrating an embodiment of a method for performing swap operations via the expanded virtual memory map of FIG. 5.

DETAILED DESCRIPTION

[0014] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects.

[0015] In this description, the term "application" or "image" may also include files having executable content, such as: object code, scripts, byte code, markup language files, and patches. In addition, an "application" referred to herein, may also include files that are not executable in nature, such as documents that may need to be opened or other data files that need to be accessed.

[0016] The term "content" may also include files having executable content, such as: object code, scripts, byte code, markup language files, and patches. In addition, "content" referred to herein, may also include files that are not executable in nature, such as documents that may need to be opened or other data files that need to be accessed.

[0017] As used in this description, the terms "component," "database," "module," "system," and the like are intended to refer to a computer-related entity, either hardware, firmware, a combination of hardware and software, software, or software in execution. For example, a component may be, but is not limited to being, a process running on a processor, a processor, an object, an executable, a thread of execution, a program, and/or a computer. By way of illustration, both an application running on a computing device and the computing device may be a component. One or more components may reside within a process and/or thread of execution, and a component may be localized on one computer and/or distributed between two or more computers. In addition, these components may execute from various computer readable media having various data structures stored thereon. The components may communicate by way of local and/or remote processes such as in accordance with a signal having one or more data packets (*e.g.,* data from one component interacting with another component in a local system, distributed system, and/or across a network such as the Internet with other systems by way of the signal).

[0018] The term "virtual memory" refers to the abstraction of the actual physical memory from the application or image that is referencing the memory. A translation or mapping may be used to convert a virtual memory address to a physical memory address. The mapping may be as simple as 1-to-1 (*e.g.*, physical address equals virtual address), moderately complex (*e.g.*, a physical address equals a constant offset from the virtual address), or the mapping may be complex (*e.g.*, every 4KB page mapped uniquely). The mapping may be static (*e.g.*, performed once at startup), or the mapping may be dynamic (*e.g.*, continuously evolving as memory is allocated and freed).

[0019] In this description, the terms "communication device," "wireless device," "wireless telephone", "wireless communication device," and "wireless handset" are used interchangeably. With the advent of third generation ("3G") wireless technology and four generation ("4G"), greater bandwidth availability has enabled more portable computing devices with a greater variety of wireless capabilities. Therefore, a portable computing device may include a cellular telephone, a pager, a PDA, a smartphone, a navigation device, or a hand-held computer with a wireless connection or link.

[0020] FIG. 1 illustrates an embodiment of a system 100 for expanding memory for a system on chip (SoC) 102. The system 100 may be implemented in any computing device, including a personal computer, a workstation, a server, a portable computing device (PCD), such as a cellular telephone, a portable digital assistant (PDA), a portable game console, a palmtop computer, or a tablet computer. As illustrated in the embodiment of FIG. 1, the system 100 comprises a system on chip (SoC) 102 electrically coupled to a DRAM memory system 104, a non-volatile memory 118, and an expandable random access memory (RAM) card 105. DRAM memory system 104 interfaces with the SoC via a high-performance memory bus 134. The non-volatile memory 118 interfaces with the SoC via a storage bus 136. Non-volatile memory 118 may comprise any non-volatile memory, such as, for example, flash memory, flash drive, a Secure Digital (SD) card, a solid-state drive (SSD), or other types. In certain embodiments, due to the large quantity of pins to support the high-performance memory bus 134, the sensitive radio frequency circuits in close proximity to the SoC 102, and the limited distance that the high-performance memory bus 134 can travel without causing interference, it may difficult and costly to implement an expandable DRAM memory system 104.

[0021] The expandable RAM card 105 is electrically coupled to the SoC 102 via an expansion bus 132. As described below in more detail, in ai

expandable RAM card 105 may comprise a removable memory card or other device, which may be loaded into a user-accessible memory socket 302. In this manner, the system 100 may enable a user to conveniently add additional memory capacity to the portable computing device after purchase. The system 100 provides an extensible high-performance swap memory system that may be leveraged by an original equipment manufacturer. As known in the art, portable computing system performance and application responsiveness improves with increasing RAM size and that it degrades with decreasing RAM. User population may vary in the types and quantity of applications that they install and engage in their daily use. For example, simple users may find 2GB of RAM completely adequate, while expert or enthusiast users running multiple complex applications or games may need 4GB or more before their user experience becomes satisfactory. One of ordinary skill in the art will appreciate that the system 100 may be desirable to an original equipment manufacturer (OEM) because it may enable the OEM to advertise increased performance while minimizing the OEM bill of materials. Other benefits of using expandable RAM card 105 may include, for example, providing much faster response than using traditional storage devices in most common practice as a swap device, and supporting asymmetric DRAM population (*e.g.*, LPDDR4 for DRAM 104 and LPDDR3 for expandable RAM card 105), in a cost-effective way that is supported by the O/S 120.

[0022] The expansion bus 132 comprises a direct memory access bus, such as, for example, a peripheral component interconnection express (PCIE) bus. As known in the art, a PCIE bus 132 comprises a high-speed serial computer expansion bus, which provides various desirable characteristics, such as, higher maximum system bus throughput, lower I/O pin count and smaller physical footprint, improved performance-scaling for bus devices, reliable error detection and reporting mechanisms, native hot-plug functionality, and hardware I/O virtualization. As illustrated in FIG. 1, the RAM card 105 may comprise a DRAM 107 and a PCIE or other interface 109 configured to communicate with a corresponding PCIE or other controller 111 via the expansion bus 132.

[0023] The SoC 102 comprises various on-chip components, including a central processing unit (CPU) 106, a DRAM controller 108, static random access memory (SRAM) 110, read only memory (ROM) 112, and a storage controller 114 interconnected via a SoC bus 116. The SoC 102 may include one or more memory clients that request memory resources from DRAM 104 and

into the socket 302. The memory clients may comprise one or more processing units (*e.g.*, central processing unit (CPU) 106, a graphics processing unit (GPU), a digital signal processor (DSP), *etc.*), a video encoder, or other clients requesting memory read/write access.

[0024] Storage controller 114 on SoC 102 is electrically coupled to non-volatile memory 118 via storage bus 136. Storage controller 114 manages the data stored on non-volatile memory 118. DRAM controller 108 is electrically coupled to DRAM 104 via, for example, a high-performance RAM bus 134. DRAM controller 108 manages the flow of data going to and from the DRAM 104. DRAM controller 108 generally comprises the logic for reading and writing to DRAM 104.

[0025] As further illustrated in FIG. 1, DRAM 104 may comprise an error correcting code (ECC) module 124. ECC module 124 detects double-bit errors and corrects single-bit errors during DRAM operations (*e.g.*, read and/or write operations). For example, during a DRAM write operation, the ECC module 124 may use the write data as input and then generate redundant parity check bits. The combined write data and parity check bits together form a unit known as a codeword and may be stored either separated or together in the DRAM cell array 126. During a read operation, the ECC module 124 may use the retrieved data portion of the codeword to recomputed the parity check bits and then compare these against the parity check bits portion of the codeword that was stored during the write operation. A mismatch between the read recomputed parity and the stored parity indicates a detected error. In addition, the parity check bits may be sufficient to provide single error correction within the codeword.

[0026] FIGS. 2 & 3 illustrate an embodiment of a package/substrate 202 for incorporating system 100 in a portable computing device. The SoC 102 and/or the DRAM 104 may be disposed at a first location 208 on the package/substrate 202. In an embodiment, the DRAM 104 may be soldered onto a CPU package and the combined DRAM/CPU may be soldered to a mainboard. As illustrated in FIG. 3, the SoC 102 and/or the DRAM 104 may be covered by a radio frequency (RF) shield 204 to shield other components from DDR signal noise. As known in the art, DDR signals may create substantial common-mode radiation that could impact other components on the package/substrate 202. In this regard, the socket 302 may be remotely located at a second location 206 on the package/substrate 202.

[0027] In an embodiment, the socket 302 is configured to carry PCIE interface signals (*e.g.*, 44 I/O pins for x4 lanes). A PCIE 4x lane provides 4

DRAM 104. A PCIE 8x lane using more pins may provide 8 GB/sec bandwidth to DRAM 104. The PCIE controller 111 may be configured to translate the PCIE bus 132, which may include memory control operations similar to DRAM controller 108. In an embodiment, RAM card 105 may be offered in various configurations, including but not limited to: different DDR JEDEC standards such as LPDDR1, LPDDR2, LPDDR3, LPDDR4, *etc.*; different capacities such as 512MB, 1GB, 2GB, *etc*; different performance grades such as 4 GB/sec, 8 GB/sec, etc.; combining with other functions such as PCIE, eMMC, or UFS flash storage expansion such as 512MB RAM expansion plus 8GB flash expansion on a single card. A combination functions may be implemented by including the relevant capability into the PCIE controller 111. For example, the PCIE controller 111 may be configured to translate the PCIE bus 132 to an eMMC flash storage bus. Furthermore, the RAM card 105 may contain multiple stacked memory chips connected to PCIE controller 111 to provide the advertised capacity.

[0028] FIG. 4 is a flowchart illustrating an embodiment of a method for expanding memory in system 100. At block 402, the system 100 detects that a memory card (*e.g.*, RAM card 105) is loaded in an expandable memory socket 302. As mentioned above, the memory socket 302 is electrically coupled to the SoC 102 via the expansion bus 132. The memory card may comprise a first volatile memory device (*e.g.*, DRAM 107 – having a capacity of 1 GB). If a memory card is detected, at block 404, the system 100 configures an expanded virtual memory map 500. FIG. 5 illustrates an embodiment of the expanded virtual memory map 500. Memory map 502 illustrates the virtual memory map for a DRAM 104 (having a capacity of 2 GB) without the memory card loaded in the expandable memory socket 302. Address range 506 is assigned to kernel and O/S 120. Address ranges 508 and 520 may be assigned to a content protection and multimedia heap and trusted zone(s), respectively. Additional address ranges may be assigned to one or more peripheral images assigned to specific hardware resources (*e.g.*, shared resources 510, video codec 512, an application digital signal processor (DSP) 514, connectivity hardware 516, modem 518, *etc.*). As illustrated in the embodiment of FIG. 5, address ranges 506 – 520 comprise 300 MB of memory capacity, leaving 1.7 GB of available user space. It should be appreciated that this is only one of many possible examples of how the images may be rearranged within memory for the purpose of increasing the user area 504.

[0029] When a memory card is detected, the expanded virtual memory map is configured with a first virtual memory space associated with the first volatile memory device (*e.g.*, 1GB DRAM 107). A second virtual memory space is associated with the 2 GB DRAM 104. At block 406, the system 100 may relocate one or more of the peripheral images associated with the second virtual memory space to a first portion of the first virtual memory space. As illustrated in FIG. 5, peripheral images associated with address ranges 510, 512, 514, 516, and 518 are relocated to 150 MB of the 1 GB RAM card. The peripheral images to be relocated may be selected according to bandwidth needs. For example, if the associated hardware resources can handle a reduced bandwidth via expansion bus 132 (as compared to the high-performance memory bus 134), they may be relocated. At block 408, the system 100 may configure a second portion of the first virtual memory space as a block device for performing swap operations associated with the second virtual memory space.

[0030] As illustrated in FIG.7, there may be a limited amount of physical memory 700 available for the user (corresponding to the user space 504 in FIG.5). Multiple processes running in a system may compete for this free memory space as shown by a first process 710 and a second process 720. While only two processes are illustrated in FIG. 7, it should be appreciated that many more processes may be running on a portable computing system. The total memory requested from all processes may exceed the available physical memory 700. The kernel and O/S 506 may categorize memory usage into one or more working sets (*e.g.*, working sets 712 and 722) and one or more nonworking sets (*e.g.*, nonworking sets 714 and 724) based upon, for example, the amount of recent activity. Although FIG. 7 shows this categorization as contiguous grouping, it should be appreciated that the memory pages shown as individual rectangles may be spread out and/or random. Memory pages that are recently and frequently accessed (*i.e.*, read and/or written) may comprise the working sets 712 and 724 and most likely to be placed into physical memory 700, while memory pages that have not been accessed recently may comprise the nonworking sets 714 and 724 and are least likely to be placed into physical memory 700. The nonworking sets 714 and 724 may be placed into the RAM card 105. As time passes, processes may access different portions of memory, changing some pages from nonworking sets to working sets and vice versa. When this happens, the relevant pages may be moved between the physical memory 700 and the RAM card 105. This process is commonly known as swap. A portion of RAM card 105 may configured as a block device.

may be performed in blocks (*e.g.*, 4KB pages). In conventional solutions, the swap block device may comprise a hard disk drive (HDD) or solid-state drive (SSD). One of ordinary skill in the art will appreciate that the RAM card 105 may significantly improve the performance of swap by, for example, offering peak bandwidth many times greater than a swap block device comprising the HDD or SSD.

[0031] As mentioned above, the system 100 may be incorporated into any desirable computing system. FIG. 6 illustrates the system 100 incorporated in an exemplary portable computing device (PCD) 600. In this embodiment, the SoC 102 may include a multicore CPU 602. The multicore CPU 602 may include a zeroth core 610, a first core 612, and an Nth core 614. One of the cores may comprise, for example, a graphics processing unit (GPU) with one or more of the others comprising the CPU.

[0032] A display controller 328 and a touch screen controller 330 may be coupled to the CPU 602. In turn, the touch screen display 606 external to the on-chip system 102 may be coupled to the display controller 328 and the touch screen controller 330.

[0033] FIG. 6 further shows that a video encoder 334, e.g., a phase alternating line (PAL) encoder, a sequential color a memoire (SECAM) encoder, or a national television system(s) committee (NTSC) encoder, is coupled to the multicore CPU 602. Further, a video amplifier 336 is coupled to the video encoder 334 and the touch screen display 606. Also, a video port 338 is coupled to the video amplifier 336. As shown in FIG. 6, a universal serial bus (USB) controller 340 is coupled to the multicore CPU 602. Also, a USB port 342 is coupled to the USB controller 340. Memory 104 and a subscriber identity module (SIM) card 346 may also be coupled to the multicore CPU 602.

[0034] Further, as shown in FIG. 6, a digital camera 348 may be coupled to the multicore CPU 602. In an exemplary aspect, the digital camera 348 is a charge-coupled device (CCD) camera or a complementary metal-oxide semiconductor (CMOS) camera.

[0035] As further illustrated in FIG. 6, a stereo audio coder-decoder (CODEC) 350 may be coupled to the multicore CPU 602. Moreover, an audio amplifier 352 may coupled to the stereo audio CODEC 350. In an exemplary aspect, a first stereo speaker 354 and a second stereo speaker 356 are coupled to the audio amplifier 352. FIG. 6 shows that a microphone amplifier 358 may be also coupled to the stereo audio CODEC 350. Additionally, a microphone 360 may be coupled to the microphone amplifier 358. In a particular aspect, a frequency modulation (FM) radio tuner 362 may be coupled to the stereo audio CODEC 350. Also, an FM antenna 364 is coupled to the FM radio tuner 362. Further, stereo headphones 366 may be coupled to the

[0036] FIG. 6 further illustrates that a radio frequency (RF) transceiver 368 may be coupled to the multicore CPU 602. An RF switch 370 may be coupled to the RF transceiver 368 and an RF antenna 372. A keypad 204 may be coupled to the multicore CPU 602. Also, a mono headset with a microphone 376 may be coupled to the multicore CPU 602. Further, a vibrator device 378 may be coupled to the multicore CPU 602.

[0037] FIG. 6 also shows that a power supply 380 may be coupled to the on-chip system 102. In a particular aspect, the power supply 380 is a direct current (DC) power supply that provides power to the various components of the PCD 600 that require power. Further, in a particular aspect, the power supply is a rechargeable DC battery or a DC power supply that is derived from an alternating current (AC) to DC transformer that is connected to an AC power source.

[0038] FIG. 6 further indicates that the PCD 600 may also include a network card 388 that may be used to access a data network, e.g., a local area network, a personal area network, or any other network. The network card 388 may be a Bluetooth network card, a WiFi network card, a personal area network (PAN) card, a personal area network ultra-low-power technology (PeANUT) network card, a television/cable/satellite tuner, or any other network card well known in the art. Further, the network card 388 may be incorporated into a chip, i.e., the network card 388 may be a full solution in a chip, and may not be a separate network card 388.

[0039] Referring to FIG. 6, it should be appreciated that the memory 104, the RAM card 105, touch screen display 606, the video port 338, the USB port 342, the camera 348, the first stereo speaker 354, the second stereo speaker 356, the microphone 360, the FM antenna 364, the stereo headphones 366, the RF switch 370, the RF antenna 372, the keypad 374, the mono headset 376, the vibrator 378, and the power supply 380 may be external to the on-chip system 102.

[0040] It should be appreciated that one or more of the method steps described herein may be stored in the memory as computer program instructions, such as the modules described above. These instructions may be executed by any suitable processor in combination or in concert with the corresponding module to perform the methods described herein.

[0041] Certain steps in the processes or process flows described in this specification naturally precede others for the invention to function as described. However, the invention is not limited to the order of the steps described if

not alter the functionality of the invention. That is, it is recognized that some steps may performed before, after, or parallel (substantially simultaneously with) other steps without departing from the scope and spirit of the invention. In some instances, certain steps may be omitted or not performed without departing from the invention. Further, words such as "thereafter", "then", "next", etc. are not intended to limit the order of the steps. These words are simply used to guide the reader through the description of the exemplary method.

[0042] Additionally, one of ordinary skill in programming is able to write computer code or identify appropriate hardware and/or circuits to implement the disclosed invention without difficulty based on the flow charts and associated description in this specification, for example.

[0043] Therefore, disclosure of a particular set of program code instructions or detailed hardware devices is not considered necessary for an adequate understanding of how to make and use the invention. The inventive functionality of the claimed computer implemented processes is explained in more detail in the above description and in conjunction with the Figures which may illustrate various process flows.

[0044] In one or more exemplary aspects, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted as one or more instructions or code on a computer-readable medium. Computer-readable media include both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may comprise RAM, ROM, EEPROM, NAND flash, NOR flash, M-RAM, P-RAM, R-RAM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to carry or store desired program code in the form of instructions or data structures and that may be accessed by a computer.

[0045] Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line ("DSL"), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium.

[0046] Disk and disc, as used herein, includes compact disc ("CD"), laser disc, optical disc, digital versatile disc ("DVD"), floppy disk and blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0047] Alternative embodiments will become apparent to one of ordinary skill in the art to which the invention pertains without departing from its spirit and scope. Therefore, although selected aspects have been illustrated and described in detail, it will be understood that various substitutions and alterations may be made therein without departing from the spirit and scope of the present invention, as defined by the following claims.

CLAIMS

What is claimed is:

1. A method for expanding memory for a system on chip (SoC), the method comprising, the method comprising:

detecting a memory card loaded in an expandable memory socket electrically coupled to a system on chip (SoC) via an expansion bus, the memory card comprising a first volatile memory device;

in response to detecting the memory card, configuring an expanded virtual memory map comprising a first virtual memory space associated the first volatile memory device and a second virtual memory space associated with a second volatile memory device electrically coupled to the SoC via a high-performance memory bus;

relocating one or more peripheral images associated with the second virtual memory space to a first portion of the first virtual memory space; and

configuring a second portion of the first virtual memory space as a block device for performing swap operations associated with the second virtual memory space.

2. The method of claim 1, wherein the expansion bus comprises a peripheral component interconnect express (PCIE) bus.

3. The method of claim 1, wherein the expansion bus comprises a direct memory access bus.

4. The method of claim 1, wherein the first and second volatile memory devices comprise dynamic random access memory (DRAM).

5. The method of claim 1, wherein the memory card is removable from the expandable memory socket.

6. The method of claim 1, wherein the SoC and first and second volatile memory devices are implemented in a portable communication device.

7. The method of claim 6, wherein the SOC and the second volatile memory device are disposed under a radio frequency (RF) shield, and the first volatile memory device is remotely located from the RF shield.

8. A system for expanding system memory associated with a system on chip (SoC), the system comprising:

means for detecting a memory card loaded in an expandable memory socket electrically coupled to a system on chip (SoC) via an expansion bus, the memory card comprising a first volatile memory device;

means for configuring an expanded virtual memory map in response to detecting the memory card, the expanded virtual memory map comprising a first virtual memory space associated the first volatile memory device and a second virtual memory space associated with a second volatile memory device electrically coupled to the SoC via a high-performance memory bus;

means for relocating one or more peripheral images associated with the second virtual memory space to a first portion of the first virtual memory space; and

means for configuring a second portion of the first virtual memory space as a block device for performing swap operations associated with the second virtual memory space.

9. The system of claim 8, wherein the means for detecting the memory card loaded in the expandable memory socket comprises a peripheral component interconnect express (PCIE) controller located on the SoC.

10. The system of claim 8, wherein the expansion bus comprises a direct memory access bus.

11. The system of claim 8, wherein the first and second volatile memory devices comprise dynamic random access memory (DRAM).

12. The system of claim 8, wherein the memory card is removable from the expandable memory socket.

13. The system of claim 8, wherein the SoC and first and second volatile memory devices are implemented in a portable communication device.

14. The system of claim 13, wherein the SOC and the second volatile memory device are disposed under a radio frequency (RF) shield, and the expandable memory socket is remotely located from the RF shield.

15. A computer program embodied in a memory and executable by a processor for expanding memory associated with a system on chip (SoC), the computer program comprising logic configured to:

detect a memory card loaded in an expandable memory socket electrically coupled to a system on chip (SoC) via an expansion bus, the memory card comprising a first volatile memory device;

in response to detecting the memory card, configure an expanded virtual memory map comprising a first virtual memory space associated the first volatile memory device and a second virtual memory space associated with a second volatile memory device electrically coupled to the SoC via a high-performance memory bus;

relocate one or more peripheral images associated with the second virtual memory space to a first portion of the first virtual memory space; and

configure a second portion of the first virtual memory space as a block device for performing swap operations associated with the second virtual memory space.

16. The computer program of claim 15, wherein the expansion bus comprises a peripheral component interconnect express (PCIE) bus.

17. The computer program of claim 15, wherein the expansion bus comprises a direct memory access bus.

18. The computer program of claim 15, wherein the first and second volatile memory devices comprise dynamic random access memory (DRAM).

19. The computer program of claim 15, wherein the memory card is removable from the expandable memory socket.

20. The computer program of claim 15, wherein the SoC and first and second volatile memory devices are implemented in a portable communication device.

21. The computer program of claim 20, wherein the SOC and the second volatile memory device are disposed under a radio frequency (RF) shield, and the first volatile memory device is remotely located from the RF shield.

22. A system for expanding memory for a system on chip (SoC), the system comprising:

a system on chip (SoC) electrically coupled to a first volatile memory device via a high-performance memory bus; and

an expandable memory socket electrically coupled to the SoC via an expansion bus;

wherein the SoC comprises a processor configured to:

detect a memory card loaded in the expandable memory socket, the memory card comprising a second volatile memory device;

in response to detecting the memory card, configure an expanded virtual memory map comprising a first virtual memory space associated the first volatile memory device and a second virtual memory space associated with the second volatile memory device;

relocate one or more peripheral images in the first virtual memory space to a first portion of the second virtual memory space; and

configure a second portion of the second virtual memory space as a block device for performing swap operations associated with the first virtual memory space.

23. The system of claim 22, wherein the SoC and the first and second volatile memory devices reside in a portable communication device.

24. The system of claim 23, wherein the SOC and the first volatile memory device are disposed under a radio frequency (RF) shield.

25. The system of claim 24, wherein the expandable memory socket is remotely located from the RF shield.

26. The system of claim 23, wherein the portable communication device comprises one of a mobile phone, a tablet computer, and a portable game console.

27. The system of claim 22, wherein the expansion bus comprises a peripheral component interconnect express (PCIE) bus, and the SoC comprises PCIE controller for translating the PCIE bus to the high-performance memory bus.

28. The system of claim 22, wherein the first and second volatile memory devices comprise dynamic random access memory (DRAM).

29. The system of claim 22, wherein the memory card is user-loadable into the expandable memory socket.

30. The system of claim 22, wherein the expansion bus comprises a direct memory access bus.

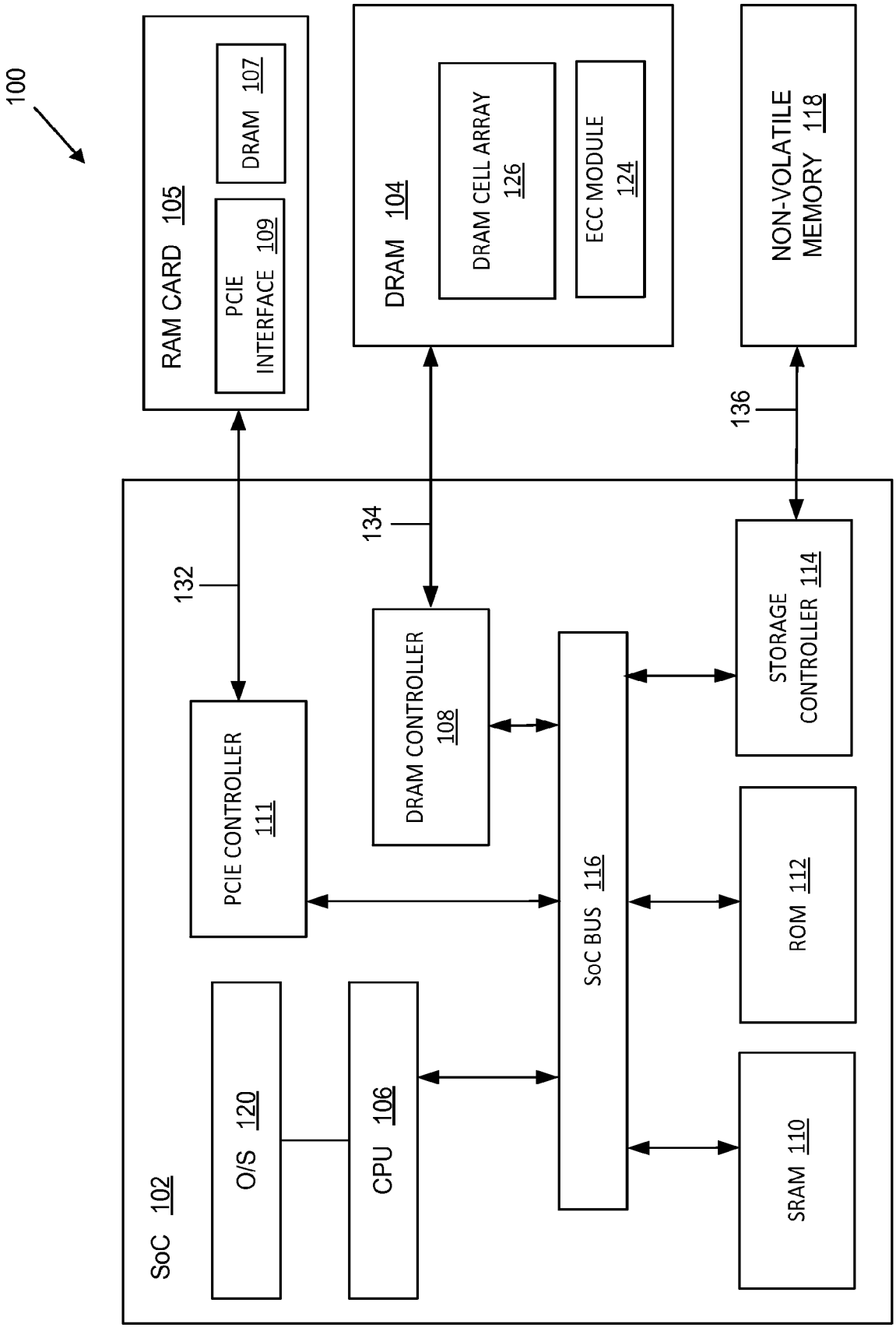
100
RAM CARD 105
DRAM 107
PCIE INTERFACE 109
DRAM 104
DRAM CELL ARRAY 126
ECC MODULE 124
NON-VOLATILE MEMORY 118
136
132
134
SoC 102
PCIE CONTROLLER 111
DRAM CONTROLLER 108
STORAGE CONTROLLER 114
SoC BUS 116
ROM 112
O/S 120
CPU 106
SRAM 110

FIG. 1

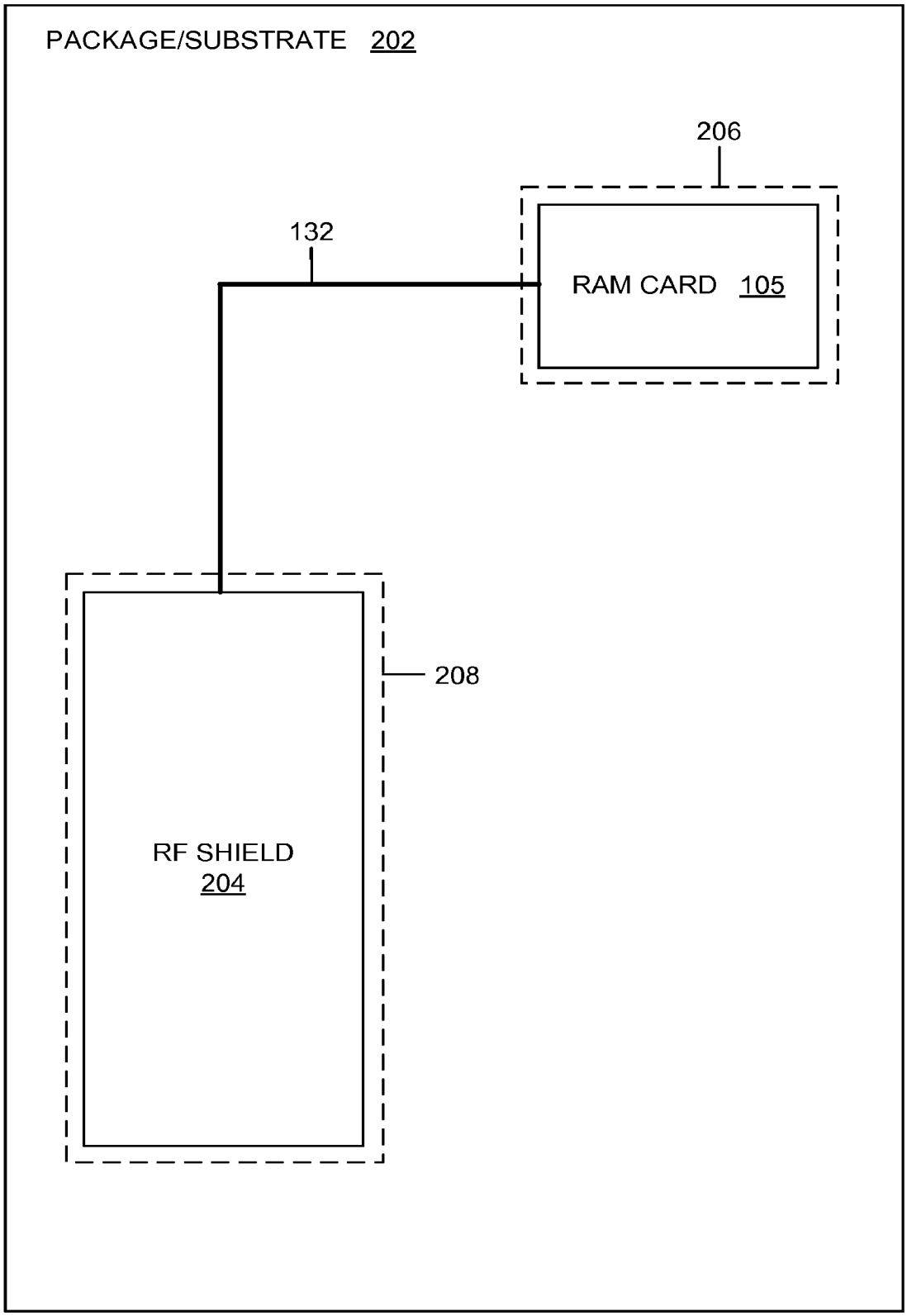

FIG. 2

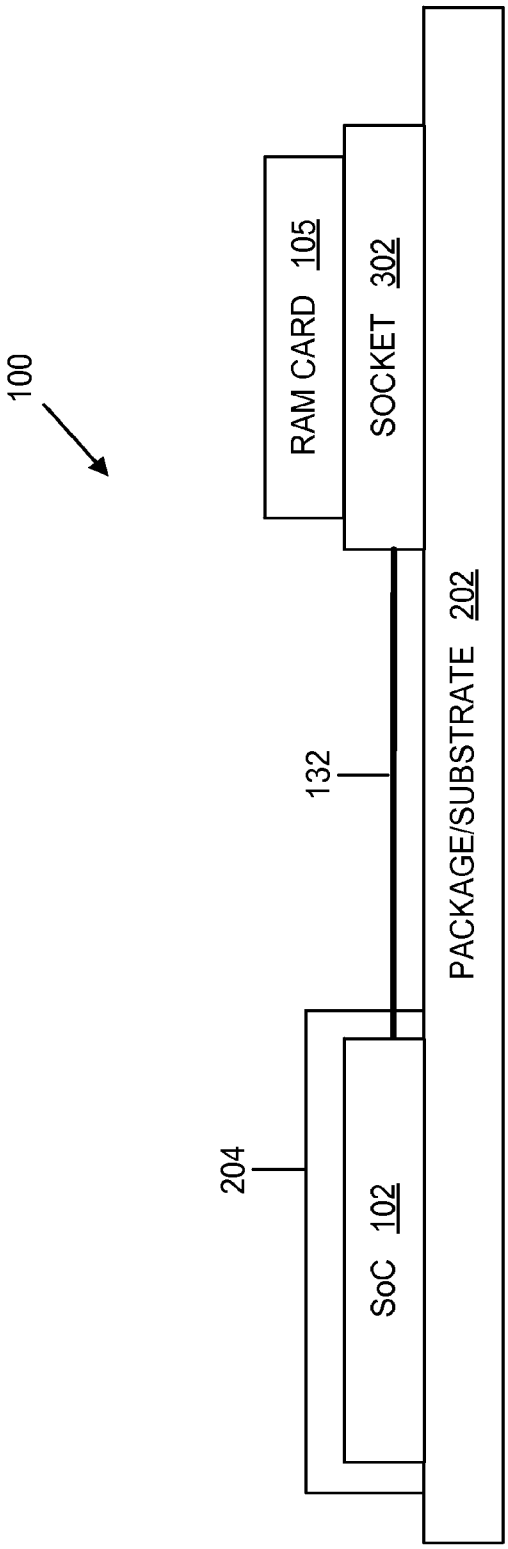
100
RAM CARD 105
SOCKET 302
132
PACKAGE/SUBSTRATE 202
204
SoC 102

FIG. 3

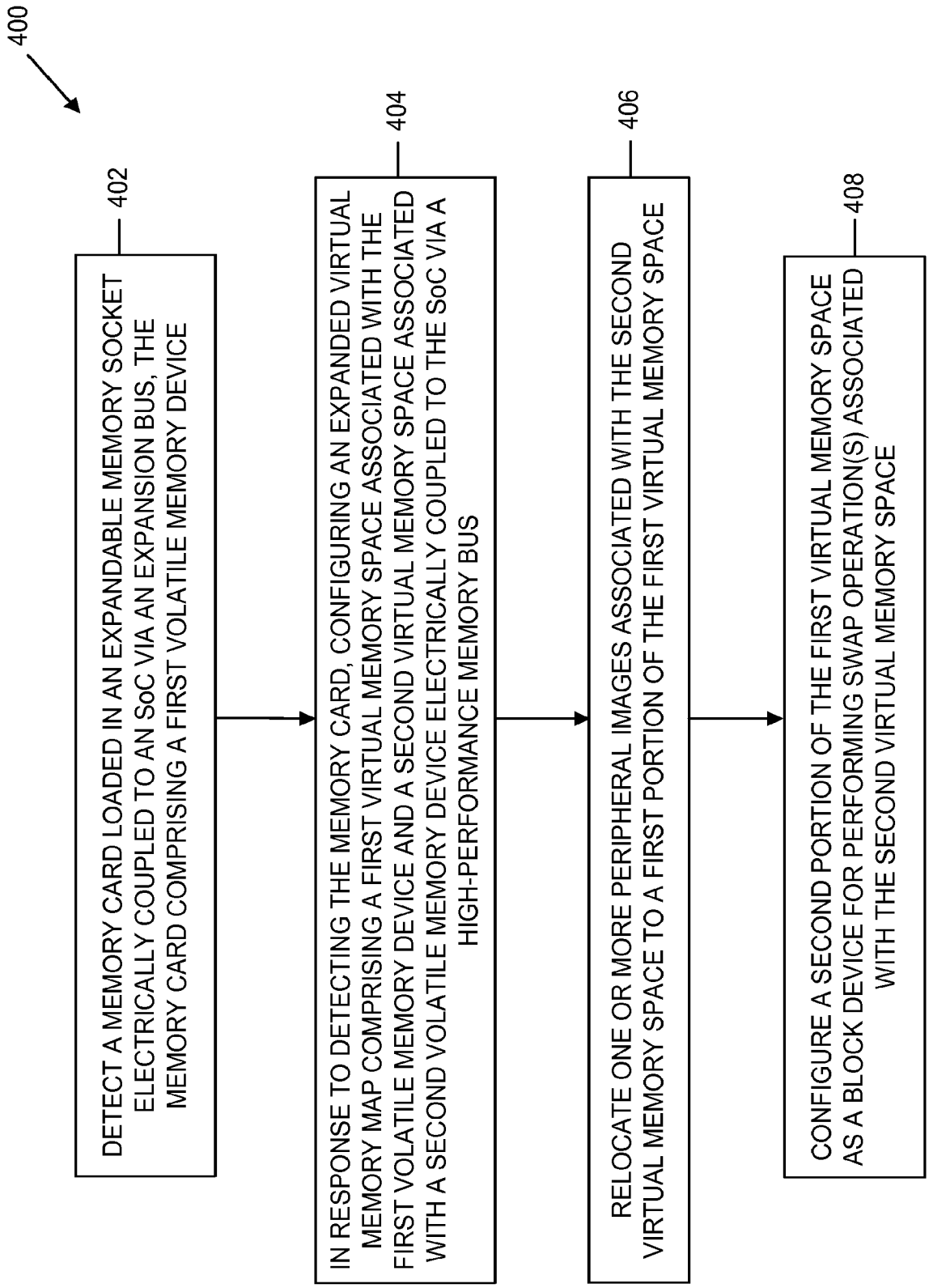
400
402
DETECT A MEMORY CARD LOADED IN AN EXPANDABLE MEMORY SOCKET ELECTRICALLY COUPLED TO AN SoC VIA AN EXPANSION BUS, THE MEMORY CARD COMPRISING A FIRST VOLATILE MEMORY DEVICE
404
IN RESPONSE TO DETECTING THE MEMORY CARD, CONFIGURING AN EXPANDED VIRTUAL MEMORY MAP COMPRISING A FIRST VIRTUAL MEMORY SPACE ASSOCIATED WITH THE FIRST VOLATILE MEMORY DEVICE AND A SECOND VIRTUAL MEMORY SPACE ASSOCIATED WITH A SECOND VOLATILE MEMORY DEVICE ELECTRICALLY COUPLED TO THE SoC VIA A HIGH-PERFORMANCE MEMORY BUS
406
RELOCATE ONE OR MORE PERIPHERAL IMAGES ASSOCIATED WITH THE SECOND VIRTUAL MEMORY SPACE TO A FIRST PORTION OF THE FIRST VIRTUAL MEMORY SPACE
408
CONFIGURE A SECOND PORTION OF THE FIRST VIRTUAL MEMORY SPACE AS A BLOCK DEVICE FOR PERFORMING SWAP OPERATION(S) ASSOCIATED WITH THE SECOND VIRTUAL MEMORY SPACE

FIG. 4

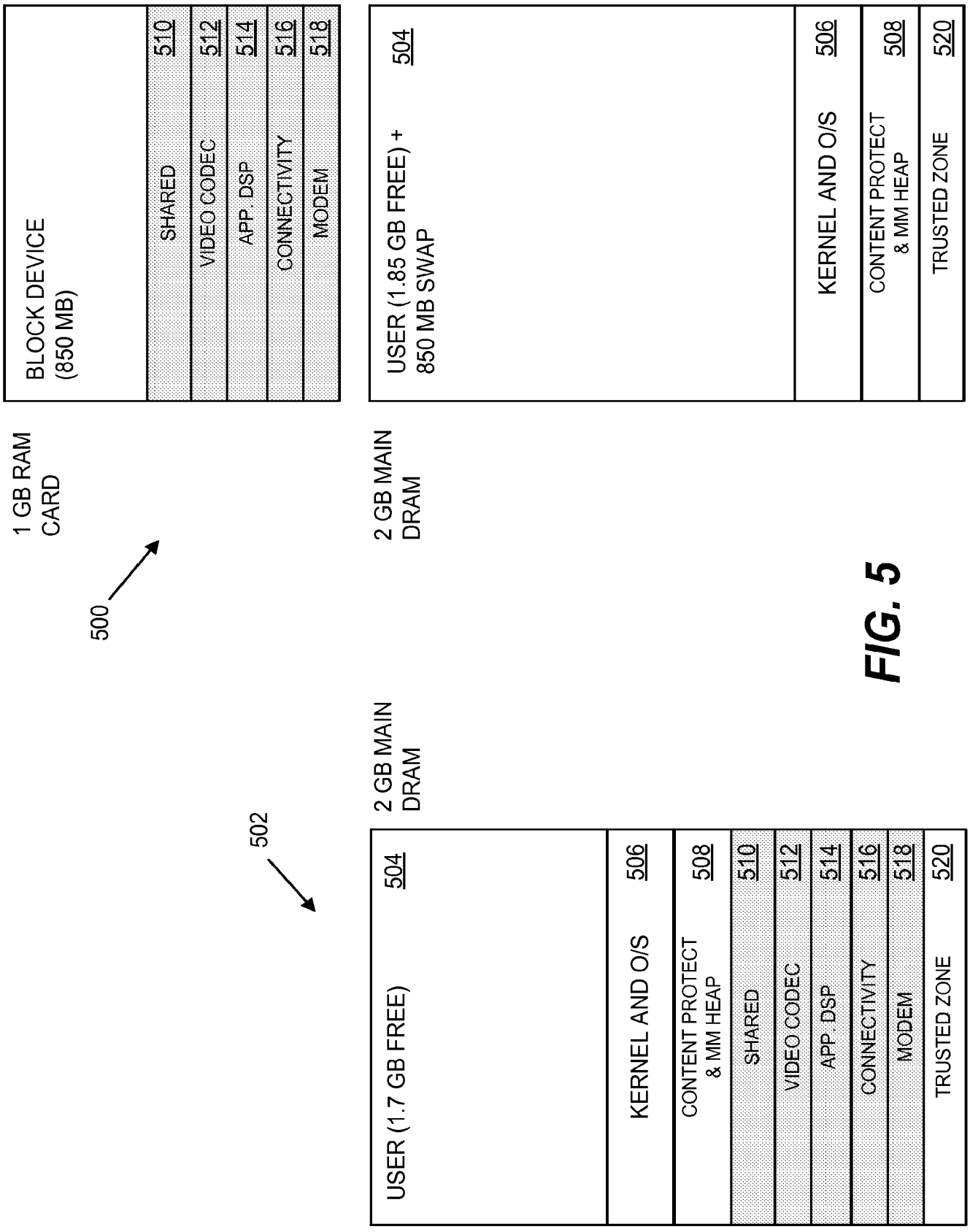
1 GB RAM CARD
500
BLOCK DEVICE (850 MB)
SHARED 510
VIDEO CODEC 512
APP. DSP 514
CONNECTIVITY 516
MODEM 518
2 GB MAIN DRAM
USER (1.85 GB FREE) + 850 MB SWAP 504
KERNEL AND O/S 506
CONTENT PROTECT & MM HEAP 508
TRUSTED ZONE 520
502
2 GB MAIN DRAM
USER (1.7 GB FREE) 504
KERNEL AND O/S 506
CONTENT PROTECT & MM HEAP 508
SHARED 510
VIDEO CODEC 512
APP. DSP 514
CONNECTIVITY 516
MODEM 518
TRUSTED ZONE 520

FIG. 5

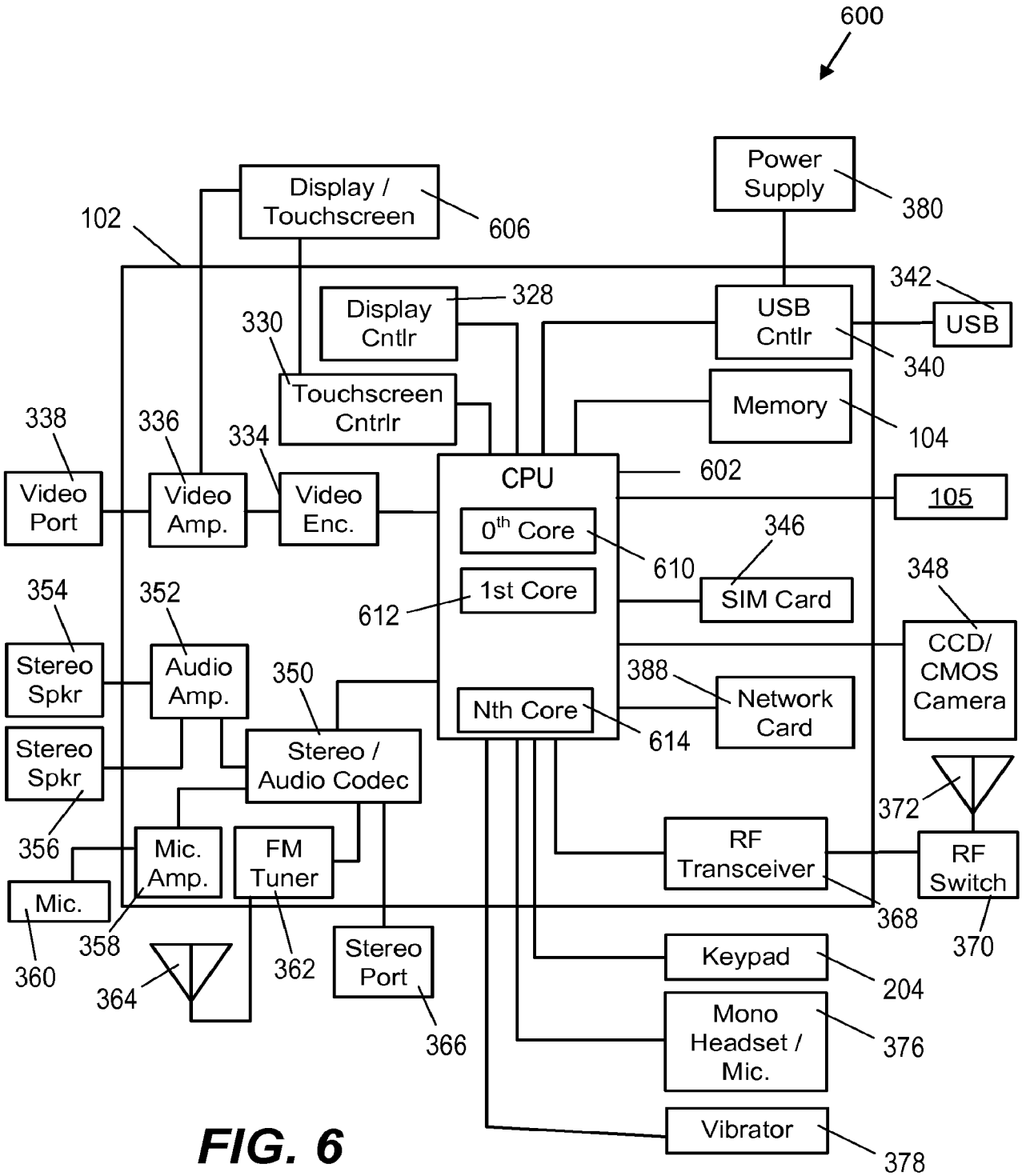
600
Power Supply
380
Display / Touchscreen
606
102
342
USB
328
Display Cntlr
USB Cntlr
330
340
Touchscreen Cntrlr
Memory
104
338
336
334
CPU
602
Video Port
Video Amp.
Video Enc.
105
0th Core
346
610
SIM Card
348
354
352
1st Core
612
CCD/ CMOS Camera
Stereo Spkr
Audio Amp.
350
388
Network Card
Nth Core
614
Stereo Spkr
Stereo / Audio Codec
372
356
Mic. Amp.
FM Tuner
RF Transceiver
RF Switch
Mic.
368
370
358
362
Stereo Port
Keypad
360
364
204
Mono Headset / Mic.
376
366
Vibrator
378

FIG. 6

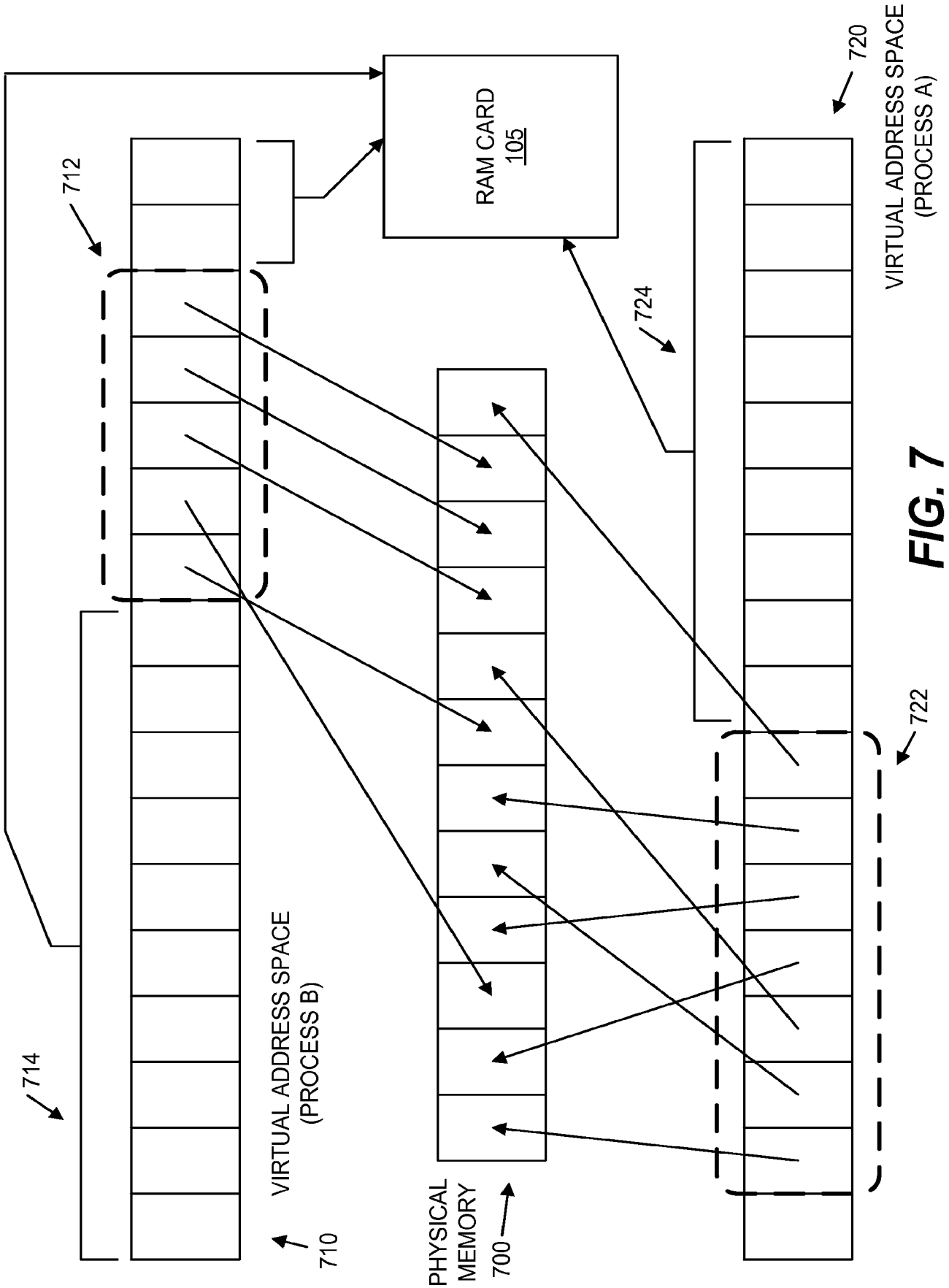
RAM CARD
105
712
714
VIRTUAL ADDRESS SPACE
(PROCESS B)
710
PHYSICAL
MEMORY
700
720
VIRTUAL ADDRESS SPACE
(PROCESS A)
722
724

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/045133

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/16 G06F12/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 757 483 A1 (SAMSUNG ELECTRONICS CO LTD [KR]) 23 July 2014 (2014-07-23)	1-6, 8-13, 15-20, 22,23, 26-30
Y	paragraph [0009] paragraph [0018] paragraph [0024] - paragraph [0042] paragraph [0053] - paragraph [0062] paragraph [0074] - paragraph [0091]	7,14,21, 24,25
Y	US 5 793 620 A (BURNWORTH [US] ET AL) 11 August 1998 (1998-08-11) column 3, line 1 - line 52	7,14,21, 24,25
A	US 2014/164720 A1 (STEWART [US] ET AL) 12 June 2014 (2014-06-12) paragraph [0030] - paragraph [0046] paragraph [0058] - paragraph [0062]	1-30

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 December 2015	18/12/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	McDonagh, Fintan

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/045133

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 2757483 A1	23-07-2014	CN 103942009 A	23-07-2014
		EP 2757483 A1	23-07-2014
		KR 20140093505 A	28-07-2014
		US 2014208006 A1	24-07-2014
US 5793620 A	11-08-1998	NONE	
US 2014164720 A1	12-06-2014	CN 104854572 A	19-08-2015
		EP 2929447 A1	14-10-2015
		KR 20150095724 A	21-08-2015
		TW 201435589 A	16-09-2014
		US 2014164720 A1	12-06-2014
		WO 2014092884 A1	19-06-2014