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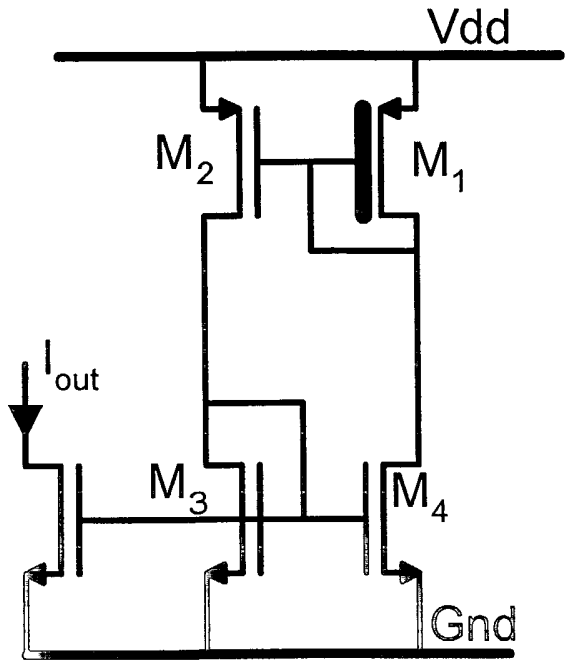
(54) Title: REFERENCE CIRCUIT



(57) Abstract: A reference circuit comprising first and second field effect transistors connected to form a first current mirror, and a third and fourth field effect transistors connected to form a second current mirror, wherein a property of the first transistor is mismatched relative to the second transistor such that the threshold voltage of the first transistor is significantly higher than the threshold voltage of the second transistor, and the drain current versus gate-source voltage responses of the first and second transistors have substantially different gradients for current levels at which the reference current is operated.

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REFERENCE CIRCUIT

The present invention relates to a reference circuit, and particularly though not exclusively to a reference circuit suitable for providing a current.

Current reference circuits are fundamental building blocks of integrated circuits, and biasing for most integrated circuits can be traced back to an on-chip current reference circuit.

A conventional prior art current reference circuit [1] is shown in figure 1. The circuit comprises two pairs of field effect transistors (FETs) and a resistor. The first pair of FETs, M_1 and M_2, are matched and are n-channel FETs. They form a first current mirror that maintains equal currents in the drains of M_3 and M_4. The term 'matched pair' refers to the fact that M_1 and M_2 are constructed such that their properties are as identical as possible. A second pair of FETs M_3 and M_4 are p-channel FETs, and form a current mirror-like structure of non-unity gain, which is connected to the first current mirror. M_4 is K times wider than M_3, and has a resistance R_S connected between the source terminal and Vdd, the positive supply rail. The first current mirror and the current mirror-like structure are connected together to minimise the effect of supply voltage variation upon the current provided. Neglecting secondary effects, the size of the current generated by the prior art reference circuit is determined by the magnitude of a resistor R_S, the mobility μ_h of the holes of the PMOS devices, the gate oxide capacitance per unit area C_{ox}, the ratio K between the width of M_3 and M_4, and the aspect ratio (W/L) of the PMOS devices according to the following relationship:

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_P} \cdot \frac{1}{R_1^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

The prior art circuit shown in figure 1 suffers from the disadvantage that a large resistor, necessary for producing small reference currents, cannot easily be incorporated into an integrated circuit design (it usually occupies a substantial chip area). This is particularly the case in implanted bio-medical applications, where the current required to be generated by a current reference circuit is very small, typically of the order of nanoamperes, and the magnitude of resistor R_1 needed to provide the current is correspondingly large. The area occupied by a resistor of suitable magnitude may be prohibitive for bio-medical applications.

Alternative reference circuits based on replacing the resistor with active devices have been proposed [2][3][4], but these circuits are much more complicated and occupy substantial chip areas.

It is an object of the present invention to provide a reference circuit that overcomes or mitigates one or more of the above disadvantages.

According to the invention there is provided a reference circuit comprising first and second field effect transistors connected to form a first current mirror, and a third and fourth field effect transistors connected to form a second current mirror, wherein a property of the first transistor is mismatched relative to the second transistor such that the threshold voltage of the first transistor is significantly higher than the threshold voltage of the second transistor, and the drain current versus gate-source voltage responses of the first and second transistors have substantially different gradients for current levels at which the reference circuit is operated.

Suitably, the property of the first transistor is selected such that, for a particular voltage applied to the common gate of the first transistor and the second transistor, the second transistor operates substantially in its strong inversion saturation region whilst the first transistor operates substantially in its weak inversion saturation region.

Suitably, the mismatch is obtained by providing the first transistor with an oxide layer having a thickness which is greater than the oxide layer of the second transistor.

Suitably, the thickness of the oxide layer provided on the first transistor is at least twice the thickness of the oxide layer provided on the second transistor.

Suitably, the thickness of the oxide layer provided on the first transistor is at least 5 nanometers greater than the thickness of the oxide layer provided on the second transistor.

Suitably, the thickness of the oxide layer provided on the first transistor is at least 10 nanometers greater than the thickness of the oxide layer provided on the second transistor.

Suitably, the mismatch is obtained by providing more doping to the substrate of the first transistor than the substrate of the second transistor.

Suitably, the first transistor comprises a modified twin tub configuration, in which a well layer separating an upper tub layer and a substrate layer is omitted during fabrication such that the upper tub layer is located directly on the substrate layer, the upper tub layer thereby providing a substrate layer having increased doping.

Suitably, the third and fourth transistors are matched such that either side of the second current mirror is constrained to draw substantially the same current, the circuit having a stable operating point where the drain current versus gate-source voltages of the first and second transistors intersect.

Suitably, the third and fourth transistors are not matched, so that one side of the second current mirror is constrained to draw more current than the other side.

Suitably, the third and fourth transistors are field effect transistors, and the width of the channel of one of the transistors is selected to be different to the width of the channel of the other transistor so that that side of the current mirror is constrained to draw a current which is a ratio of the current on the other side.

Suitably, the third and fourth transistors are field effect transistors, and the length of the channel of one of the transistors is selected to be different to the length of the channel of the other transistor so that that side of the current mirror is constrained to draw a current which is a ratio of the current on the other side.

Suitably, the third and fourth transistors are bipolar transistors.

Suitably, the length of the first transistor is selected to be different to the length of the second transistor.

Suitably, the width of the first transistor is selected to be different to the width of the second transistor.

Suitably, a reference voltage is obtained from the common gate of the third and fourth transistors.

Suitably, a copy of the reference current is obtained by connecting a FET to the common gate of the third and the fourth transistor.

Suitably, the first and second transistors are p-channel field effect transistors, and the third and fourth transistors are n-channel field effect transistors.

A specific embodiment of the invention will now be described by way of example only, with reference to the accompanying figures in which:

Figure 1 is a circuit diagram which represents a conventional prior art current reference circuit;

Figure 2 is a circuit diagram which represents a current reference circuit according to the invention;

Figure 3 is a graph which illustrates drain current versus gate-source voltage responses of field effect transistors of the circuit shown in figure 2; and

Figure 4 is a schematic illustration of a prior art twin tub field effect transistor.

Referring to figure 2, a circuit according to the invention comprises two n-channel field effect transistors M_3 and M_4 connected to form a first current mirror, and two p-channel field effect transistors M_1 and M_2 connected to form a second current mirror. The sources of the p-channel transistors M_1 and M_2 are connected to a voltage rail V_{dd} which provides between 3.5 and 5 volts (the voltage source may be for example a lithium battery which provides 4 volts). The sources of the n-channel transistors M_3 and M_4 are connected to ground.

In a conventional arrangement the field effect transistors M_1 and M_2 would be of different width and have a resistor in series with M_1 such that, for a given gate voltage, the current provided from the drain of each of the transistors is equal. However, in the circuit shown in figure 2 the transistors M_3 and M_4 have no need for a series resistance, but instead the thickness of the oxide layer provided on transistor M_1 is significantly thicker than the oxide thickness provided on transistor M_2. In one embodiment of the invention the thickness of the oxide layer on M_2 is 17 nanometers, whereas the thickness of the oxide layer on M_1 is 40 nanometers. The effect of the oxide thickness mismatch is that the threshold voltage of M_1 is much greater than that of M_2.

In operation, M_2 is turned on first and enters the square law saturation region (i.e. the rate of increase of current with respect to gate source voltage is quadratic). M_1 is weakly turned on at a higher voltage, and operates in the weak inversion region (i.e. the rate of increase of current with respect to gate source voltage is exponential). Since M_1 is turned on at a higher voltage than M_2, and provides current which increases with a steeper gradient, it follows that there is a value of gate voltage for which both M_1 and M_2 provide the same output current. This is the stable operating

point of the circuit, given that the gain of the current mirror comprising of M_3 and M_4 is unity.

It will be understood that the output current of the reference circuit is stable, under stable ambient conditions. If the ambient conditions, e.g. the temperature varies, then the output current of the reference circuit may vary accordingly. This property may be used to provide a reference current which tracks changes in ambient conditions.

Figure 3 is a graph that represents drain current as a function of gate source voltage for both M_1 and M_2. Referring to figure 3, M_2 enters the weak inversion region at a gate source voltage of around 0.3V. The current provided by M_2 at 0.3V is very low, and consequently is not apparent in figure 3. M_2 enters the square law saturation region at around 0.9V, and remains in the square law saturation region up to 2.5V and beyond as is apparent from figure 3.

M_1 enters the weak inversion region at a gate source voltage of around 1.6V, and remains in the weak inversion region over the range of currents represented in figure 3. Since M_1 remains in the weak inversion region, the current provided by M_1 rises exponentially.

The currents provided by M_1 and M_2 intersect at a value of approximately 3.2μA for a gate source voltage of approximately 2.25V. This intersection provides a current which satisfies the operating requirements of the current mirror formed by n-channel transistors M_3 and M_4, i.e. that the current provided by each side of the circuit is equal. The intersection is a stable operating point for the circuit, and the circuit will consequently generate a fixed current of approximately 3.2μA which is independent of the voltage V_{dd} at the bias rail.

The currents provided by M_1 and M_2 will not intersect at higher values, since the gradient of M_1 will never be less than the gradient of M_2 (M_1 will eventually enter the square law saturation region). This means that the circuit has no stable operating

points at higher currents. The currents provided by M_1 and M_2 will converge at zero gate-source voltage and zero current, therefore this could be considered to be a stable operating point of the circuit. The circuit will leave the zero current operating point given a sufficient voltage at V_{dd} and an initial startup charge at the gates of M_3 and M_4 and move to the stable intended operating point which generates the approximately 3.2μA current, in this particular case. Leakage currents can sometime be sufficient to start-up the circuit.

Different current settings for the circuit may be achieved by scaling the response of M_1 and M_2 with respect to each other. For example, by providing M_1 with a thicker oxide layer, the voltage at which M_1 is weakly turned on will increase, and the current provided by the stable operating point will increase.

The quadratic behaviour of a field effect transistor operating in the square law saturation region is determined by the following:

$$I_d = \frac{\mu_h C_{ox} W}{L}(V_{gs} - V_T)^2$$

where I_d is the drain current, μ_h is the mobility of holes, C_{ox} is the capacitance per unit area of the gate, W is the width of the channel, L is the length of the channel, V_{gs} is the gate/source voltage and V_T is the threshold voltage.

The exponential behaviour of a field effect transistor operating in the weak inversion region is determined by the following:

$$I_d = I_k\left(\frac{W}{L}\right)\exp(V_{gs}/nV_T)$$

where I_d is the drain current, I_k is a constant, W is the width of the channel, L is the length of the channel, n is a constant, V_{gs} is the gate/source voltage and V_T is the threshold voltage.

From the above it is clear that different current settings for the circuit may be achieved by modifying the channel width and/or the channel length of the transistors, and in particular by selecting the ratio of width to length. For example, referring to

figure 2, if the width W of the channel of M_2 were to be doubled then the current provided by the circuit would double. Similarly, if the length L of the channel of M_2 were to be doubled then the current provided by the circuit would halve.

The modification of the width or length need not be confined to the p-channel transistors M_1 and M_2, but may instead be used to adjust the properties of the n-channel transistors M_3 and M_4. For example, instead of matching M_3 and M_4, the channel width of M_3 could be double of M_4. This would constrain the circuit to provide twice as much current on the left hand side as on the right hand side. The stable operating point of the circuit would then be at approximately 2.13 volts as indicated by the vertical line A in figure 3. Where n-channel transistors M_3 and M_4 are not matched, it will be appreciated that there is no requirement for the drain currents M_1 and M_2 to be identical.

One suitable combination of channel widths and channel lengths is as follows:

M_2:	Width = 2 Length = 10	M_1:	Width = 40 Length = 5
M_3:	Width = 2 Length = 20	M_4:	Width = 2 Length = 20

Since M_3 and M_4 are matched, the stable operating point of the circuit is the point at which M_1 and M_2 provide the same current. The large channel width of M_1 compared to M_2 is necessary since the threshold voltage of M_1 is much higher than that of M_2.

The circuit may be used to generate a reference current via a copy of the drain current of M_3 by connecting yet another matched device to the common gate of M_1 and M_2. Alternatively, the gate voltage of M_1 and M_2, can be used as a reference voltage.

In the described embodiment of the invention the transistors are field effect transistors. It will be appreciated that any suitable field effect transistors may be used. M_1 and M_2 could be bipolar transistors, for example where biCMOS is used.

The invention may be implemented as a single semiconductor chip, making it particularly suited to biomedical applications.

In the above mentioned semiconductor technology process, the chip has a standard feature size of 0.8μm, and the low voltage field effect transistors provided on the chip has a typical standard gate oxide layer of around 17nm. Where the invention is used, the mid-gate oxide layer of transistor M_1 is approximately 50nm. Some semiconductor manufacturers already provide transistors with oxide layers of similar this thickness, for use in high voltage processors (high voltage typically means around 20-30V rather than a normal voltage of around 5.5V). It would be possible therefore to manufacture a chip which incorporates the invention using existing techniques.

For a semiconductor chip having a standard feature size of 0.25μm, the field effect transistors provided on the chip will have an oxide layer of around 5 or 6nm. Where the invention is used, the oxide layer of transistor M_1 could be approximately 13nm. Again, a chip that incorporates the invention could be manufactured using existing manufacturing processes that support two different voltages e.g. 3V and 5V devices.

An alternative, or additional, means of modifying the threshold voltage of transistor M_1 is by modifying the doping of the substrate. An increase of the doping of the substrate will cause a corresponding increase of the threshold voltage required to invert the channel of the transistor.

One manner in which the substrate doping may be increased in a silicon chip is by modifying a conventional twin tub field effect transistor configuration. A prior art twin tub FET is shown in figure 4. The FET comprises a contact 10 and silicon oxide layer 11, located on top of a negatively doped p-tub 12. Positively doped n+

source 13 and drain 14 regions are provided at either side of the silicon oxide layer 11. The entire p-well 12 is located in a negatively doped n-well 15. The n-well 15 is located in a positively doped p-substrate 16. The n-well 15 isolates the p-well 12 from the p-substrate 16, providing the FET with advantageous features, and this is why the twin tub FET is used in prior art silicon chips.

The invention may be implemented by omitting the n-well 15 during fabrication of the FET, so that the p-well layer lies directly over the p-substrate layer. The effect of doing this will be to provide a conventionally configured FET having a substrate layer which is more strongly doped than the substrate layers of other FET's provided on the chip. The threshold of the FET is increased by the higher doping of the p-substrate.

Use of technologies with two different gate oxide thickness is preferred over modification of the doping because the oxide thickness is better controlled and supplied device models are more accurate.

Where different gate oxide thickness devices are used to implement the invention, the thicknesses should be carefully controlled in order to ensure that the invention functions correctly. The thickness of the oxide layer provides separation of the current versus gate source voltage curves as shown in figure 3. If the thicknesses of the oxide layers are very close, then small changes of the doping or device size may influence the operation of the invention. Thus, it is preferred to provide oxide layers having very different thicknesses, for example a difference of a factor of two or greater.

It will be appreciated by those skilled in the art that the circuit shown in figure 2 may be constructed in an 'opposite' sense by replacing n-channel transistors with p-channel transistors, and vice versa. Other modifications of the invention will be apparent to those skilled in the art.

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Claims

1. A reference circuit comprising first and second field effect transistors connected to form a first current mirror, and third and fourth field effect transistors connected to form a second current mirror, wherein a property of the first transistor is mismatched relative to the second transistor such that the threshold voltage of the first transistor is significantly higher than the threshold voltage of the second transistor, and the drain current versus gate-source voltage responses of the first and second transistors have substantially different gradients for current levels at which the reference current is operated.

2. A reference circuit according to claim 1, wherein the property of the first transistor is selected such that, for a particular voltage applied to the common gate of the first transistor and the second transistor, the second transistor operates substantially in its strong inversion saturation region whilst the first transistor operates substantially in its weak inversion saturation region.

3. A reference circuit according to claim 1 or claim 2, wherein the mismatch is obtained by providing the first transistor with an oxide layer having a thickness which is greater than the oxide layer of the second transistor.

4. A reference circuit according to claim 3, wherein the thickness of the oxide layer provided on the first transistor is at least twice the thickness of the oxide layer provided on the second transistor.

5. A reference circuit according to claim 3 or claim 4, wherein the thickness of the oxide layer provided on the first transistor is at least 5 nanometers greater than the thickness of the oxide layer provided on the second transistor.

6. A reference circuit according to claim 4, wherein the thickness of the oxide layer provided on the first transistor is at least 10 nanometers greater than the thickness of the oxide layer provided on the second transistor.

7. A reference circuit according to any preceding claim, wherein the mismatch is obtained by providing more doping to the substrate of the first transistor than the substrate of the second transistor.

8. A reference circuit according to claim 7, wherein the first transistor comprises a modified twin tub configuration, in which a well layer separating an upper tub layer and a substrate layer is omitted during fabrication such that the upper tub layer is located directly on the substrate layer, the upper tub layer thereby providing a substrate layer having increased doping.

9. A reference circuit according to any preceding claim, wherein the third and fourth transistors are matched such that either side of the second current mirror is constrained to draw substantially the same current, the circuit having a stable operating point where the drain current versus gate-source voltages of the first and second transistors intersect.

10. A reference circuit according to any of claims 1 to 8, wherein the third and fourth transistors are not matched, so that one side of the second current mirror is constrained to draw more current than the other side.

11. A reference circuit according to claim 10, wherein the third and fourth transistors are field effect transistors, and the width of the channel of one of the transistors is selected to be different to the width of the channel of the other transistor so that that side of the current mirror is constrained to draw a current which is a ratio of the current on the other side.

12. A reference circuit according to claim 10 or claim 11, wherein the third and fourth transistors are field effect transistors, and the length of the channel of one of the transistors is selected to be different to the length of the channel of the other transistor so that that side of the current mirror is constrained to draw a current which is a ratio of the current on the other side.

13. A reference circuit according to any of claims 1 to 10, wherein the third and fourth transistors are bipolar transistors.

14. A reference circuit according to any preceding claim, wherein the length of the first transistor is selected to be different to the length of the second transistor.

15. A reference circuit according to any preceding claim, wherein the width of the first transistor is selected to be different to the width of the second transistor.

16. A reference circuit according to any preceding claim, wherein a reference voltage is obtained from the common gate of the third and fourth transistors.

17. A reference circuit according to any preceding claim, wherein a copy of the reference current is obtained by connecting a FET to the common gate of the third and the fourth transistor.

18. A reference circuit according to any preceding claim, wherein the first and second transistors are p-channel field effect transistors, and the third and fourth transistors are n-channel field effect transistors.

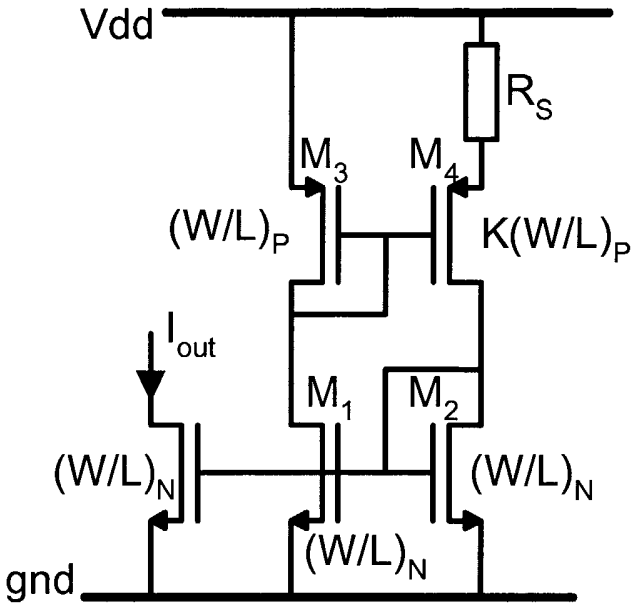

FIGURE 1- PRIOR ART

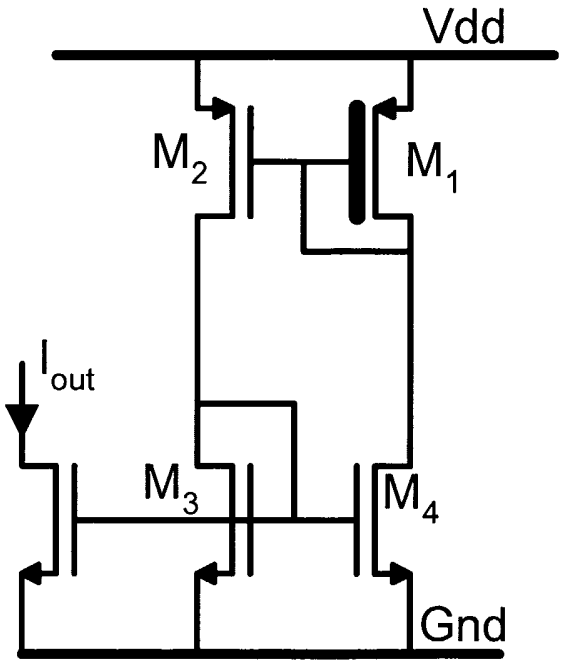

FIGURE 2

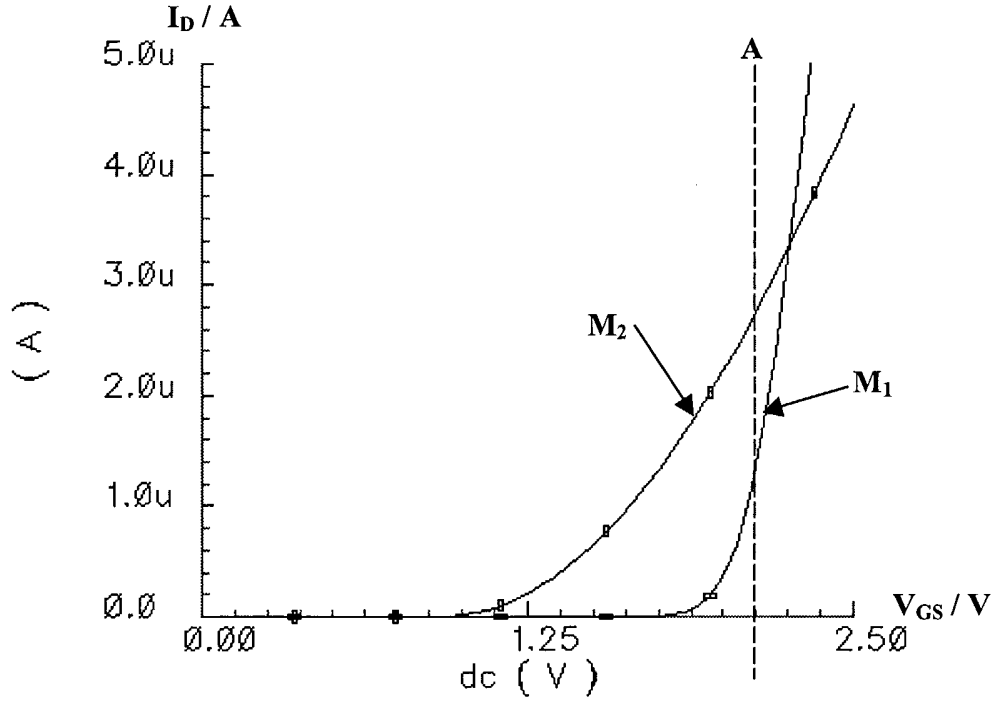

FIGURE 3

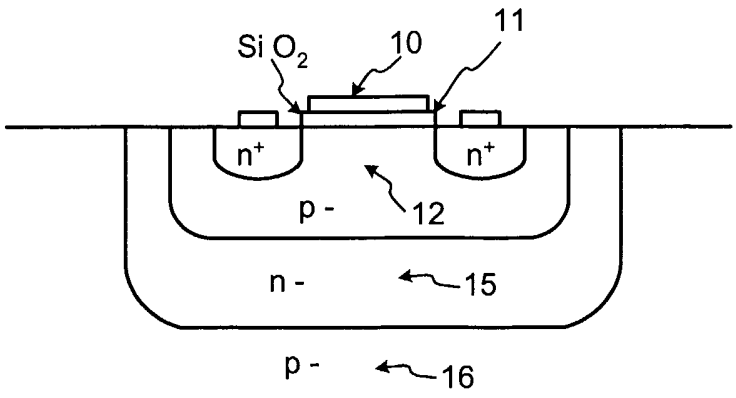

FIGURE 4 – Prior Art

INTERNATIONAL SEARCH REPORT

Interna pplication No
PCT/GB 03/02156

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G05F3/24 G05F3/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 6 096 610 A (GHANI TAHIR ET AL) 1 August 2000 (2000-08-01) column 9, line 66 -column 12, line 10; figures 3A-4	7,8

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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