



US 20060289950A1

(19) **United States**

(12) **Patent Application Publication**
Weimer

(10) **Pub. No.: US 2006/0289950 A1**

(43) **Pub. Date: Dec. 28, 2006**

(54) **METHOD OF COMPOSITE GATE FORMATION**

of application No. 09/935,255, filed on Aug. 22, 2001.

(75) Inventor: **Ronald A. Weimer**, Boise, ID (US)

Correspondence Address:
WHYTE HIRSCHBOECK DUDEK S.C.
555 EAST WELLS STREET
SUITE 1900
MILWAUKEE, WI 53202 (US)

Publication Classification

(51) **Int. Cl.**
H01L 29/94 (2006.01)
H01L 29/76 (2006.01)
H01L 31/00 (2006.01)
(52) **U.S. Cl.** **257/411**

(73) Assignee: **Micron Technology Inc.**, Boise, ID

(21) Appl. No.: **11/513,659**

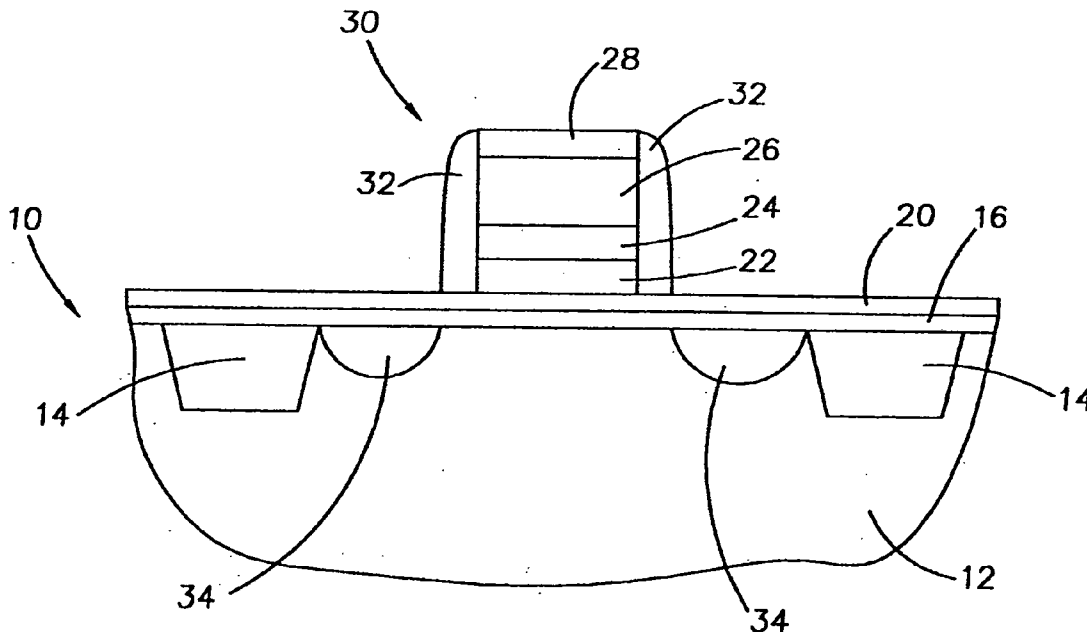
(22) Filed: **Aug. 31, 2006**

(57) **ABSTRACT**

Methods for forming a nitride barrier film layer in semiconductor devices such as gate structures, and barrier layers, semiconductor devices and gate electrodes are provided. The nitride layer is particularly useful as a barrier to boron diffusion into an oxide film. The nitride barrier layer is formed by selectively depositing silicon onto an oxide substrate as a thin layer, and then thermally annealing the silicon layer in a nitrogen-containing species or exposing the silicon to a plasma source of nitrogen to nitridize the silicon layer.

Related U.S. Application Data

(62) Division of application No. 10/931,840, filed on Sep. 1, 2004, which is a division of application No. 10/236,841, filed on Sep. 6, 2002, which is a division



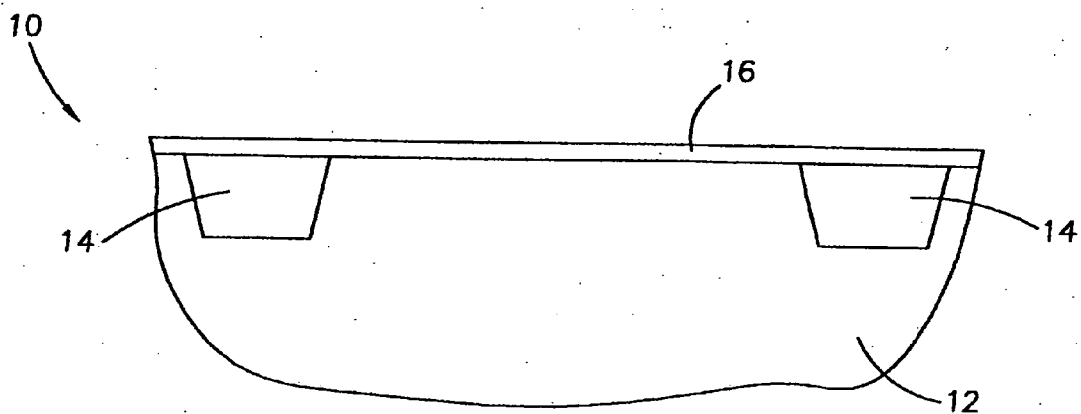


FIG.1

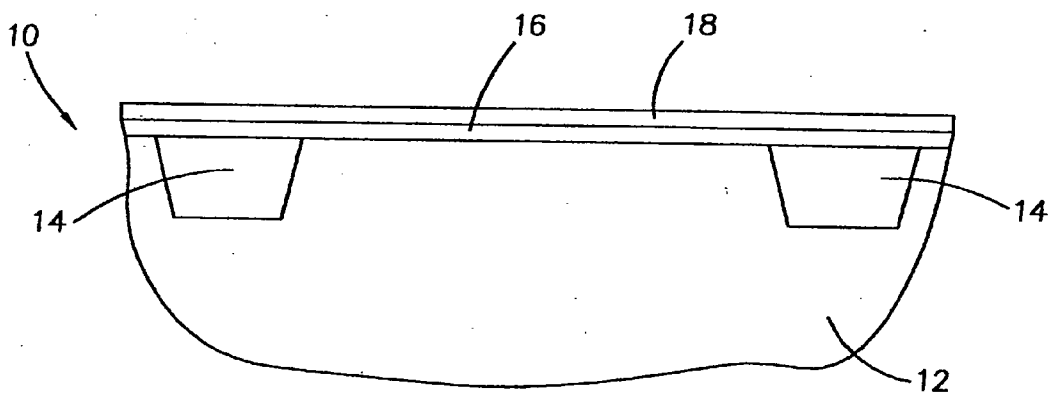


FIG.2

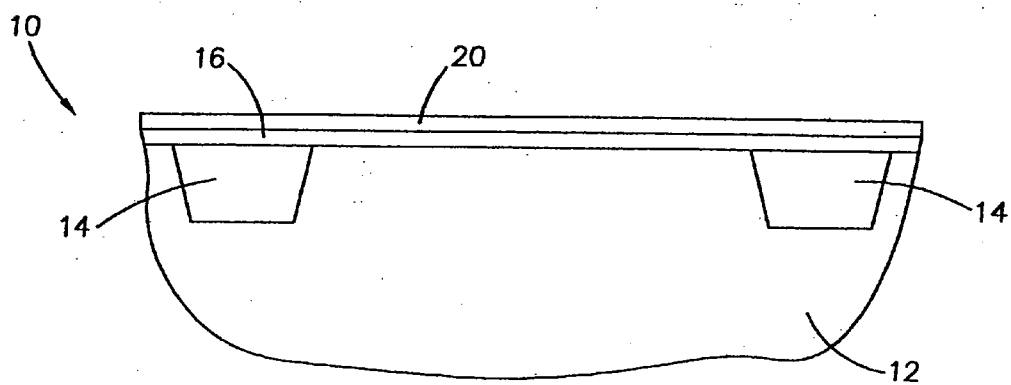


FIG. 3

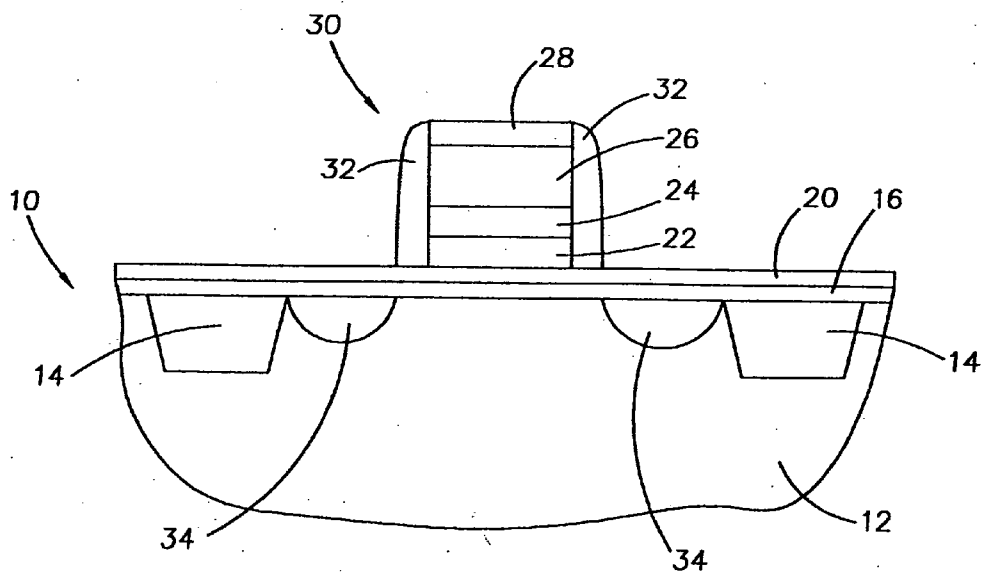


FIG. 4

METHOD OF COMPOSITE GATE FORMATION

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is a division of U.S. patent application Ser. No. 10/931,840, filed Sep. 1, 2004, currently pending, which is a division of U.S. patent application Ser. No. 10/236,841, filed Sep. 6, 2002, currently pending, which is a division of U.S. patent application Ser. No. 09/935,255, filed Aug. 22, 2001, currently pending.

FIELD OF THE INVENTION

[0002] The present invention relates generally to semiconductor fabrication and, more particularly, to methods of forming nitride barrier layers used in semiconductor devices.

BACKGROUND OF THE INVENTION

[0003] Metal-insulator-silicon (MIS) transistors, including metal-oxide-silicon (MOS) transistors, are comprised of doped source and drain regions formed in the surface of a semiconductor substrate, a channel region between the source and drain, and a gate electrode situated over the channel region. The gate electrode is physically and electrically separated from the channel by a thin gate dielectric (oxide) layer, typically silicon dioxide. The gate electrode typically comprises a doped polysilicon material. Diffusion of dopants such as boron from the doped polysilicon gate through the gate oxide layer into the underlying silicon substrate poses serious problems in processing and the functioning of the device.

[0004] To inhibit boron diffusion, nitrogen has been incorporated into the gate oxide layer. One conventional method of incorporating nitrogen into the oxide layer is by anneal of the oxide layer in nitric oxide (NO), nitrous oxide (N₂O), ammonia (NH₃) or other nitrogen-containing species. However, thermal nitridation of the gate oxide layer results in nitrogen incorporation at the silicon/oxide interface, which increases the ability of the gate oxide layer to suppress boron penetration but can result in transconductance loss.

[0005] Another method of forming a nitrided gate oxide layer is by remote plasma nitridation by exposing the surface of the oxide layer to a plasma generated species of nitrogen. This results in the polysilicon/oxide interface being nitridized as opposed to the gate oxide/silicon interface, thus avoiding transconductance loss. However, data indicates that the plasma nitridation may not be scaleable below 25 angstroms for integrated circuit (IC) devices with high processing thermal budgets such as DRAMS or flash devices due to the loss of integrity of the gate oxide as well as the loss of transconductance due to the proximity of nitrogen to the gate oxide-silicon interface.

[0006] Another conventional method to incorporate nitrogen into the gate oxide layer is to form a composite gate dielectric layer comprising a silicon nitride layer and an oxide layer. An issue with forming such a composite gate oxide is that the interface between the silicon nitride and oxide layers typically requires rigorous post-treatment processing to eliminate potential sources of charge trapping. In addition, composite gate dielectrics that comprise nitride and thermal oxides have limitations due to the total effective

oxide thickness that can be achieved due to poor nucleation of nitride on oxide. This requires the formation of a relatively thick nitride layer resulting in an overall effective oxide thickness that is higher than that which is considered as usable.

[0007] Thus, a need exists for a nitride barrier layer that avoids such problems.

SUMMARY OF THE INVENTION

[0008] The present invention provides methods for forming a nitride barrier film layer useful in fabrication of semiconductor devices such as gate structures. The nitride layer is particularly useful as a barrier to boron diffusion into an oxide film.

[0009] In one aspect, the invention provides methods for forming a nitride barrier layer over a dielectric (oxide) substrate. The dielectric layer is exposed to a silicon-containing species under low partial pressure, high vacuum to nucleate the surface of the dielectric layer and deposit a thin layer of silicon, which is then exposed to a nitrogen-containing species to nitridize the silicon and form a silicon nitride barrier layer. The silicon-containing species can be deposited, for example, by plasma enhanced chemical vapor deposition, low pressure chemical vapor deposition, rapid thermal chemical vapor deposition, among other processes. The silicon layer can comprise polysilicon or amorphous silicon. In an embodiment of the method, an oxide layer is irradiated with a silicon-containing species at a low partial pressure of about 10⁻² Torr (10 mTorr) or less to selectively deposit a thin layer of silicon onto the oxide surface, preferably about 10 to about 20 angstroms thick. The silicon layer can then be thermally annealed in a nitrogen-containing species at a preferred temperature of about 700° C. to about 900° C., or exposed to a plasma source of nitrogen to nitridize the silicon. The plasma nitrogen can be produced, for example, by a downstream microwave system, an electron cyclotron resonance system, an inductive coupled plasma system, a radio frequency (RF) system, among others.

[0010] In another aspect, the invention provides methods for forming a semiconductor device. In one embodiment, the method comprises exposing a dielectric layer disposed on a silicon substrate to a silicon-containing species under a low partial pressure of about 10⁻² Torr or less, and a flow rate of less than 100 sccm to deposit a layer of about 10 to about 20 angstroms silicon; and exposing the silicon layer to a nitrogen-containing species to nitridize the silicon and form a silicon nitride barrier layer. The silicon layer can be thermally annealed in a nitrogen-containing species, preferably at a temperature of about 700° C. to about 900° C., or exposed to a plasma source of a nitrogen-containing species.

[0011] In another aspect, the invention provides methods for forming a gate electrode. In one embodiment, the method comprises exposing a gate oxide (dielectric) layer disposed on a silicon substrate to a silicon-containing species at a low partial pressure of about 10⁻² Torr or less to deposit a layer of about 10 to about 20 angstroms silicon; and exposing the silicon layer to a nitrogen-containing species to form a silicon nitride barrier layer. In one embodiment, the silicon layer can be thermally annealed in a nitrogen-containing species, preferably at a temperature of about 700° C. to about 900° C. In another embodiment, the silicon layer can

be exposed to a plasma source of nitrogen. The method can further comprise forming a conductive polysilicon layer comprising a boron dopant over the nitride barrier layer, and additional layers as desired including, for example, a metal silicide layer such as tungsten silicide (WSi_x), a barrier layer such as titanium nitride (TiN), a conductive metal layer such as tungsten (W), and an insulative nitride cap. The nitride barrier layer inhibits passage of boron from the conductive polysilicon layer into the gate oxide layer.

[0012] In another aspect, the invention provides a nitride barrier layer. The barrier layer comprises a nitridized silicon layer of about 10 to about 20 angstroms formed on an oxide layer by irradiating the oxide layer with a silicon-containing species under a low partial pressure of about 10^{-2} Torr or less, and nitridizing the silicon layer to silicon nitride by exposure to a nitrogen-containing species. In one embodiment, the nitride barrier layer comprises thermally annealed nitridized silicon having a thickness of about 10 to about 20 angstroms, and disposed adjacent an oxide layer. In another embodiment, the nitride barrier layer comprises a plasma nitrogen annealed silicon layer.

[0013] In yet another aspect, the invention provides a semiconductor device. The device comprises a semiconductor substrate comprising silicon, an oxide layer disposed adjacent to the semiconductor substrate, and a diffusion barrier layer of about 10 to about 20 angstroms disposed adjacent the oxide layer and comprising a nitridized silicon layer formed by irradiating an oxide layer with a silicon-containing species under low partial pressure of about 10^{-2} Torr or less, and nitridizing the silicon to silicon nitride by exposure to a nitrogen-containing species. In one embodiment, the semiconductor device comprises a diffusion barrier layer comprising a thin layer of nitrogen annealed silicon, the silicon being thermally annealed or plasma annealed in a nitrogen-containing species.

[0014] In a further aspect, the invention provides a gate electrode. The gate electrode comprises a gate oxide layer disposed adjacent to a semiconductor substrate, typically silicon, and a diffusion barrier layer disposed adjacent the gate oxide layer; the diffusion barrier layer having a thickness of about 10 to about 20 angstroms and comprising a nitridized silicon layer formed by irradiating the gate oxide layer with a silicon-containing species under low partial pressure (about 10^{-2} Torr or less), and nitridizing the silicon to silicon nitride by exposure to a nitrogen-containing species. In one embodiment, the diffusion barrier layer of the gate electrode comprises silicon thermally annealed in a nitrogen-containing species. In another embodiment, the gate electrode comprises a diffusion barrier comprising a plasma nitrogen annealed silicon.

[0015] The invention advantageously provides an improved interface between a silicon nitride barrier layer and an underlying dielectric (oxide) layer, having less traps and requiring less post treatment (e.g., oxidation) of the gate dielectric. In addition, the invention achieves a relatively thin nitride layer thus decreasing the effective oxide thickness as compared to conventionally used methods.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Preferred embodiments of the invention are described below with reference to the following accompanying drawings, which are for illustrative purposes only.

Throughout the following views, the reference numerals will be used in the drawings, and the same reference numerals will be used throughout the several views and in the description to indicate same or like parts.

[0017] FIG. 1 is a diagrammatic cross-sectional view of a semiconductor wafer fragment at a preliminary step of a processing sequence.

[0018] FIGS. 2-4 are views of the wafer fragment of FIG. 1 at subsequent and sequential processing steps, showing fabrication of a nitride barrier layer in a stacked gate electrode according to an embodiment of the method of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] The invention will be described generally with reference to the drawings for the purpose of illustrating the present preferred embodiments only and not for purposes of limiting the same. The figures illustrate processing steps for use in the fabrication of semiconductor devices in accordance with the present invention. It should be readily apparent that the processing steps are only a portion of the entire fabrication process.

[0020] In the current application, the terms "semiconductive wafer fragment" or "wafer fragment" or "wafer" will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials such as a semiconductor wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure including, but not limited to, the semiconductive wafer fragments or wafers described above.

[0021] An embodiment of a method of the present invention is described with reference to FIGS. 1-4, in a method of forming a gate electrode in a stacked configuration. The gate electrode generally comprises a stack of materials including a gate oxide (dielectric), a conductively doped polysilicon, and can further include a metal silicide layer, a barrier layer, a conductive layer, and an insulative cap.

[0022] While the concepts of the invention are conducive to the fabrication of gate electrodes, the concepts described herein can be applied to other semiconductor devices that would likewise benefit from the fabrication of a nitride barrier film as described herein. Therefore, the depiction of the invention in reference to the manufacture of a stacked gate configuration is not meant to limit the extent to which one skilled in the art might apply the concepts taught herein.

[0023] Referring to FIG. 1, a portion of a semiconductor wafer 10 is shown at a preliminary processing step. The wafer fragment 10 in progress can comprise a semiconductor wafer substrate or the wafer along with various process layers formed thereon, including one or more semiconductor layers or other formations, and active or operable portions of semiconductor devices.

[0024] The wafer fragment 10 is shown as comprising a semiconductor substrate 12, an exemplary substrate being a bulk substrate material of semiconductive or semiconductor material, for example, monocrystalline silicon. The substrate

12 is provided with isolation regions **14** formed therein, for example, shallow trench isolation regions. A gate oxide (dielectric) layer **16** overlies the substrate **12**. The gate oxide layer **16** can comprise, for example, silicon dioxide (SiO_2), tantalum pentoxide (Ta_2O_5), hafnium dioxide (HfO_2), and aluminum trioxide (Al_2O_3), among others. The gate oxide layer **16** can be formed by conventional methods, and is typically an oxide layer grown directly on the base silicon substrate material **12**, but can also be a deposited layer.

[0025] According to the invention, the gate oxide layer **14** is irradiated with a silicon-containing species under low partial pressure, high vacuum conditions to deposit (nucleate) a thin layer **18** of silicon onto the surface **16** of the gate oxide layer **14**, as shown in **FIG. 2**. The silicon layer can comprise polysilicon or amorphous silicon. The processing conditions results in a silicon layer **18** that is thinner than can be achieved under standard silicon growth conditions, i.e., a temperature greater than 600°C ., and a pressure greater than 100 mTorr, with SiH_2 , Si_2H_7 , or dichlorosilane (DCS, SiH_2Cl_2). Preferably, the silicon layer **18** is less than about 30 angstroms, preferably about 10 to about 20 angstroms thick. Exemplary silicon source materials include SiH_2Cl_2 , silicon tetrachloride (SiCl_4), and a silicon that contains a hydride such as silane (SiH_4), and disilane (Si_2H_6). The silicon material can be deposited as a layer utilizing any known deposition process including plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), and rapid thermal chemical vapor deposition (RTCVD).

[0026] Preferably, the silicon material is deposited using a thermal deposition process. Processing conditions include a low partial pressure of about 10^{-2} Torr or less, preferably about 10^{-2} to about 10^{-7} Torr, preferably about 10^{-3} to about 10^{-5} Torr, a temperature of about 500°C . to about 700°C ., with a flow rate of the silicon-containing species of less than 100 sccm, preferably about 1 sccm to about 50 sccm, for a duration of about 1 second to about 5 minutes.

[0027] Referring to **FIG. 3**, the silicon layer **18** is then nitridized to convert the silicon to silicon nitride (SiN_x) **20** by exposure to a nitrogen-containing gas using conventional methods. Such conventional methods include a rapid thermal nitridization (RTN), and plasma nitridization, among others. Examples of nitrogen-containing gases for use in such methods include nitrogen (N_2), ammonia (NH_3), nitrogen trifluoride (NF_3), nitrogen oxides (NO_x), and an N_2/He mixture in plasma. The use of a plasma source of nitrogen-containing gas is preferred.

[0028] The nitridation of the silicon layer **18** takes place under conditions that are optimal for nitridation of silicon. An example and preferred rapid thermal nitridization includes exposing the silicon layer to ammonia (NH_3) or other nitrogen-containing ambient at a temperature of about 700°C . to about 900°C ., a pressure of about 1 to about 760 Torr, with a flow rate of about 100 sccm to about 10,000 sccm, for a duration of about 1 second to about 180 minutes. The partial pressure of the nitrogen-containing ambient can range from a low partial pressure, for example, of about 1 to about 10 Torr, up to full atmospheric pressure to optimize processing as desired.

[0029] In a plasma nitridization of the silicon layer **18**, the plasma stream can be produced by a variety of plasma sources, such as a downstream microwave system, an elec-

tron cyclotron residence (ECR) system, an inductive coupled plasma (ICP) system, a radio frequency (RF) system, among others. Exemplary plasma nitridization processes comprise exposing the wafer **10** to a remote microwave plasma source of nitrogen or an inductive coupled plasma (ICP) at a pressure of about 1 to about 20 Torr. The plasma typically comprises the nitrogen-containing gas, preferably nitrogen (N_2) or ammonia (NH_3), and an inert gas such as helium or argon to increase the plasma density.

[0030] The resulting nitride layer **20** functions as a barrier to inhibit the passage of boron through the gate dielectric layer from an overlying boron-doped gate polysilicon layer into the substrate **12**.

[0031] The structure can then be processed by conventional methods to complete the gate electrode. An example of a gate stack comprises a gate oxide layer **16**, a doped polysilicon layer **22**, a barrier layer **24** such as tungsten nitride (WN), a layer **26** of tungsten or other conductive metal, and a nitride cap **28**, as shown in **FIG. 4**. Another example of a gate stack (not shown) comprises a gate oxide, a doped polysilicon, tungsten silicide (WSi_x), titanium silicide (TiSi_x), cobalt silicide (CoSi_x), and a nitride cap. The gate layers can then be patterned and etched utilizing photolithographic processing (i.e., by dry etching) to form a transistor gate stack **30**, as shown. Sidewalls **32** are provided adjacent the transistor gate, and can comprise, for example, silicon dioxide or silicon nitride.

[0032] Thereafter, a dopant implantation, typically with an n-type conductivity-enhancing dopant, can be performed to form the source/drain (S/D) regions **34** in the silicon substrate **12** proximate the gate **30**. The source/drain regions together with the gate form an operative field effect transistor device.

[0033] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

What is claimed is:

1. An integrated circuit, comprising:
 - a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising a gate dielectric layer on a substrate, and a diffusion barrier layer on the gate dielectric layer, consisting essentially of a nitridized silicon layer having a deposited thickness of less than about 30 angstroms.
 2. The circuit of claim 1, being a DRAM.
 3. The circuit of claim 1, being a flash device.
 4. The circuit of claim 1, wherein the diffusion barrier layer has a deposited thickness of about 10-20 angstroms.
 5. An integrated circuit, comprising:
 - a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising a gate dielectric layer on a substrate, and a diffusion barrier layer on the gate dielectric layer,

consisting essentially of nitridized silicon of less than about 30 angstroms being formed by irradiation of the oxide layer with a silicon gas under low partial pressure, followed by exposure to a nitrogen gas.

6. An integrated circuit, comprising:
- a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising a gate dielectric layer on a substrate, and a diffusion barrier layer on the gate dielectric layer, consisting essentially of a silicon layer deposited to a thickness of less than about 30 angstroms and nitridized by exposure to a nitrogen gas.
7. An integrated circuit, comprising:
- a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising a gate dielectric layer on a substrate, and a diffusion barrier layer on the gate dielectric layer, consisting essentially of a thermally annealed and nitridized silicon layer having a thickness of less than about 30 angstroms.
8. An integrated circuit, comprising:
- a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising a gate dielectric layer on a substrate, and a diffusion barrier layer on the gate dielectric layer, consisting essentially of a plasma nitrogen annealed silicon layer having a thickness of less than about 30 angstroms.
9. An integrated circuit, comprising:
- a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising a gate dielectric layer on a substrate, and a diffusion barrier layer on the gate dielectric layer, consisting essentially of chemical vapor deposited and nitridized silicon effective to inhibit diffusion of a dopant therethrough and having a deposited thickness of less than about 30 angstroms.
10. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:
- a gate dielectric layer overlying a substrate;
 - a diffusion barrier layer on the gate dielectric layer, consisting essentially of a nitridized silicon layer having a deposited thickness of less than about 30 angstroms; and
 - a doped polysilicon layer overlying the diffusion barrier layer; and
- the diffusion barrier layer effective to inhibit diffusion of dopant therethrough to the gate dielectric layer.
11. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:
- a gate dielectric layer overlying a substrate;
 - a diffusion barrier layer overlying the gate dielectric layer and consisting essentially of a nitridized silicon layer having a deposited thickness of less than about 30 angstroms; and
 - a conductive metal layer overlying the diffusion barrier layer.

12. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:

- a gate dielectric layer overlying a substrate; and
- a diffusion barrier layer overlying the gate dielectric layer and having a deposited thickness of less than about 30 angstroms, the diffusion barrier layer comprising a nitrogen annealed silicon layer; and
- a doped polysilicon layer overlying the diffusion barrier layer; the diffusion barrier layer effective to inhibit diffusion of dopant therethrough from the polysilicon layer to the gate dielectric layer.

13. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:

- a gate dielectric layer overlying a substrate; and
- a diffusion barrier layer overlying the gate dielectric layer and having a deposited thickness of less than about 30 angstroms, the diffusion barrier layer consisting essentially of chemical vapor deposited and nitridized silicon; and
- a doped polysilicon layer overlying the diffusion barrier layer; the diffusion barrier layer effective to inhibit diffusion of dopant therethrough from the polysilicon layer to the gate dielectric layer.

14. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:

- a gate dielectric layer overlying a substrate;
- a diffusion barrier layer overlying and in contact with the gate dielectric layer, and consisting essentially of a silicon layer deposited to a thickness of less than about 30 angstroms and nitridized by exposure to a nitrogen gas;
- a doped polysilicon layer overlying the diffusion barrier layer;
- a metal silicide layer overlying the polysilicon layer;
- a conductive metal layer overlying the metal silicide layer; and
- an insulative layer over the conductive metal layer;
- the diffusion barrier layer effective to inhibit diffusion of dopant therethrough from the polysilicon layer to the gate dielectric layer.

15. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:

- a gate dielectric layer overlying a substrate;
- a diffusion barrier layer comprising nitridized silicon over the gate dielectric layer, and having a deposited thickness of less than about 30 angstroms;
- a doped polysilicon layer overlying the diffusion barrier layer;
- a metal silicide layer overlying the polysilicon layer; and
- an insulative layer over the metal silicide layer;

the diffusion barrier layer effective to inhibit diffusion of dopant therethrough from the polysilicon layer to the gate dielectric layer.

16. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:

- a gate dielectric layer overlying a substrate;
 - a diffusion barrier layer comprising nitridized silicon over the gate dielectric layer, and having a deposited thickness of less than about 30 angstroms;
 - a doped polysilicon layer overlying the diffusion barrier layer;
 - a metal oxide layer overlying the polysilicon layer;
 - a conductive metal layer overlying the metal oxide layer; and
 - an insulative layer overlying the conductive metal layer;
- wherein the diffusion barrier layer inhibits passage of dopant from the polysilicon layer to the gate dielectric layer.

17. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:

- a gate dielectric layer overlying a substrate;
- a diffusion barrier layer comprising nitridized silicon over the gate dielectric layer, and having a deposited thickness of less than about 30 angstroms;

a doped polysilicon layer overlying the diffusion barrier layer; and

an insulative layer over the doped polysilicon layer;

wherein the diffusion barrier layer inhibits passage of dopant from the polysilicon layer to the gate dielectric layer.

18. An integrated circuit, comprising a transistor comprising a gate stack situated adjacent source/drain regions in a substrate, the gate stack comprising:

- a gate dielectric layer overlying a substrate;
- a diffusion barrier layer overlying and in contact with the gate dielectric layer, the diffusion barrier layer having a deposited thickness of less than about 30 angstroms and comprising a nitrogen annealed silicon layer;
- a doped polysilicon layer overlying the diffusion barrier layer;
- a metal nitride layer overlying the doped polysilicon layer;
- a conductive metal layer over the metal nitride layer; and
- a nitride layer overlying the conductive metal layer;

wherein the diffusion barrier layer inhibits passage of dopant from the polysilicon layer to the gate dielectric layer.

* * * * *