



(51) International Patent Classification:
G09G 3/32 (2006.01)

(21) International Application Number:
PCT/GB2009/000866

(22) International Filing Date:
31 March 2009 (31.03.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0808178.8 7 May 2008 (07.05.2008) GB

(71) Applicant (for all designated States except US): **CAMBRIDGE DISPLAY TECHNOLOGY LIMITED** [GB/GB]; Building 2020, Cambourne Business Park, Cambridgeshire CB23 6DW (GB).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SMITH, Euan** [GB/GB]; IP Department, Cambridge Display Technology Ltd, Building 2020, Cambourne Business Park, Cambourne, Cambridgeshire CB23 6DW (GB). **THOMPSON, Barry** [US/US]; 874 Partridge Ave. Menlo Park, CA 94025. USA, Mento Park, California 94025 (US).

(74) Agent: **KAY, Christopher**; IP Department, CAMBRIDGE DISPLAY TECHNOLOGY LTD, Building 2020 Cam-

bourne Business Park, Cambridgeshire Cambridgeshire CB23 6DW (GB).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: ACTIVE MATRIX DISPLAYS

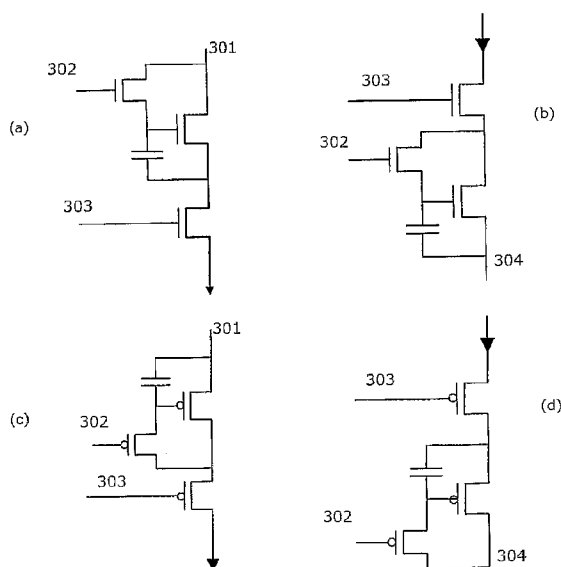


Figure 4

(57) Abstract: An active matrix OLED display (200) comprising a data line (202), a plurality of pixel circuits (203) connected to the data line (202), a drive circuit (201) connected towards one end of the data line (202) for writing display data to the pixel circuits (203), and a programmable drive boost circuit (204) connected towards another end of the data line (202) from the drive circuit (201).

ACTIVE MATRIX DISPLAYS

This invention generally relates to active matrix displays and to related display driving methods. More particularly the invention relates to additional driving circuitry for active matrix driven Organic Light Emitting Diode (OLED) displays employed to improve the performance characteristics of the device.

Displays fabricated using OLEDs provide a number of advantages over LCD and other flat panel technologies. They are bright, colourful, fast-switching (compared to LCDs), provide a wide viewing angle and are easy and cheap to fabricate on a variety of substrates. Organic (which here includes organometallic) LEDs may be fabricated using materials including polymers, small molecules and dendrimers, in a range of colours which depend upon the materials employed. Examples of polymer-based organic LEDs are described in WO 90/13148, WO 95/06400 and WO 99/48160; examples of dendrimer-based materials are described in WO 99/21935 and WO 02/067343; and examples of so called small molecule based devices are described in US 4,539,507.

A typical OLED device comprises two layers of organic material, one of which is a layer of light emitting material such as a light emitting polymer (LEP), oligomer or a light emitting low molecular weight material, and the other of which is a layer of a hole transporting material such as a polythiophene derivative or a polyaniline derivative.

Organic LEDs may be deposited on a substrate in a matrix of pixels to form a single or multi-colour pixellated display. A multicoloured display may be constructed using groups of red, green, and blue emitting pixels. So-called active matrix (AM) displays have a memory element, typically a storage capacitor and a transistor, associated with each pixel whilst passive matrix displays have no such memory element and instead are repetitively scanned to give the impression of a steady image. Examples of polymer and small-

molecule active matrix display drivers can be found in WO 99/42983 and EP 0,717,446A respectively.

A display may be either bottom-emitting or top-emitting. In a bottom-emitting display light is emitted through the substrate on which the active matrix circuitry is fabricated; in a top-emitting display light is emitted towards a front face of the display without having to pass through a layer of the display in which the active matrix circuitry is fabricated.

Top-emitting OLED displays are less common than bottom-emitting displays because, typically, the upper electrode comprises the cathode and this must be at least partially transparent, as well as having sufficient conductivity and, preferably, providing a degree of encapsulation of the underlying organic layers. Nonetheless a large variety of top-emitting structures has been described, including in the applicant's published PCT application WO 2005/071771 (hereby incorporated by reference in its entirety) which describes a cathode incorporating an optical interference structure to enhance the amount of light escaping from the OLED pixel.

An OLED display conventionally displays an image built from a rectilinear matrix of picture elements (or pixels). An Active Matrix OLED display conventionally has a row data line and a column data line for each colour of each pixel. One such data line 102 is shown in Figure 1. Referring to Figure 1, a drive circuit 101 is connected to the data line 102 which is connected to a plurality of pixel circuits 103. Each pixel circuit 103 corresponds to one pixel display element and contains a memory element (not shown). Each data line 102 will typically be connected to many hundred pixel circuits 103.

Within an active matrix OLED display, the data lines 102 utilise either a voltage driving method or a current driving method. The present state of the art enjoys increases in electrical efficiency when using current driving methods over voltage driving methods. Where the current driving method is used, the pixel circuits 103 may be used as either a current source or a current sink.

Figure 2, which is taken from our application WO 03/038790, shows an example of a current-controlled pixel driver circuit. In this circuit the current through an OLED 152 is set by setting a drain source current for OLED driver transistor 158 using a reference current sink 166 and memorising the driver transistor gate voltage required for this drain-source current. Thus the brightness of OLED 152 is determined by the current, I_{col} , flowing into reference current sink 166, which is preferably adjustable and set as desired for the pixel being addressed. In addition, a further switching transistor 164 is connected between drive transistor 158 and OLED 152. In general one current sink 166 is provided for each column data line.

A problem shared by current driven active matrix pixel circuits is that where, as is often the case, the pixel "programming" currents are small leakage and/or data line capacitance may dominate, particularly in large displays.

As best seen in Figure 1, conventional current-driven active matrix OLED displays must overcome the resistor-capacitor constant of the data line 102. The drive circuit 101 must overcome the inherent resistance and capacitance of the data line 102 in addition to supplying sufficient current to the pixel circuits 103 to achieve the desired light output.

According to a first aspect of the present invention, there is provided an active matrix OLED display comprising a data line, a plurality of pixel circuits connected to the data line, a drive circuit connected towards one end of the data line for writing display data to the pixel circuits, and a programmable drive boost circuit connected towards another end of the data line from the drive circuit.

The invention preferably provides a programmable drive boost circuit connected to the data line at an opposite end to which the drive circuit is connected. The addition of such a circuit enables a more rapid pre-charging of the active matrix OLED data line. As will be appreciated by a person skilled in the art, the programmable drive boost circuit can be a voltage controlled circuit or a current controlled circuit.

Preferably, the programmable drive boost circuit is a current source or current sink. Using the programmable drive boost circuit as a current source or current sink reduces the current required to overcome the resistor-capacitor coefficient of the data line. The benefits of the present invention include increased device power efficiency and lower time to display an image and consequential higher image display refresh rates.

Preferably, the programmable drive boost circuit comprises a select or enable circuit. More preferably, the drive circuit is connected to the enable circuit by a data bus. This allows the drive circuit to control the programmable drive boost circuit by transmitting an enable data bit and/or one or more program data bits.

Preferably, the programmable drive boost circuit is a current copier. Optionally, the current copier can be controlled as a variable current sink with a duty programmed enable signal or by a most significant bit of a programmed data signal or the copier can be enabled for a fixed period of time.

The programmable drive boost circuit can be n-channel or a p-channel depending upon circuit design requirements.

Preferably, the programmable drive boost circuit and the drive circuit are located on the same substrate. A suitable substrate or backplane can be one fabricated from amorphous silicon (a-Si).

According to a second aspect of the present invention, there is provided a method of programming an active matrix OLED display, the OLED display having a current programmed data line, a plurality of pixel circuits connected to the data line, a drive circuit connected towards one end of the data line to write display data to the pixel circuits, and a programmable drive boost circuit connected towards another end of the data line from the drive circuit; the method comprising a first addressing period including programming the programmable drive boost circuit with a first current; and a second addressing period including writing display data to the pixels and supplying the first current to the data line.

In this way, a current is programmed onto the data line by the programmable booster circuit. This method substantially reduces the charge time and charging the data line from both ends reduces the resistor-capacitor constant by around 75%.

Preferably, the method of programming comprises, in the first addressing period activating the programmable drive boost circuit with an enable data bit and one or more program data bits to provide a current biased with respect to the current provided to the data line from the drive circuit.

Preferably, the first addressing period comprises the programmable drive boost circuit being enabled for a fixed time period. Such an arrangement provides the benefits of the programmable booster circuit while avoiding the inefficiency of continuous use of the programmable booster circuit.

Preferably, the first addressing period comprises the programmable drive boost circuit being enabled and providing a current corresponding to the most significant bit of the digital signal information transmitted by the driver circuit. In such an arrangement, the maximum current provided by the programmable booster circuit and the drive circuits is reduced.

Preferably also, the first addressing period comprises the programmable booster circuit being programmed to vary according to a duty cycle. In such an arrangement the duty cycle may be selected, for example to overcome physical impurities in the material of the data line, to achieve an optimal display time or electrical efficiency, for example dependant upon the information content of the image to be displayed, or to follow a fixed duty cycle, for example to minimise the numerical calculations required to achieve the desired image display.

Embodiments of the present invention will now be further described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a schematic diagram of a row or column display layout as is known in the art;

Figure 2 is a schematic diagram of an active matrix pixel driver circuit as is known in the art;

Figure 3 is a schematic diagram of a row or column display layout according to an embodiment of the present invention; and

Figures 4a to 4d are schematic diagrams of four sample circuits for use as a programmable circuit booster circuit according to an embodiment of the present invention.

Referring to Figure 3, a schematic diagram of a row or column display layout according to an embodiment of the present invention comprises an active matrix OLED display 200. The display 200 comprises a programmable booster circuit, showing drive chip circuit 201, data line 202, pixel circuits 203 and programmable drive boost circuit 204.

The programming of the display 200 has two stages due to the active matrix arrangement of the pixel circuits 203. In a first stage, drive circuit 201 identifies from the digital signal information the required current or range of current to be supplied to the pixel circuits 203 and supplies current to a plurality of pixel circuits 203 which store current in memory cells (not shown). Additionally, programmable booster circuit 204 is engaged during this first stage of programming. In a second stage, the drive circuit 201 ceases to supply current and the pixel circuits 203 drive an OLED (not shown) within the pixel circuit to illuminate a portion of the intended display image corresponding to the digital signal data supplied. In this arrangement, the drive circuit 201 is assisted by the programmable drive boost circuit 204 in the task of supplying current to charge the memory cells of the pixel circuits 203 and also to supply enough current to overcome the resistor-capacitor constant of the data line 202.

The programmable drive boost circuit 204 can function as a current copier in cooperation with the drive circuit 201 wherein both circuits 201, 204 source or sink current to the pixel circuits 203. Alternatively, the programmable booster circuit 204 may function in opposition to the drive circuit 201, wherein the programmable booster circuit 204 sinks current while the drive circuit 201 sources current or the programmable booster circuit 204 sources current while the drive circuit 201 sinks current.

The programmable booster circuit 204 can be enabled only during a pre-charge portion of the first stage of programming the display 200. Additionally, the programmable drive boost circuit 204 can be programmed to a level of current associated with the most significant bit of the digital signal information against which fixed level the drive circuit 201 programs the pixel circuits 203 during a first stage of programming the display 200. Additionally, the programmable drive boost circuit 204 can be programmed to follow a variable duty program, for example to optimise the current delivered according to the content of the intended display image.

Figures 4a to 4d are schematic diagrams of four sample circuits for use as a programmable circuit booster circuit 204 according to an embodiment of the present invention. Common in parts (a), (b), (c) and (d) of Figure 4 are voltage source V_{DD} 301, program data 302, enable data 303 and circuit ground 304.

Figure 4(a) shows a typical layout for an example programmable booster circuit 204 using n-type transistors to provide a current source programmable booster circuit.

Figure 4(b) shows a typical layout for an example programmable booster circuit 204 using n-type transistors to provide a current sink programmable booster circuit.

Figure 4(c) shows a typical layout for an example programmable booster circuit 204 using p-type transistors to provide a current source programmable booster circuit.

Figure 4(d) shows a typical layout for an example programmable booster circuit using p-type transistors to provide a current sink programmable booster circuit.

No doubt other effective alternative will occur to the skilled person. It will be understood that the invention is not limited to the described embodiments and encompasses modifications apparent to those skilled in the art lying within the spirit and scope of the claims appended hereto.

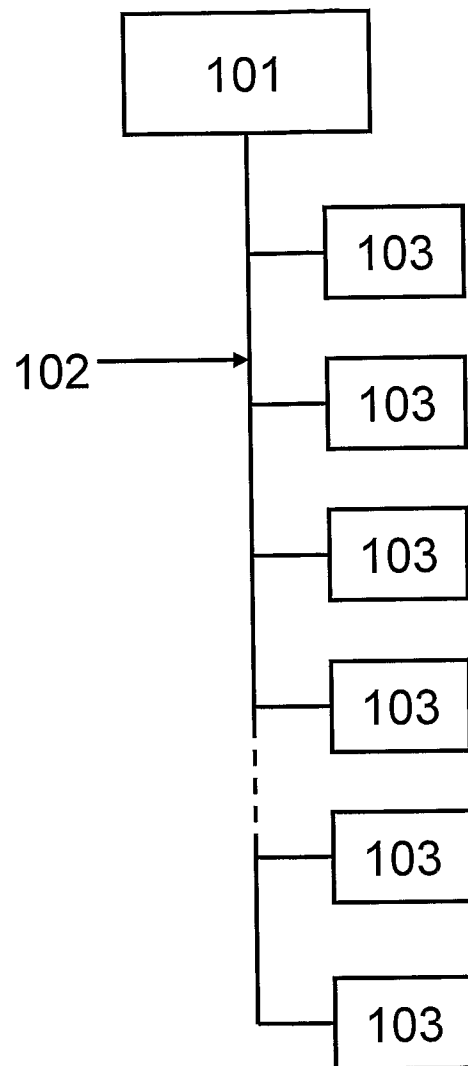
Claims

1. An active matrix OLED display comprising a data line, a plurality of pixel circuits connected to the data line, a drive circuit connected towards one end of the data line for writing display data to the pixel circuits, and a programmable drive boost circuit connected towards another end of the data line from the drive circuit.
2. An active matrix OLED display as claimed in claim 1, wherein the programmable drive boost circuit is connected to the data line at an opposite end to which the drive circuit is connected.
3. An active matrix OLED display, wherein the programmable drive boost circuit is a current source or current sink.
4. An active matrix OLED display, wherein the programmable drive boost circuit comprises a select or enable circuit.
5. An active matrix OLED display as claimed in claim 4, wherein the drive circuit is connected to the enable circuit by a data bus.
6. An active matrix OLED display as claimed in any preceding claim, wherein the programmable drive boost circuit is a current copier.
7. An active matrix OLED display as claimed in claim 6, wherein the current copier is controllable as a variable current sink with a duty programmed enable signal.
8. An active matrix OLED display as claimed in claim 6, wherein the current copier is controllable by a most significant bit of a programmed data signal.

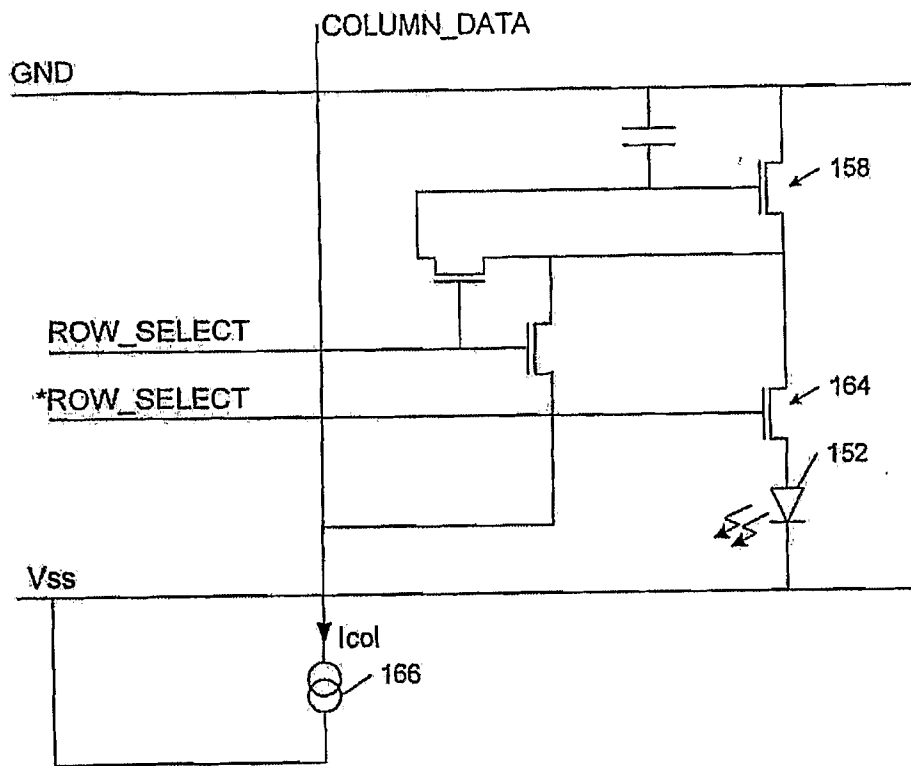
9. An active matrix OLED display as claimed in any preceding claim, wherein the programmable drive boost circuit and the drive circuit are located on the same substrate.
10. An active matrix OLED display as claimed in claim 9, wherein the substrate comprises an amorphous silicon (a-Si) backplane.
11. An active matrix OLED display as claimed in claim 1, wherein the programmable drive boost circuit is a programmable current boost circuit.
12. An active matrix OLED display as claimed in claim 1, wherein the programmable drive boost circuit is a programmable voltage boost circuit.
13. A method of programming an active matrix OLED display, the OLED display having a current programmed data line, a plurality of pixel circuits connected to the data line, a driver circuit connected towards one end of the data line to write display data to the pixels, and a programmable drive boost circuit connected towards another end of the data line from the driver circuit; the method comprising a first addressing period including programming the programmable drive boost circuit with a first current; and a second addressing period including writing display data to the pixels and supplying the first current to the data line.
14. A method as claimed in claim 13, including activating the programmable drive boost circuit with an enable data bit and one or more program data bits to provide a current biased with respect to the current provided to the data line from the driver circuit.
15. A method as claimed in claim 14, including the programmable drive boost circuit being enabled for a fixed time period.
16. A method as claimed in claim 14, including the programmable drive boost circuit being enabled and providing a current corresponding to the

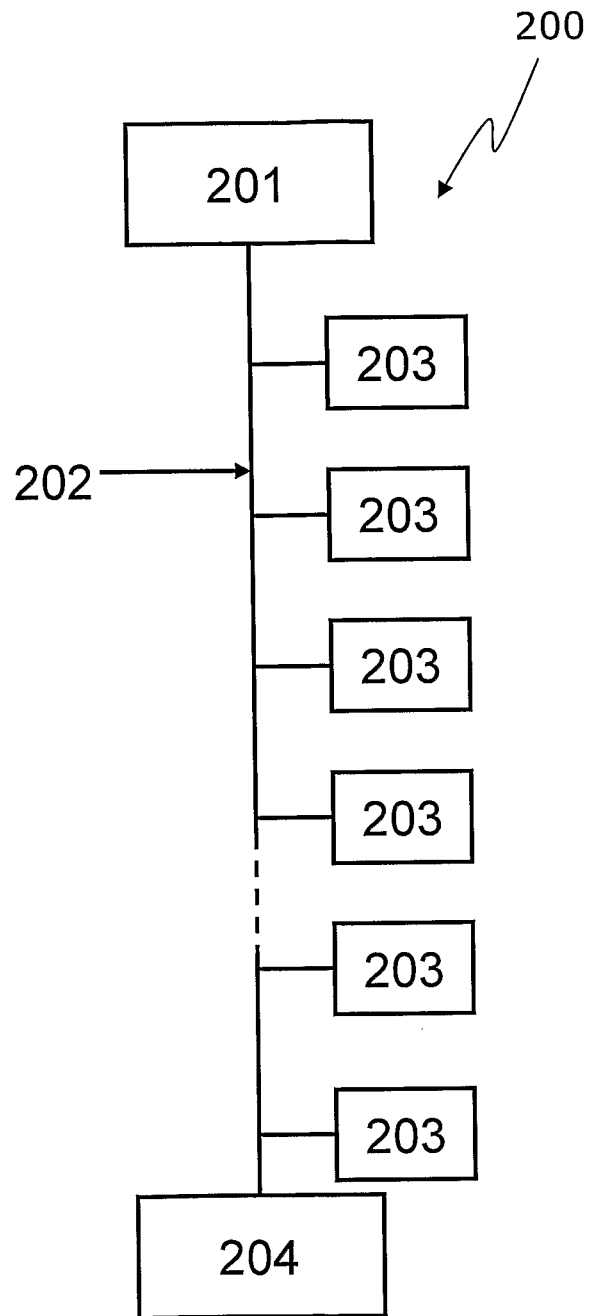
most significant bit of the digital signal information transmitted by the driver circuit.

17. A method as claimed in claim 14, including the programmable booster circuit being programmed to vary according to a duty cycle.
18. A method as claimed in any one of claims 13 to 17, wherein the display comprises a flat panel display.
19. A method as claimed in any one of claims 13 to 18, wherein the display comprises a top-emitting active matrix OLED display.
20. A method of programming an active matrix OLED display substantially as hereinbefore described and/or with reference to figures 2, 3 and 4 of the accompanying drawings.
21. An active matrix OLED display comprising a programmable drive boost circuit substantially as hereinbefore described and/or with reference to figures 2, 3 and 4 of the accompanying drawings.

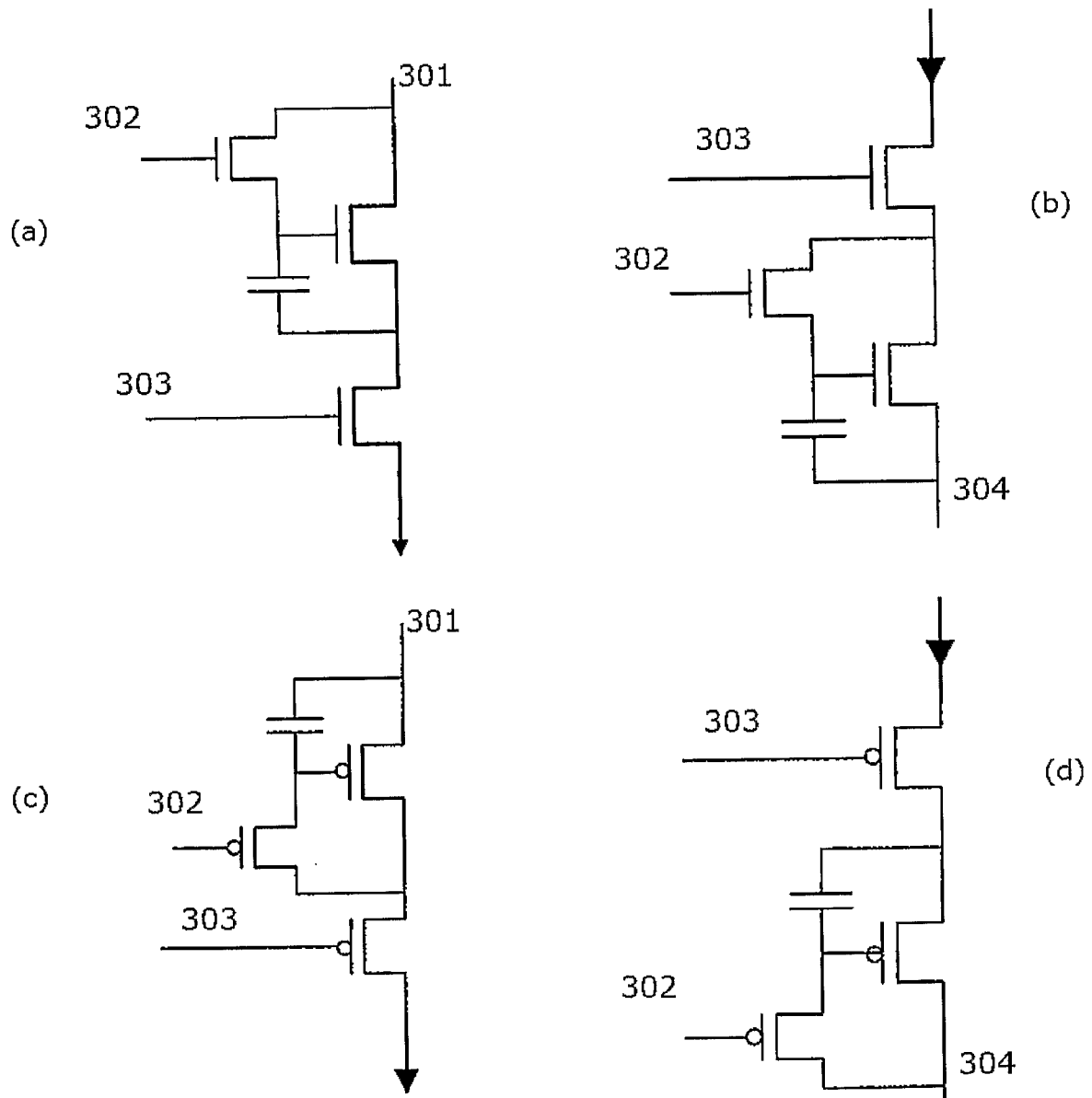
1/4**Figure 1**

2/4

**Figure 2**

3/4**Figure 3**

4/4

**Figure 4**

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2009/000866

A. CLASSIFICATION OF SUBJECT MATTER

INV. G09G3/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/195964 A1 (YUMOTO AKIRA [JP]) 26 December 2002 (2002-12-26) paragraphs [0001], [0012], [0029], [0038] - [0126]; figures 8, 10-16, 22 -----	1-6, 8, 10-14, 16, 18, 19
X	EP 1 624 436 A (TOSHIBA MATSUSHITA DISPLAY TEC [JP]) 8 February 2006 (2006-02-08) paragraphs [0011] - [0080]; figures 15-21 -----	1-3, 9, 11, 13, 18
X	WO 2006/020468 A (EASTMAN KODAK CO [US]; KAWABE KAZUYOSHI [JP]) 23 February 2006 (2006-02-23) page 18, line 4 - page 21, line 11; figures 6-211 -----	1-3, 6-8, 10-12, 15-19

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *Z* document member of the same patent family

Date of the actual completion of the international search

7 July 2009

Date of mailing of the international search report

17/07/2009

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Gartlan, Michael

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2009/000866

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 2002195964	A1	26-12-2002	CN 1388498 A	01-01-2003
			JP 3610923 B2	19-01-2005
			JP 2002351400 A	06-12-2002
			KR 20020092220 A	11-12-2002
			SG 104968 A1	30-07-2004
			TW 544652 B	01-08-2003
EP 1624436	A	08-02-2006	WO 2004102515 A1	25-11-2004
			KR 20060023528 A	14-03-2006
			TW 285355 B	11-08-2007
			US 2006066536 A1	30-03-2006
WO 2006020468	A	23-02-2006	EP 1776690 A1	25-04-2007
			JP 2006053347 A	23-02-2006