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Tarczy-Hornoch

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[54] **DIGITAL GRAPHIC DISPLAY APPARATUS, SYSTEM AND METHOD**

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[52] **U.S. Cl.**.....**340/324 A,** 178/DIG. 3, 235/198

[51] **Int. Cl.**.....**G06f 3/14**

[58] **Field of Search**.....340/324 A; 235/151, 235/197, 198; 178/DIG. 3

[56] **References Cited**

UNITED STATES PATENTS

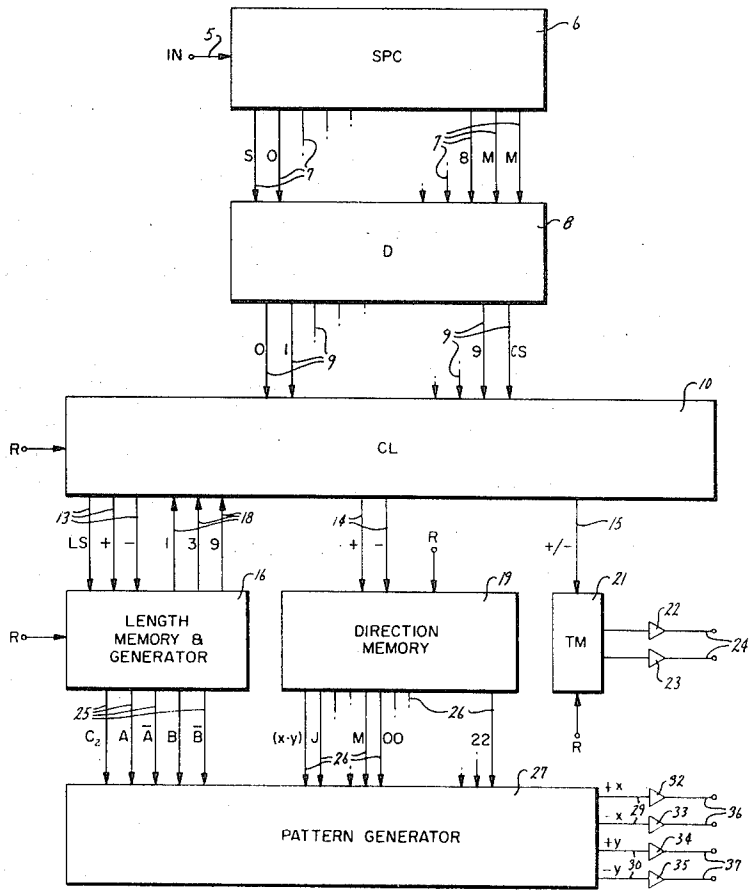
3,569,951	3/1971	Lavenir et al.	340/324 A
3,459,926	8/1969	Heilweil et al.	340/324 A
3,576,574	4/1971	Baskin	340/324 A
3,471,847	10/1969	McCollough et al.	340/324 A
3,329,948	7/1967	Halsted	340/324 A
3,543,240	11/1970	Miller et al.	340/324 A
3,333,147	7/1967	Henderson	340/324 A
2,766,444	10/1956	Sheftelman	340/324 A
3,533,096	10/1970	Bouchard	340/324 A
3,514,616	5/1970	Kolb	340/324 A
2,875,951	3/1959	Schreiner	340/324 A
3,430,207	2/1969	Davis	340/324 A

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[57] **ABSTRACT**

Apparatus, system and method is provided for operating graphic display devices at high speed while receiving digitally coded data at a low input rate. The display is synthesized from line segments of predetermined lengths and finely quantized directions, generated by a pattern generator. Straight lines in any direction and a variety of curves can be displayed at or near the maximum speed of the display device, such as a plotter. The dominant input information consists of incremental update instructions for the length and direction parameters memorized by respective memory means, and the updated parameters are utilized by the pattern generator for generating subsequent line segments.

27 Claims, 11 Drawing Figures



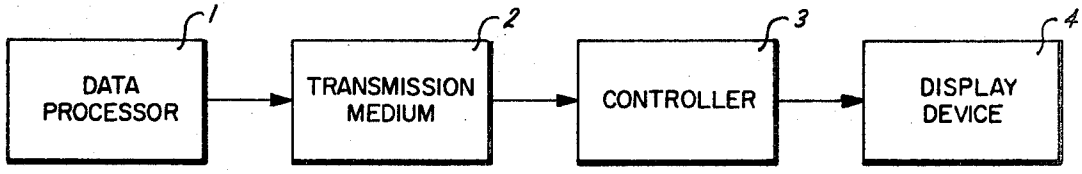


Fig. 1

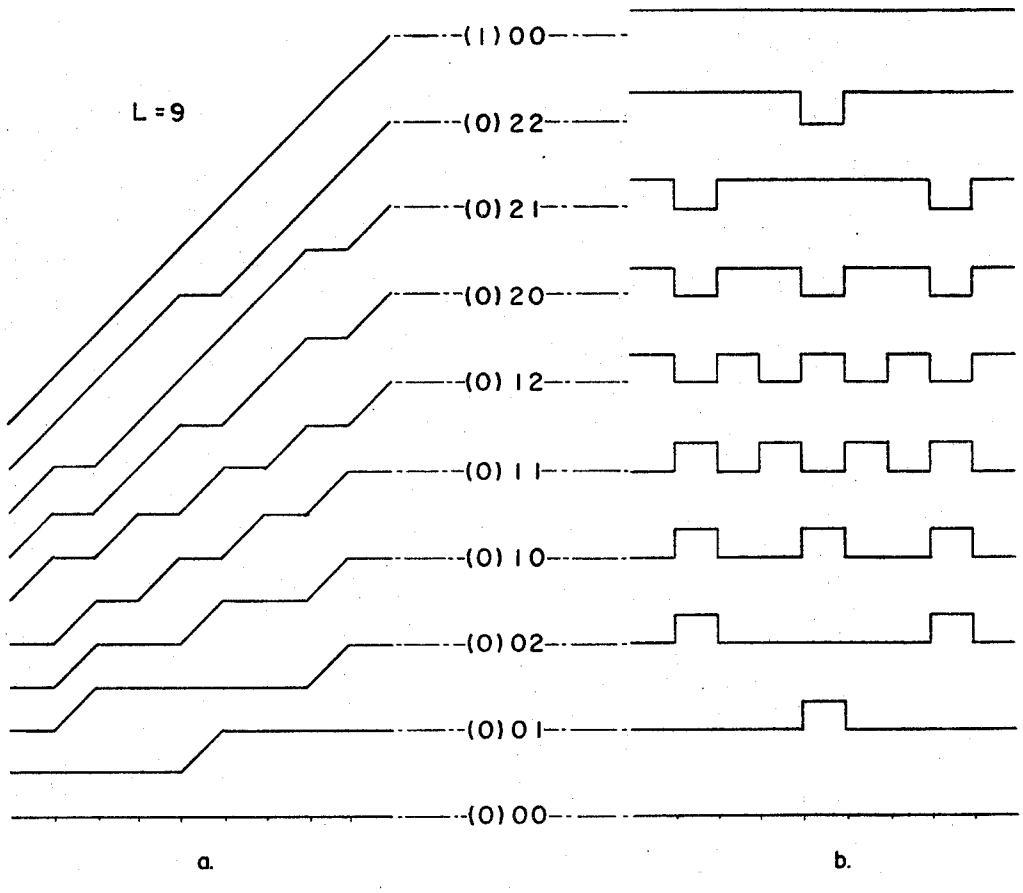
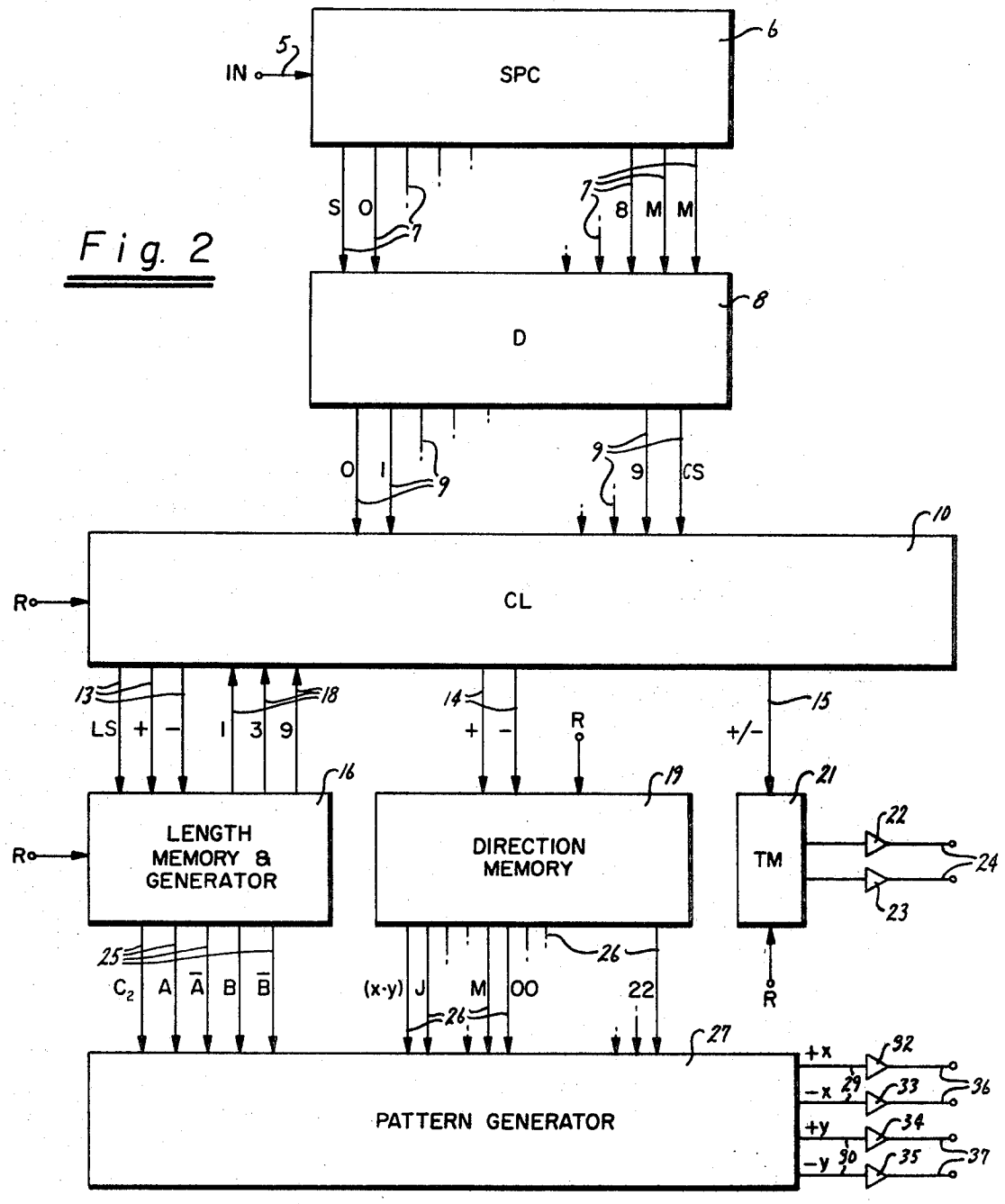


Fig. 5

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Fig. 2



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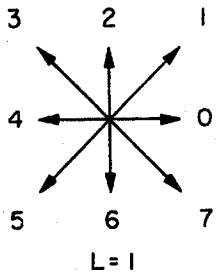


Fig. 3

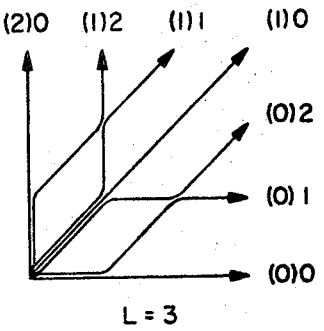


Fig. 4

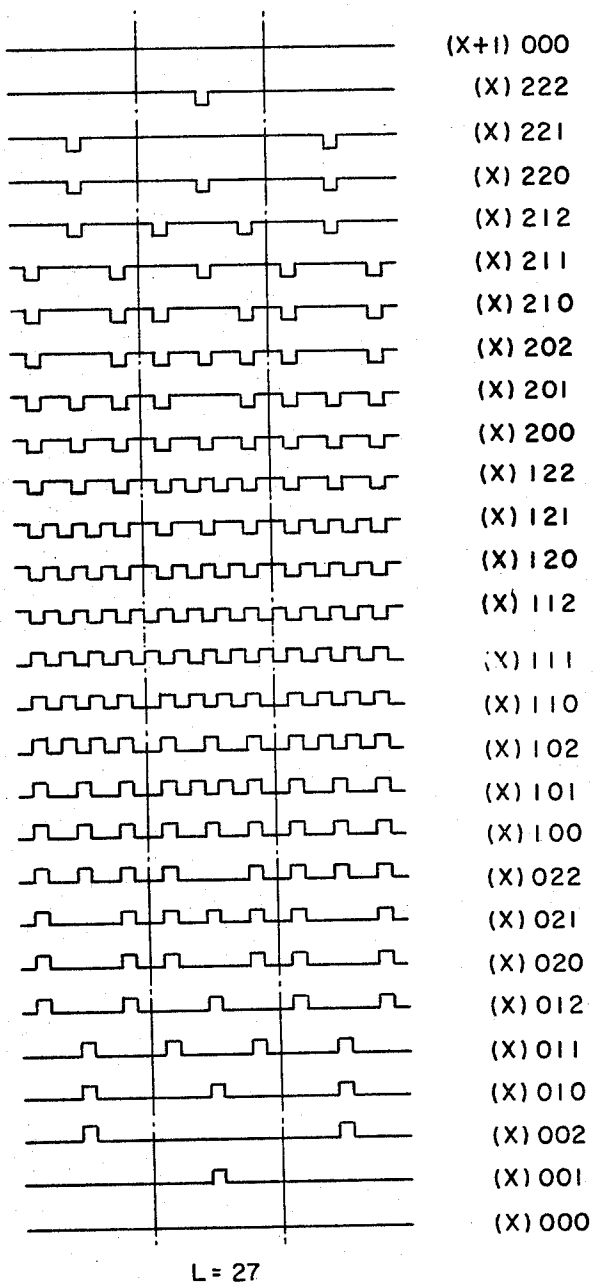


Fig. 6

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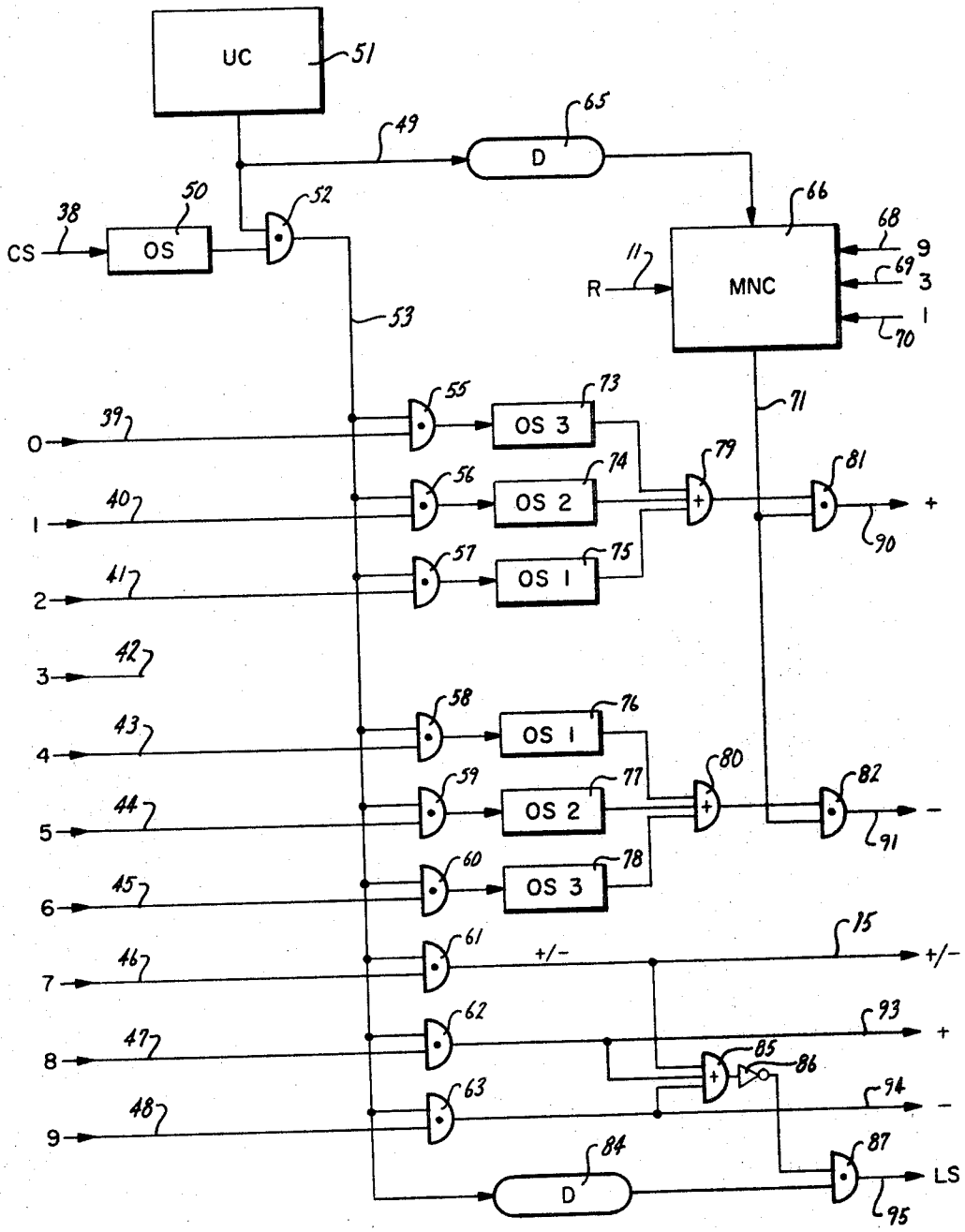


Fig. 7

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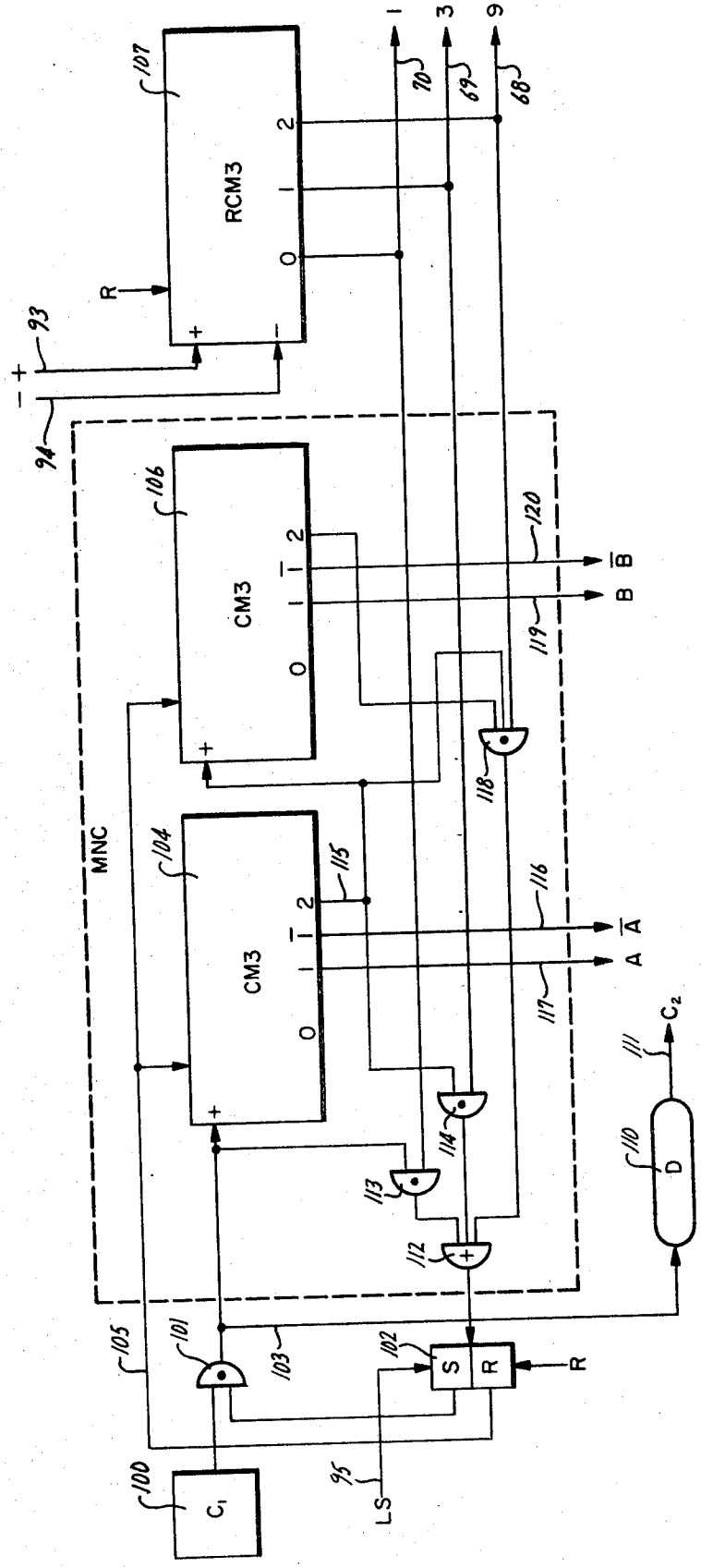


Fig. 8

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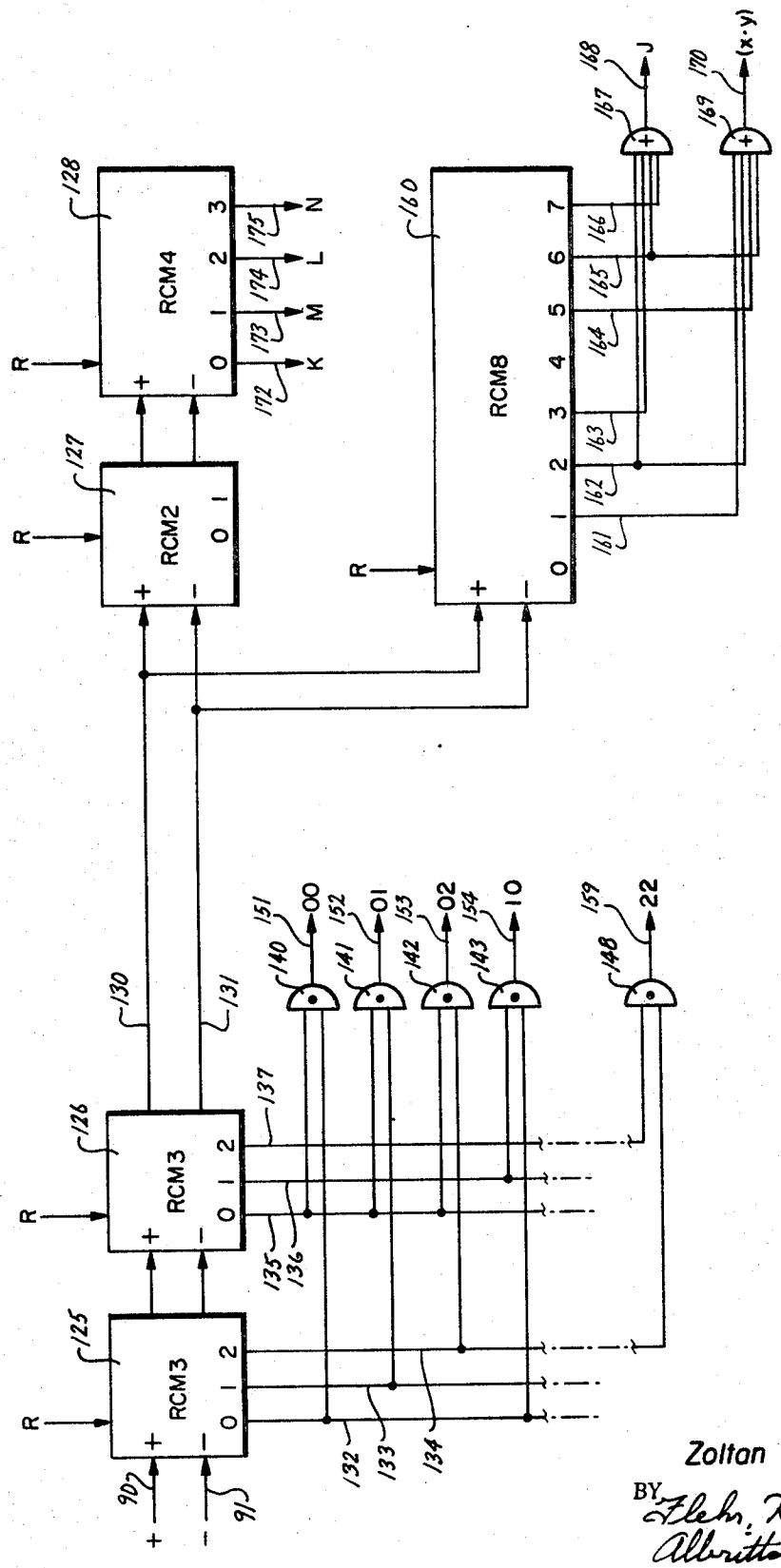


Fig. 9

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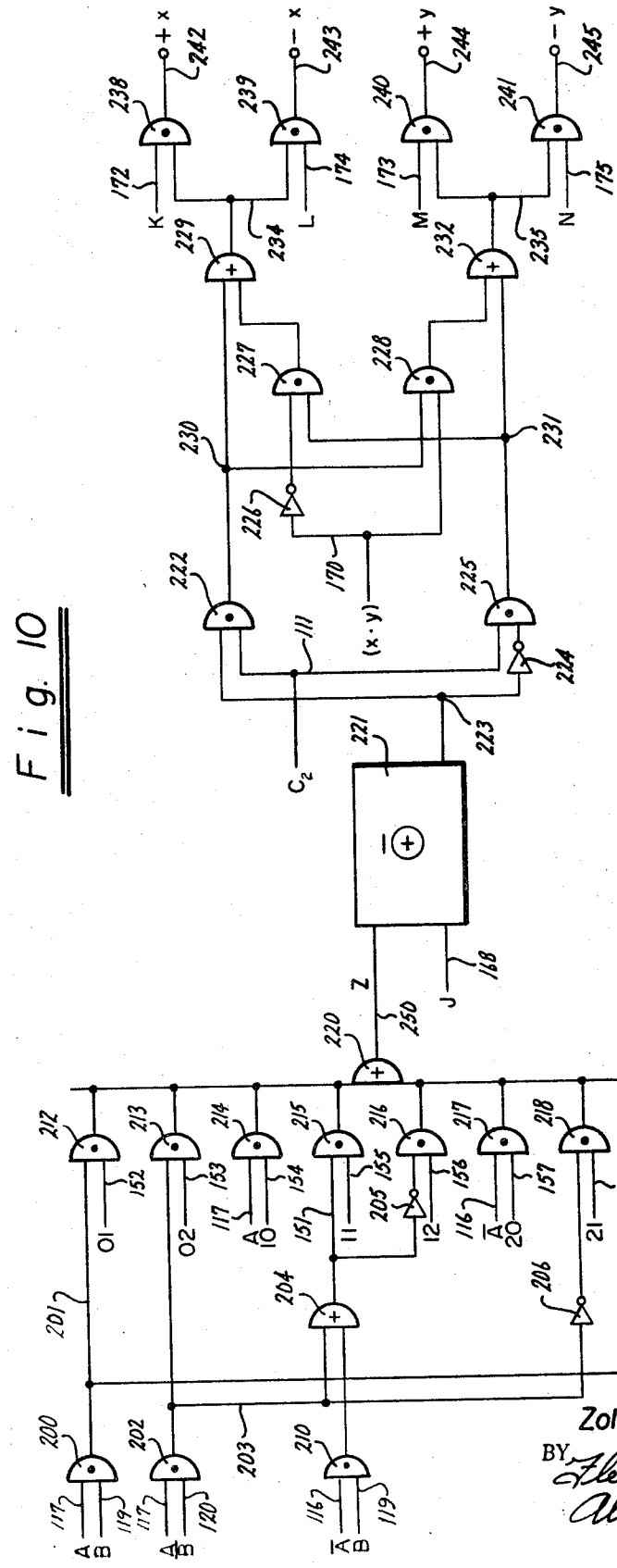


Fig. 10

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DIGITAL GRAPHIC DISPLAY APPARATUS, SYSTEM AND METHOD

BACKGROUND OF THE INVENTION

Remote operation of graphic display devices such as plotters or cathode ray tube devices (CRT) operated from a digital computer through narrow bandwidth transmission lines is well known to those skilled in the state of the art. The speed of operation of such systems is usually limited by the data carrying capacity of the transmission line utilized. Various methods have been employed to overcome such limitations of the transmission medium. This particular problem and one solution to the problem is described in U.S. Pat. No. 3,434,113. As described therein, transmitted in each eight bit American Standard Code for Information Interchange (ASCII) character there are three bits of direction and five bits of length determining information. For the eight possible straight line segments in horizontal, vertical and diagonal directions, this is an adequate solution and permits the operation of a graphic display device such as a plotter near its maximum stepping rate. When it is desired to plot lines of arbitrary directions or curved lines, this coding forces the plotting speed to be seriously reduced. The limitations are even more pronounced when inherently high speed devices such as CRTs are utilized. The cited prior art plotter can generate line segments in D possible directions where $D = 8$, regardless of the length of the line segment or the number of increments, L, required to display the line segment. Therefore in order to display long lines in directions other than the eight directions available, multiple commands must be transmitted to generate multiple short line segments which, in combination, equal the long line desired. This limitation in the number of directions per command causes undue use of graphic display system time in a large number of applications. With the coding utilized in U.S. Pat. No. 3,434,113, the bit capacity of an ASCII character is exhausted, even for limited directional resolution and thus such coding does not permit redundant coding for error checking or correction. There is, therefore, a need for an improved graphic display apparatus, system and method which overcomes the above named limitations and which is capable of operating remote graphic display devices through a narrow bandwidth transmission medium in such a manner that straight lines of arbitrary direction or a variety of curves can be displayed at or near the maximum speed of operation of the graphic display device. The present invention removes the above described limitation of the prior art by allowing $D = 8 \times L$, so that long line segments of arbitrary direction can be displayed without requiring multiple commands, thus increasing the effective speed of the graphic display device.

SUMMARY OF THE INVENTION AND OBJECTS

The graphic display system consists of display means capable of displaying graphic patterns consisting of line segments characterized by at least two parameters including length and direction and a controller for controlling the display means. The controller has input means for receiving input information in the form of digitally encoded signals. Memory means is provided in the controller for memorizing at least one of the parameters of at least one line segment previously displayed by the display means. Control logic means is connected to the input means and the memory means for recognizing if the digitally encoded signal contains a change instruction for the parameter which has been memorized. The means for recognizing the digitally encoded signal includes means for updating the memorized parameter in accordance with any change instruction. Pattern generating means is provided which is connected to the memory means and utilizes the updated memorized parameter in the generation of signals representing one or more subsequent line segments for the display means.

In general, it is an object of the present invention to provide a graphic display apparatus, system and method capable of high display speed while receiving digitally coded data at a low input rate.

Another object of the invention is to provide a system, apparatus and method of the above nature which can be more effectively utilized in connection with a relatively narrow bandwidth transmission medium.

Another object of the invention is to provide an apparatus, system and method of the above nature which makes it possible to plot in response to a single command a vector of quantized length with complete directional resolution within the resolution of the graphic display device.

Another object of the invention is to provide a system, apparatus and method of the above nature which is capable of displaying straight lines of arbitrary direction or a variety of curves at or near the maximum display speed of display devices such as plotters.

Another object of the invention is to provide a system, apparatus and method of the above nature in which a compressed data transmission code is utilized which requires fewer bits for the transmission of additional information, and thereby could permit, for example, code redundancy for error checking and correction or the coding of two independent line segment instructions within a single character of transmission.

Another object of the invention is to provide a system, apparatus and method of the above nature in which only incremental length change and direction change information is transmitted rather than absolute values of length and direction.

Another object of the invention is to provide a system, apparatus and method of the above nature in which an odd number base number system is utilized.

Another object of the invention is to provide an apparatus, system and method of the above nature in which the number system is a ternary number system.

Another object of the invention is to provide an apparatus, system and method of the above nature in which the length and direction parameters are memorized for use in generating subsequent line segment information.

Another object of the invention is to provide a system, apparatus and method of the above nature which is particularly useful with high speed graphic display devices.

Additional objects and features of the invention will appear from the following description in which the preferred embodiment is set forth in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a graphic display system which includes a controller incorporating the present invention;

FIG. 2 is a block diagram of the controller shown in FIG. 1;

FIG. 3 is a graph showing the eight possible line segments which can be displayed with the present invention with a length of one increment;

FIG. 4 is a graph showing the maximum number of possible line segments in one quadrant which can be displayed with the present invention with a length of three increments;

FIG. 5A is a graph showing the maximum possible number of line segments in one octant which can be displayed with the present invention with a length of nine increments;

FIG. 5B is a graph showing the signal patterns which are required out of the pattern generator within the controller for generating the line segments shown in FIG. 5A;

FIG. 6 is a graph showing the signal patterns required from the pattern generator to display 27 different line segments in one octant where the length is 27 increments;

FIG. 7 is a block diagram of the control logic shown in FIG. 2;

FIG. 8 is a block diagram of the length memory and generator shown in FIG. 2;

FIG. 9 is a block diagram of the direction memory shown in FIG. 2; and

FIG. 10 is a block diagram of the pattern generator shown in FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in FIG. 1, the graphic display system consists of the data processor or computer 1 which supplies information in the form of digital data over a transmission medium which generally may be a voice grade telephone line or other medium of limited bandwidth and which typically includes modulators and demodulators. The information is supplied to a controller 3 which converts the form of the data transmitted from the computer 1 into a form which is directly useful to the graphic display device 4. The controller alternatively can receive information from a conventional storage medium such as magnetic tape or punch cards. In addition, the input signals for the controller 3 can be generated by manually operated keyboard devices such as a Teletype terminal.

FIG. 2 is a block diagram of the controller 3 shown in FIG. 1. The controller is provided with an input terminal 5 which receives an electrical input signal that carries information in the form of ASCII characters. The electrical signal is supplied to a conventional serial to parallel converter 6 labeled SPC which converts the input signal into parallel form which is supplied as a plurality of parallel output lines 7. The lines 7 carry certain designations which represent an ASCII 11 bit code. It is well known to those skilled in the art that the ASCII code typically includes a start bit, eight information bits and one or two stop or marking bits. These are represented by the eleven lines 7 connected to the decoder 8. The information is supplied on the lines 7 in parallel binary form and is decoded by the conventional decoder 8 labeled D into a 1 of 10 code which is supplied on the lines 9 consisting of 10 separate lines and a clock start line.

The lines 9 which represent the output of the decoder 8 are supplied to a control logic block 10. The lines 9 which have been identified with the designations 0 to 9 contain update information about the line segment which is to be displayed. This information carried by the lines 9 is information relating to parameters which characterize the line segment, such as length, direction, and visibility of the trace. By way of example, one of the ten lines can carry the instruction to repeat the previously displayed line segment, another line can carry the instruction to change the state of the trace, two of the lines can be utilized to change the content of the length memory, and the remaining six lines of the ten can be used to update the memorized direction. In other words, the control logic 10 receives the decoded information and classifies whether received information specifies length, direction or trace updating and supplies the appropriate length, direction or trace memory update signals on signal lines 13, 14 and 15.

As shown in FIG. 2, lines 13 are connected to a length memory and generator 16. The three lines 13 are identified as length start line, and plus and minus lines which indicate, respectively, whether the memorized length is to be incremented or decremented. The lines 14 are connected to a direction memory 19. The two lines 14 carry instructions which indicate whether the memorized direction should be incremented or decremented. The line 15 is connected to a trace memory 21. This memory 21 may be a conventional flip-flop which is toggled by pulses received on the line 15.

The blocks 16, 19 and 21 are all memories and each has an initial state (Reset or 0 state) which can be established by the generation of a reset pulse which is applied to each block as indicated by the lines labeled R. For example, in the length memory and generator 16, the initial state can mean that the memorized length is the minimum value, such as one. In the direction memory 19, the initial state can represent the positive X direction. In the trace memory 21, the initial state can represent a "no-trace" or "pen-up" position whereas the other condition of the trace memory can represent a "visible-trace" or "pen-down" position. The trace memory 21 has two outputs which are supplied through two conventional buffer amplifiers 22 and 23 to two output terminals 24 which are to be connected to the ± trace input terminals of the display device utilized.

The length memory and generator 16 is provided with outputs which are supplied on lines 18 to the control logic 10. The basic function of the outputs on lines 18 is to control the quanta of incrementing or decrementing of the direction memory 19.

The length memory and generator 16 also has additional outputs which are supplied on lines 25 to a pattern generator 27. The direction memory 19 also has outputs supplied on lines 26 to the pattern generator 27.

The first line of lines 25 identified as C2 carries a number of clock pulses which corresponds to the number of increments in the line segment which is to be displayed in response to a pattern supplied by the pattern generator 27.

The pattern generator 27 is provided with two X outputs and two Y outputs identified as +X, −X, +Y and −Y, respectively, which are connected through conventional amplifiers 32, 33, 34 and 35 that are connected to two sets of outputs 36 and 37 which are to be connected to the graphic display device with which the controller is utilized.

Typically, if the graphic display device were a plotter, the terminals 36 can be connected to the input terminals of the graphic display device so that the signals supplied will control the movement of the chart and the output from the terminals 37 will be supplied to the graphic display device so that they will drive the pen carriage.

Although detailed operation of the entire system and the various blocks which form the controller in FIG. 2 will be described hereinafter, a brief description of the operation of the controller in FIG. 2 is as follows. For the purposes of the description, let it be assumed that the pattern generator 27 is capable of generating line segments of one, three or nine increments in length and eight, 24 or 72 different directions, respectively. By this it is meant that a line segment one increment in length can be generated in eight different directions, a line formed of three increments can be generated in 24 different directions and a line segment formed of nine increments can be generated in 72 different directions. To generate such line segments there must be supplied to the terminals 36 and 37 ±X and ±Y output signals in an appropriate sequence or pattern until the desired length is reached as controlled by the length memory and generator 16. The exact manner in which such patterns are generated and how they will appear when displayed will be discussed in detail hereinafter. In general, the direction of the line segment to be displayed is under the control of the direction memory 19. For example, the memory 19 could have a capacity of 72 sequential quantized directions for a length of nine increments.

As would be apparent to one skilled in the art, the capacity of the direction memory 19 must be compatible with the length of the line segment to be generated and the number of possible directions for the line segment. Lower length direction patterns may be generated by truncating the longest direction patterns as hereinafter described. The content of direction memory 19 is updated on the receipt of update information from the control logic 10. The updating as hereinbefore described is incremental in nature and the last memorized direction can be changed in sequence by ± I increments, where $I = A \times B$, where $A = 0, 1, 2,$ or 3 and $B = 1, 3,$ or 9.

The length memory and generator 16 memorizes the length of the line segment and generates a pulse train consisting of a number of pulses representing the number of increments required to make up the line segment, as well as the other control waveforms required. Updating of the information in length memory and generator 16 is also incremental as hereinbefore described. The incrementing or decrementing can increase or decrease the memorized length by factors of three.

After reset signal R is applied, a new display can be started. Length memory and generator 16 will be reset at length 1 and direction memory 19 will be reset at direction 0.

An assignment of ASCII numbers 0 to 9 to specific display commands could be as follows: 0, 1, 2, 3, 4, 5 and 6 mean update previous direction memorized by 3, 2, 1, 0, −1, −2 and −3 quanta, respectively, and generate a pattern in the new direction at the previously memorized length; 7 means change the state of the trace memory, 8 and 9 mean increase and decrease the memorized length by one quantum, respectively. Assuming that input 5 receives character 8, after conversion and decoding the control logic 10 will recognize it as a shift-up length command and will change the memorized length from 1 to 3. No display yet will take place. The following character is assumed to be 7, which after decoding will cause the trace memory 21 to display all subsequent line segments, until changed again, as a visible trace. The next character by way of example could be number 3. Neither length nor direction will be changed, and the control logic 10 will generate a length start command as hereinafter described. The length start command will cause length memory and generator 16 to generate three pulses on line C2 of lines 25. Direction memory 19 is still at the initial 0 state, meaning +X direction. The direction number assignment is hereinafter described. The pattern generator in response to signals 25 and 26, will generate three incremental advancing signals for the display device on line +X through buffer 32, generating the desired segment of the display line.

As a further example, the next input will be character 0. The direction memory will be updated by three quanta counterclockwise and a new line segment generated at the old length 3. As will be shown later, this new direction corresponds to a 45° line. Accordingly, pattern generator 27 will supply through buffers 32 and 34 three each +X and +Y incremental commands.

It is evident from the foregoing to those skilled in the state of the art that with the very simple input code shown, any type of graph including curves, alphanumeric characters, etc. can be generated. It will be also evident, that more elaborate input code for example full four bits providing larger change in length or direction can also be generated. The principle used can be extended to longer patterns and more directions. Other than the shown length sequence can be utilized such as 1, 5, 25 or 1, 3, 7, 21, 49. Spare bits of the ASCII character can be used for error checking and correction.

Two four bit instructions could be included in one ASCII character, permitting the plotting of other than straight lines in response to a single character. Other codes providing absolute length and incremental direction information or incremental length and absolute direction information can be generated using the principles shown, eliminating the need for length or direction memory, respectively. Additional possible changes and modifications within the scope of the present invention will be seen by those skilled in the state of the art.

FIG. 3 is a graph which shows the eight possible line segments which can be displayed when the memorized length equals one. For example, a line segment consisting of one increment can be displayed in any one of the directions labeled 0 through 7, inclusive, in FIG. 3 where the starting point of the line segment to be displayed is the center of FIG. 3 which is defined as the position of the trace of a graphic display device at the time that the display of the line segment is commenced.

FIG. 3 with its eight possible line segments defines the eight octants which are found in 360° with each octant comprising 45°. Thus, in FIG. 3, octant 0 is the area between the line segment 0 and line segment 1 and including line segment 0 but not including line segment 1. Octant 1 is the area between the line segment 1 and line segment 2 including line segment 1 but not including line segment 2. The remaining octants are similarly defined. Quadrant 1 is defined as including octants 0 and 1, quadrant 2 includes octants 2 and 3, quadrant

3 includes octants 4 and 5, and quadrant 4 includes octants 6 and 7.

FIG. 3 in summary represents the eight possible directions in which line segments can be drawn in digital incremental XY graphic display devices. However, the system which is shown in FIGS. 1 and 2 is limited to such display directions only when the line segment length is one increment.

Numbers at the end of the line segments indicate the information, or state, in the direction memory 19. Also it can be seen from FIG. 4, the numbers of the ternary code are assigned in a counter-clockwise direction to the line segments until all 360° have been covered. In FIG. 4 only one quadrant or two octants are shown. The designation $L = 3$ refers to the number of increments in each line segment. It also reflects the state of the length memory and generator 16 when the line segments shown in FIG. 4 are to be generated. Thus, as can be seen from FIG. 4, the line segment 00 would be generated by three increments in the +X direction. The line segment 01 would be generated by one positive X increment followed by a combined positive X and positive Y increment followed by a positive X increment. Similarly, line segment 02 would be generated by one positive X and Y increment, a positive X increment and again a combined positive X and positive Y increment. The manner in which the other line segments are generated can be readily determined merely by examining the line segments as shown in FIG. 4.

It can be seen that when the graph shown in FIG. 4 is expanded into all four quadrants, a total of 24 different direction line segments are possible. The number of possible different direction line segments is determined by taking the number of increments in each line segment and multiplying the same by eight. Thus, where the number of line segments equals three, the total number of directions allowed is 24, or $D = 8 \times L$ where $L = 3$.

FIG. 5*a* is a graph showing the number of possible line segments in a single octant where the number of increments in each line segment is equal to nine. As explained above, when the line segments comprised of nine increments each are utilized, there are possible 72 different direction line segments in 360° or $D = 8 \times L$ where $L = 9$. In each octant nine different line segments are possible as can be seen from FIG. 5.

Each of the line segments is identified with a number or ternary code. In FIG. 5, the ternary code is in three digits. By way of example, the line segment 002 would be generated first by a positive X increment followed by a combined +X +Y increment followed by five +X increments followed by a combined +X +Y increment and lastly followed by a +X increment.

FIG. 5*b* is a graph which shows the patterns which must be generated in the pattern generator 27 to display the line segments which are shown in FIG. 5*a*.

FIG. 6 is a graph which shows the signal patterns which would be produced in the pattern generator 27 in the event that each line segment is comprised of 27 increments. For reasons hereinbefore explained, this increases the possible number of line segment directions to 8×27 which is a total of 216; that is, $D = 8 \times L$ where $L = 27$. In FIG. 6, the patterns have been provided with the appropriate ternary coding. It will be noted that the designation given the patterns also includes an octal code X which runs from 0 to 7 corresponding to the octants in which the patterns are being generated.

Observation of FIGS. 3, 4, 5 and 6 shows that for the increment size and line segment lengths given, no finer end point resolution or directional resolution is possible by any other sequence of increments, a condition which will be defined as "complete directional resolution."

A detailed description of the various components of the controller 3 as shown in FIG. 2 will now be given. FIG. 7 is a circuit diagram partially in block form of the control logic 10. It consists of four main sections, a control start pulse input designated CS and clock synchronization circuit, an update clock 51, a divide by N modulus counter 66, and 10 control inputs designated 0 through 9 and labeled 39 – 48 together with the associated circuitry.

The clock synchronization circuit includes a conventional one-shot 50 which is responsive to a control start input on line 38 from the decoder output CS which serves as one input of an AND gate 52. The CS signal appears on line 38 whenever a control signal is supplied from the decoder 8 to any one of the lines 39 – 48. The other input from the update clock 51 provides a strobing output on line 49. One shot 50, when activated by the control start input, provides a window for a single clock pulse to line 53 since its output pulse width is slightly less than the pulse repetition period of the clock 51. The output of update clock 51 is also coupled to the divide-by-N modulus counter 66 through a delay element 65. N modulus counter 66 has three inputs 68, 69, 70 designated 1, 3, and 9 which are for the various length moduli possible with this embodiment of the present invention. These inputs are from the length modulus memory 107 of the length memory and generator 16 as illustrated in FIG. 8. The other input labeled R provides for reset of the counter to its initial state. The detailed construction of counter 66 may be identical to the dashed block of FIG. 8, labeled MNC, except that there is only a single output without the A, $\overline{A}$ and B, $\overline{B}$ outputs.

Referring now to control inputs 0 – 9, inputs 1 and 2 are coupled through AND gate 55, 56 and 57 to one shot generators 73, 74 and 75 respectively. The outputs of the one shots are coupled through an OR gate 79 to an AND gate 81 which has its other input line 71 from the counter 66. The output of AND gate 81 on line 90 provides positive update direction commands and is coupled to direction memory 19 (FIG. 2).

Input 3 is shown in the drawing but in this embodiment need not be connected. However, from a functional point of view when an input is received on input 3, a control start pulse will still be generated as hereinafter described strobing a clock pulse onto line 53 which will be coupled to delay element 84, through AND gate 87 to provide a length start (LS) control signal on line 95 which is coupled to length memory and generator 16 (FIG. 2). This will result in the generation of a line segment identical in length and direction to previous line segment as stored in the length memory 16 and direction memory 19.

Inputs 4, 5 and 6 are similar in function to 0, 1 and 2 in that they are coupled to AND gates 58, 59 and 60 through corresponding one shot circuits 76, 77 and 78 through an OR gate 80 and to AND gate 82 which has as an input the output from counter 66. The output of AND gate 82 on line 91 also provides direction update

commands, but in a negative direction. Line 91 is coupled to the direction memory 19 (FIG. 2). Lines 90 and 91 in the drawing of FIG. 2 are referred to as line pair 14 and designated with plus and minus signs in a manner similar to FIG. 7.

Input 7 serves to change the state of, and is coupled to the trace memory 21 (FIG. 2) through AND gate 61. Inputs 8 and 9 serve to control inputs to the length memory and generator 16 (FIG. 2) to provide update control information. Specifically, they are coupled through AND gates 62 and 63 to output lines 93 and 94.

Also coupled to the outputs of AND gates 61, 62 and 63 is an OR gate 85 which through an inverter 86 provides an inhibiting input to AND gate 87 preventing generation of a length start pulse if the last received character is 7, 8, or 9. The specific final control operations which are accomplished on the graphic display device as discussed in this embodiment of the invention are shown by Table 1 below.

Table 1

0 — update previous direction memorized by 3 quanta counter-clockwise (+) and generate a pattern in the new direction at the previously memorized length
1 — same as 0 except update by 2 quanta counter-clockwise (+)
2 — same as 0 except update by 1 quanta counter-clockwise (+)
3 — generate a pattern in the previously memorized direction at the previously memorized length
4 — update previous direction memorized by 1 quanta clockwise (−) and generate a pattern in the new direction at the previously memorized length
5 — same as 4 except update by 2 quanta clockwise (−)
6 — same as 4 except update by 3 quanta clockwise (−)
7 — toggle trace memory
8 — update previous length memorized by 1 positive quanta
9 — update previous length memorized by 1 negative quanta

The Table 1, as illustrated, describes the fundamental control actions of the present invention as presented in this embodiment. This description of the control inputs illustrate the variability of the length and direction parameters of the invention. The table in essence shows that digits 0 through 6 provide direction change instructions, digits 8 and 9 provide length change instructions, and digit 7 provides trace change instructions, such as lifting the pen off the paper or blanking off the C.R.T. beam. In effect inputs 0 – 9 provide the incremental update information for generating subsequent line segments based on previous line segment parameters.

The conventional one shots 1, 2 and 3 of FIG. 7, which are associated with control inputs 0, 1 and 2, and 4, 5 and 6, have varying pulse output times. Specifically, one shot 1 provides a pulse through OR gate 79 which will provide an enable input to AND gate 81 of sufficient width to allow 9 clock pulses from update clock 51 on line 71 to be generated on the output of AND gate 81 when the length modulus of the counter 66 has been set to 1. In the case where it is set to 3 only 3 pulses would appear at the output of AND gate 81 and in the case where the length modulus has been set to 9 only 1 output would appear. In the case of one shot 2 its pulse width allows 18 pulses on the output of AND gate 81 and in the case of one shot 3, 27 pulses when length modulus of counter 66 is set to 1. With length modulus 3 in counter 66 and with one shot 2 actuated, 6 pulses would appear on line 90, and with one shot 3 actuated, 9 pulses would appear on line 90. With length modulus 9 in counter 66 and with one shot 2 actuated, two pulses would appear on line 90, and with one shot 3 actuated, 3 pulses would appear on line 90.

A detailed block diagram of the length memory and generator 16 of FIG. 2 is shown in FIG. 8. The length memory 107 determines how many pulses should be generated at C2 to control the length of the line segment to be displayed. In the present embodiment a line segment may consist of either 1, 3 or 9 increments. The length generator starts generating pulses, counts the pulses being generated, compares the count with the length memory requirement, and when the count equals the required number it stops generating pulses. The length memory and generator 16 consist of the foregoing two basic parts interconnected by lines 68, 69 and 70. The reversible length memory is a reversible counter modulo 3 (RCM3) 107 which remembers the length of the previous pattern and can be incremented up or down for the next pattern. The reversible counter 107 known by those skilled in the art as a 3-bit shift counter based on an N bit reversible shift register functioning as shown in Truth Table 2

TRUTH TABLE 2

	Modulo 3		
	Counter outputs		
Counter state	0	1	2
	1	0	0
	0	1	0
	0	0	1

and is described, for example, in *Transistor Logic Circuits*, Richard B. Hurley, John Wiley and Sons, First edition, Section 9.4, pp. 268–269.

The length generator consists of a length counter clock (C_1) 100, a clock control flip-flop 102, a clock control and gate 101, a delay element 110, and modulo 'N' counter (MNC) which is composed of two shift counters; modulo 3 (CM3) counters 104 and 106, control and gates 113, 114, 118 and one OR gate 112. The length generator must generate a number of pulses, controlled by the length memory, and control lines to the pattern generator (FIG. 10).

The length start (LS) line 95 is connected to the set side of flip-flop 102. The S output of 102 is connected to one input of AND gate 101 with the clock 100 connected to the other input of gate 101. The output of gate 101 is connected to delay element 110, to one input of AND gate 113, and to the positive shift input of counter 104. The R output of flip-flop 102, line 105, is connected to the reset-to-0 state inputs of counters 104 and 106. Output 2 (see Table 2) of counter 104, line 115, is connected to the positive shift input of counter 106, to one input of AND gate 114, and to one input of AND gate 118. Outputs 1 and $\bar{1}$ of counter 104 are lines 117 and 116, respectively and are designated A and $\bar{A}$. Outputs 1 and $\bar{1}$ of counter 106 are lines 119

and **120**, respectively, and are also designated B and $\overline{B}$. Output **2** of counter **106** is connected to one input of AND gate **118**.

Input lines **93** (+) and **94** (−) from control logic unit **10** (FIG. **2**) are connected to the positive shift and negative shift inputs, respectively, of counter **107**. Outputs 0, 1, and 2 of counter **107** appear on lines **70, 69,** and **68** respectively. Line **70** is connected to one input of AND gate **113,** line **69** is connected to one input of AND gate **114,** and line **68** is connected to AND gate **118.** The outputs of AND gates **113, 114,** and **118** each are connected to an input of OR gate **112** whose output is connected to the toggle input of control flip-flop **102.**

When a signal pulse is received on line **93** (+) or on line **94** (−), counter **107** will shift up or down, respectively. One, and only one of the three output lines **70, 69** and **68** is high in each state (see Table 2).

When a signal pulse is received on line **95** (LS), flip flop **102** is set with the S output going high enabling AND gate **101** to pass C_1 clock signals to line **103.** The delay element **110** then generates the delayed length counter clock signal C_2 on line **111.**

Line **103** is also tied to one input of AND gate **113.** If the other input line **70,** is high (Table 2) the output signal of gate **113** will go to the OR gate **112,** whose output will toggle flip-flop **102** to disable clock control gate **101** and reset counter **104** and **106** through line **105.** Only one C_2 clock pulse will have been generated on line **111,** and control lines A (line **117**) and $\overline{A}$ (line **116**) which are coupled to the pattern generator will remain in the reset (0) state during the C_2 period.

If the other input, line **70,** to gate **113** is low, the gate is disabled and the trailing edges of clock pulses on line **103** will start positive shifting of counter **104.**

If line **69** is high, enabling AND gate **114,** then when output **2** of counter **104,** line **115,** goes high after three shifts of **104** (Table 2) an output signal is produced by AND gate **114,** enabling OR gate **112,** whose output will toggle **102.** This will disable gate **101** and reset counter **104** and **106.** Three C_2 pulses will have been generated.

If line **68** is high, only AND gate **118** can be enabled, and the negative transitions from output 2 of **104** on line **115** will positive shift counter **106.** After nine C_2 pulses on line **103** output 2 of counter **104** and **106** will be high. (See Table 3)

TRUTH TABLE 3

Counter state	Counter outputs A			Counter outputs B		
1	1	0	0	1	0	0
2	0	1	0	1	0	0
3	0	0	1	1	0	0
4	1	0	0	0	1	0
5	0	1	0	0	1	0
6	0	0	1	0	1	0
7	1	0	0	0	0	1
8	0	1	0	0	0	1
9	0	0	1	0	0	1

AND gate **118** is now enabled and its output goes to OR gate **112,** whose output in turn toggles **102** which disables **101.** Each of the nine pulses generated on line **111,** will have been associated with the appropriate condition of lines A, $\overline{A}$, B, $\overline{B}$ (lines **117, 116, 119, 120,** respectively) as shown in Table 4.

TRUTH TABLE 4

Output state	Length generator outputs A	$\overline{A}$	B	$\overline{B}$
1	0	1	0	1
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
5	1	0	1	0
6	0	1	1	0
7	0	1	0	1
8	1	0	0	1
9	0	1	0	1

A detailed block diagram of the direction memory **19** of FIG. **2** is shown in FIG. **9.** It consists of a ternary and an octal section interconnected by lines **130** and **131.** The ternary section consists of two reversible counter modulo 3's (RCM3) **125** and **126,** and a one-of-nine decoder which includes **9** AND gates, **140** through **148** inclusive. The octal section consists of one reversible counter modulo **2** (RCM2) **127,** one reversible counter modulo **4** (RCM4) **128,** a reversible counter modulo **8** (RCM8) **160,** and decoding OR gates **167** and **169.**

The ternary counters, **125** and **126,** and the octal counters **127, 128,** and **160,** must hold in memory the direction of the previous pattern and be able to be incremented to a new direction to provide a new pattern (see FIGS. **3, 4,** and **5***a*).

When signal pulses are received on line **90** (+) or line **91** (−), counter **125** will shift positive or negative, respectively (Table 2). Each time counter **125** passes its modulo limit of **3,** one pulse is passed through to counter **126.** Counter **125** and **126** taken together, then form a length counter memory of modulo **9.** Table 3 illustrates a typical count sequence. Output 0 of counter **125,** line **132,** is connected to the inputs of AND gates **140, 143,** and **146.** Output 1 of counter **125,** line **133,** is connected to the inputs of AND gates **141, 144,** and **147.** Output 2 of counter **125,** line **134,** is connected to the inputs of AND gates **142, 145,** and **148.** Output 0 of counter **126,** line **135,** is connected to the inputs of AND gates **140, 141** and **142.** Output 1 of counter **126,** line **136,** is connected to the inputs of AND gates **143, 144** and **145.** Output 2 of counter **126,** line **137,** is connected to inputs of AND gates **146, 147** and **148.** The outputs of AND gates **140** through **148** inclusive, lines **151** through **159** inclusive form a one-of-nine decoder, where one and only one of the nine outputs is high at a time.

Interconnection lines **130** and **131** are the positive carry and negative carry signal lines, respectively, from the reversible modulo **9** counter (formed by counter **125** and **126** together) to the positive shift and negative shift inputs, respectively, of counter RCM2 **127** and RCM8 **160.** Counter **127** and **128** together form a reversible counter modulo **8.** Counter **127** provides positive carry and negative carry from which serve as input shift pulses to counter **128.** The outputs of counter **128** designated K, M, L, N on lines **172, 173, 174,** and **175,** respectively, are described by Truth Table 5.

TRUTH TABLE 5

	Quadrant sign +x	+y	−x	−y	Quadrant number
R⟶	K	M	L	N	
	1	1	0	0	I
	0	1	1	0	II
	0	0	1	1	III
	1	0	0	1	IV

Counter **160** is a conventional reversible shift register of modulo **8** where one and only one of the **8** possible outputs is high at one time. Outputs 1, 2, 5, 6, on lines **161, 162, 164, 165** respectively, are connected to inputs of OR gate **169**, whose output in turn forms the X·Y signal on line **170** for use in the pattern generator. Outputs 2, 3, 6, 7, on lines **162, 163, 165, 166**, respectively, are connected to inputs of OR gate **167**, whose output forms the J signal on line **168** for use in the pattern generator.

All the counters (**125, 126, 127, 128, 160**) in the direction memory can be reset to the 0 state by a signal on line R.

FIG. **10** shows the pattern generator **27** of FIG. **2** in greater detail. The pattern generator is divided into two sections connected by signal line **250**; a combinational network on the left and an octant and sign steering network on the right. The combinational network in association with the length generator (FIG. **8**) forms an operational multiplier. Digital operational multipliers are known by those skilled in the state of the art. In addition to the one described in this embodiment, see *Computer Handbook*, Husky and Korn, McGraw-Hill, First edition, Section 21.5.3, pp. 21–89.

The multiplier will implement incrementally as a function of length change those equations shown in the following table:

TABLE 6

	Direction number		Function equations
R⟶		00=0	(51)
		01=$A\cdot B$	(52)
		02=$A\cdot\overline{B}$	(53)
		10=A	(54)
		11=$(A\cdot\overline{B})+(\overline{A}\cdot B)$	(55)
		12=$(A\cdot\overline{B})+(\overline{A}\cdot B)$	(56)
		20=$\overline{A}$	(57)
		21=$\overline{A\cdot B}$	(58)
		22=$\overline{A\cdot B}$	(59)

The multiplier output appears on line **250** and is schematically represented by FIG. **5***b*. When combined in the steering network with delayed length clock C2 on line **111**, J complements control input on line **168**, and an X·Y steering control input on line **170**, incremental direct command signals will be produced on lines **242–245** designated +X, −X, +Y, −Y, and coupled into a conventional display device to produce graphic display traces as shown by FIG. **5***a*.

A and B inputs to AND gate **200** are provided by the similarly lettered outputs **117, 119** of the length generator of FIG. **8**. An output signal on line **201** is applied to an AND gate **212** and an inverter **207**. The coincidence input to gate **212** is provided by direction memory output line **152** (FIG. **9**) designated "01" to implement function equation (2) of Table **6**. The output of gate **212** is connected through OR gate **220** to output line **250** of the multiplier.

The A input line **117** together with $\overline{B}$ input line **120** from the length generator causes AND gate **202** to implement function equation 3 on output signal line **203** which is applied to AND gate **213**, OR gate **204** and inverter **206**. The 02 input line **153** from the direction decoder is applied together with line **203** as inputs to AND gate **213** to implement function equation (3), Table 6, whose output is connected to one input terminal of OR gate **220**.

The A input line **117** is applied together with the "10" output line **154** as inputs to AND gate **214** to implement function equation (4), Table 6. The "11" output line **155** is connected to AND gate **215**. The $\overline{A}$ input line **116** is applied together with B input line **119** to AND gate **210** whose output is applied together with signal line **203** as inputs to OR gate **204** to implement the function equation (5) Table 6, on output signal line **151** which serves as an input to AND gate **215** and inverter **205**. Signal lines **151** and **155** combine as inputs to AND gate **215** to implement function equation (5), Table 6, whose output is connected to one output terminal of OR gate **220**.

The "12" input line **156** is applied together with the output line of inverter **205** as inputs to AND gate **216** to implement function equation (6), Table 6 whose output is connected to one input terminal of OR gate **220**.

The $\overline{A}$ input line **116** is applied together with "20" input line **157** to AND gate **217** to implement function equation (7), Table 6, whose output is connected to one input terminal of OR gate **220**.

The "21" input line **158** is applied together with the output line of inverter **206** as inputs to AND gate **218** to implement function equation (8), Table 6, whose output is connected to one input terminal of OR gate **220**.

The "22" output line **159** is applied together with the output line of inverter **207** as inputs to AND gate **219** to implement function equation (9), Table 6, whose output is connected to one input terminal of OR gate **220**.

Inputs to OR gate **220** combine to implement all function equations listed in Table 6, forming a pattern generator output signal, Z, on line **250**, which is connected to one terminal of Exclusive-NOR gate **221** of the octant and sign steering network portion of the pattern generator. In general this network performs the logical equation $(\overline{X}\cdot\overline{Y})+(X\cdot Y)=\overline{X\oplus Y}$ on ±X and ±Y output commands.

The Exclusive-NOR function gate is well known by those skilled in the state of the art and is commercially available. For example, the Signetics **8242** may be implemented by using an external collector pull-up resistor on output signal line **223**.

A Quadrant complement control input signal, J, line **168** is applied together with pattern generator signal line **250** to Exclusive-NOR gate **221** to implement the Exclusive-NOR function as described by the Truth Table 7

		−	
		+	
R →	250	J	223
	0	0	1
	1	0	0
	0	1	0
	1	1	1

TRUTH TABLE 7

whose output signal on line **223** is connected to the octant steering network through AND gate **222** and inverter **224**.

Delayed length generator clock output C2 is connected by signal line **111** to AND gates **222** and **225**. When signal output line **223** and clock C_2 are high, AND gate **222** outputs a high signal on line **230** which

is connected to inputs of AND gate **228** and OR gate **229.**

When signal output line **223** is low, inverter **224** outputs a high signal to AND gate **225.** When clock C_2 is high, AND gate **225** outputs a high signal on line **231** which is connected to inputs of AND gate **227** and OR gate **232.**

X·Y steering signal line **170** is connected to the inputs of inverter **226** and AND gate **228.** When signal line **170** is low and line **231** is high, inverter **226** outputs a high signal to an input of OR gate **229** through AND gate **227.** When signal lines **170** and **230** are high, AND gate **228** outputs a high signal to an input of OR gate **232.** A high signal on either input to OR gate **229** will output a high signal on line **234** which is connected to inputs of AND gates **238** and **239.** A high signal on either input to OR gate **232** will output a high signal on line **235** which is connected to inputs of AND gates **240** and **241.**

When either input K or L of sign control signal lines **172** or **174** are high and signal line **234** is high, then either AND gate **238** or **239** will output a high signal on +X output signal line **242** or −X output signal line **243** respectively.

When either input M or N of sign control signal lines **173** or **175** are high and signal line **235** is high, then either AND gate **240** or **241** will output a high signal on +Y output signal line **244** or −Y output signal line **245.**

An example of the operation of this embodiment in octant O, quadrant I, direction **00** (in other words the horizontal line of FIG. **5***a*) with length memory **107** (FIG. **8**) equal to modulus **9,** is as follows: Since no input signal is provided to OR gate **220** for direction **00** (**00** output line **151** of the direction memory of FIG. **9** is not connected) signal line **250** will remain low for all states of the incremental length generator outputs A, $\overline{A}$, B, and $\overline{B}$, on input lines **117, 116, 119,** and **120.** J complement control line **168** has a low signal in octant "0" (see Truth Table **8**).

TRUTH TABLE 8

Output number	(x·y)	J	Octant output 0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
2	1	1	0	0	1	0	0	0	0	0
3	0	1	0	0	0	1	0	0	0	0
4	0	0	0	0	0	0	1	0	0	0
5	1	0	0	0	0	0	0	1	0	0
6	1	1	0	0	0	0	0	0	1	0
7	0	1	0	0	0	0	0	0	0	1

Since line **250** is low also, Exclusive-NOR gate **221** will produce a high output state on line **223** (see Truth Table 7). Signal line **223** is complemented by inverter **224** to inhibit AND gate **225** whose low output signal on line **231** in turn inhibits AND gate **227.** The X·Y steering signal on line **170** is low (see Truth Table 8) inhibiting AND gate **228.** Since both signal inputs to OR gate **232** are low, both Y output sign AND gates **240** and **241** will be inhibited by OR gate **232** output signal line **235,** which will produce a low signal on +Y and −Y output signal lines **244** and **245** respectively. A high on signal line **223** and the coincidence of a C2 clock pulse to AND gate **222,** will produce a high on output signal line **230.** The low output signal of inhibited AND gate **227** combines with the high input signal on line **230** to produce a high output signal on line **234** from OR gate **229,** which serves to enable X output sign AND gates **238** and **239.** Since X is positive in quadrant I, X output sign steering lines K and L will be high and low respectively (see Truth Table **5**). Input lines **172** and **234** combine to produce a high signal on +X output signal line **242** from AND gate **238,** while input lines **174** and **234** combine to produce a low signal on −X output signal line **243** from AND gate **243.** Therefore, length generator clock pulse C_2 will appear **9** times on +X output line **242** to produce a trace shown by FIG. **5***a* for direction **00.**

To further illustrate the operation of the octant and sign steering network, assume octant **3,** quadrant II is presently stored in the direction memory of FIG. **9,** with a direction **00** at length modulus **9.**

The output line **250** will again remain low for all states of the incremental length generator outputs A, $\overline{A}$, B and $\overline{B}$ on inputs **117, 116, 119** and **120.** J complement control line **168** has a high signal (see Truth Table **8**) which together with a low signal on line **250** applied to Exclusive-NOR gate **221** will produce a low output state on line **223** (see Table 7) which serves to inhibit AND gate **222,** whose low output signal on line **230** in turn inhibits AND gate **228.** Inverter **224** complements signal line **223** which enables AND gate **225** to produce a high signal on line **231** when a C_2 clock signal on line **111** is high. The X·Y steering signal on **170** is low, Table **8,** inhibiting AND gate **228** whose low output signal combined with a high signal on line **231** as inputs to OR gate **232** will produce a high on output signal line **235.** Since Y is positive in quadrant II, Table **5,** Y output sign steering lines M and N combine with signal line **235** as inputs to AND gates **240** and **241** to produce a high output signal on +Y output signal line **244** and a low output signal on −Y output signal line **245.** Inverter **226** complements X·Y signal line **170** producing a high output signal which combined with a high signal on line **231** to AND gate **227** will produce a high output signal from OR gate **229** on line **234.** Since X is negative in quadrant II, Table **5,** X output sign steering lines K and L are low and high respectively and combine with signal line **234** as inputs to AND gates **238** and **239** to produce a low output signal on +X output signal line **242** and a high output signal on −X output signal line **243.** Thus, for direction **00,** length **9,** −X and +Y, output signal commands are combined by a graphic display device to produce a line displaced by 45° from the X and Y axes in quadrant II.

By examination of the above example and the Tables **5, 7** and **8,** it may be seen that for any combination of inputs to the octant and sign steering network, appropriate ±X and ±Y signal commands will appear on lines **242, 243, 244** and **245.** Further examination will reveal that by truncation of the incremental length generator output states from **9** to **3** or **1,** the traces represented by FIGS. **5***a*, **4,** or **3** respectively, would be generated from the output signal commands by a graphic display device.

Directions **00** to **22** as illustrated by FIG. **5***a*, are each represented by a decoded output signal line of the direction memory (FIG. **9**) and are applied together as one input factor to the combinational network comprising the digital operational multiplier of FIG. **10.** The other input factor is the A, B outputs from the length generator (FIG. **8**) Truth Table 4 illustrates the sequence of output states for a length modulus of **9.** The resulting pulse output on signal line **250** as shown by FIG. **5***b* for modulus **9,** represents the digital product of the two input factors.

An example of the operation of this embodiment for Direction "12" with (see FIG. 5*a*) length memory equal to a modulus of 9 follows. Truth Table 4 represents output signal lines A, $\overline{A}$, B and $\overline{B}$ during the successive states allowed the length generator. Output lines A and B and their complements form the output signals that when combined by AND gates 200 and 210, OR gate 204, and inverter 205 in FIG. 10 with direction "12" by AND gate 216 will serve to implement function equation (6) (Table 6) to produce output pulse pattern "12" of FIG. 5*b* as follows: Still referring to FIG 10, A and $\overline{B}$ input signals on lines 117 and 120 appear as inputs to AND gate 202 to produce a high on output signal line 203 when both inputs are high during length generator states 2 and 8 (see Truth Table 4). $\overline{A}$ and B output signals on lines 116 and 119 appear as inputs to AND gate 210 to produce a high output signal when both inputs are high during length generator states 4 and 6. Both signal output lines of gates 210 and 202 are combined by OR gate 204 and complemented by inverter 205 to produce an input signal at AND gate 216. An input on line 156 which is direction line "12", is high during length generator states 1, 3, 5, 7 and 9. These signals produce output pulse pattern 12 of FIG. 5*b* on signal line 250. This pulse pattern, when appropriately combined with J, X·Y and C_2, KLMN inputs to the output and sign steering network as previously outlined above, will produce output signal commands to a graphic display device to produce trace 12 as shown in FIG. 5*a*. By examination, it may be seen that for appropriate combination of direction and length generator outputs, pulse patterns 00 through 22 referring to FIG. 5*b* will be generated.

It may be seen by those skilled in the state of the art that pattern generation may be accomplished by other means For example, read only memories, diode matrices or other intelligence storage devices may be addressed and sequenced to produce patterns described by FIG. 5*b*.

It should be further evident that the pattern generator output signals are essentially output commands describing vector segments and may be coupled to other than two dimensional graphic display devices; for example, X, Y and Z machine tool systems, or any other type of process control. Outputs may also be temporarily stored by a digital storage system such as a magnetic tape recorder for use at a later time.

From the foregoing, it also would be evident to those skilled in the state of the art that unused code combinations, such as alphabetic ASCII characters, could be utilized to perform such customary tasks as start plot, end plot, reset plotter and select plotter or pen in case of multiple plotters or pens respectively.

Although in the embodiment ASCII characters were assumed as being used for the input signal, other serially or parallel coded digital signals can also be utilized. For example, if the input signal is parallel coded, the serial to parallel converter may be omitted. The number of parallel input lines can be increased or decreased as required by the number of bits in the parallel code.

It is apparent from the foregoing that there has been provided a new and improved graphic display apparatus, system and method. There has been provided the capability of a high display speed while receiving digitally coded data at a low input rate. This makes possible the utilization of a transmission medium having a relatively narrow band width. There is also provided the capability of providing patterns representing line segments for substantially all possible end points for any line segment which has a length greater than one increment and which is plottable in response to a single input character. There also is provided the capability of displaying straight lines of arbitrary direction or a variety of curves at or near the maximum display speed of display devices such as plotters. It is also evident from the foregoing that due to the essentially unlimited expandability of the code and apparatus to display line segments of longer length and more directions, this apparatus, system and method is particularly adaptable to operate inherently high speed display devices such as CRT. Since fewer bits are required for the transmission of information, there is provided the capability for code redundancy which can be utilized for error checking and correction. There is also provided the capability for the coding of two independent line segment instructions within a single character. It is also apparent that the other objects and features of the invention herein before set forth have been met.

I claim:

1. In a graphic display system display means for displaying graphic patterns consisting of end to end linked line segments characterized by at least one of the two parameters of length and direction and controller means for generating control signal sequences for controlling said display means, said controller having

input means for receiving input information in the form of digitally encoded signals,

memory means for storing at least one of said length and direction parameters of at least one line segment previously displayed by said display means,

logic means connected to said input means and said memory means for recognizing if said digitally encoded signals represent a differential value change, including polarity, by which said parameter which has been stored must be altered, said logic means also including means for algebraically adding said differential value change to said stored parameter in order to obtain an updated parameter to be stored in said memory means,

and generator means connected to the memory means utilizing the updated stored parameter in the generation of subsequent control signal sequences representing at least one subsequent line segment, said display means being responsive to said subsequent control signal sequences for providing a display.

2. A system as in claim 1 wherein said memory means include both length and direction memories for both said length and direction parameters.

3. A system as in claim 1 wherein the generator means comprises a pattern generator, said pattern generator in response to a single input character being capable of generating output signal patterns representing line segments for substantially all possible end points for any line segment having a length greater than one increment.

4. A system as in claim 1 wherein said memory means includes a length memory and a direction memory, wherein the means for algebraically adding consists of control logic means capable of updating stored length and stored direction in the length memory and the direction memory in response to and in accordance with the type of signals received by the control logic means,

and wherein the generator means consists of length and pattern generating means under the control of the length memory and the direction memory.

5. A system as in claim 4 wherein said input information is in the form of serially coded characters consisting of binary bits together with means included in the input means for converting the serially coded characters to parallel coded characters and together with decoding means connected to the input means for receiving the parallel coded characters and supplying it in decoded form to the control logic means.

6. A system as in claim 1 together with a transmission medium having a limited band width coupled to the input means for carrying the input information.

7. A system as in claim 2 wherein the length parameter which has been stored is incremented or decremented according to an odd number base number system.

8. A system as in claim 7 wherein said odd number base number system is a ternary number system.

9. A system as in claim 1 together with a transmission medium having a limited band width coupled to the input means for carrying the input information.

10. A system as in claim 2 wherein the length parameter which has been stored is incremented or decremented according to an odd number base number system.

11. A system as in claim 7 wherein said odd number base number system is a ternary number system.

12. In a controller for generating signal patterns representing linked vectors, the starting point of one vector being the end point of the previous vector, with each pattern being characterized by at least one of the two quantized vector parameters of length and direction, input means for receiving input information in the form of digitally coded signals, memory means for storing at least one of said length and direction parameters related to at least one signal pattern previously generated, logic means, connected to said input means and said memory means, for recognizing if said digitally coded signals contain an instruction for an incremental change by which said stored parameter must be altered digitally, said logic means also including computing means for performing said digital altering of updating said stored parameter in response to any change instruction whereby an updated parameter is obtained to replace the previously stored parameter in said memory means, said logic means further recognizing the absence of an instruction for incremental change of said parameter in said digitally coded signals to designate the previously stored parameter for signal pattern generation, and generator means connected to the memory means utilizing the updated stored parameter in the generation of at least one subsequent signal pattern.

13. A controller as in claim 12 wherein said generator means comprises a pattern generator, said pattern generator in response to a single input character being capable of generating output signal patterns representing vectors for substantially all possible end points for any vector having a length greater than one increment.

14. A controller as in claim 12 wherein said memory means includes a length memory and a direction memory, wherein the computing means consists of control logic means capable of updating the stored length and stored direction in the length memory and the direction memory in response to and in accordance with the type of character, including a character designating zero change, received by the control logic means, and wherein the generator means consists of the length and pattern generating means under the control of the length memory and the direction memory.

15. A system as in claim 14 wherein said control logic means includes means for generating a plurality of pulse trains having different predetermined lengths corresponding to the amount of change in said parameters and said memory means includes counter means for storing said parameters of said most recently generated signal pattern and said memory means being responsive to said pulse train for sequencing to a new state representative of the updated parameters.

16. A system as in claim 12 wherein said memory means serve to store both said length and direction parameters.

17. A controller as in claim 12 wherein said generator means comprises a pattern generator including function generator means responsive to the length parameter and a part of the direction parameter for generating a functional representation of a line segment, said functional representation defining one of a set of line segments within each octant of a plane, and steering means responsive to said functional representation and to the remaining part of said direction parameter for generating said one line segment within the octant specified by said remaining part.

18. In a method of generating by an apparatus signal patterns representing linked vectors, the starting point of one vector being the end point of the previous vector, with such patterns being characterized by at least one of the two quantized vector parameters of length and direction, comprising the steps of, digitally storing at least one of said length and direction parameters of at least one signal pattern previously generated, receiving input information in the form of digitally encoded signals, recognizing if said signals contain an encoded instruction for an incremental change by which said stored parameter must be digitally altered, digitally altering said stored parameter in response to any change instruction in order to obtain an updated stored parameter, and generating at least one subsequent signal pattern utilizing said updated stored parameter.

19. A system as in claim 14 wherein said input information is in the form of serially coded characters consisting of binary bits together with means included in the input means for converting the serially coded characters to parallel coded characters and together with decoding means connected to the input means for receiving the parallel coded characters and supplying it in decoded form to the control logic means.

20. A graphic display system for displaying graphic patterns of end to end linked line segments having controlling means for generating control signals for the display of said segments, the input of said controlling means receiving digitally encoded signals comprising information for the next segment to be displayed, said controlling means including memory means for storing information of the last segment displayed and producing from the information fed in at the input and the stored information the control signals for the next segment to be displayed, characterized in that the memory means stores at least one of the two parameters of length and direction of the last segment displayed, that the input signals indicate the value and the sign of an alteration of the stored parameter, that a control logic means algebraically adds the alteration value decoded

in a decoder to the stored value of the corresponding parameter and again stores the new value of the parameter thus obtained in the memory means and that a pattern generator utilizing said new value of the parameter generates a control signal sequence for the display of the next segment.

21. In an apparatus for generating vector signal patterns representing vectors, the starting point of one vector being the end point of the previous vector, with each vector signal pattern being characterized by at least the two parameters of length and direction, means for receiving input information in the form of digitally coded signals, means for storing at least one of said length and direction parameters of at least one vector signal pattern previously generated, logic means for recognizing if said digitally coded signals contain incremental change instructions for said stored parameter including means for updating by computation said stored parameter in response to any change instruction whereby an updated parameter is obtained to replace the previously stored parameter in said memory means, said logic means also serving in absence of an instruction for incremental change to designate the prviously stored parameter as an unchanged and still updated stored parameter for signal pattern generation, and means for generating at least one subsequent vector signal pattern utilizing the updated stored parameter.

22. In a method for displaying graphic patterns on display means by control signal sequences generated by controller means, said graphic patterns consisting of end to end linked line segments characterized by at least one of the two parameters of length and direction, the method comprising the steps of, storing at least one of said length and direction parameters of at least one segment previously displayed by said display means, receiving input information in the form of digitally encoded signals, recognizing if the digitally encoded signals represent a differential value change by which said parameter which has been stored must be altered, altering said stored parameter in accordance with said value change, and utilizing the updated stored parameter to generate subsequent control signal sequences representing at least one subsequent line segment for display.

23. In a method for displaying graphic patterns consisting of line segments grouped in lowest to highest length sets according to lowest to highest number of increments, receiving a sequence of single input commands, generating in response to at least some of said single input commands, output signal patterns representing line segments in such a manner that all the members of the higher length line segment sets are generated by the step of systematic series combination of the members of the lower length set, said combination being further characterized by each set containing the same number of different direction line segments as eight times the number of increments in the set, thereby representing complete directional selectivity.

24. In a pattern generator for generating output signal patterns representing line segments consisting of a predetermined number of discrete increments based on data representing the length and direction of the segments, the pattern generator comprising function generator means for computing and generating from the length data and a first portion of the direction data a signal sequence as a functional representation of a line segment having a predetermined number of increments, said functional representation defining one of a set of line segments within each octant of a plane, and steering means for combining said functional representation with a second portion of the direction data to produce an output signal pattern for generating said one line segment within the octant specified by said second portion of the direction data.

25. A pattern generator as in claim 24 wherein said function generator means includes an operational multiplier.

26. In a method for generating signal patterns representing line segments consisting of a predetermined number of discrete increments, each of said line segments being characterized by at least two parameters including length and direction, the steps of computing and generating from the length and direction parameters a functional representation of a line segment having a predetermined number of increments, said functional representation defining one of a set of line segments within each octant of a plane, and the step of combining the functional representation with an additional direction parameter to produce a signal pattern for generating said one line segment within the octant specified by said additional parameter.

27. In a method of generating patterns consisting of successive segments characterized by at least one of the parameters of length and direction in response to a succession of electrically coded input commands, comprising the steps of receiving an input command, decoding whether the command contains an instruction to incrementally change at least one of the two parameters of length and direction of the next segment to be generated compared with the said one parameter of the immediately preceding segment, computing at least one new parameter for the next segment in response to a decoded incremental change instruction, generating said next segment characterized by said computed new parameter, and memorizing at least one of said parameters of the preceding segment for use in said step of computing said new parameter for the next segment.

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