(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 January 2009 (15.01.2009)

PCT

(10) International Publication Number
WO 2009/007886 A1

(51) International Patent Classification:
H01L 33/00 (2006.01)

(21) International Application Number:
PCT/IB2008/052681

(22) International Filing Date: 3 July 2008 (03.07.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/775,059 9 July 2007 (09.07.2007) US

(71) Applicant *(for all designated States except US)*: **PHILIPS LUMILEDS LIGHTING COMPANY, LLC** [US/US]; 370 West Trimble Road MS 91/MG, San Jose, CA 95131 (US).

(71) Applicant *(for DM only)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors: **BASIN, Grigoriy**; c/o 370 West Trimble Road MS 91/MG, San Jose, CA 95131 (US). **WEST, Robert S.**; c/o 370 West Trimble Road MS 91/MG, San Jose, CA 95131 (US). **MARTIN, Paul S.**; c/o 370 West Trimble Road MS 91/MG, San Jose, CA 95131 (US).

(74) Agents: **BEKKERS, Joost, J.J.** et al.; High Tech Campus Building 44, NL-5656 AE Eindhoven (NL).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: SUBSTRATE REMOVAL DURING LED FORMATION

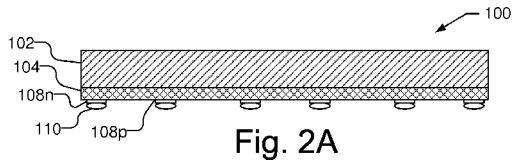

Fig. 2A

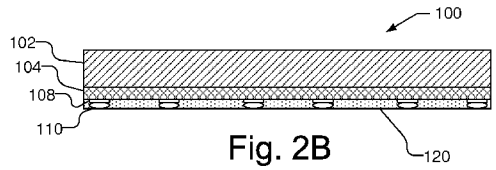

Fig. 2B

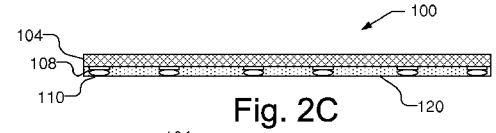

Fig. 2C

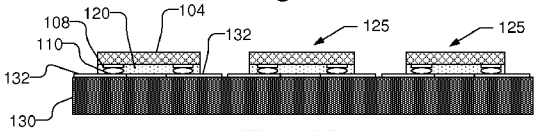

Fig. 2D

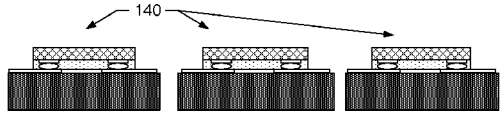

Fig. 2E

(57) Abstract: A light emitting diode (LED) is fabricated using an underfill layer that is deposited on either the LED or the submount prior to mounting the LED to a submount. The deposition of the underfill layer prior to mounting the LED to the submount provides for a more uniform and void free support, and increases underfill material options to permit improved thermal characteristics. The underfill layer may be used as support for the thin and brittle LED layers during the removal of the growth substrate prior to mounting the LED to the submount. Additionally, the underfill layer may be patterned to and/or polished back so that only the contact areas of the LED and/or submount are exposed. The patterns in the underfill may also be used as a guide to assist in the singulating of the devices.

WO 2009/007886 A1

European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

SUBSTRATE REMOVAL DURING LED FORMATION

Grigoriy Basin
Robert S. West
Paul S. Martin

FIELD OF THE INVENTION

[0001] The present invention is related to the fabrication of a light emitting diode.

BACKGROUND

[0002] Semiconductor light-emitting diodes (LEDs) are among the most efficient light sources currently available. Materials systems currently of interest in the manufacture of high-brightness light emitting devices capable of operation across the visible spectrum include Group III-V semiconductors; for example, binary, ternary, and quaternary alloys of gallium, aluminum, indium, nitrogen, phosphorus, and arsenic. III-V devices emit light across the visible spectrum. GaAs- and GaP-based devices are often used to emit light at longer wavelengths such as yellow through red, while III-nitride devices are often used to emit light at shorter wavelengths such as near-UV through green.

[0003] Gallium nitride LEDs typically use a transparent sapphire growth substrate due to the crystal structure of sapphire being similar to the crystal structure of gallium nitride.

[0004] Some GaN LEDs are formed as flip chips, with both electrodes on the same surface, where the LED electrodes are bonded to electrodes on a submount without using wire bonds. A submount provides an interface between the LED and an external power supply. Electrodes on the submount bonded to the LED electrodes may extend beyond the LED or extend to the opposite side of the submount for wire bonding or surface mounting to a circuit board.

[0005] Figs. 1A-1D are simplified cross-sectional views of the process of mounting GaN LEDs 10 to a submount 12 and removing the sapphire growth substrate 24. The submount 12 may be formed of silicon or may be a ceramic insulator. If the submount 12 is silicon, an oxide layer may insulate the metal pattern on the submount surface from the silicon, or different schemes of ion implantation can be realized for added functionality such as electro-static discharge protection.

[0006] As can be seen in Fig. 1A, a number of LED dies 10 are formed with a thin GaN LED layer 18 formed on a sapphire growth substrate 24. Electrodes 16 are formed in electrical contact with the n-type and p-type layers in the GaN layer 18. Gold stud bumps 20 are placed on the electrodes 16 on the LEDs 10 or alternatively on the metal pads 14 on the submount 12. The gold stud bumps 20 are generally spherical gold balls placed at various points between the LED electrodes 16 and the submount metal pads 14. The LED layers 18 and electrodes 16 are all formed on the same sapphire substrate 24, which is then diced to form the individual LED dies 10.

[0007] As illustrated in Fig. 1B, the LEDs 10 are bonded to the substrate 12 with the metal pads 14 on the submount 12 electrically bonded to the metal electrodes 16 on the GaN layers 18. Pressure is applied to the LED structure while an ultrasonic transducer rapidly vibrates the LED structure with respect to the submount to create heat at the interface. This causes the surface of the gold stud bumps to interdiffuse at the atomic level into the LED electrodes and submount electrodes to create a permanent electrical connection. Other types of bonding methods include soldering, applying a conductive paste, and other means.

[0008] Between the LED layers 18 and the surface of the submount 12 there is a large void that is filled with an epoxy to provide mechanical support and to seal the area, as illustrated in Fig. 1C. The resulting epoxy is referred to as an underfill 22. Underfilling is very time-consuming since each LED dies 10 must be underfilled separately, and a precise amount of underfill material needs to be injected. The underfill material must be a low enough viscosity that it can flow under the LED dies 10, which may include a complicated geometry of electrodes, without trapping any bubbles that could result in poorly supported regions, as illustrated as region 22a. The underfill material, however, must not spread in an uncontrolled fashion onto undesirable surfaces, such as the top of the LED device, as illustrated at 22b, or pads on the submount where wire bonds must be subsequently applied.

[0009] The sapphire substrates 24 are removed after the LED dies 10 are bonded to the submount 12 and the submount 12 is separated into individual elements to form the LED structures illustrated in Fig. 1D. Since the LED layers 18 are very thin and brittle, the underfill serves the additional purpose to provide the necessary mechanical support to prevent fracturing of the fragile LED layers when the supporting substrate 24 is removed. The gold stud bumps

20 do not provide sufficient support by themselves to prevent fracturing of the LED layers since, given their limited shape and are spaced far apart. Conventionally used underfill materials are typically composed of organic substances and possess very different thermal expansion properties from metal and semiconductor materials. Such spurious expansion behavior is particularly aggravated at high operating temperatures--typical of high power LED applications--where underfill materials approach their glass transition point and begin to behave as elastic substances. The net effect of such mismatch in thermal expansion behavior is to induce stresses on the LED devices that limit or reduce their operability at high power conditions. Lastly, underfill materials have low thermal conductivity properties that result in unnecessarily high temperature operation for the semiconductor devices.

[0010] What are needed are techniques for mechanically supporting the thin LED layers during a substrate removal process which provides a more uniform and void free support; provides support with more closely matched thermal expansion behavior, provide a support with high temperature operability, not limited by the glass transition point of organic materials; and provides a support with improved thermal conductivity for superior heat sinking.

SUMMARY

[0011] A light emitting diode (LED) is fabricated using an underfill layer that is deposited on either the LED or the submount prior to mounting the LED to a submount. The deposition of the underfill layer prior to mounting the LED to the submount provides for a more uniform and void free support, and increases underfill material options to permit improved thermal characteristics. In one embodiment, the underfill layer may be deposited on the LEDs and used support for the thin and brittle LED layers during the removal of the growth substrate. The growth substrate can then be removed at the wafer level prior to mounting the LED to the submount. In other embodiments, the underfill layer may be patterned and/or polished back so that only the contact areas of the LED and/or submount are exposed. The LEDs and submount can then be bonded with the underfill layer between them. The patterned underfill layer may also be used as a guide to assist in the singulating of the devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figs. 1A-1D are simplified cross-sectional views of the process of mounting LEDs to a submount, followed by injecting an underfill and removing the sapphire growth substrate.

[0013] Figs. 2A-2E are simplified cross-sectional views of a process of removing the growth substrate from LEDs on the wafer level and mounting the LEDs to a submount in accordance with one embodiment of the present invention.

[0014] Fig. 3 illustrates a portion of the LED structure including a sapphire growth substrate and GaN layers.

[0015] Figs. 4A and 4B illustrate the deposition of the underfill material over a portion of the LEDs at the wafer level.

[0016] Figs. 5A-5C are simplified cross-sectional views of mounting LEDs to a submount and removing the growth substrate after the LEDs are mounted to the submount.

[0017] Figs. 6A-6E are simplified cross-sectional views of a process of mounting LEDs to a submount that has an underfill coating.

[0018] Figs. 7A-7D illustrate another embodiment in which wafer level LEDs with a patterned underfill layer are mounted to a submount.

[0019] Figs. 8A-8G illustrate another embodiment in which individual LED dies are mounted to a submount on which an underfill layer has been deposited.

DETAILED DESCRIPTION

[0020] Figs. 2A-2E are simplified cross-sectional views of a process of mounting GaN LEDs to a submount and removing the growth substrate in accordance with one embodiment of the present invention.

[0021] Fig. 2A illustrates a portion of a wafer level LED structure 100 including a growth substrate 102, which may be, e.g., sapphire, upon which has been formed the thin GaN LED layers 104. The GaN LED layers 104 may be conventionally grown on the sapphire substrate, as described, e.g., in U.S. Publication No. 2007/0096130, which is incorporated herein by reference. Fig. 3 illustrates a portion of the wafer structure 100 including a sapphire substrate 102 over which an n-type GaN layer 104n is grown using conventional techniques. The GaN layer 104n may be multiple layers including a clad layer. The GaN layer 104n may include Al, In, and an n-type dopant. An active layer 104a is then grown over the GaN layer 104n. The

active layer 104n will typically be multiple GaN-based layers and its composition (e.g., $In_xAl_yGa_{1-x-y}N$) depends on the desired wavelength of the light emission and other factors. The active layer 104a may be conventional. A p-type GaN layer 104p is then grown over the active layer 104a. The GaN layer 104p may be multiple layers including a clad layer and may also be conventional. The GaN layer 104p may include Al, In, and a p-type dopant. The LED structure of FIG. 3 is referred to as a double heterostructure.

[0022] In one embodiment, the growth substrate is about 90 microns thick, and the GaN layers 104 have a combined thickness of approximately 4 microns.

[0023] Although a GaN based LED with a sapphire growth substrate is used in the example, other types of LEDs using other substrates such as SiC (used to form an InAlGaN LED) and GaAs (used to form an AlInGaP LED) may benefit from the present invention.

[0024] Metal bonding layers are formed over the wafer to form n-contacts 108n and p-contacts 108p, referred to herein as contacts 108. The contacts 108 may be patterned by forming a masking layer at positions where the metal contacts are not desired, then depositing the metal contact layer over the entire wafer, and then stripping the masking layer to lift off the metal deposited over it. The metal layers could also be negatively patterned by depositing similarly stacked blanket metal layers and then selectively etching them back using a masking scheme. The contacts may be formed from one or more metals, such as TiAu, Au, Cu, Al, Ni or other ductile material, or a combination of such layers. Stud bumps 110, which may be, e.g., gold, are then formed over the contacts 108. The stud bumps 110 are generally spherical gold balls placed at various points on the contact 108. The stud bumps 110 serve as part of the contacts for the LED and are used to bond the LED to a submount. If desired, other types of bonding material or structures such as plates may be used in place of stud bumps 110.

[0025] As illustrated in Fig. 2, the underfill 120 is then deposited over the GaN layers 104, contacts 108 and bumps 110. Because the underfill 120 is applied prior to bonding the LEDs to a submount, any suitable material may be used for the underfill 120 without depending on the flow characteristics that are needed in the case of traditional underfill. For example, a polymer polyimide based materials, which have high glass transition temperature, may be used as the underfill layer 120. With the use of polyimide material, a solvent may be used to adjust the

viscosity to 400-1000Pa*s to assist in the deposition of the material. A filler powder, such as small particle SiO_2, may be added to the polyimide material, e.g., in the amount of 50% to 90%) in order to match the CTE (coefficient of thermal expansion). During deposition, the LEDs and polyimide material may be heated below the glass transition temperature, and then allowed to cool down to cure. Such materials will help the device withstand high temperature/high current condition without deformation of thin LEDs. The underfill material may be a bi-stage cured material, using a low temperature cure for cross-linking of additives, .e.,g epoxy additives, in the underfill material that are responsible for the first stage cure. The underfill material should have B-stage cure properties in order to adhere to both LED and support wafer surfaces.

[0026] Figs. 4A and 4B illustrate the deposition of the underfill 120 material over a portion of the wafer 100. As shown in Fig. 4A, the underfill 120 may be blanket deposited over the surface of the GaN layers 104. In one embodiment, the underfill 120 is patterned, e.g., using stencil printing or mesh screen-printing, so that areas 122, such as area where the LED dies are to be separated, have no underfill 120. For example, the material may be deposited in the form of a viscous paste using, e.g., stencil printing techniques. Areas where underfill is not desired, e.g., the areas around the LEDs where there is wire bonding, are protected by a mask. Openings in the mask allow the underfill material to be deposited in desired areas. After deposition, e.g., by screen printing, the underfill layer is cured at low temperature, e.g., 120°-130°C, until it is sufficiently hard to be polished. As shown in Fig. 4B, the underfill 120 is then polished back until the metal connection, i.e., bumps 110, are exposed. In one embodiment, the underfill 120 has a final thickness of 30μm.

[0027] The underfill 120 advantageously serves as a support layer for the GaN layers 104 and, accordingly, the growth substrate 102 can be removed, as illustrated in Fig. 2C. The substrate 102 can be removed, e.g., by laser lift-off using an excimer laser beam that is transmitted through the transparent sapphire substrate 102 and evaporates a top layer of the n-GaN layer 104n. The removal of the substrate 102 produces tremendous pressure at the substrate/n-GaN layer 104n interface. The pressure forces the substrate 102 off the n-GaN layer 104n, and the substrate 102 is removed. The support provided by the underfill 120 prevents the high pressure during the substrate lift-off from fracturing the thin brittle LED layers 104. Additionally, if

desired, the exposed n layer 104n (shown in Fig. 3) may be roughened for increasing light extraction, e.g., using photo-electro-chemical etching, or by small scale imprinting or grinding. Alternatively, roughening can include forming prisms or other optical elements on the surface for increased light extraction and improved control of the radiation pattern.

[0028] After the substrate is removed, the GaN layers 104 with the underfill 120 are scribed and separated into individual LED elements. The scribing and separation may be accomplished using, e.g., a saw that uses the areas 122 in the underfill 120 as a guide. Alternatively, a laser scribe process may be used. Prior to separating, the wafer of LEDs is adhered to a stretchable plastic sheet, and after the wafer is broken along the scribe lines, the sheet is stretched to separate the dies while the dies remain adhered to the stretchable sheet. An automatic pick and place device then removes each die 125 from the sheet, and mounts the die 125 on a submount 130 as illustrated in Fig. 2D. The bonding metal, i.e., bumps 110 on the LED dies 125 are ultrasonically or thermosonically welded directly to corresponding bonding metal patterns 132 on the submount 130, which may be, e.g., gold or other appropriate material. The submount 130 may be formed of silicon or a ceramic insulator. If the submount 130 is silicon, an oxide layer may insulate the metal pattern on the submount surface from the silicon, or different schemes of ion implantation can be realized for added functionality such as Zener diodes for electro-discharge protection. If the submount is a ceramic instead of silicon, the metal patterns can be directly formed on the ceramic surfaces.

[0029] An ultrasonic transducer (thermosonic metal-to-metal interdiffusion process) may be used to apply a downward pressure to the dies 125 and rapidly vibrates the dies 125 with respect to the submount 130 so that the atoms from the opposing bonding metals merge to create an electrical and mechanical connection between the die 125 and the submount 130. Other methods for LED die-to-submount interconnection can also be used, such as using a soldering layer. During die attach process, e.g., with an Au-Au interconnect, the substrate temperature is maintained above (e.g., 40-50°C) the glass transition temperature Tg, which causes the underfill material to be in the elastic stage to soften and comply with the LEDs and to prevent the formation of voids. Subsequently, the underfill layer is permitted to cure at approximately the glass transition temperature, e.g., 200°C, for 1-2 hours in order to harden.

The submount 130 can then be scribed and singulated to form LEDs 140 as illustrated in Fig. 2E.

[0030] In another embodiment, the growth substrate 102 is not removed until after the wafer is separated into separate dies and mounted to the submount 130, as illustrated in Figs. 5A, 5B, and 5C. As shown in Fig. 5A, the sapphire substrate 102 with LED GaN layers 104 are scribed and separated into individual dies 150. The scribing and separation may be accomplished using, e.g., a saw that cuts through the sapphire substrate 102 using areas 122 in the underfill 120 as a guide. The separate dies 150 are then mounted to the submount 130, as described above. Once the dies 150 are mounted to the submount 130, the sapphire substrate 102 can be lifted-off described above and as illustrated in Fig. 5B. The submount 130 is then singulated to form LEDs 140, as illustrated in Fig. 5C.

[0031] In another embodiment, the underfill may be deposited on the submount instead of the GaN layers. Figs. 6A-6E are simplified cross-sectional views of a process of mounting GaN LEDs to a submount with an underfill coating.

[0032] Fig. 6A illustrates a portion of a submount 202 with bonding metal patterns 204 with bumps 206. By way of example, a silicon submount 202 with Au bonding metal patterns 204 and Au bumps 206 may be used. Alternatively, other materials may be used if desired. An underfill layer 210 is deposited over submount 202, bonding metal patterns 204 and bumps 206. As discussed above, the underfill layer 210 may be patterned, e.g., using stencil printing or mesh screen-printing, so that areas, such as area where the LED dies are to be separated, have no underfill material. Because the underfill 210 is applied prior to bonding LEDs to the submount, any suitable material may be used for the underfill 210 without depending on the flow characteristics that are needed in the case of traditional underfill. For example, a polymer polyimide based materials, which have high glass transition temperature, may be used as the underfill layer 210. Such materials will help the device withstand high temperature/high current condition without deformation of thin LEDs. The underfill material should have B-stage cure properties in order to adhere to both LED and support wafer surfaces. Moreover, an inorganic dielectric material may be used if desired. As illustrated in Fig. 6B, the underfill layer 210 is polished back until the metal connection, i.e., bumps 206, are exposed.

[0033] A growth substrate 230 with an LED GaN layer 232 and contacts 234 is separated into separate LED dies 235, which are then mounted on the submount 202 with underfill layer 210 as illustrated in Fig. 6C. The contacts on the LED dies 234 are ultrasonically or thermosonically welded directly to corresponding the bonding bumps 206 on the submount 130, as described above. Once mounted, the growth substrate 230 is removed, e.g., using a laser lift-off process, resulting in the structure illustrated shown in Fig. 6D. The submount 202 is then singulated to form LEDs 240, as illustrated in Fig. 6E.

[0034] Figs. 7A-7D illustrate wafer level LEDs with a patterned underfill layer that are mounted to a submount in accordance with another embodiment.

[0035] Fig. 7A is a simplified cross-sectional view of portions of wafer level LEDs 300 with a patterned underfill layer 310 and Fig. 7B is a plan view of the bottom surface of the wafer level LEDs 300 along line AA shown in Fig. 7A. The wafer level LEDs 300 include a growth substrate 302 along with LED layers 304 and contacts 306. The underfill layer 310 is deposited, e.g., using stencil printing or mesh screen-printing to form a pattern that exposes the contacts 306 on the bottom surface of the LED layers 304 and cured. The underfill pattern matches the pattern of contacts 322 that are present on the submount 320, as can be seen in Fig. 7C so that only the areas where the LEDs will be attached are exposed.

[0036] As illustrated in Figs. 7C and 7D, the wafer level LEDs 300 are mounted at the wafer level with a submount 320 with contacts 322. The waver level LEDs 300 are mounted to the submount 320, e.g. ultrasonically or thermosonically, to bond the contacts 306 on the LED layers 304 with the contacts 322 on the submount 320, as described above. The growth substrate 302 can then be lift-off, e.g., using a laser lift-off process, and the LEDs singulated into individual dies.

[0037] Figs. 8A-8G illustrate another embodiment in which individual LED dies are mounted to a submount on which an underfill layer has been deposited. Fig. 8A is a simplified cross-sectional view of portions of a submount 402 with contacts 404. Fig. 8B is a plan view of the top surface of the submount 402 along line BB shown in Fig. 8A. As illustrated in Fig. 8C, an underfill layer 410 is deposited over the submount 402 and in particular is patterned to cover the contacts 404. Once the underfill layer 410 cures, the underfill layer 410 is polished back to

expose the contacts 404, as illustrated in Fig. 8D and Fig.8E, which illustrates another plan view of the submount 402.

[0038] LED dies 420, each of which includes a growth substrate 422, LED layers 424 and contacts 426 on the bottom surface of the LED layers 424 are then individually mounted to the submount 402, as illustrated in Fig. 8F. Once mounted, the growth substrate 422 can be lifted off, as illustrated in Fig. 8G, and the submount 402 can be singulated to form individual LED elements as described above.

[0039] Although the present invention is illustrated in connection with specific embodiments for instructional purposes, the present invention is not limited thereto. Various adaptations and modifications may be made without departing from the scope of the invention. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description.

CLAIMS

What is claimed is:

1. A method of fabricating a light emitting diode (LED) structure comprising:

forming LED layers including an n-type layer, an active layer, and a p-type layer over a growth substrate;

forming metal contacts on a bottom surface of the LED layers;

providing a submount having metal contacts on a top surface;

depositing an underfill layer on the bottom surface of the LED layers;

removing the growth substrate from the LED layers; and

mounting the LED layers to the submount with the metal contacts on the bottom surface of the LED layers in contact with the metal contacts on the top surface of the submount and the underfill layer between the bottom surface of the LED layers and the top surface of the submount.

2. The method of Claim 1, further comprising separating the LED layers into individual dies before mounting the LED layers to the submount.

3. The method of Claim 1, further comprising singulating the LED layers mounted to the submount to form a plurality of individual elements.

4. The method of Claim 1, wherein depositing an underfill layer on the bottom surface of the LED layers comprises depositing the underfill layer over the metal contacts on the bottom surface of the LED layers and polishing the underfill layer back until at least a portion of the metal contacts on the bottom surface of the LED layers are exposed.

5. The method of Claim 1, wherein the underfill layer comprises a polyimide based material.

6. A method of fabricating a light emitting diode (LED) structure comprising:

forming LED layers including an n-type layer, an active layer, and a p-type layer over a growth substrate;

forming metal contacts on a bottom surface of the LED layers;

providing a submount having metal contacts on a top surface;

depositing a patterned underfill layer on at least one of the bottom surface of the LED layers and the top surface of the submount; and

mounting the LED layers to the submount with the metal contacts on the bottom surface of the LED layers in contact with the metal contacts on the top surface of the submount and the underfill layer between the bottom surface of the LED layers and the top surface of the submount.

7. The method of Claim 6, wherein the underfill layer is deposited using one of stencil printing and mesh screen printing to pattern the underfill layer.

8. The method of Claim 6, wherein the underfill layer is deposited on the bottom surface of the LED layers, the method further comprising removing the growth substrate from the LED layers prior to mounting the LED layers to the submount.

9. The method of Claim 6, wherein the underfill layer comprises a polyimide based material.

10. A method of fabricating a light emitting diode (LED) structure comprising:

forming LED layers including an n-type layer, an active layer, and a p-type layer over a growth substrate;

forming metal contacts on a bottom surface of the LED layers;

providing a submount having metal contacts on a top surface;

depositing an underfill layer over at least one of the bottom surface of the LED layers and the top surface of the submount, the underfill layer covering the metal contacts associated with the at least one of the bottom surface of the LED layers and the top surface of the submount;

polishing the underfill layer back until at least a portion of the covered metal contacts are exposed;

mounting the LED layers to the submount with the metal contacts on the bottom surface of the LED layers in contact with the metal contacts on the top surface of the submount and the underfill layer between the bottom surface of the LED layers and the top surface of the submount.

11. The method of Claim 10, wherein the underfill layer is deposited on the bottom surface of the LED layers, the method further comprising removing the growth substrate from the LED layers prior to mounting the LED layers to the submount.

12. The method of Claim 10, further comprising separating the LED layers into individual dies before mounting the LED layers to the submount.

13. The method of Claim 10, further comprising singulating the LED layers mounted to the submount to form a plurality of individual elements.

14. The method of Claim 10, wherein depositing an underfill layer on the bottom surface of the LED layers comprises patterning the underfill layer on the bottom surface of the LED layers.

15. The method of Claim 14, wherein the underfill layer is deposited using one of stencil printing and mesh screen printing to pattern the underfill layer.

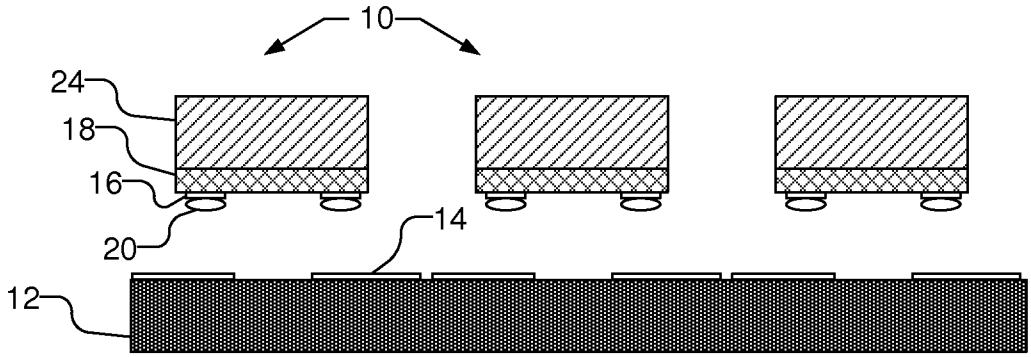

Fig. 1A

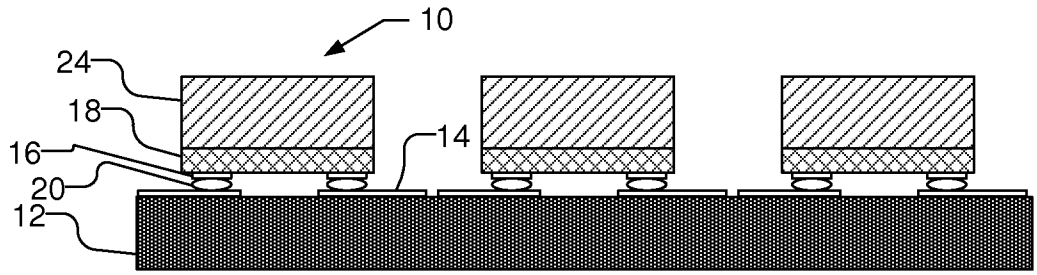

Fig. 1B

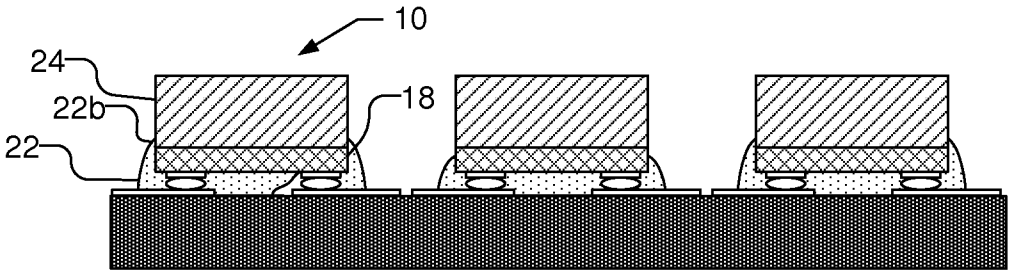

Fig. 1C

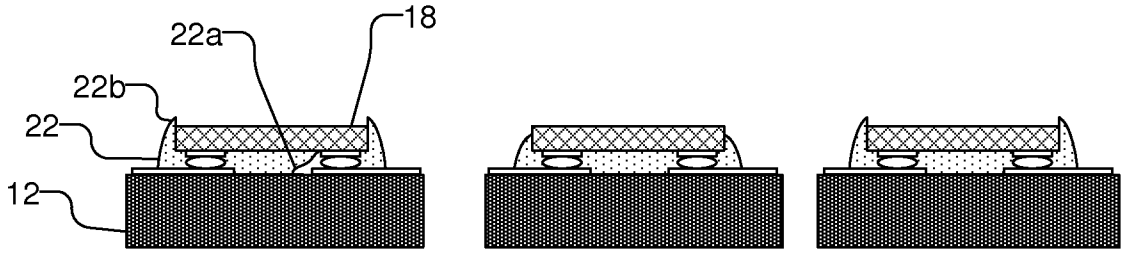

Fig. 1D

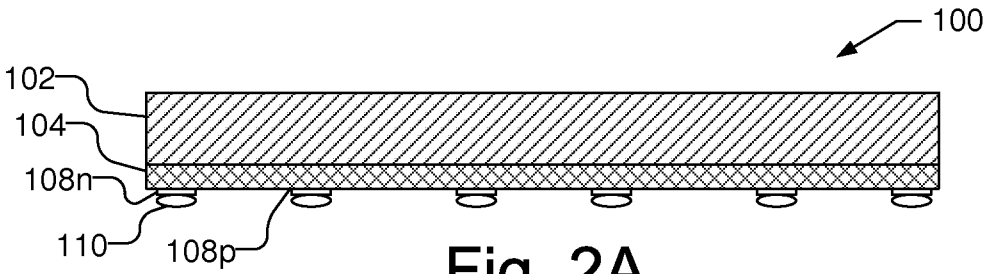

Fig. 2A

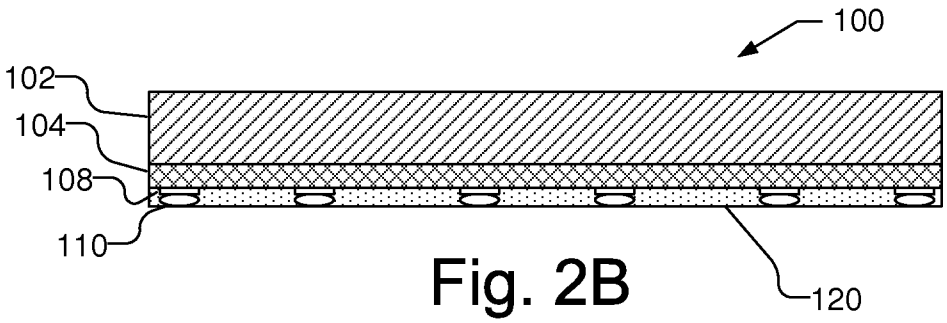

Fig. 2B

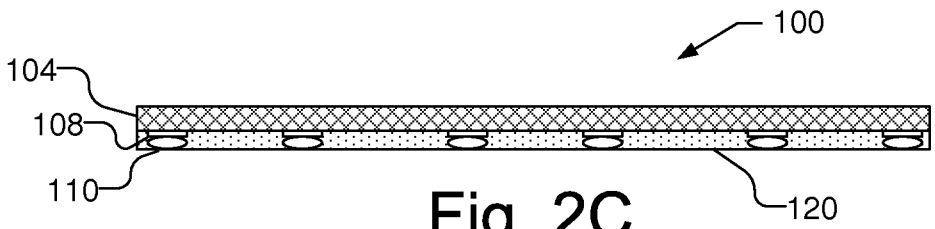

Fig. 2C

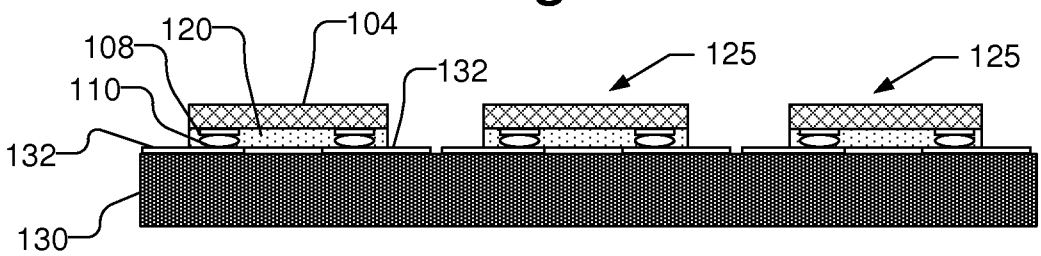

Fig. 2D

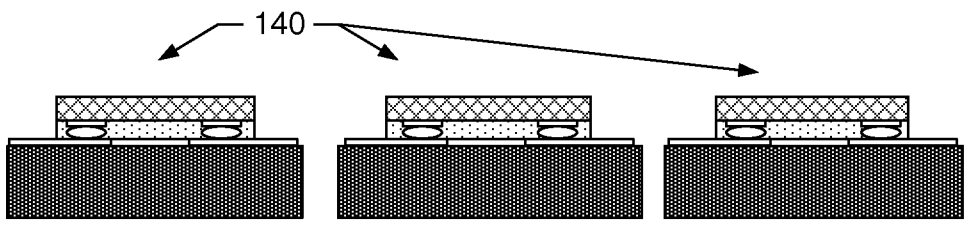

Fig. 2E

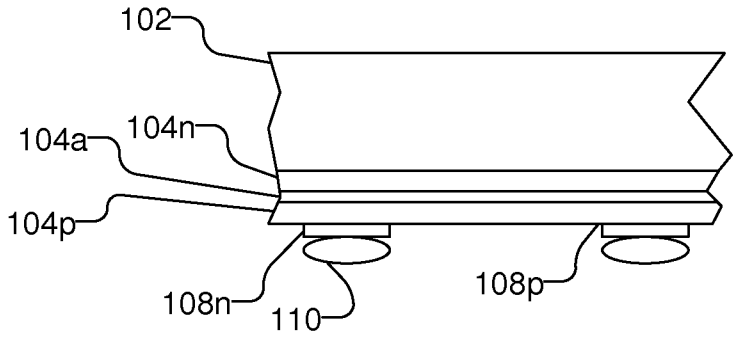

Fig. 3

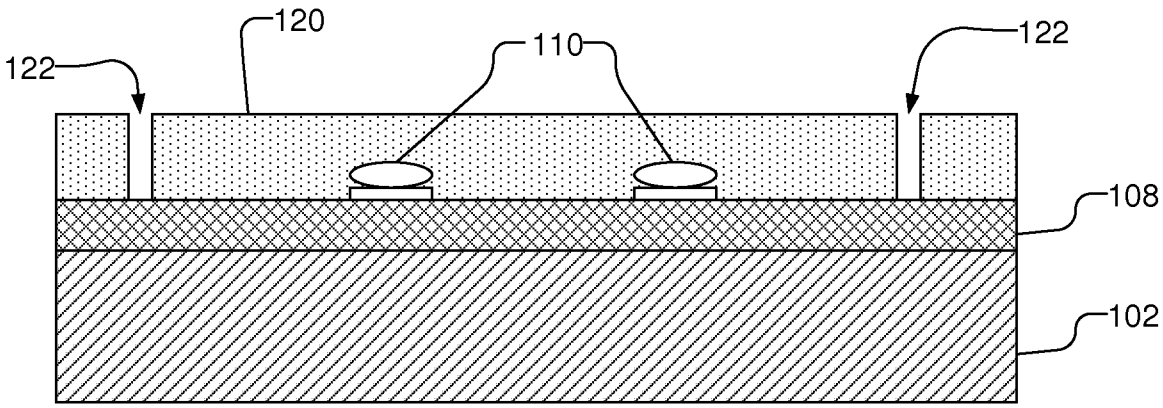

Fig. 4A

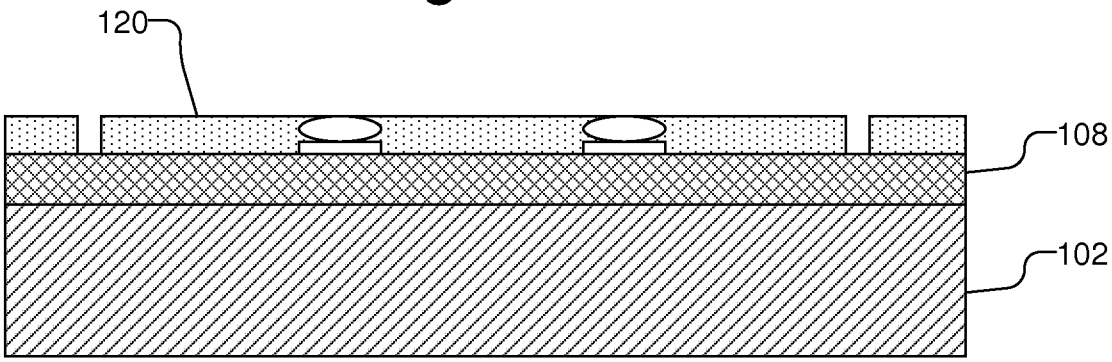

Fig. 4B

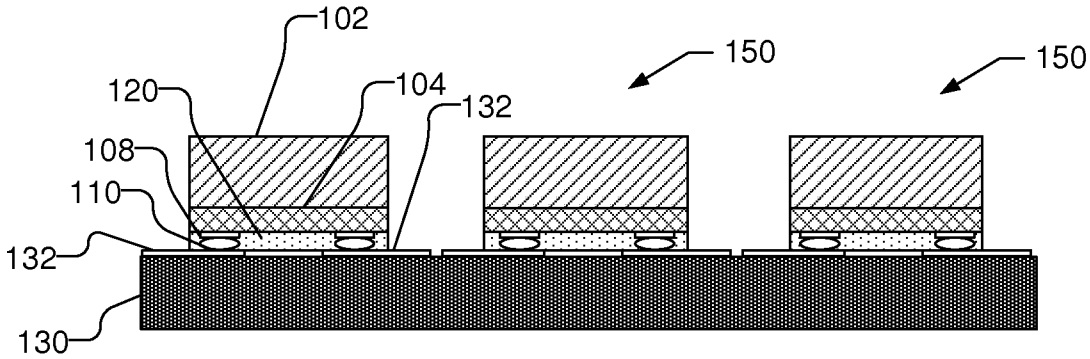

Fig. 5A

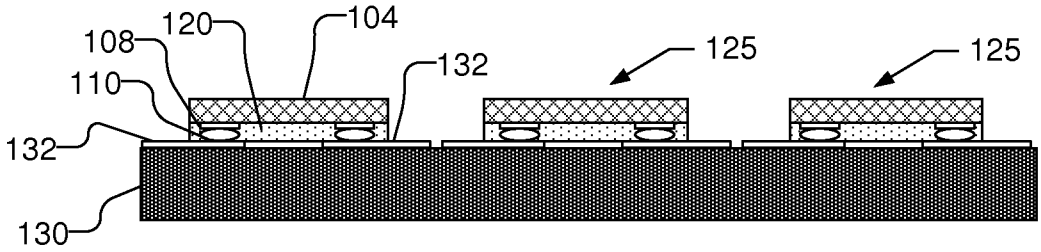

Fig. 5B

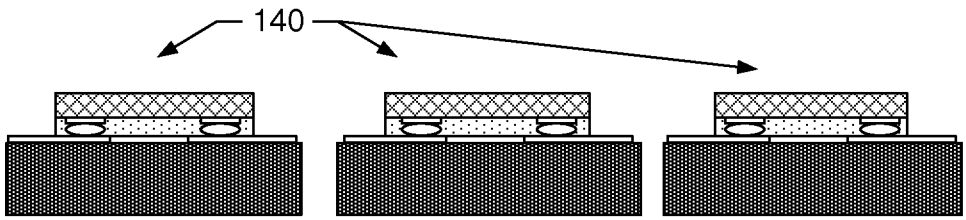

Fig. 5C

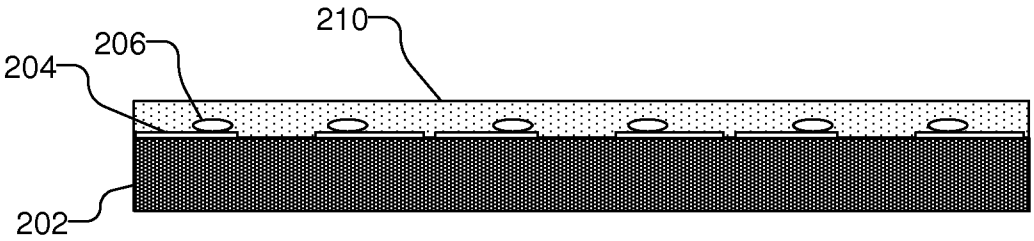

Fig. 6A

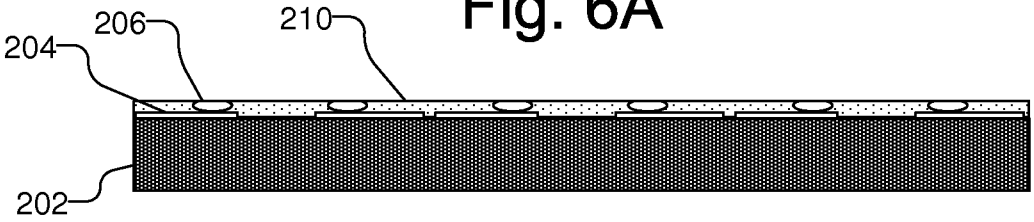

Fig. 6B

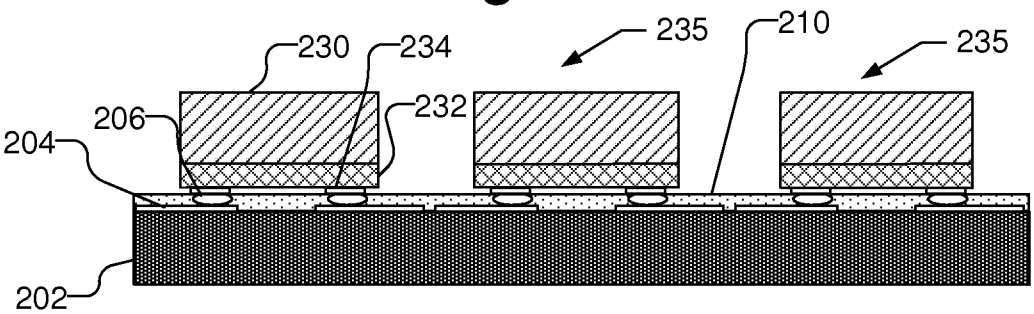

Fig. 6C

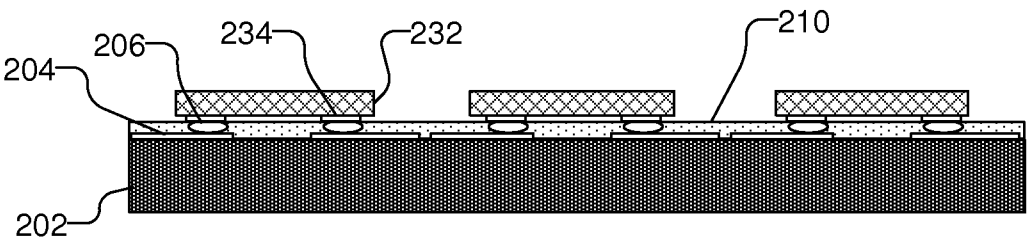

Fig. 6D

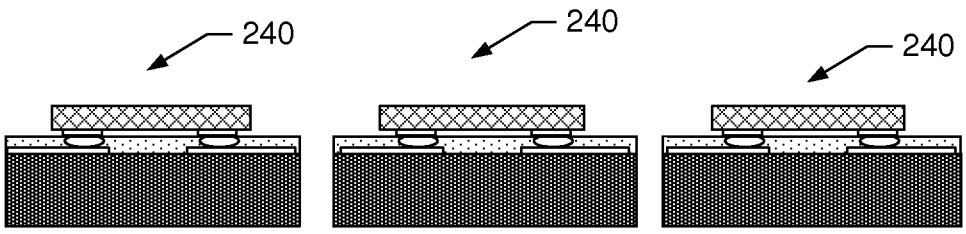

Fig. 6E

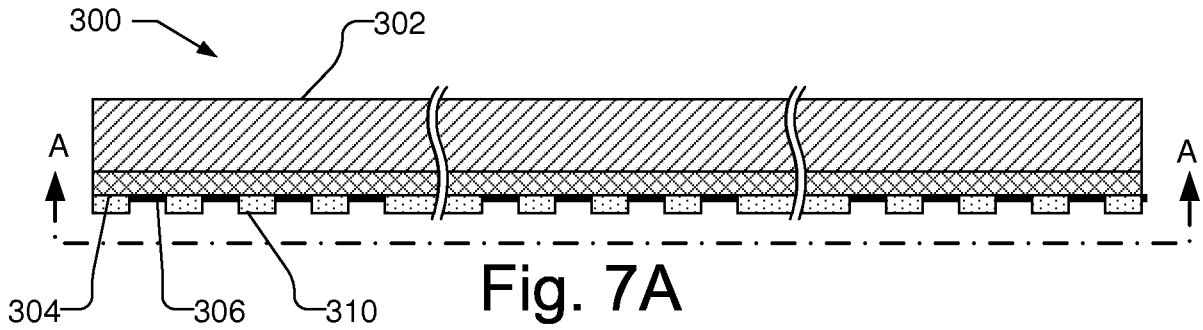

Fig. 7A

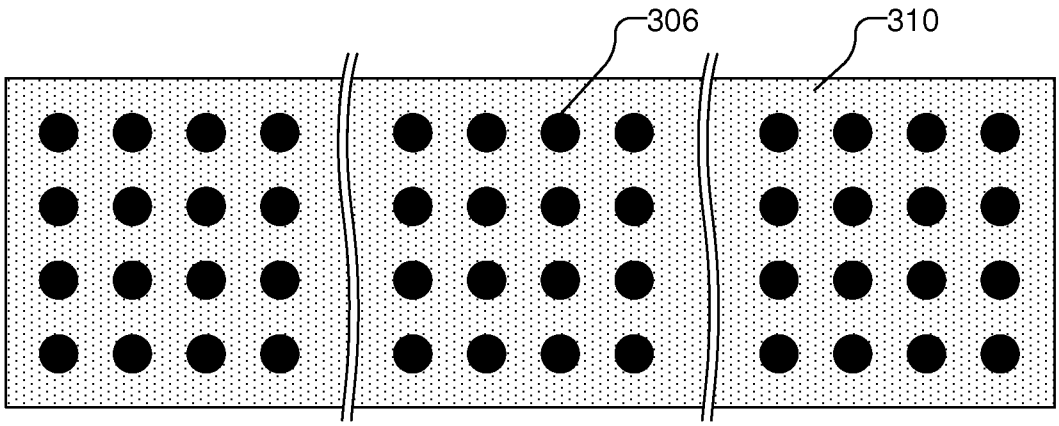

Fig. 7B

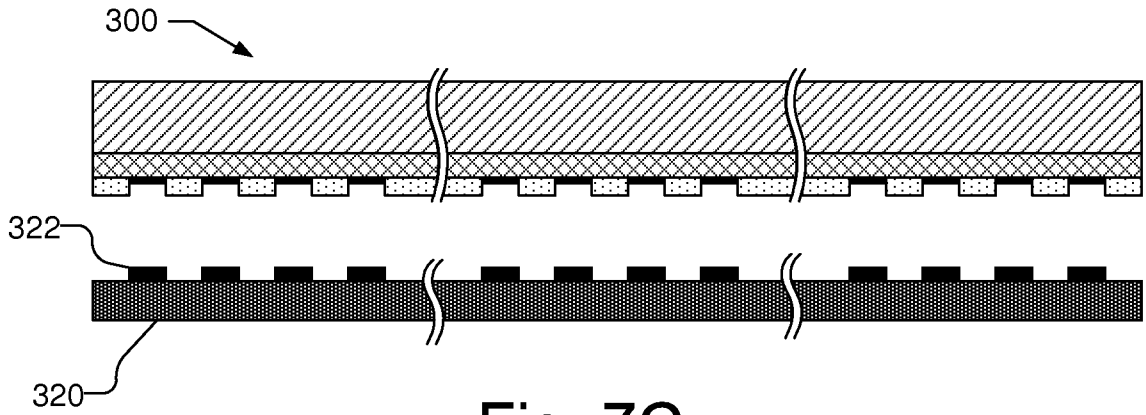

Fig. 7C

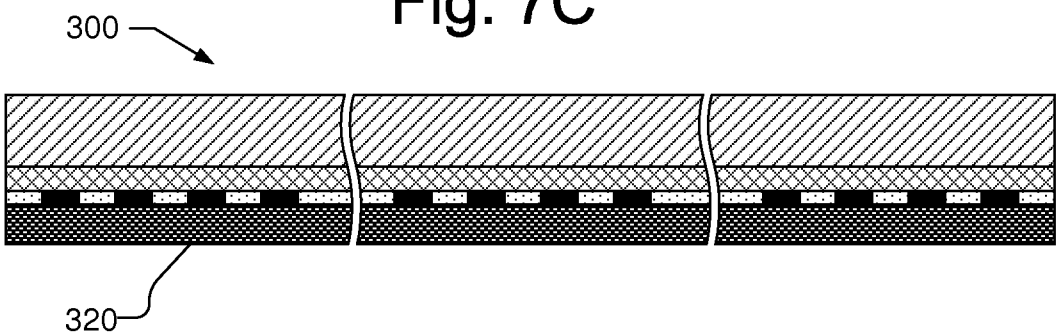

Fig. 7D

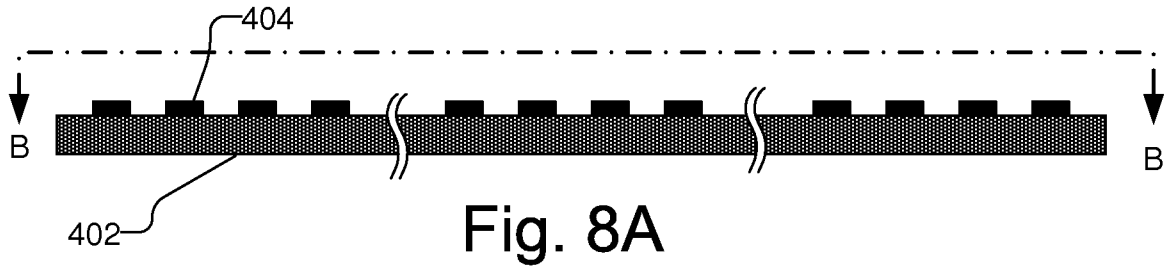

Fig. 8A

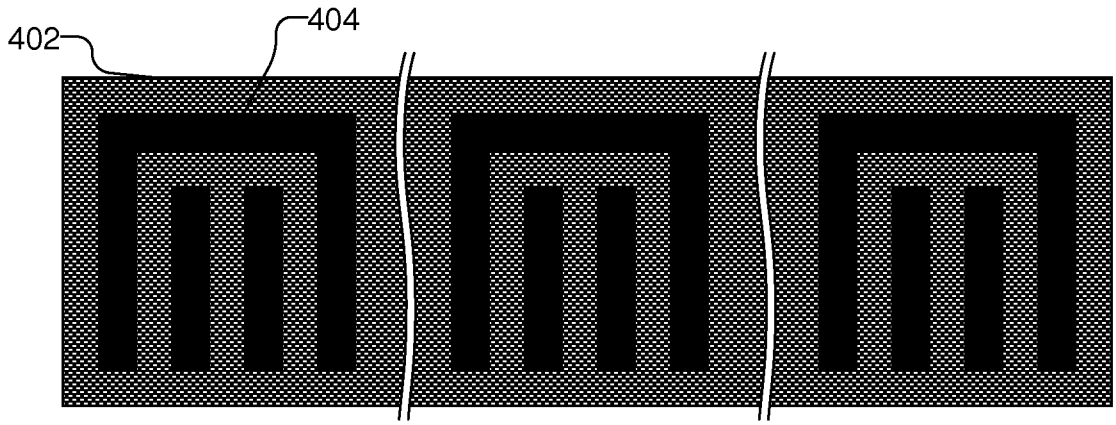

Fig. 8B

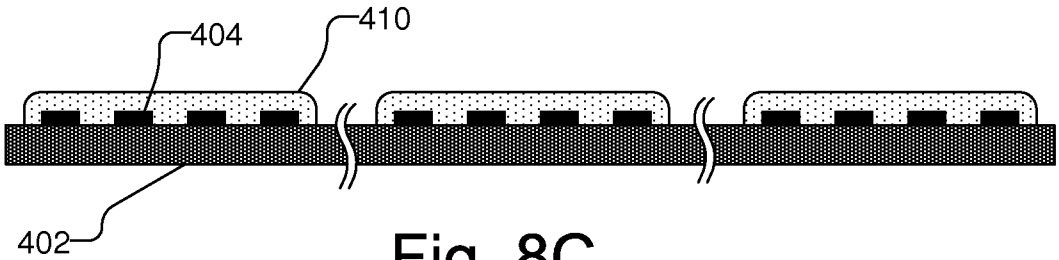

Fig. 8C

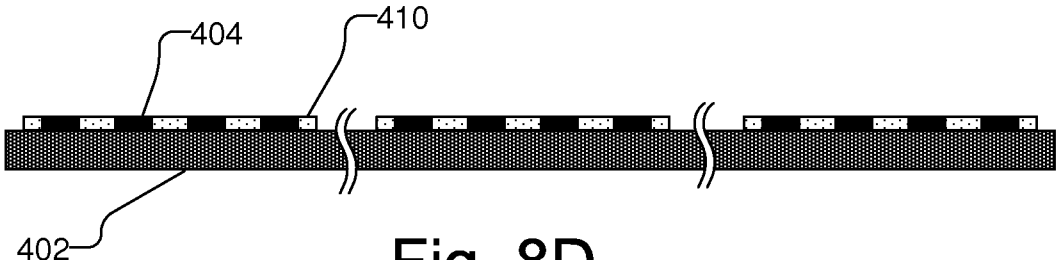

Fig. 8D

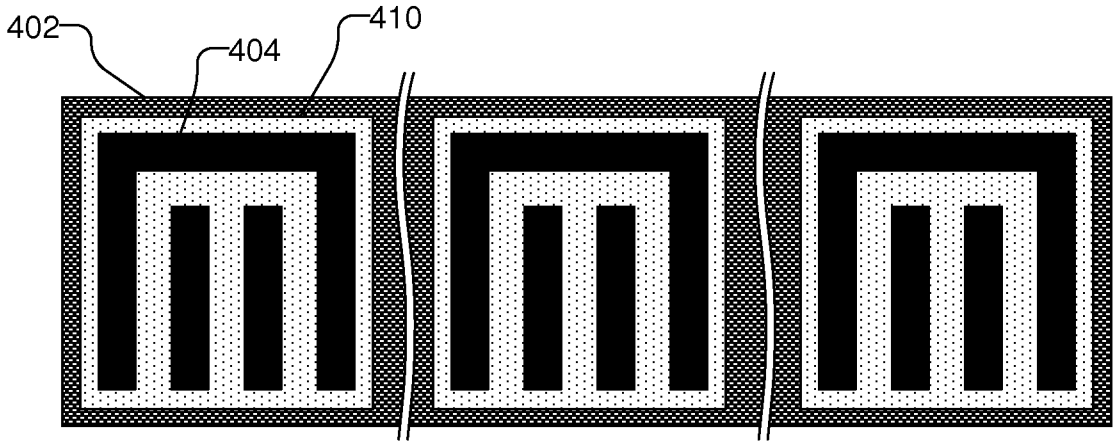

Fig. 8E

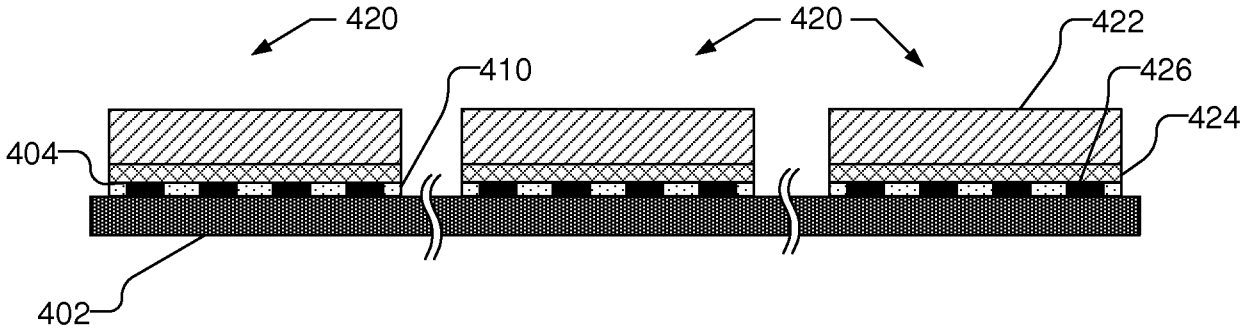

Fig. 8F

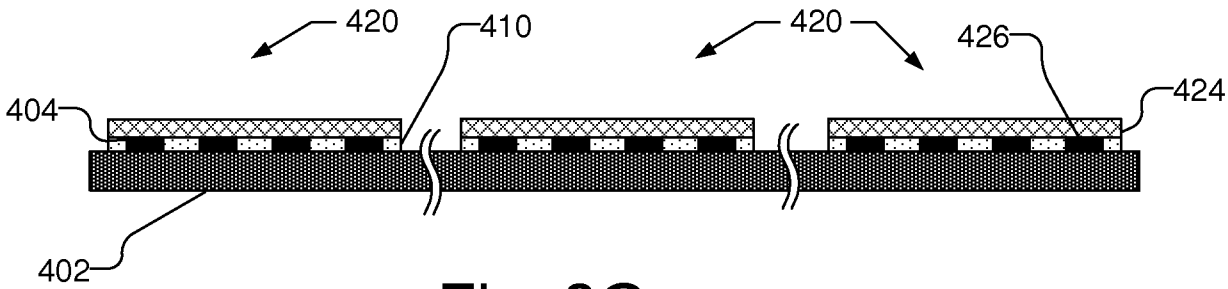

Fig. 8G

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/052681

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2006/131843 A (KONINKL PHILIPS ET AL) 14 December 2006 (2006-12-14) page 6, line 7 - page 8, line 3	1-15
X	WO 2005/062905 A (GELCORE) 14 July 2005 (2005-07-14) page 9, line 23 - page 15, line 18	1-15
X	US 2006/043402 A1 (SUEHIRO Y ET AL) 2 March 2006 (2006-03-02) paragraphs [0052] - [0057]	1-15
X	EP 1 653 523 A (LUMILEDS LIGHTING) 3 May 2006 (2006-05-03) paragraph [0050]	1-15

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 November 2008	25/11/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	van der Linden, J

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/052681

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/161779 A1 (PENG H ET AL) 28 July 2005 (2005-07-28) paragraphs [0060] - [0091] -----	1-15
X	WO 2007/009042 A (GELCORE) 18 January 2007 (2007-01-18) paragraphs [0013] - [0031] -----	1-15
X	WO 01/47039 A (LUMILEDS LIGHTING) 28 June 2001 (2001-06-28) page 21 -----	6,9
P,X	WO 2008/007235 A (KONINKL PHILIPS ET AL) 17 January 2008 (2008-01-17) page 7, line 28 - page 8, line 11 -----	1-15
P,X	WO 2008/038249 A (KONINKL PHILIPS ET AL) 3 April 2008 (2008-04-03) page 5, line 14 - page 11 -----	1-15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2008/052681

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2006131843 A	14-12-2006	CN 101194373 A	04-06-2008
		EP 1894255 A2	05-03-2008
		JP 2006344971 A	21-12-2006
		US 2006281203 A1	14-12-2006
WO 2005062905 A	14-07-2005	CN 1918691 A	21-02-2007
		EP 1706893 A2	04-10-2006
		JP 2007517404 T	28-06-2007
		US 2008113460 A1	15-05-2008
US 2006043402 A1	02-03-2006	DE 102005041095 A1	11-05-2006
		JP 2006100787 A	13-04-2006
EP 1653523 A	03-05-2006	JP 2006128710 A	18-05-2006
		US 2006240585 A1	26-10-2006
		US 2006091409 A1	04-05-2006
US 2005161779 A1	28-07-2005	CN 1619844 A	25-05-2005
WO 2007009042 A	18-01-2007	DE 112006001835 T5	15-05-2008
		EP 1905104 A1	02-04-2008
WO 0147039 A	28-06-2001	AU 2738901 A	03-07-2001
		EP 1161772 A1	12-12-2001
		JP 2001237458 A	31-08-2001
		US 6514782 B1	04-02-2003
		US 6573537 B1	03-06-2003
WO 2008007235 A	17-01-2008	JP 2007335879 A	27-12-2007
		US 2007284607 A1	13-12-2007
WO 2008038249 A	03-04-2008	JP 2008085356 A	10-04-2008
		US 2008081397 A1	03-04-2008