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(54) Title: MICROPROCESSOR CONTROLLED CLASS E DRIVER

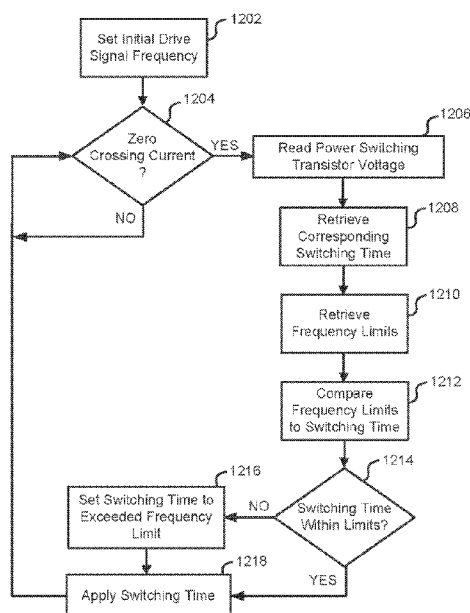


FIG. 12

(57) Abstract: A charger including a class E power driver, a frequency-shift
keying ("FSK") module, and a processor. The processor can receive data re-
lating to the operation of the class E power driver and can control the class E
power driver based on the received data relating to the operation of the class
E power driver. The processor can additionally control the FSK module to
modulate the natural frequency of the class E power transformer to thereby
allow the simultaneous recharging of an implantable device and the trans-
mission of data to the implantable device. The processor can additionally
compensate for propagation delays by adjusting switching times.



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MICROPROCESSOR CONTROLLED CLASS E DRIVER

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CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 61/859,471 entitled "MICROPROCESSOR CONTROLLED CLASS E DRIVER," and filed on July 29, 2013, the entirety of which is hereby incorporated by reference herein.

10

BACKGROUND OF THE INVENTION

[0002] The prevalence of use of medical devices in treating ailments is increasing with time. In many instances, and as these medical devices are made smaller, these medical devices are frequently implanted within a patient. While the desirability of implantable devices is increasing as the size of the devices has decreased, the implantation process still frequently requires complicated surgery which can expose the patient to significant risks and protracted recovery times. In light of this, further methods, systems, and devices are desired to increase the ease of implantation of medical devices, and the ease of use of such implanted medical devices.

20

BRIEF SUMMARY OF THE INVENTION

[0003] One aspect of the present disclosure relates to a charger. The charger includes a charging coil, which charging coil is configured to magnetically couple with an implantable device to recharge the implantable device, a class E driver electrically connected to the charging coil, which class E driver includes a switching circuit that is switched by the application of a first voltage to the switching circuit, and a current sensor positioned to sense a current passing through the charging coil. The charger can include a processor electrically connected to the class E driver to receive data indicative of the current passing through the charging coil and electrically connected to the class E driver to control the switching circuit via the application of the first voltage to the switching circuit. In some embodiments, the processor can receive data indicative of the current passing through the charging coil and control the switching circuit in response to the received data.

[0004] In some embodiments, the switching circuit can be a transistor. In some embodiments, the transistor can be a MOSFET. In some embodiments, the processor is electrically connected to the class E driver to receive data indicative of a second voltage of the switching circuit. In some embodiments, the processor can receive data indicative of the second voltage of the switching circuit, and control the switching circuit in response to the received data indicative of the second voltage of the switching circuit.

[0005] In some embodiments, the second voltage is measured at the drain of the switching circuit and the first voltage is applied to the gate of the switching circuit. In some embodiments, the processor is electrically connected to the class E driver via a voltage divider including a first resistor and a second resistor. In some embodiments, the processor can sense a power switching transistor voltage, and determine whether to adjust a first frequency with which the first voltage is applied to the switching circuit, which adjustment of the first frequency mitigates one or several propagation delays.

[0006] In some embodiments, the processor can retrieve a stored value identifying a second frequency with which the first voltage is applied based on the sensed power switching transistor voltage. In some embodiments, the processor can compare the retrieved stored value identifying the second frequency with which the first voltage is applied to one or several frequency limits. In some embodiments, the first frequency is set to the second frequency if the second frequency does not exceed the one or several frequency limits. In some embodiments, when the second frequency exceeds one of the one or several frequency limits, the first frequency is set to the exceeded one of the one or several frequency limits.

[0007] One aspect of the present disclosure relates to a charger. The charger includes a charging coil that can generate a magnetic field having a frequency and can magnetically couple with an implantable device to recharge the implantable device, a class E driver electrically connected to the charging coil, and an FSK module that can modulate the frequency of the magnetic field among at least three frequencies.

[0008] In some embodiments, the at least three frequencies include a first frequency, a second frequency, and a third frequency. In some embodiments, the third frequency is the highest frequency and the second frequency is the lowest frequency. In some embodiments, the charger includes a processor electrically connected to the FSK module and that can control the FSK module. In some embodiments, the processor can selectively operate the charger in either a data non-transmitting state or in a data transmitting state.

[0009] In some embodiments, a carrier signal has the first frequency when the charger operates in the data non-transmitting state. In some embodiments, the processor controls the FSK module to modulate the carrier signal between the second frequency and the third frequency when the charger operates in the data transmitting state.

5 [0010] In some embodiments, the FSK module includes two capacitors and two transistors. In some embodiments, the two capacitors and the two transistors of the FSK module are electrically connected such that the two capacitors can be selectively included within the circuit by the FSK module. In some embodiments, the processor can control the two transistors of the FSK module to selectively include the two capacitors within the circuit by
10 the FSK module. In some embodiments, the selective inclusion of the two capacitors within the circuit of the FSK modulates the frequency of the magnetic field between the first, second, and third frequencies.

[0011] One aspect of the present disclosure relates to a method of communicating with an implantable device during charging of the implantable device. The method includes
15 generating a charging signal with a charging coil, which charging signal has an initial, first frequency, and transmitting data by modulating the frequency of the charging signal between a second frequency that is lower than the first frequency and a third frequency that is higher than the first frequency.

[0012] In some embodiments, the method can include generating transmission data, which
20 can be the data that is transmitted. In some embodiments, the transmission data can be in binary format. In some embodiments, modulating the frequency of the charging signal between the second frequency and the third frequency transmits the transmission data in binary format.

[0013] In some embodiments, the frequency of the charging signal is modulated by an FSK
25 module. In some embodiments, the FSK module can include two capacitors and two transistors. In some embodiments, the two capacitors and the two transistors of the FSK module are electrically connected such that the two capacitors can be selectively included within the circuit of by the FSK module to thereby modulate the frequency of the charging signal.

30 [0014] One aspect of the present disclosure relates to a method of controlling a charger. The method includes creating a magnetic coupling between a charger and an implantable

device, which magnetic coupling charges the implantable device, setting an initial frequency of a drive signal, which frequency of the drive signal is set by a processor, and which drive signal controls the opening and closing of a switch, sensing a voltage at the switch at a first time, based on the voltage at the switch at the first time, retrieving a value identifying a
5 second frequency, and changing the frequency of the drive signal.

[0015] In some embodiments, changing the frequency of the drive signal can include changing the frequency of the drive signal from the first frequency to the second frequency.

In some embodiments, the method can include retrieving one or several frequency limits, which frequency limits provide an upper and lower bound to a range of acceptable

10 frequencies of the drive signal. In some embodiments, the method can include comparing the second frequency to the one or several frequency limits.

[0016] In some embodiments, changing the frequency of the drive signal can include changing the frequency of the drive signal from the first frequency to the one of the one or several frequency limits if the second frequency exceeds the one of the one or several

15 frequency limits. In some embodiments, changing the frequency of the drive signal can include changing the frequency of the drive signal from the first frequency to the second frequency if the second frequency does not exceed the one or several frequency limits. In some embodiments, changing of the frequency of the drive signal can mitigate an effect of a propagation delay. In some embodiments, the frequency of the drive signal can be adjusted
20 multiple times to mitigate the effect of the propagation delay.

[0017] Further areas of applicability of the present disclosure will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating various embodiments, are intended for purposes of illustration only and are not intended to necessarily limit the scope of the
25 disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Figure 1 is a schematic illustration of one embodiment of an implantable neurostimulation system.

[0019] Figure 2 is a schematic illustration of one embodiment of interconnectivity of the
30 implantable neurostimulation system.

[0020] Figure 3 is a schematic illustration of one embodiment of the architecture of the external pulse generator and/or of the implantable pulse generator that is a part of the implantable neurostimulation system.

5 [0021] Figure 4 is a schematic illustration of one embodiment of the charger that is a part of the implantable neurostimulation system.

[0022] Figure 5 is a functional block diagram of one embodiment of a charging circuit.

[0023] Figure 6 is schematic illustration of one embodiment of a charging circuit.

[0024] Figure 7 is a graphical illustration of one embodiment of a transition from a charging mode to a simultaneous charging/data transmission mode.

10 [0025] Figure 8 is a chart illustrating one embodiment of measurements from the charging circuit.

[0026] Figure 9 is a chart illustrating one embodiment of measurements from the charging circuit when the switching time is properly tuned.

15 [0027] Figure 10 chart illustrating one embodiment of measurements from the charging circuit when the switching time is too slow.

[0028] Figure 11 is a chart illustrating one embodiment of measurements from the charging circuit when the switching time is too fast.

[0029] Figure 12 is a flowchart illustrating one embodiment of a process for controlling the switching time of a charging circuit.

20 [0030] In the appended figures, similar components and/or features may have the same reference label. Where the reference label is used in the specification, the description is applicable to any one of the similar components having the same reference label.

DETAILED DESCRIPTION OF THE INVENTION

25 [0031] A significant percentage of the Western (EU and US) population is affected by Neuropathic pain (chronic intractable pain due to nerve damage). In many people, this pain is severe. There are thousands of patients that have chronic intractable pain involving a nerve. Neuropathic pain can be very difficult to treat with only half of patients achieving partial relief. Thus, determining the best treatment for individual patients remains challenging.

Conventional treatments include certain antidepressants, anti-epileptic drugs and opioids. However, side effects from these drugs can be detrimental. In some of these cases, electrical stimulation can provide effective treatment of this pain without the drug-related side effects.

[0032] A spinal cord stimulator is a device used to deliver pulsed electrical signals to the spinal cord to control chronic pain. Because electrical stimulation is a purely electrical treatment and does not cause side effects similar to those caused by drugs, an increasing number of physicians and patients favor the use of electrical stimulation over drugs as a treatment for pain. The exact mechanisms of pain relief by spinal cord stimulation (SCS) are unknown. Early SCS trials were based on the Gate Control Theory, which posits that pain is transmitted by two kinds of afferent nerve fibers. One is the larger myelinated A δ fiber, which carries quick, intense-pain messages. The other is the smaller, unmyelinated "C" fiber, which transmits throbbing, chronic pain messages. A third type of nerve fiber, called A β , is "non-nociceptive," meaning it does not transmit pain stimuli. The gate control theory asserts that signals transmitted by the A δ and C pain fibers can be thwarted by the activation/stimulation of the non-nociceptive A β fibers and thus inhibit an individual's perception of pain. Thus, neurostimulation provides pain relief by blocking the pain messages before they reach the brain.

[0033] SCS is often used in the treatment of failed back surgery syndrome, a chronic pain syndrome that has refractory pain due to ischemia. SCS complications have been reported in a large portion, possibly 30% to 40%, of all SCS patients. This increases the overall costs of patient pain management and decreases the efficacy of SCS. Common complications include: infection, hemorrhaging, injury of nerve tissue, placing device into the wrong compartment, hardware malfunction, lead migration, lead breakage, lead disconnection, lead erosion, pain at the implant site, generator overheating, and charger overheating. The occurrence rates of common complications are surprisingly high: including lead extension connection issues, lead breakage, lead migration and infection.

[0034] Peripheral neuropathy, another condition that can be treated with electrical stimulation, may be either inherited or acquired. Causes of acquired peripheral neuropathy include physical injury (trauma) to a nerve, viruses, tumors, toxins, autoimmune responses, nutritional deficiencies, alcoholism, diabetes, and vascular and metabolic disorders. Acquired peripheral neuropathies are grouped into three broad categories: those caused by systemic disease, those caused by trauma, and those caused by infections or autoimmune disorders

affecting nerve tissue. One example of an acquired peripheral neuropathy is trigeminal neuralgia, in which damage to the trigeminal nerve (the large nerve of the head and face) causes episodic attacks of excruciating, lightning-like pain on one side of the face.

[0035] A high percentage of patients with peripheral neuropathic pain do not benefit from SCS for various reasons. However, many of these patients can receive acceptable levels of pain relief via direct electrical stimulation to the corresponding peripheral nerves. This therapy is called peripheral nerve stimulation (PNS). As FDA approved PNS devices have not been commercially available in the US market, Standard spinal cord stimulator (SCS) devices are often used off label by pain physicians to treat this condition. A significant portion of SCS devices that have been sold may have been used off-label for PNS.

[0036] As current commercially-available SCS systems were designed for stimulating the spinal cord and not for peripheral nerve stimulation, there are more device complications associated with the use of SCS systems for PNS than for SCS. Current SCS devices (generators) are large and bulky. In the event that an SCS is used for PNS, the SCS generator is typically implanted in the abdomen or in the lower back above the buttocks and long leads are tunneled across multiple joints to reach the target peripheral nerves in the arms, legs or face. The excessive tunneling and the crossing of joints leads to increased post-surgical pain and higher device failure rates. Additionally, rigid leads can lead to skin erosion and penetration, with lead failure rates being far too high within the first few years of implantation. Many or even most complications result in replacement surgery and even multiple replacement surgeries in some cases.

[0037] One embodiment of an implantable neurostimulation system 100 is shown in Figure 1, which implantable neurostimulation system 100 can be, for example, a peripherally-implantable neurostimulation system 100. In some embodiments, the implantable neurostimulation system 100 can be used in treating patients with, for example, chronic, severe, refractory neuropathic pain originating from peripheral nerves. In some embodiments, the implantable neurostimulation system 100 can be used to either stimulate a target peripheral nerve or the posterior epidural space of the spine.

[0038] The implantable neurostimulation system 100 can include one or several pulse generators. The pulse generators can comprise a variety of shapes and sizes, and can be made from a variety of materials. In some embodiments, the one or several pulse generators can generate one or several non-ablative electrical pulses that are delivered to a nerve to control

pain. In some embodiments, these pulses can have a pulse amplitude of between 0-1,000 mA, 0-100 mA, 0-50 mA, 0-25 mA, and/or any other or intermediate range of amplitudes. One or more of the pulse generators can include a processor and/or memory. In some embodiments, the processor can provide instructions to and receive information from the other components of the implantable neurostimulation system 100. The processor can act according to stored instructions, which stored instructions can be located in memory, associated with the processor, and/or in other components of the implantable neurostimulation system 100. The processor can, in accordance with stored instructions, make decisions. The processor can comprise a microprocessor, such as a microprocessor from Intel® or Advanced Micro Devices, Inc.®, or the like.

[0039] In some embodiments, the stored instructions directing the operation of the processor may be implemented by hardware, software, scripting languages, firmware, middleware, microcode, hardware description languages, and/or any combination thereof. When implemented in software, firmware, middleware, scripting language, and/or microcode, the program code or code segments to perform the necessary tasks may be stored in a machine readable medium such as a storage medium. A code segment or machine-executable instruction may represent a procedure, a function, a subprogram, a program, a routine, a subroutine, a module, a software package, a script, a class, or any combination of instructions, data structures, and/or program statements. A code segment may be coupled to another code segment or a hardware circuit by passing and/or receiving information, data, arguments, parameters, and/or memory contents. Information, arguments, parameters, data, etc. may be passed, forwarded, or transmitted via any suitable means including memory sharing, message passing, token passing, network transmission, etc.

[0040] In some embodiments, the memory of one or both of the pulse generators can be the storage medium containing the stored instructions. The memory may represent one or more memories for storing data, including read only memory (ROM), random access memory (RAM), magnetic RAM, core memory, magnetic disk storage mediums, optical storage mediums, flash memory devices and/or other machine readable mediums for storing information. In some embodiments, the memory may be implemented within the processor or external to the processor. In some embodiments, the memory can be any type of long term, short term, volatile, nonvolatile, or other storage medium and is not to be limited to any particular type of memory or number of memories, or type of media upon which memory is stored. In some embodiments, the memory can include, for example, one or both of volatile

and nonvolatile memory. In one specific embodiment, the memory can include a volatile portion such as RAM memory, and a nonvolatile portion such as flash memory.

[0041] In some embodiments, one of the pulse generators can be an external pulse generator 102 or an implantable pulse generator 104. The external pulse generator 102 can be used to evaluate the suitability of a patient for treatment with the implantable neurostimulation system 100 and/or for implantation of an implantable pulse generator 104.

[0042] In some embodiments, one of the pulse generators can be the implantable pulse generator 104, which can be sized and shaped, and made of material to allow implantation of the implantable pulse generator 104 inside of a body. In some embodiments, the implantable pulse generator 104 can be sized and shaped so as to allow placement of the implantable pulse generator 104 at any desired location in a body, and in some embodiments, placed proximate to a peripheral nerve such that leads (discussed below) are not tunneled across joints and/or such that extension cables are not needed.

[0043] The implantable pulse generator 104 can include one or several energy storage features. In some embodiments, these features can be configured to store energy, such as, for example, electric energy, that can be used in the operation of the implantable pulse generator 104. These energy storage features can include, for example, one or several batteries, including rechargeable batteries, one or several capacitors, one or several fuel cells, or the like.

[0044] In some embodiments, the electrical pulses generated by the pulse generator can be delivered to one or several nerves 110 and/or to tissue proximate to one or several nerves 110 via one or several leads. The leads can include conductive portions, such as electrodes or contact portions of electrodes, and non-conductive portions. The leads can have a variety of shapes, can be a variety of sizes, and can be made from a variety of materials, which size, shape, and materials can be dictated by the application or other factors.

[0045] In some embodiments, the leads can include an anodic lead 106 and/or a cathodic lead 108. In some embodiments, the anodic lead 106 and the cathodic lead 108 can be identical leads, but can receive pulses of different polarity from the pulse generator.

[0046] In some embodiments, the leads can connect directly to the pulse generator, and in some embodiments, the leads can be connected to the pulse generator via a connector 112 and a connector cable 114. The connector 112 can comprise any device that is able to electrically

connect the leads to the connector cable 114. Likewise, the connector cable can be any device capable of transmitting distinct electrical pulses to the anodic lead 106 and the cathodic lead 108.

[0047] In some embodiments, the implantable neurostimulation system 100 can include a charger 116 that can be configured to recharge the implantable pulse generator 104 when the implantable pulse generator 104 is implanted within a body. The charger 116 can comprise a variety of shapes, sizes, and features, and can be made from a variety of materials. Like the pulse generators 102, 104, the charger 116 can include a processor and/or memory having similar characteristics to those discussed above. In some embodiments, the charger 116 can recharge the implantable pulse generator 104 via an inductive coupling.

[0048] In some embodiments, one or several properties of the electrical pulses can be controlled via a controller. In some embodiments, these properties can include, for example, the frequency, strength, pattern, duration, or other aspects of the timing and magnitude of the electrical pulses. In one embodiment, these properties can include, for example, a voltage, a current, or the like. In one embodiment, a first electrical pulse can have a first property and a second electrical pulse can have a second property. This control of the electrical pulses can include the creation of one or several electrical pulse programs, plans, or patterns, and in some embodiments, this can include the selection of one or several pre-existing electrical pulse programs, plans, or patterns. In the embodiment depicted in Figure 1, the implantable neurostimulation system 100 includes a controller that is a clinician programmer 118. The clinician programmer 118 can be used to create one or several pulse programs, plans, or patterns and/or to select one or several of the created pulse programs, plans, or patterns. In some embodiments, the clinician programmer 118 can be used to program the operation of the pulse generators including, for example, one or both of the external pulse generator 102 and the implantable pulse generator 104. The clinician programmer 118 can comprise a computing device that can wiredly and/or wirelessly communicate with the pulse generators. In some embodiments, the clinician programmer 118 can be further configured to receive information from the pulse generators indicative of the operation and/or effectiveness of the pulse generators and the leads.

[0049] In some embodiments, the controller of the implantable neurostimulation system 100 can include a patient remote 120. The patient remote 120 can comprise a computing device that can communicate with the pulse generators via a wired or wireless connection.

The patient remote 120 can be used to program the pulse generator, and in some embodiments, the patient remote 120 can include one or several pulse generation programs, plans, or patterns created by the clinician programmer 118. In some embodiments, the patient remote 120 can be used to select one or several of the pre-existing pulse generation programs, plans, or patterns and to select, for example, the duration of the selected one of the one or several pulse generation programs, plans, or patterns.

[0050] Advantageously, the above outlined components of the implantable neurostimulation system 100 can be used to control and provide the generation of electrical pulses to mitigate patient pain.

[0051] With reference now to Figure 2, a schematic illustration of one embodiment of interconnectivity of the implantable neurostimulation system 100 is shown. As seen in Figure 2, several of the components of the implantable neurostimulation system 100 are interconnected via network 110. In some embodiments, the network 110 allows communication between the components of the implantable neurostimulation system 100.

The network 110 can be, for example, a local area network (LAN), a wide area network (WAN), a wired network, a custom network, wireless network, a telephone network such as, for example, a cellphone network, the Internet, the World Wide Web, or any other desired network or combinations of different networks. In some embodiments, the network 110 can use any desired communication and/or network protocols. The network 110 can include any communicative interconnection between two or more components of the implantable neurostimulation system 100. In one embodiment, the communications between the devices of the implantable neurostimulation system 100 can be according to any communication protocol including, for example those covered by Near Field Communication (NFC), Bluetooth, or the like. In some embodiments, different components of the system may utilize different communication networks and/or protocols.

[0052] As will be described in greater detail below, in some embodiments, the charger 116 can directly communicate with the implantable pulse generator 104, without relying on the network 110. This communication is indicated in Figure 2 by line 140. In some embodiments, this communication can be accomplished via integrating data transmission functionality into one or several of the components or systems of one or both the charger 116 and the implantable pulse generator 104, or other implantable device. In one particular embodiment, this can be achieved by, for example, incorporating frequency-shift keying ("FSK")

capability into the charging systems of one or both of the charger 116 and the implantable pulse generator 104. In one such embodiment, charger 116 would generate a carrier frequency during normal recharging. In the event that communication or other data transmission is desired the carrier frequency can be modulated between two or more frequencies to perform the communication or to transmit the data.

[0053] With reference now to Figure 3, a schematic illustration of one embodiment of the architecture of the external pulse generator 102 and/or of the implantable pulse generator 104 is shown. In some embodiments, each of the components of the architecture of the one of the pulse generators 102, 104 can be implemented using the processor, memory, and/or other hardware component of the one of the pulse generators 102, 104. In some embodiments, the components of the architecture of the one of the pulse generators 102, 104 can include software that interacts with the hardware of the one of the pulse generators 102, 104 to achieve a desired outcome.

[0054] In some embodiments, the pulse generator 102/104 can include, for example, a network interface 300, or alternatively, a communication module. The network interface 300, or alternatively, the communication module, can be configured to access the network 110 to allow communication between the pulse generator 102, 104 and the other components of the implantable neurostimulation system 100. In some embodiments, the network interface 300, or alternatively, a communication module, can include one or several antennas and software configured to control the one or several antennas to send information to and receive information from one or several of the other components of the implantable neurostimulation system 100.

[0055] The pulse generator 102, 104 can further include a data module 302. The data module 302 can be configured to manage data relating to the identity and properties of the pulse generator 102, 104. In some embodiments, the data module can include one or several databases that can, for example, include information relating to the pulse generator 102, 104 such as, for example, the identification of the pulse generator, one or several properties of the pulse generator 102, 104, or the like. In one embodiment, the data identifying the pulse generator 102, 104 can include, for example, a serial number of the pulse generator 102, 104 and/or other identifier of the pulse generator 102, 104 including, for example, a unique identifier of the pulse generator 102, 104. In some embodiments, the information associated with the property of the pulse generator 102, 104 can include, for example, data identifying

the function of the pulse generator 102, 104, data identifying the power consumption of the pulse generator 102, 104, data identifying the charge capacity of the pulse generator 102, 104 and/or power storage capacity of the pulse generator 102, 104, data identifying potential and/or maximum rates of charging of the pulse generator 102, 104, and/or the like.

- 5 [0056] The pulse generator 102, 104 can include a pulse control 304. In some embodiments, the pulse control 304 can be configured to control the generation of one or several pulses by the pulse generator 102, 104. In some embodiments, for example, this information can identify one or several pulse patterns, programs, or the like. This information can further specify, for example, the frequency of pulses generated by the pulse generator
10 102, 104, the duration of pulses generated by the pulse generator 102, 104, the strength and/or magnitude of pulses generated by the pulse generator 102, 104, or any other details relating to the creation of one or several pulses by the pulse generator 102, 104. In some embodiments, this information can specify aspects of a pulse pattern and/or pulse program, such as, for example, the duration of the pulse pattern and/or pulse program, and/or the like.
15 In some embodiments, information relating to and/or for controlling the pulse generation of the pulse generator 102, 104 can be stored within the memory.

- [0057] The pulse generator 102, 104 can include a charging module 306. In some embodiments, the charging module 306 can be configured to control and/or monitor the charging/recharging of the pulse generator 102, 104. In some embodiments, for example, the
20 charging module 306 can include one or several features configured to receive energy for recharging the pulse generator 102, 104 such as, for example, one or several inductive coils/features that can interact with one or several inductive coils/features of the charger 116 to create an inductive coupling to thereby recharge the pulse generator 102, 104.

- [0058] In some embodiments, the charging module 306 can include hardware and/or
25 software configured to monitor the charging of the pulse generator 102, 104. In some embodiments, the hardware can include, for example, a charging coil, which can be, for example, a receiving coil, configured to magnetically couple with a charging coil of the charger 116. In some embodiments, the pulse generator 102, 104 can be configured to receive and/or send data via FSK during charging of the pulse generator 102, 104.

- 30 [0059] The pulse generator 102, 104 can include an energy storage device 308. The energy storage device 308, which can include the energy storage features, can be any device configured to store energy and can include, for example, one or several batteries, capacitors,

fuel cells, or the like. In some embodiments, the energy storage device 308 can be configured to receive charging energy from the charging module 306.

[0060] With reference now to Figure 4, a schematic illustration of one embodiment of the charger 116 is shown. . In some embodiments, each of the components of the architecture of the charger 116 can be implemented using the processor, memory, and/or other hardware component of the charger 116. In some embodiments, the components of the architecture of the charger 116 can include software that interacts with the hardware of the charger 116 to achieve a desired outcome.

[0061] In some embodiments, the charger 116 can include, for example, a network interface 350, or alternatively, a communication module. The network interface 350, or alternatively, a communication module, can be configured to access the network 110 to allow communication between the charger 116 and the other components of the implantable neurostimulation system 100. In some embodiments, the network interface 350, or alternatively, a communication module, can include one or several antennas and software configured to control the one or several antennas to send information to and receive information from one or several of the other components of the implantable neurostimulation system 100.

[0062] The charger 116 can include a charging module 352. The charging module 352 can be configured to control and/or monitor the charging of one or several of the pulse generators 102, 104. In some embodiments, the charging module 352 can include one or several features configured to transmit energy during charging. In one embodiment, these can include one or several charging coils, which can be, for example, one or several transmitting coils, that can magnetically couple with the charging coil of the pulse generator 102, 104 to thereby recharge the pulse generator 102, 104. In some embodiments, the charging coil can be described by a plurality of parameters including, for example, inductance and/or a quality factor (Q). Similarly, in some embodiments, the magnetic coupling between the transmitting coil and the receiving coil can be described by one or more parameters including, for example, a coupling coefficient.

[0063] In some embodiments, charging module 352 of the charger 116 can be configured to send and/or receive data via FSK during charging of the pulse generator 102, 104. The details of these components of the charging module 352 will be discussed in greater detail below.

[0064] The charger 116 can include a data module 354. The data module 354 can be configured to manage data for transmission to the pulse generator 102, 104 and/or data received from the pulse generator 102, 104. This information can include, for example, updates to software on the pulse generator 102, 104, pulse patterns, updates relating to the user of the pulse generator 102, 104, or the like. In some embodiments, the data module 354 can be configured to generate transmission data, which can then be communicated to the implantable pulse generator 104. In some embodiments, transmission data is generated by converting data into an encoded form corresponding to the communication capabilities of the charging module 352. In one embodiment in which the charging module 352 can modulate between two frequencies to communicate data, the data can be converted to binary format.

[0065] With reference now to Figure 5, a functional block diagram of one embodiment of the charging circuit 500 of the charging module 352 of the charger 116 is shown. As seen, the charging circuit includes a processor 502, which can correspond to the processor discussed above with respect to charger 116. In some embodiments, the processor 502 can be electrically connected to other components of the charging module 352 to thereby receive signals from these other components of the charging module 352 and to thereby control these other components of the charging module 352.

[0066] In some embodiments, and in different circumstances, the charging module 352 may operate at one or several different frequencies. In some embodiments, the processor 502 allows for monitoring the frequency of operation of the charging circuit. In such an embodiment, the processor 502 can be used to control the frequencies of operation of the charging module 352 and to ensure that the frequencies of operation of the charging module are within a desired range or ranges. This can be particularly important in embodiments in which the range of operation frequencies is specified by, for example, a government or government agency. In such embodiments, the processor 502 can ensure operation within regulatory limits and can provide the ability to shut down the charging module 352 if it is operating out of frequency tolerances.

[0067] The processor 502 can be connected to a class E driver 504, which can be, for example, a class E type power converter. The class E driver 504 can be used to convert AC to DC. In some embodiments, the class E driver 504, can be an efficient circuit, which efficiency can be obtained by switching an active element (typically a FET, including a MOSFET) of the class E driver 504 fully on or off to thereby avoid the linear region of

operation. In some embodiments, this switching can occur when both the voltage and current through the active element are at or near zero. In some embodiments, switching the active element on can occur when the dv/dt across the active element is zero, so that small errors in the switch timing or tuning of the matching network do not significantly degrade the circuit's efficiency. The details of the class E driver 504 will be discussed at greater length below.

[0068] As seen in Figure 5, in some embodiments, the class E driver 504 can include, or be connected with a charging coil 506, which can be a transmitting coil. In some embodiments, the class E driver 504 can be used in powering an implantable device via inductive coupling. In such an embodiment, an inductive coil of the class E driver 504, can serve a dual purpose in functioning as the charging coil 506 while also functioning in a load network of the class E driver 504.

[0069] Additionally, in some embodiments, the class E driver can include, or be connected with an FSK module 508. In some embodiments, the FSK module can include one or several features that can be controlled by the processor 508 to modulate and/or change the frequency of the magnetic field created by the charging coil 506. In some embodiments, the FSK module 508 can be controlled to create at least 2 frequencies, at least 3 frequencies, at least 4 frequencies, at least 5 frequencies, and/or any other or intermediate number of frequencies. In one embodiment, the FSK module 508 can be controlled to switch between a first frequency, a second frequency, and a third frequency. In one embodiment, the first frequency can be an intermediate frequency, with the second frequency being a relatively lower frequency and the third frequency being a relatively higher frequency. The details of the FSK module 508 will be discussed at greater length below.

[0070] With reference now to Figure 6, a schematic illustration of one embodiment of the charging circuit 500 of the charging module 352 of the charger 116 is shown. As seen in Figure 6, the charging circuit 500 includes the processor 502, the class E driver 504, the charging coil 506, and the FSK module 508.

[0071] The class E driver 504 comprises a power switching transistor (SW1), which can be, for example, a FET transistor. The power switching transistor (SW1) can have a drain (D1) connected to inductor (L1) which acts as a current source to supply DC power to the class E driver 504, a source (S1) connected to ground 602, and a gate (G1) connected to the processor 502. In some embodiments, processor 502 can control the power switching

transistor (SW1) by varying the degree to which, or whether a voltage is applied to the gate (G1). The voltage applied to the gate (G1) is identified as drive signal (VG1) in Figure 6.

[0072] The class E driver 504 can include a load matching network 604 that can include capacitors (Cs) and (Cp), and charging coil (L2). In some embodiments, the properties of the load matching network 604, and of capacitors (Cs) and (Cp) and charging coil (L2) can, in combination with other components of the class E driver 504, give the charging circuit 500 a natural frequency, which can be an impulse response frequency.

[0073] In some embodiments, and as mentioned above, the charging coil (L2) can be a component of the load matching network 604, and can also be the transmitting coil that magnetically couples with the receiving coil of the implantable pulse generator 104. In such an embodiment, coil current (IL2) passes through charging coil (L2) and creates a magnetic field which can couple with the receiving coil of the implantable pulse generator 104.

[0074] The class E driver 504 can include a current sensor (T1) in some embodiments, and as depicted in Figure 6, the current sensor (T1) can be in series with the charging coil (L2) and can be used to measure the amount of current passing through the charging coil (L2). As depicted in, Figure 6, the current sensor (T1) can be connected to processor 502 to thereby allow current data generated by the current sensor (T1) to be received by the processor 502. In some embodiments, and as mentioned above, this current data can be used, at least in part, in the generation of control signals by the processor 502.

[0075] In some embodiments, the processor 502 can be connected to the class E driver 504 via a switch voltage circuit 606. In some embodiments, the switch voltage circuit 606 can comprise an electrical connection between the drain side of power switching transistor (SW1) and the processor 502. In some embodiments, the switch voltage circuit 606 can comprise features to adjust the voltage measured at the drain side of the power switching transistor (SW1) so that the voltage received at the processor 502 is compatible with the processor 502. In some embodiments, this may include use of an amplifier if the voltage at the drain side of the power switching transistor (SW1) is too low, and in some embodiments, this may include the use of one or several voltage reduction features if the voltage at the drain side of the power switching transistor (SW1) is too high. In the embodiment depicted in Figure 6, a divider network 608 comprising resistors R4 and R5 is positioned between the drain side of the power switching transistor (SW1) and the processor 502. In some embodiments, the

divider network 608 can be further supplemented by a buffer which can further condition the voltage for receipt by the processor 502.

[0076] In some embodiments, the processor 502 and the class E driver 504, including the charging coil 506, can operate as follows. Power is supplied to the class E-driver 504 via the inductor (L1), which acts as a current source. Coil current (IL2) is provided to the charging coil (L2), which current produces a magnetic field that can magnetically couple with the receiving coil of the implantable pulse generator 104 to recharge the implantable pulse generator. The load current (IL2) is sensed by the current sensor (T1), and in some embodiments, buffered and squared up, and provided to the processor 502. The processor 502 monitors the zero crossing current transitions of load current (IL2) and adjusts the drive signal (VG1) to the gate (G1) of the switching power transistor (SW1). The use of the processor 502 allows for both the on and off transitions of SW1 to be optimized for efficiency, and allows for these points to change as the operating frequency changes to maintain closer control of the circuit.

[0077] In some embodiments, the processor 502 can adjust one or both of the on and off times for power switching transistor (SW1) to maximize efficiency at all conditions of magnetic coupling and external influences on the transmitting coil. For example, if it is desired to switch on power switching transistor (SW1) before the zero crossing signal is received at the processor 502, then the timing can be adjusted for the next cycle based on the last cycle or last few cycles of the feedback signal from current sensor (T1). Additional feedback on circuit operation can also be obtained from the switch voltage circuit 606, which monitors the voltage across the power switching transistor (SW1). In some embodiments, the data from the switch voltage circuit 606 can be used to control the power switching transistor (SW1), with a turn on point based on the minimum voltage across the FET. In some embodiments, the switch voltage circuit 606 can be configured to provide feedback on the peak amplitude of the power switching transistor's (SW1) drain voltage, as a check that the class E driver 504 is operating normally and help ensure safe and reliable operation.

[0078] In some embodiments, and as depicted in Figure 6, the charging circuit 500 can include the FSK module 508. The FSK module 508 can include one or several components configured to allow modulation of the natural frequency of the class E driver 504. In some embodiments, these one or several components can be selectively included in, or excluded

from the circuit of the class E driver 504 to thereby selectively modulate the natural frequency of the class E driver 504.

[0079] In the embodiment depicted in Figure 6, the FSK module 508 can comprise a second capacitor (C2) and a third capacitor (C3) as well as a second switching transistor (SW2) and a third switching transistor (SW3). In some embodiments, the capacitors (C2, C3) can have any desired properties, and can be any desired capacitors. Similarly, the transistors (SW2, SW3) can have any desired properties and be any desired type of transistors. In some embodiments, the transistors (SW2, SW3) can comprise FET transistors.

[0080] In some embodiments, and as depicted in Figure 6, the FSK module 508 can be configured such that the capacitors (C2, C3) can be selectively electrically included in the charging circuit 500. Specifically, in some embodiments, the processor 502 can be electrically connected to the gates (G2, G3) of the switch transistors (SW2, SW3) to allow the controlled switching of the switch transistors (SW2, SW3). As depicted in Figure 6, for example, when the third transistor (SW3) is switched to on, the class E driver 504 is connected to ground 610, and none of capacitors (C2, C3) are included in the charging circuit 500. Alternatively, if the second transistor (SW2) is switched to on and the third transistor (SW3) is switched to off, the class E driver 503 is connected to ground 612 and the third capacitor (C3) is included in the charging circuit 500. Finally, if both transistors (SW2, SW3) are switched to off, then the class E driver 504 is connected to ground 614 and both the second and third capacitors (C2, C3) are included in the charging circuit 500. This selective inclusion of the second and third capacitors (C2, C3) in the charging circuit 500 allows the selective modulation between three natural frequencies of the charging circuit, which selective modulation can be used to transmit data from the charger 116 to the implantable pulse generator 104.

[0081] With reference now to Figure 7, a graphical illustration of one embodiment of a transition from a charging mode to a simultaneous charging/data transmission mode is shown. In some embodiments in which the charging circuit 500 includes the FSK module 508, the natural frequency of the charging circuit 500 can be modulated to, in addition to recharging the implantable pulse generator 104, communicate with and/or transmit data to the implantable pulse generator 104. In some embodiments, and as depicted in Figure 7, the FSK module 508 of the charger 116 can be configured to alternate between a first frequency, a second frequency that is lower than the first frequency, and a third frequency that is higher

than the first frequency. In some embodiments, the FSK module 508 can configure the charger 116 to generate a magnetic field for recharging the implantable pulse generator 104 at the first, intermediate frequency.

[0082] As depicted in Figure 7, the operation of the charging circuit 500 at the first frequency during the charging mode can continue until time, t1, at which point, the processor 502 controls the FSK module 508 to modulate the natural frequency of the charging circuit 500 to begin transmission of data and to enter into a charging/data transmission mode of operation of the charging circuit 500. As depicted in Figure 7, this change in modes can begin by modulating the natural frequency of the charging circuit 500 to the third frequency, however, this change in modes can likewise being by modulating the natural frequency of the charging circuit 500 to the second frequency. At time, t2, the processor 502 controls the FSK module 508 to modulate the natural frequency of the charging circuit 500 from the third frequency to the second frequency, and finally, at time, t3, the processor 502 controls the FSK module 508 to modulate the natural frequency of the charging circuit 500 from the second frequency to the first frequency. As depicted, at time, t3, the charging circuit 500 exits the charging/data transmission mode of operation and re-enters the charging mode of operation. In some embodiments, the charging can be performed at an intermediate frequency, which can be a carrier frequency, and the data transmission can be performed by modulating between frequencies that are each either higher or lower than the intermediate frequency.

[0083] With reference now to Figure 8, a chart 800 depicting one embodiment of measurements from charging circuit 500 is shown. Chart 800 depicts four traces, a first trace 802 corresponding to the actual coil current (IL2) passing through charging coil (L2) with respect to time. As depicted in chart 800, in some embodiments, the coil current (IL2) can sinusoidally vary with respect to time. Chart 800 further identifies the time 803 at which one of the several zero crossing current transitions of the coil current (IL2) passing through the charging coil (L2) occurs.

[0084] Chart 800 depicts a second trace 804 that corresponds to the drive signal (VG1). As seen in chart 800, the drive signal (VG1) can comprise a repeated boxcar function. In some embodiments, the second trace can comprise a first position 806, at which position the power switching transistor (SW1) is open, and a second position 808, at which position the power switching transistor (SW1) is closed. In some embodiments, the drive signal (VG1) can be

characterized by a frequency with which the subsequent second position 808 corresponding to the power switching transistor (SW1) closed times occurs, and a length of time in which the drive signal (VG1) remains in the second position 808.

[0085] Chart 800 depicts a third trace 810 that corresponds to the current sensed by current sensor T1, with voltage clamping applied. As seen, the combination of this current output and the voltage clamping results in a periodic, truncated function. Chart 800 identifies the time 812 at which the current sensor T1 senses the zero crossing current transition of time 803. As seen, time 803 and time 812 are separated by a propagation delay (DY1).

[0086] Chart 800 depicts a fourth trace 814 that corresponds to the output from the buffer to T1 and input into the processor 502. This fourth trace 814 further corresponds to buffer affected output based on the third trace 810. The fourth trace 814 can be a repeated boxcar function having a first level 816 and a second level 818. As seen in chart 800, time 820 identifies the instant of the first transition from the first level 816 to the second level 818 after the zero crossing current transition of the coil current (IL2) at time 803. The temporal separation between time 820 and time 812 is propagation delay (DY2).

[0087] In addition to delays (DY1, DY2), two additional propagation delays arise in the operation of charging circuit 500. In one embodiment, these delays can include (1) processing time taken by the processor 502, and (2) the turn-on time of the power switching transistor (SW1). In some embodiments, these propagation delays can adversely affect the operation of the charging circuit 500, because immediate correction of improper timing cannot be made using presently utilized control methods. In the prior art, by the time the need for a timing change is identified, the proper time to make that change has passed. In one embodiment, and to counteract these propagation delays, the processor 502 can comprise a table identifying different frequencies for drive signal (VG1) and/or different lengths of time in which the drive signal (VG1) can remain in the second position 808. In some embodiments, the values in this table can be generated during evaluation of the charging circuit 500 under different load conditions which can, for example, replicate different magnetic couplings with the implantable pulse generator. By using processor control to implement a change in drive signal timing, which results in a change of the frequency of the drive signal (VG1) and/or different lengths of time in which the drive signal (VG1) is in the second position 808, the drive signal enters the second position 808 in the next (or later) cycle of the coil driving circuit, such as shown in Figure 9 below. By this, any propagation delays such as those

identified above are inherently compensated for in the next (or later) cycle, and do not compromise the transmitter operating efficiency.

[0088] Figures 9-11 depict charts 900, 1000, 1100 showing the impact of different drive signal frequencies on the operation of charging circuit 500. Specifically, chart 900 depicts a first trace 902 corresponding to the current sensed by current sensor T1, with voltage clamping applied. As seen, the combination of this current output and the voltage clamping results in a periodic, truncated function. Chart 900 identifies the time 904 at which the current sensor T1 senses the zero crossing current transition.

[0089] Chart 900 depicts a second trace 906 that corresponds to the drive signal (VG1). As seen in chart 900, the drive signal (VG1) can comprise a repeated boxcar function. In some embodiments, the second trace 906 can comprise a first position 908, at which position the power switching transistor (SW1) is open, and a second position 910, at which position the power switching transistor (SW1) is closed. In some embodiments, the closing of the power switching transistor (SW1) can connect the drain (D1) to ground 602 via source (S1). This connection can drive the voltage across the power switching transistor (SW1) to zero.

[0090] Chart 900 further depicts a third trace 912 corresponding to the sensed voltage across power switching transistor (SW1). The third trace 912 has a first, sinusoidal portion 914, and a second, flat portion 916. In some embodiments, the first, sinusoidal portion 914 of the third trace 912 indicates the varying voltage across the power switching transistor (SW1), and the second, flat portion 916 can identify the voltage across the power switching transistor (SW1) after the power switching transistor (SW1) is closed, which voltage, in the embodiment of Figure 6, is zero. In some embodiments, in which the frequency of the drive signal (VG1) is properly tuned for the condition of the charging circuit 500, the second, flat portion 916 of the third trace 912 can be flat, or in other words, without a step.

[0091] Chart 1000 of Figure 10 depicts one embodiment of traces of the same properties of chart 900, but in which the frequency of the drive signal (VG1) is too low, and the power switching transistor (SW1) is switched too late. Specifically, chart 1000 depicts a first trace 1002 corresponding to the current sensed by current sensor T1, with voltage clamping applied and identifying the time 1004 at which the current sensor T1 senses the zero crossing current transition. Chart 1000 further identifies a second trace 1006 that corresponds to the drive signal (VG1). This second trace 1006 includes a first position 1008, at which position the

power switching transistor (SW1) is open, and a second position 1010, at which position the power switching transistor (SW1) is closed.

[0092] Chart 1000 depicts a third trace 1012 corresponding to the sensed voltage across power switching transistor (SW1). The third trace 1012 has a first, sinusoidal portion 1014, and a second, flat portion 1018. As seen in chart 1000, as the frequency of the drive signal (VG1) is too low, the voltage indicated by the third trace 1012 drops below zero before the power switching transistor (SW1) is closed, and jumps via step 1018 to a zero voltage when the power switching transistor (SW1) is closed.

[0093] Chart 1100 of Figure 11 depicts one embodiment of traces of the same properties of chart 900, but in which the frequency of the drive signal (VG1) is too high, and the power switching transistor (SW1) is switched too early. Specifically, chart 1100 depicts a first trace 1102 corresponding to the current sensed by current sensor T1, with voltage clamping applied and identifying the time 1104 at which the current sensor T1 senses the zero crossing current transition. Chart 1100 further identifies a second trace 1106 that corresponds to the drive signal (VG1). This second trace 1106 includes a first position 1108, at which position the power switching transistor (SW1) is open, and a second position 1110, at which position the power switching transistor (SW1) is closed.

[0094] Chart 1100 depicts a third trace 1112 corresponding to the sensed voltage across power switching transistor (SW1). The third trace 1112 has a first, sinusoidal portion 1114, and a second, flat portion 1118. As seen in chart 1100, as the frequency of the drive signal (VG1) is too high, the voltage indicated by the third trace 1012 does not reach zero before the power switching transistor (SW1) is closed, and jumps via step 1118 to a zero voltage when the power switching transistor (SW1) is closed. In the embodiments of Figures 10 and 11 the efficiency of the charging circuit is adversely affected by the frequency of the drive signal (VG1) being either too low or too high.

[0095] With reference now to Figure 12, a flowchart illustrating one embodiment of a process 1200 for controlling the frequency of a charging circuit 500 is shown. The process begins at block 1202, wherein an initial frequency of the drive signal (VG1) is set. In some embodiments, this initial frequency can be a default frequency that can be, for example, stored in the memory of the charger 116 and/or other component of the implantable neurostimulation system 100.

[0096] After the initial frequency of the drive signal (VG1) is set, the process 1200 proceeds to decision state 1204, wherein it is determined if a current zero-crossing transition has occurred. In some embodiments, this determination can be made based on data received from the current sensor (T1). If it is determined that no current zero-crossing transition has occurred, the process 1200 waits a length of time which length of time can be, for example, predetermined, and then returns to decision state 1204.

[0097] If it is determined that a current zero-crossing transition has occurred, the process 1200 proceeds to block 1206 wherein the power switching transistor voltage is sensed or read. In some embodiments, this voltage can be read from the switch voltage circuit 606. In some embodiments, the reading of the power switching transistor voltage can include determining whether the voltage at the power switching transistor (SW1) at the instant before and/or of the closing of the power switching transistor (SW1) is greater than, less than, or equal to the voltage at the power switching transistor (SW1) after the closing of the power switching transistor (SW1). In some embodiments, the voltage of the power switching transistor can be read at a first time that corresponds to the current zero-crossing.

[0098] After the power switching transistor voltage has been read, the process 1200 proceeds to block 1208 wherein the switching time corresponding to the read power switching transistor voltage is read. In some embodiments, this switching time can be the frequency of the drive signal (VG1). The switching time can be read from an entry in a table of switching times, which table of switching times can be generated by analyzing the charging circuit 500 under a variety of circumstances and load conditions. In some embodiments, this step can result in retrieving a value for adjusting the frequency of the drive signal (VG1) to more closely match the properties and/or load conditions of the charging circuit 500.

[0099] After the switch time corresponding to the read voltage of the power switching transistor (SW1) is retrieved, the process 1200 proceeds to block 1210, wherein frequency limits are retrieved. In some embodiments, the frequency limits can correspond to one or several limits on the frequencies of operation of the charging circuit 500 such as, for example, one or several legal limits, regulatory limits, or the like. In one embodiment, for example, the frequency limits can correspond to one or both of an upper limit (high limit) and a lower limit (low limit).

[00100] After the frequency limits have been retrieved, the process 1200 proceeds to block 1212, wherein the frequency limits are compared to the retrieved corresponding switching time. In some embodiments, this comparison can be performed by the processor of the charger 116. After the frequency limits are compared to the switching time, the process 1200 proceeds to decision state 1214, wherein it is determined if the retrieved corresponding switching time is within the frequency limits. This comparison can be performed by the processor of the charger 116.

[00101] If it is determined that the retrieved corresponding switching time is not within the frequency limits, the process 1200 proceeds to block 1216, wherein the switching time is set to one of the upper and lower frequency limits. In some embodiment, the one of the upper and lower frequency limits can be whichever of the upper frequency limit and the lower frequency limit is implicated in decision state 1214. After the switching time has been set to one of the upper and lower frequency limits, or returning to decision state 1214, if it is determined that the switching time is within the frequency limits, then the process 1200 proceeds to block 1218, wherein the switching time is applied in that the frequency of the drive signal (VG1) is set to the retrieved corresponding switching time. After the switching time has been applied, the process 1200 returns to decision state 1204, and proceeds as outlined above. In some embodiments, and as is the case with propagation delays, the cycle can be repeated multiple times until a switching time is identified that mitigates the propagation delays and corresponds to the functioning of the charging circuit 500. In some embodiments, and after a switching time has been identified that satisfactorily mitigates the propagation delays and/or the effects of the propagation delays, the charging circuit 500 can be operated at a steady state at that switching time.

[00102] In the foregoing specification, the invention is described with reference to specific embodiments thereof, but those skilled in the art will recognize that the invention is not limited thereto. Various features and aspects of the above-described invention can be used individually or jointly. Further, the invention can be utilized in any number of environments and applications beyond those described herein without departing from the broader spirit and scope of the specification. The specification and drawings are, accordingly, to be regarded as illustrative rather than restrictive. It will be recognized that the terms “comprising,” “including,” and “having,” as used herein, are specifically intended to be read as open-ended terms of art.

WHAT IS CLAIMED IS:

1 1. A charger comprising:
2 a charging coil, wherein the charging coil is configured to magnetically couple
3 with an implantable device to recharge the implantable device;
4 a class E driver electrically connected to the charging coil, wherein the class E
5 driver comprises:
6 a switching circuit, wherein the switching circuit is switched by the
7 application of a first voltage to the switching circuit; and
8 a current sensor positioned to sense a current passing through the
9 charging coil; and
10 a processor electrically connected to the class E driver to receive data
11 indicative of the current passing through the charging coil and electrically connected to the
12 class E driver to control the switching circuit via the application of the first voltage to the
13 switching circuit, wherein the processor is configured to receive data indicative of the current
14 passing through the charging coil and control the switching circuit in response to the received
15 data.

1 2. The charger of claim 1, wherein the switching circuit comprises a
2 transistor.

1 3. The charger of claim 2, wherein the transistor comprises a MOSFET.

1 4. The charger of claim 3, wherein the processor is electrically connected
2 to the class E driver to receive data indicative of a second voltage of the switching circuit.

1 5. The charger of claim 4, wherein the processor is further configured to:
2 receive data indicative of the second voltage of the switching circuit; and
3 control the switching circuit in response to the received data indicative of the
4 second voltage of the switching circuit.

1 6. The charger of claim 4, wherein the second voltage is measured at the
2 drain of the switching circuit and wherein the first voltage is applied to the gate of the
3 switching circuit.

1 7. The charger of claim 6, wherein the processor is electrically connected
2 to the class E driver via a voltage divider comprising a first resistor and a second resistor.

1 8. The charger of claim 1, wherein the processor is configured to:
2 sense a power switching transistor voltage; and
3 determine whether to adjust a first frequency with which the first voltage is
4 applied to the switching circuit, wherein the adjustment of the first frequency mitigates one or
5 several propagation delays.

1 9. The charger of claim 8, wherein the processor is configured to retrieve
2 a stored value identifying a second frequency with which the first voltage is applied based on
3 the sensed power switching transistor voltage.

1 10. The charger of claim 9, wherein the processor is configured to compare
2 the retrieved stored value identifying the second frequency with which the first voltage is
3 applied to one or several frequency limits.

1 11. The charger of claim 10, wherein the first frequency is set to the
2 second frequency if the second frequency does not exceed the one or several frequency
3 limits.

1 12. The charger of claim 10, wherein when the second frequency exceeds
2 one of the one or several frequency limits, the first frequency is set to the exceeded one of the
3 one or several frequency limits.

1 13. A charger comprising:
2 a charging coil, wherein the charging coil is configured to generate a magnetic
3 field having a frequency and to magnetically couple with an implantable device to recharge
4 the implantable device;
5 a class E driver electrically connected to the charging coil; and
6 an FSK module configured to modulate the frequency of the magnetic field
7 among at least three frequencies.

1 14. The charger of claim 13, wherein the at least three frequencies
2 comprise a first frequency, a second frequency, and a third frequency, and wherein the third
3 frequency is the highest frequency and the second frequency is the lowest frequency.

1 15. The charger of claim 14, further comprising a processor electrically
2 connected to the FSK module and configured to control the FSK module.

1 16. The charger of claim 15, wherein the processor is configured to
2 selectively operate the charger in either a data non-transmitting state or in a data transmitting
3 state.

1 17. The charger of claim 16, wherein a carrier signal has the first
2 frequency when the charger operates in the data non-transmitting state.

1 18. The charger of claim 16, wherein the processor controls the FSK
2 module to modulate the carrier signal between the second frequency and the third frequency
3 when the charger operates in the data transmitting state.

1 19. The charger of claim 13, wherein the FSK module comprises two
2 capacitors and two transistors.

1 20. The charger of claim 19, wherein the two capacitors and the two
2 transistors of the FSK module are electrically connected such that the two capacitors can be
3 selectively included within the circuit by the FSK module.

1 21. The charger of claim 20, wherein the processor is configured to control
2 the two transistors of the FSK module to selectively include the two capacitors within the
3 circuit by the FSK module.

1 22. The charger of claim 21, wherein the selective inclusion of the two
2 capacitors within the circuit of the FSK modulates the frequency of the magnetic field
3 between the first, second, and third frequencies.

1 23. A method of communicating with an implantable device during
2 charging of the implantable device, the method comprising:
3 generating a charging signal with a charging coil, wherein the charging signal
4 has an initial, first frequency; and
5 transmitting data by modulating the frequency of the charging signal between
6 a second frequency that is lower than the first frequency and a third frequency that is higher
7 than the first frequency.

1 24. The method of claim 23, further comprising generating binary
2 transmission data during the charging of the implantable device, wherein the transmission
3 data is the transmitted data.

1 25. The method of claim 24, wherein modulating the frequency of the
2 charging signal between the second frequency and the third frequency transmits the binary
3 transmission data.

1 26. The method of claim 23, wherein the frequency of the charging signal
2 is modulated by an FSK module.

1 27. The method of claim 26, wherein the FSK module comprises two
2 capacitors and two transistors.

1 28. The method of claim 27, wherein the two capacitors and the two
2 transistors of the FSK module are electrically connected such that the two capacitors can be
3 selectively included within the circuit of by the FSK module to thereby modulate the
4 frequency of the charging signal.

1 29. A method of controlling a charger comprising:
2 creating a magnetic coupling between a charger and an implantable device,
3 wherein the magnetic coupling charges the implantable device;
4 setting an initial frequency of a drive signal, wherein the frequency of the
5 drive signal is set by a processor, and wherein the drive signal controls the opening and
6 closing of a switch;
7 sensing a voltage at the switch at a first time;
8 based on the voltage at the switch at the first time, retrieving a value
9 identifying a second frequency; and
10 changing the frequency of the drive signal.

1 30. The method of claim 29, wherein changing the frequency of the drive
2 signal comprises changing the frequency of the drive signal from the first frequency to the
3 second frequency.

1 31. The method of claim 29, comprising retrieving one or several
2 frequency limits, wherein the frequency limits provide an upper and lower bound to a range
3 of acceptable frequencies of the drive signal.

1 32. The method of claim 31, comprising comparing the second frequency
2 to the one or several frequency limits.

1 33. The method of claim 32, wherein changing the frequency of the drive
2 signal comprises changing the frequency of the drive signal from the first frequency to the
3 one of the one or several frequency limits if the second frequency exceeds the one of the one
4 or several frequency limits.

1 34. The method of claim 32, wherein changing the frequency of the drive
2 signal comprises changing the frequency of the drive signal from the first frequency to the
3 second frequency if the second frequency does not exceed the one or several frequency
4 limits.

1 35. The method of claim 29, wherein the changing of the frequency of the
2 drive signal mitigates an effect of a propagation delay.

1 36. The method of claim 35, wherein the frequency of the drive signal can
2 be adjusted multiple times to mitigate the effect of the propagation delay.

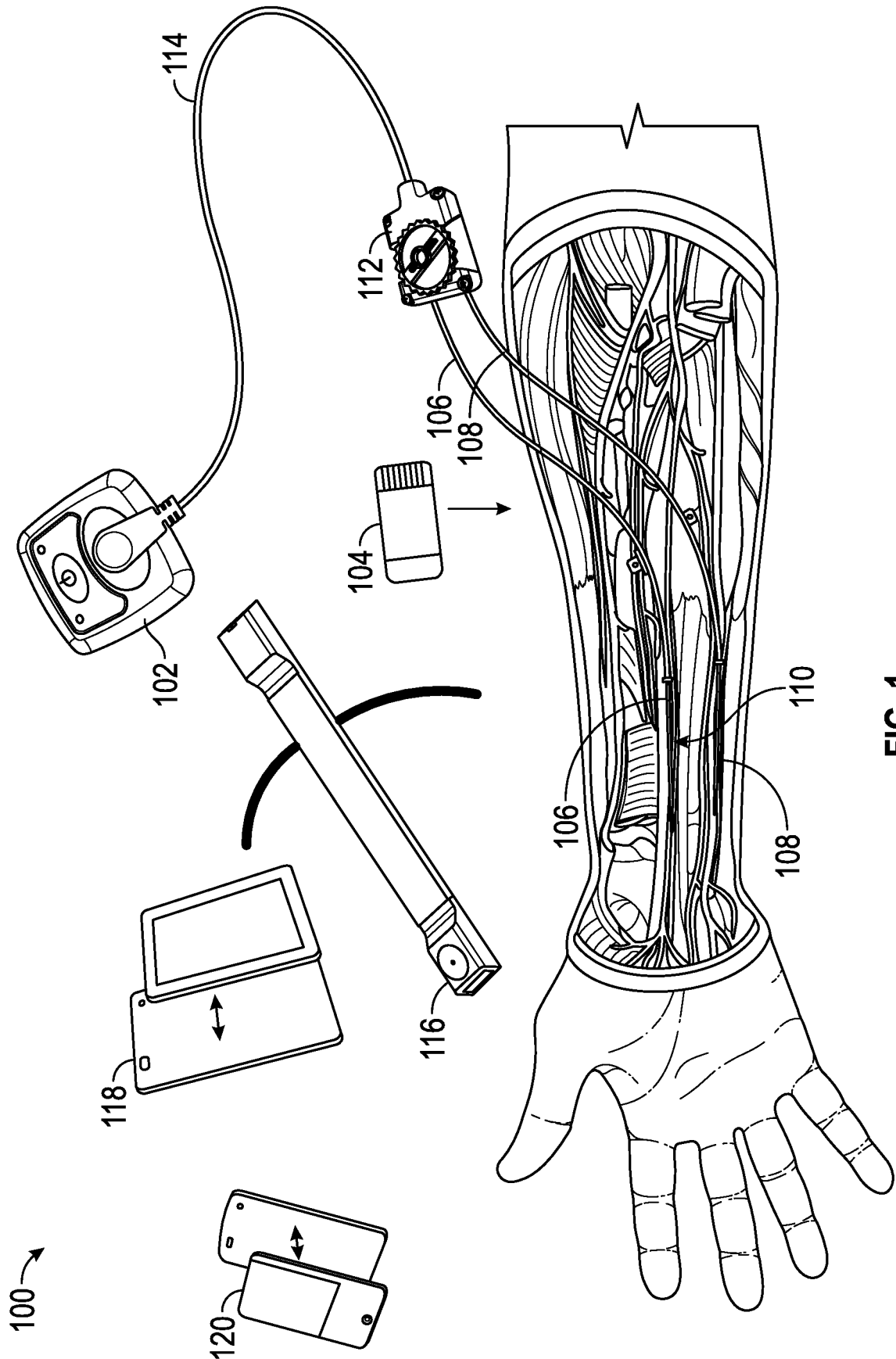


FIG. 1

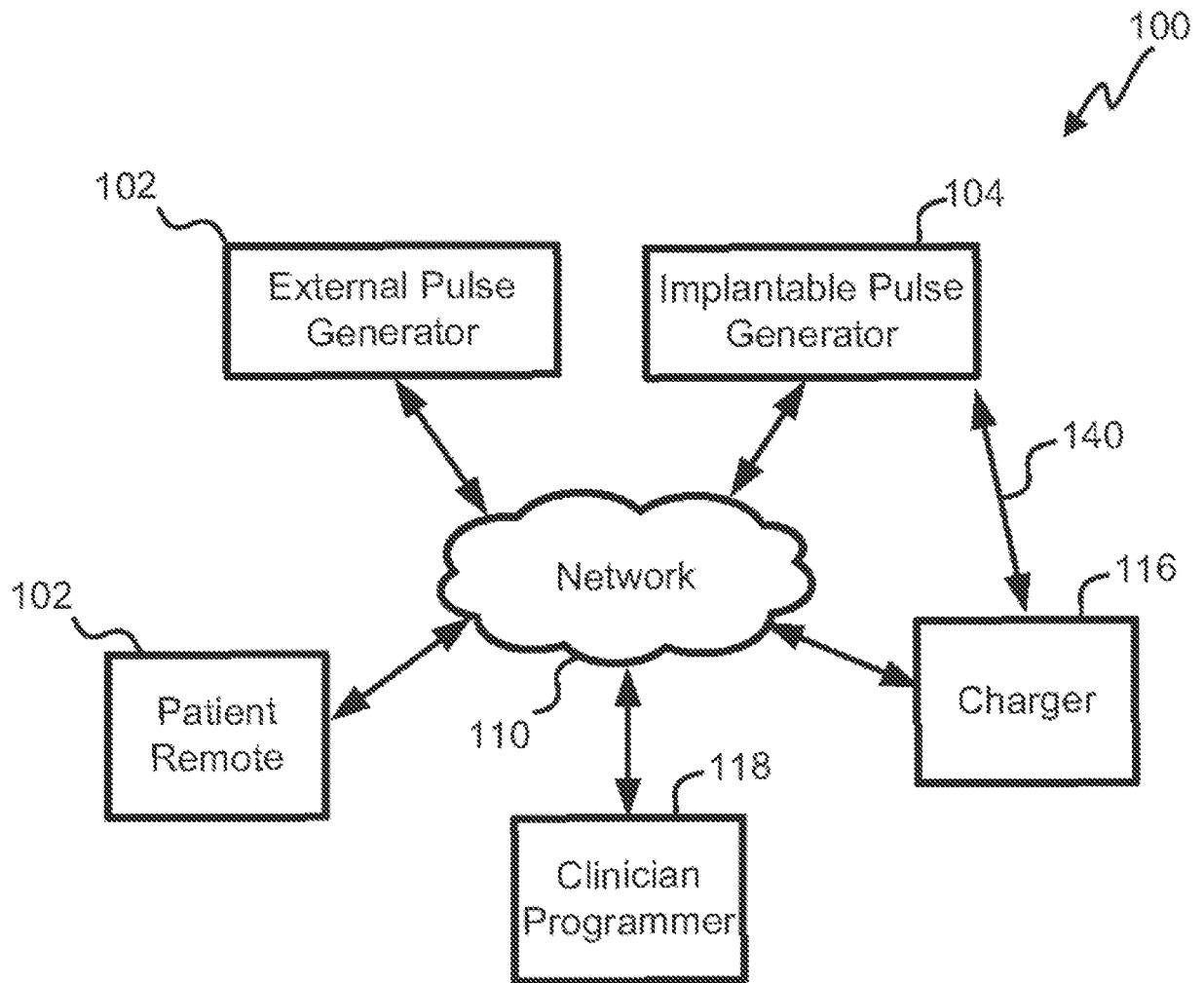


FIG. 2

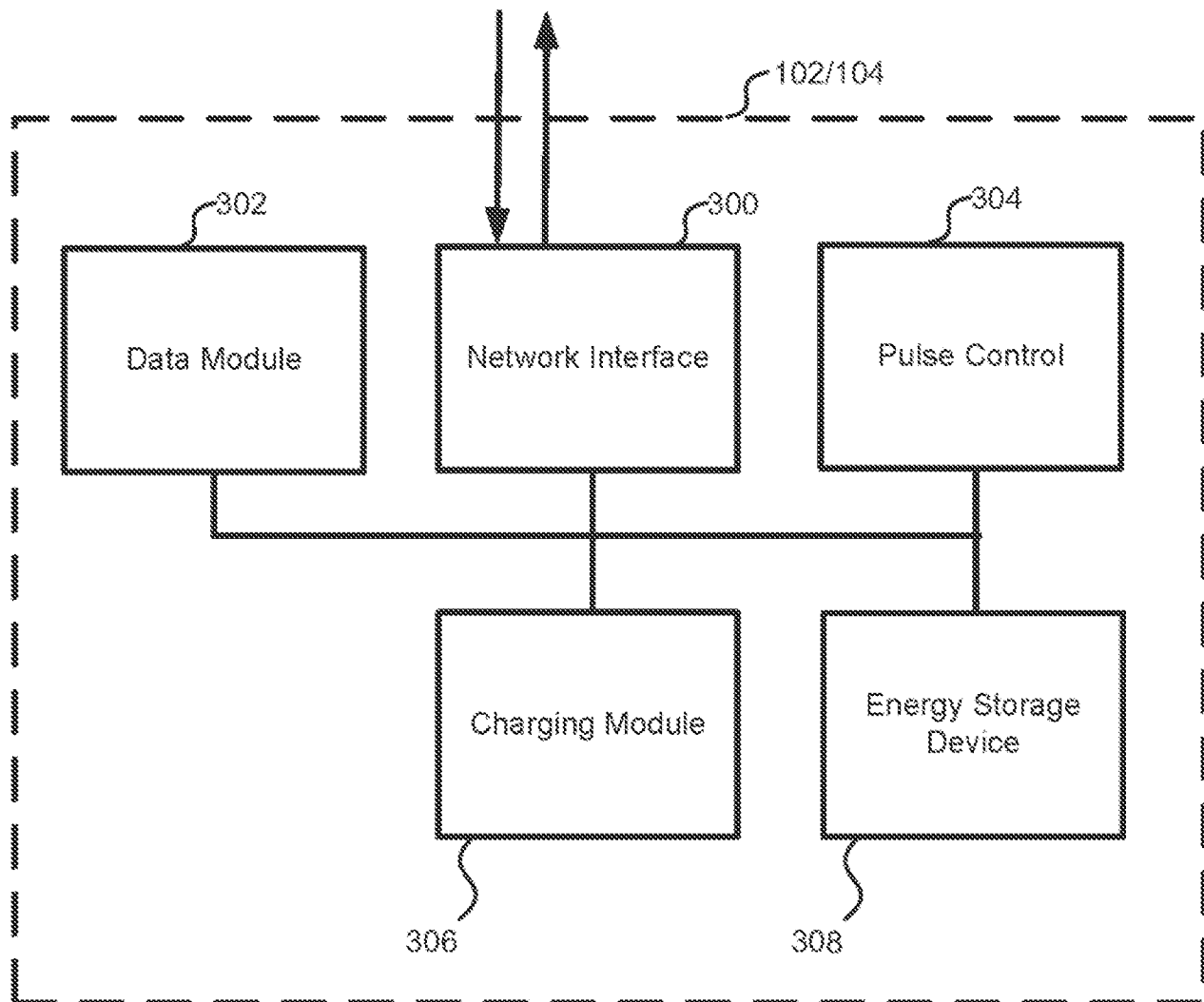


FIG. 3

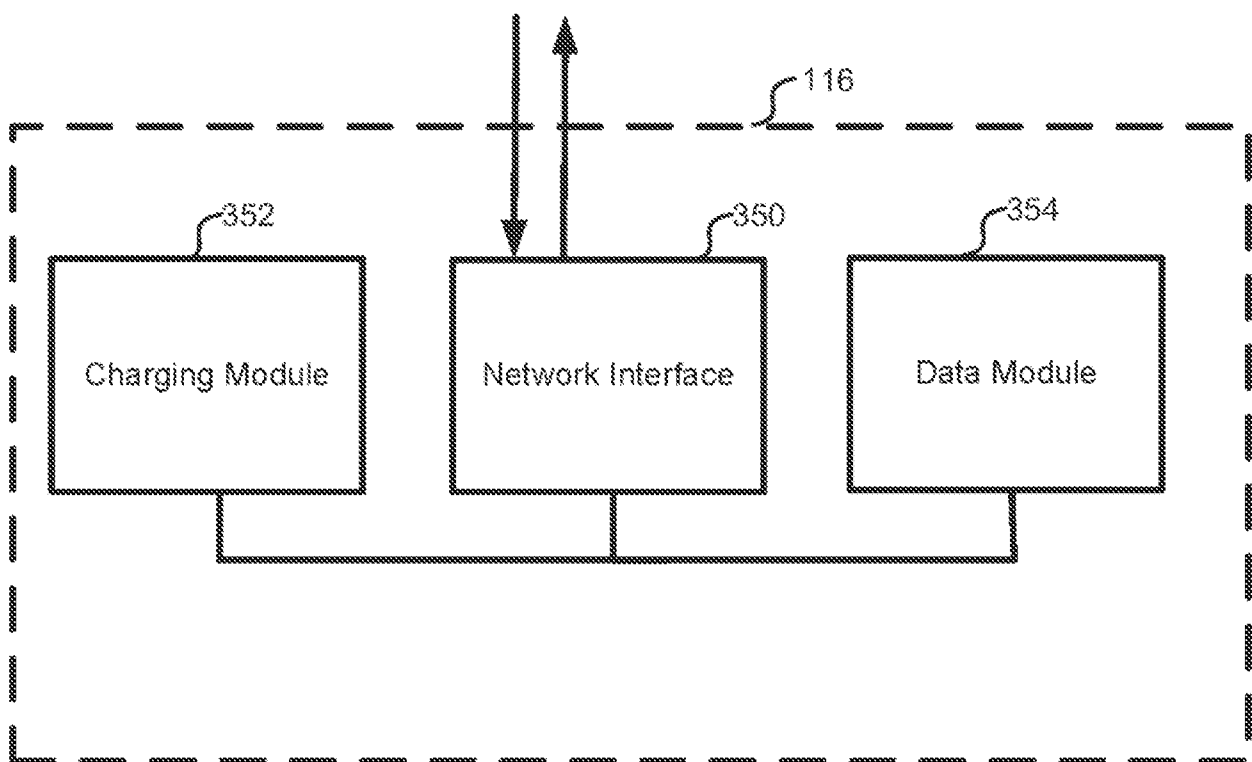


FIG. 4
SUBSTITUTE SHEET (RULE 26)

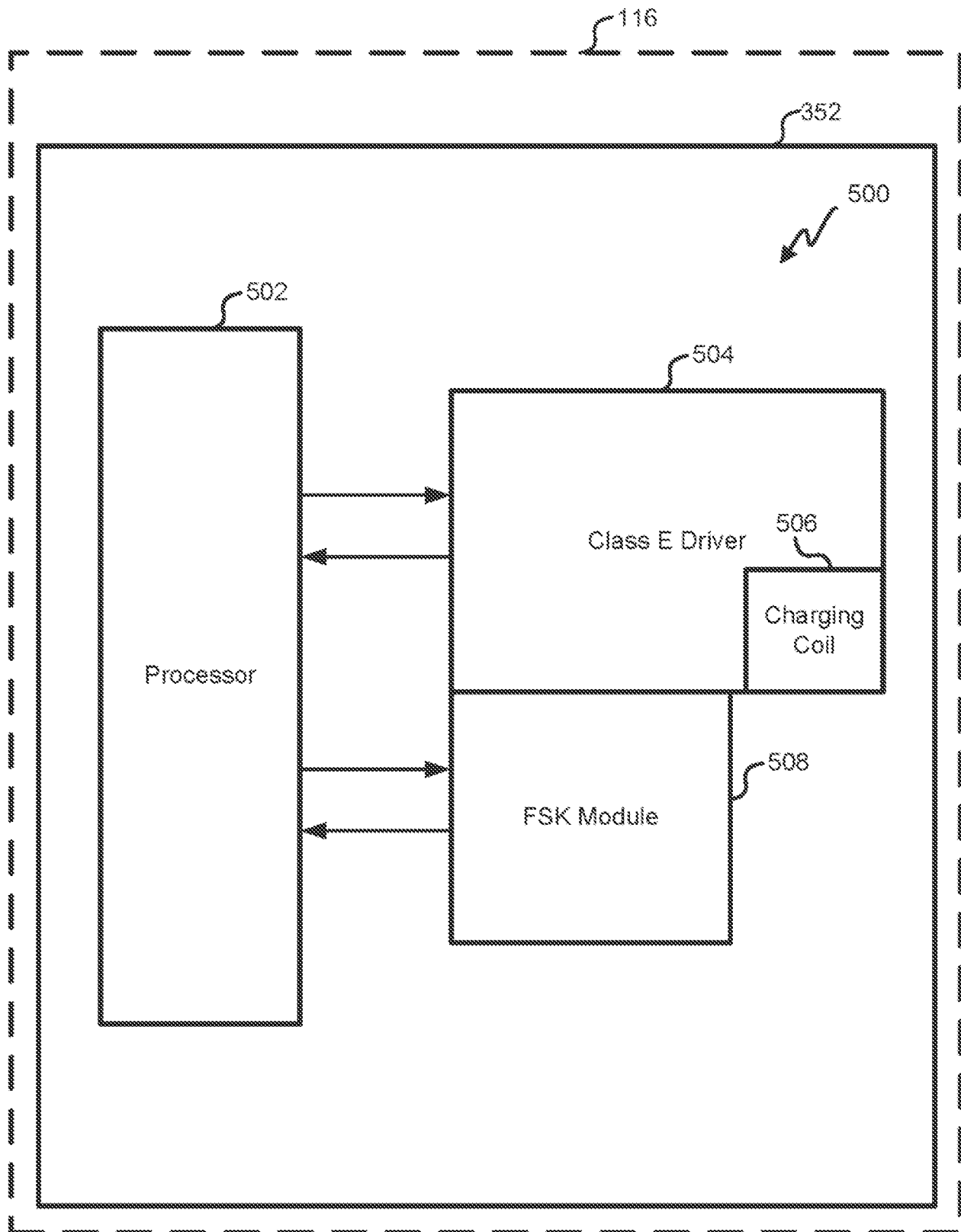


FIG. 5

SUBSTITUTE SHEET (RULE 26)

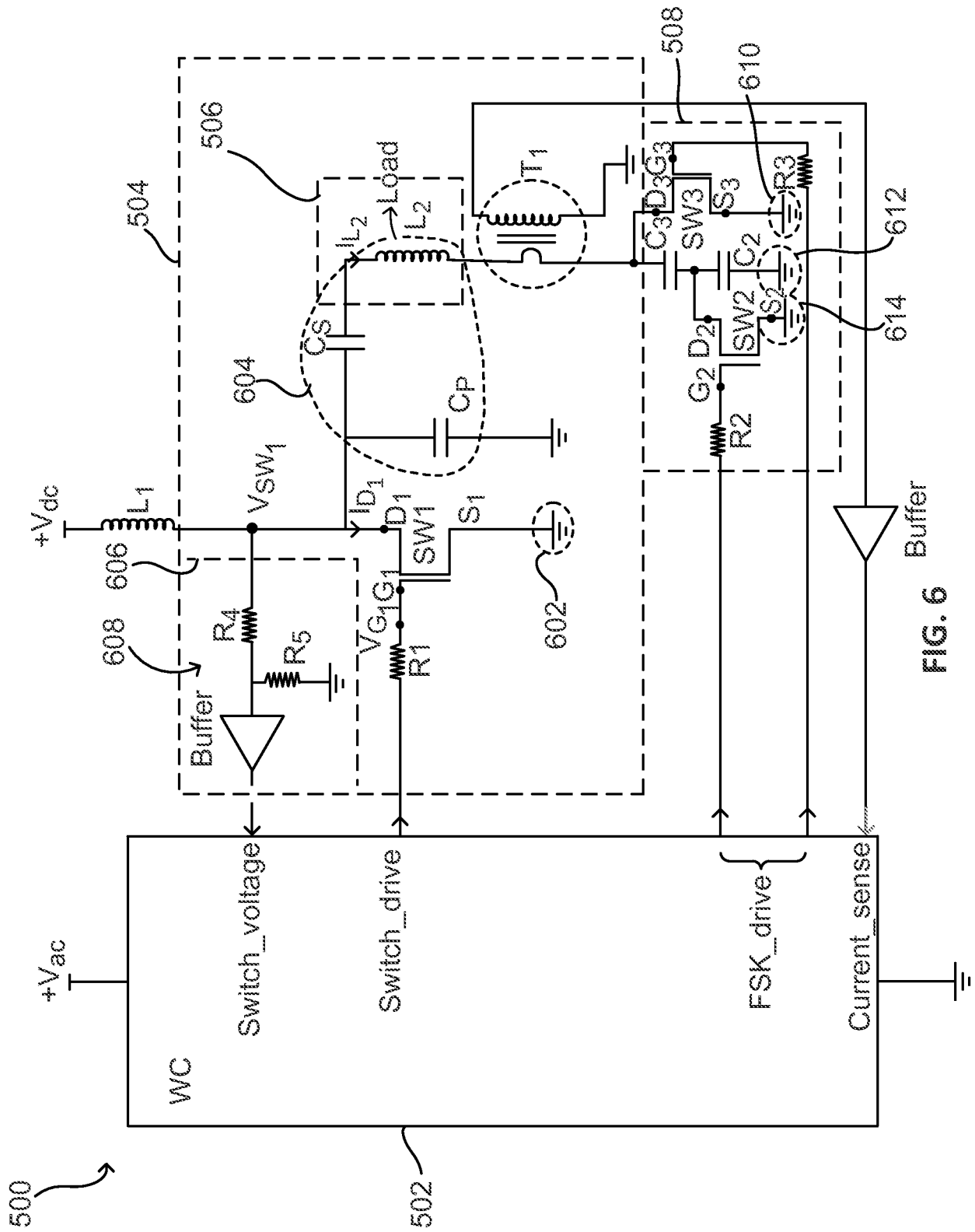


FIG. 6

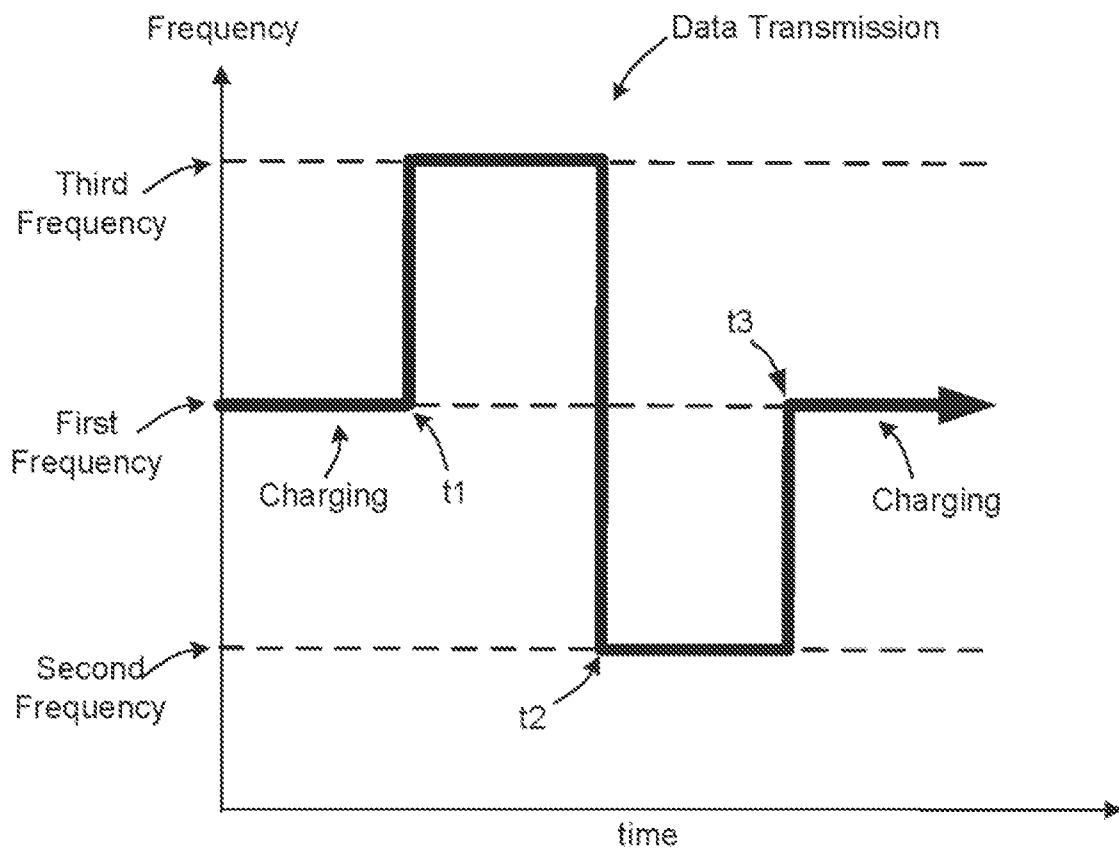


FIG. 7

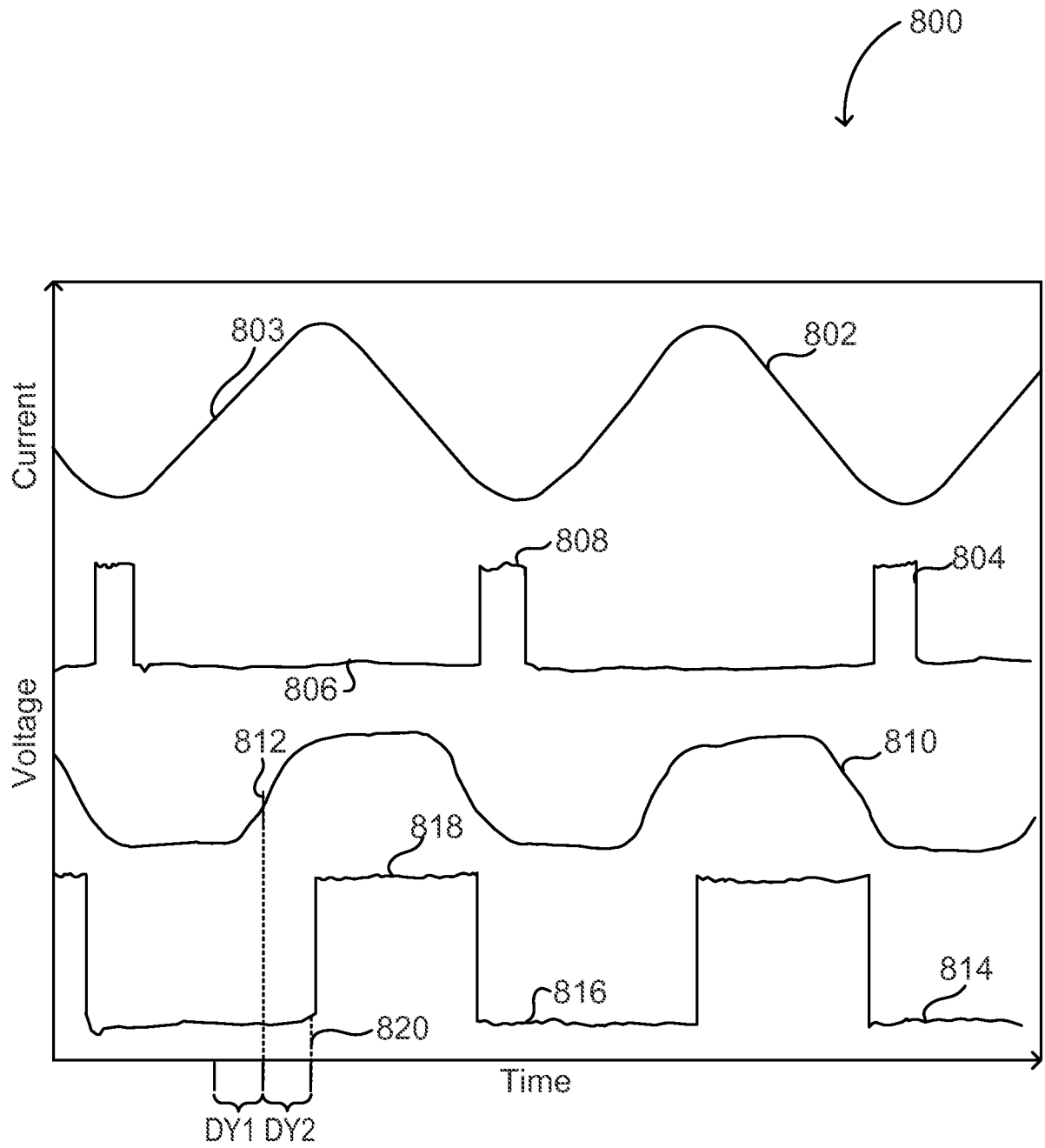


FIG. 8
SUBSTITUTE SHEET (RULE 26)

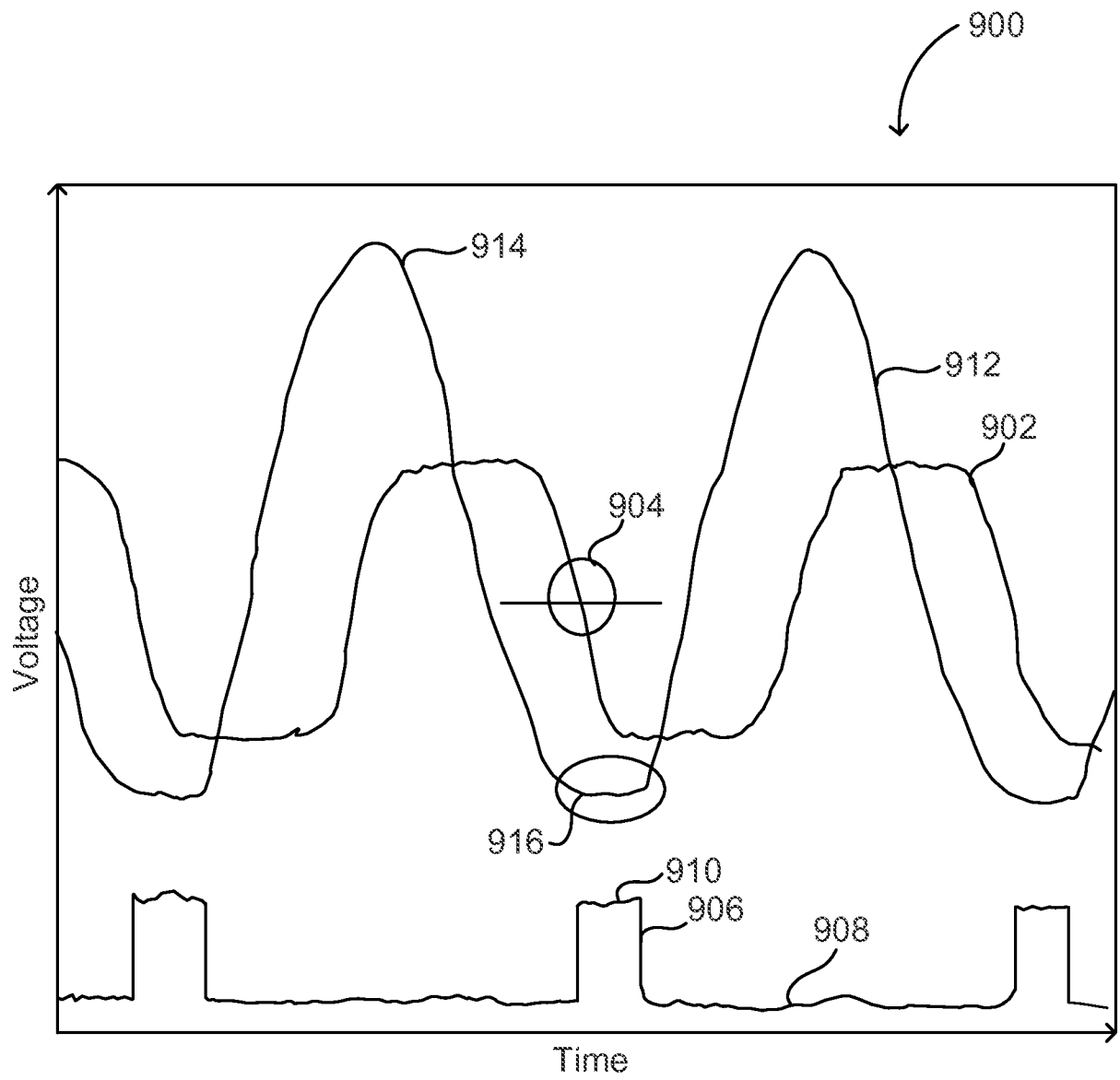


FIG. 9

SUBSTITUTE SHEET (RULE 26)

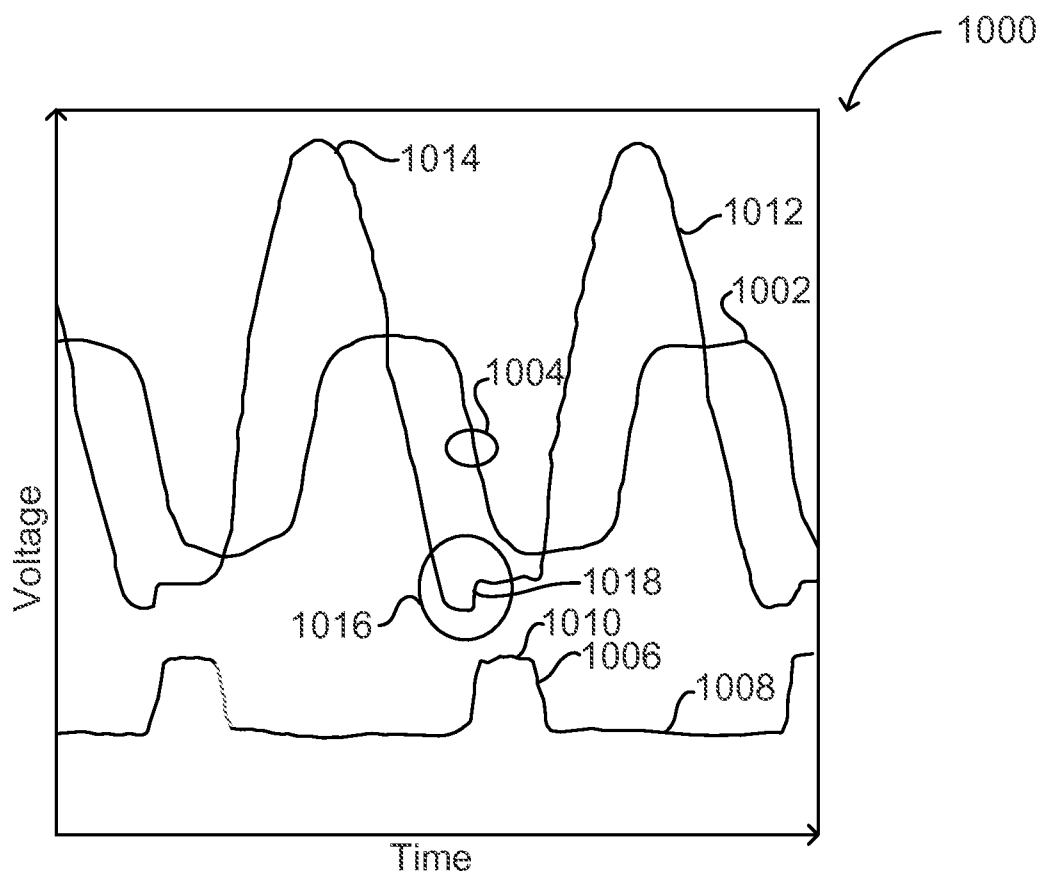


FIG. 10

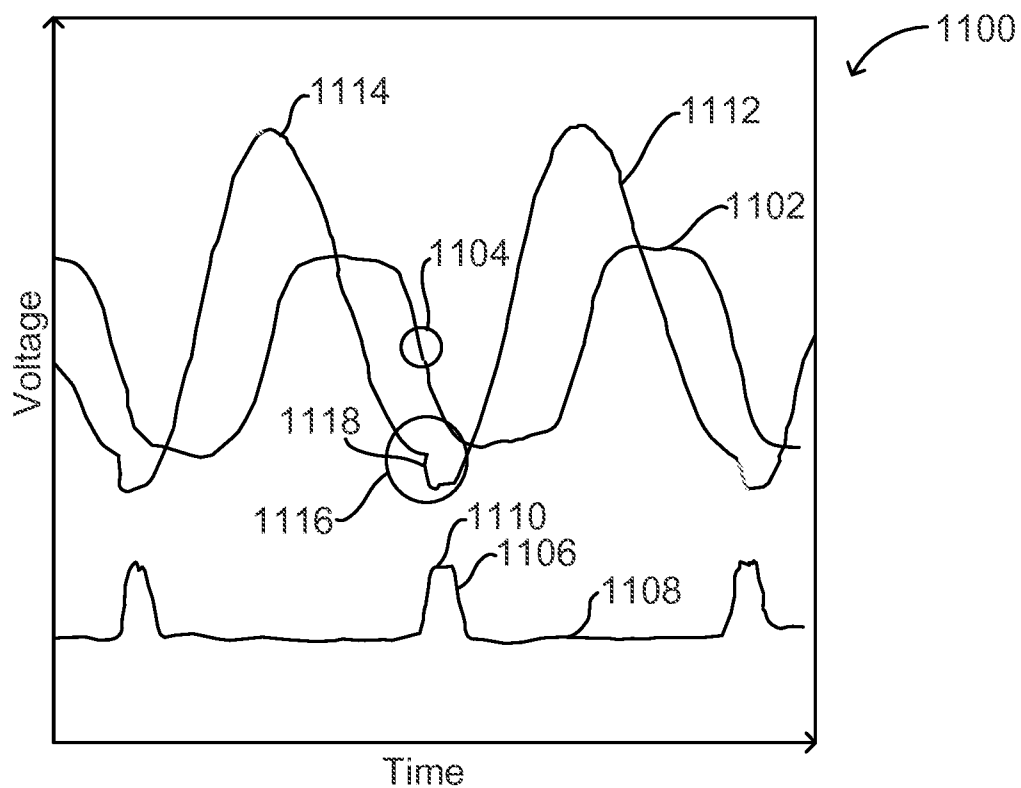


FIG. 11

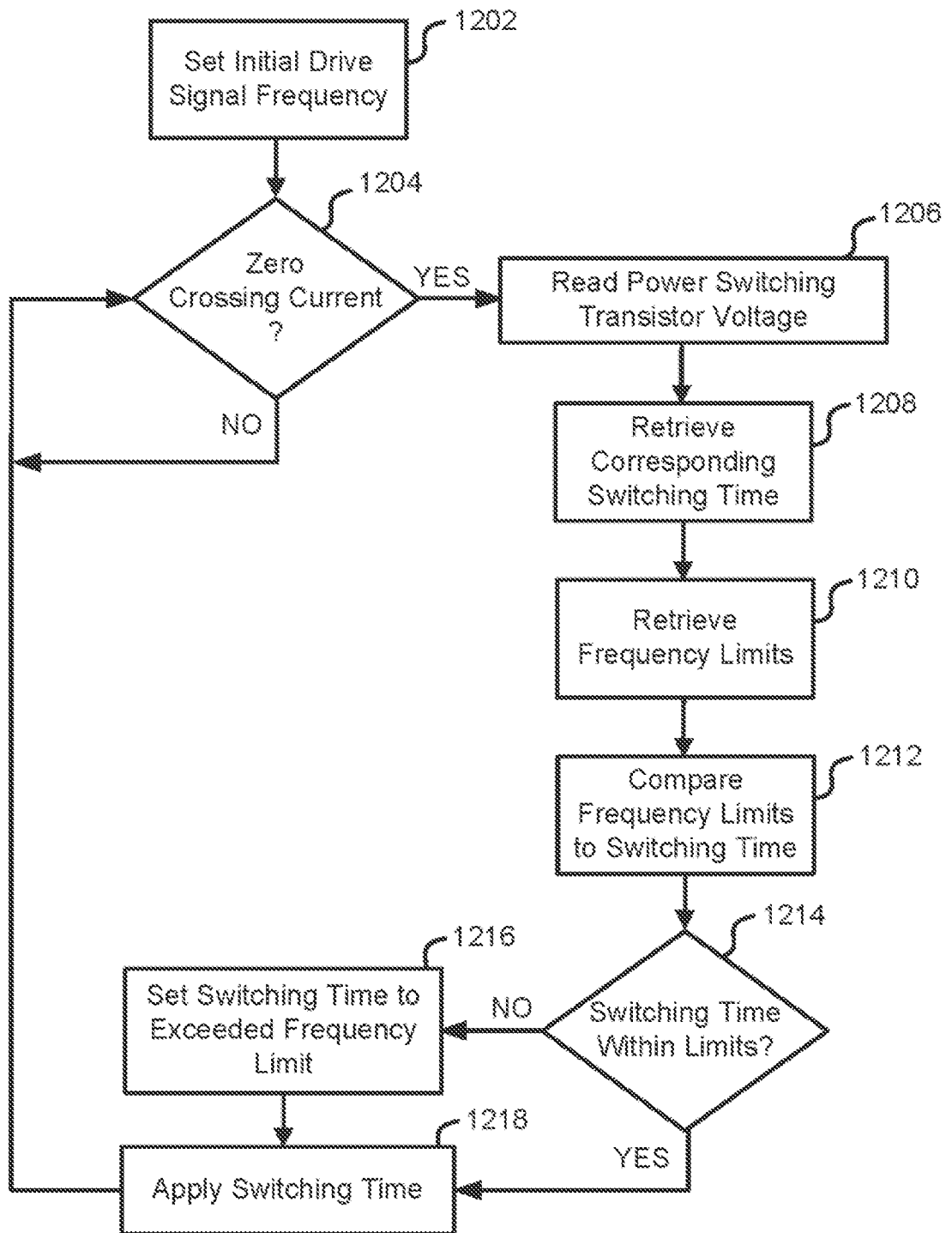


FIG. 12
SUBSTITUTE SHEET (RULE 26)