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(54) Title: ULTRA-SHALLOW JUNCTION AND METHOD FOR FORMING THE SAME

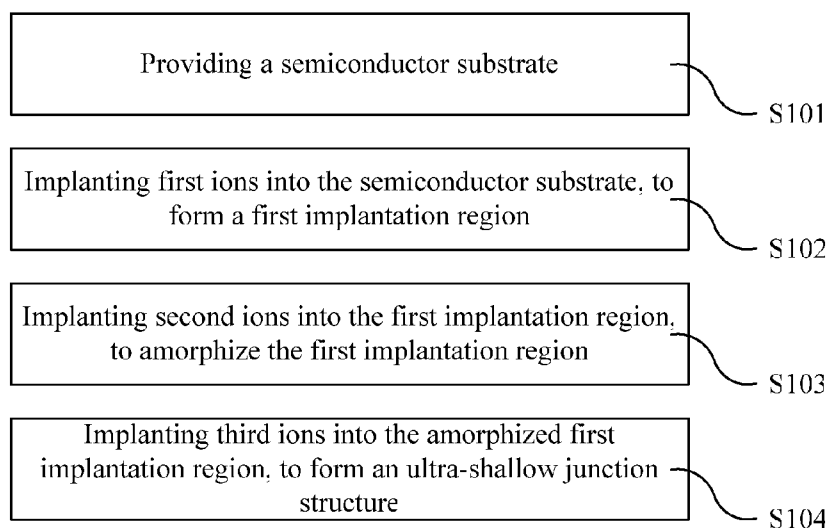


FIG. 1

(57) Abstract: A method for forming an ultra-shallow junction includes implanting first ions into a semiconductor substrate(101), to form a first implantation region(104); implanting second ions into the first implantation region(104) to amorphize the first implantation region(104); and implanting third ions into the amorphized first implantation region, to form an ultra-shallow junction structure.



EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, **Published:**

LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,

GW, ML, MR, NE, SN, TD, TG).

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Ultra-shallow junction and method for forming the same

Technology Field

[0001] The present disclosure relates to the field of semiconductor technology and, more particularly, to an ultra-shallow junction and a method for forming the same and a PMOS transistor.

Background of the Disclosure

[0002] Ion implantation is an impurity doping technique widely used in forming a variety of semiconductor devices and integrated circuits. The amount of ions implanted by an ion beam into a semiconductor substrate and their distribution can be accurately adjusted by controlling the current and voltage of the ion beam.

[0003] Feature size of semiconductor devices becomes smaller as the technology advances. Vertical size of a device (i.e., depth of the device) needs to be reduced as horizontal size (i.e., linewidth represented by the feature size) of the device shrinks. Consistent with this need, ion implementation is used to form shallow junctions or ultra-shallow junctions, e.g., a lightly-doped source region or a lightly-doped drain region of a Metal–Oxide–Semiconductor (MOS) transistor.

[0004] Threshold voltage of a MOS transistor is a parameter that reflects performance of the MOS transistor. The threshold voltage of the MOS transistor may be improved by enhancing substrate bias effect, also known as body effect.

[0005] The substrate bias effect can be provided for a PMOS transistor, if its substrate and its source are reverse biased (i.e., a negative voltage is applied to the P substrate) such that a depletion region in the substrate becomes thicker, causing an increase in fixed electric charges in the depletion layer. The increase of the electric charges in the depletion layer leads to a reduction of mobile electric charges in the channel, for a balance requirement of charges on both sides of a gate capacitance. Therefore, the reduction of mobile electric charges in the channel results in degraded electric conductivity. Improvement of gate voltage may increase the electric charges on the gate, thus maintaining electric conductivity level. For a device, the threshold voltage of the PMOS transistor is increased by substrate bias.

[0006] The body effect may be characterized using a body effect parameter γ . A higher body effect γ parameter represents a greater body effect and a higher threshold voltage. The body effect parameter γ may be determined by the following equation:

$$\gamma = \sqrt{2\varepsilon_0 q N_a} / C_{ox} \quad ,$$

[0007] wherein ϵ_0 is vacuum permittivity, q is a quantity of elementary charges, N_a is an ion doping concentration in the channel region, and C_{ox} is a capacitance per unit of area of the gate dielectric layer.

5 [0008] The body effect parameter γ may be improved by increasing N_a , the ion doping concentration in the channel region.

[0009] N_a may be increased by increasing the distance between the source and the drain. When the distance between the source and the drain increases, impurity diffusion in the source and the drain can be better controlled, such that the amount of electric charges in the depletion layer is reduced, thereby increasing N_a and improving
10 the body effect.

[0010] The body effect can also be improved by thickening sidewall spacers. However, this may reduce the saturation drain current, affecting other electric parameters of the MOS device.

Summary of the Disclosure

15 [0011] In accordance with the present disclosure, there is provided a method for forming an ultra-shallow junction. The method includes:

implanting first ions into a semiconductor substrate, to form a first implantation region;

20 implanting second ions into the first implantation region, to amorphize the first implantation region; and

implanting third ions into the amorphized first implantation region, to form an ultra-shallow junction structure.

[0012] In accordance with the present disclosure, there is also provided a method for forming a PMOS transistor. The method includes:

25 forming a gate structure on a semiconductor substrate, wherein a source region and a drain region are defined in the substrate on opposite sides of the gate structure;

implanting first ions into the source region and the drain region by using the gate structure as a mask, to form a first implantation region;

30 implanting second ions into the first implantation region by using the gate structure as a mask, to amorphize the first implantation region; and

implanting third ions into the amorphized first implantation region by using the gate structure as a mask, to form an ultra-shallow junction structure.

[0013] In accordance with the present disclosure, there is also provided an ultra-shallow junction. The ultra-shallow junction includes:

a semiconductor substrate; and

5 a junction structure in the substrate, the junction structure including a first ion implantation region including an amorphized structure; and

second ions implanted into the amorphized structure.

[0014] In accordance with the present disclosure, there is also provided a method for manufacturing a PMOS transistor. The method includes:

implanting first ions into a source region and a drain region of a substrate;

10 implanting second ions into regions of the first ion implanting region; and

implanting third ions into regions of the second ion implanting.

[0015] Features and advantages consistent with the present disclosure will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the present disclosure. Such features and advantages
15 will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

[0016] Fig. 1 illustrates a flow chart of a method for forming an ultra-shallow junction structure according to an embodiment;

20 [0017] Fig. 2 to Fig. 6 illustrate cross-sectional views of a method for forming an ultra-shallow junction structure according to an embodiment;

[0018] Fig. 7 illustrates a flow chart of a method for forming a PMOS transistor according to an embodiment;

25 [0019] Fig. 8 and Fig. 9 illustrate cross-sectional views of a method for forming a PMOS transistor according to an embodiment.

Detailed Description of the Embodiments

[0020] Technical details are described below for the person skilled in the art to understand the disclosure. However, the present disclosure may be implemented in a variety of ways other than those described herein, and various modifications may be
30 made without departing from the scope of the present disclosure. Therefore, the disclosure is not limited to the embodiments described herein.

[0021] A method disclosed herein of forming an ultra-shallow junction may include implantation of boron fluoride ions before amorphization of a substrate. The method takes advantage of easier diffusion of fluoride ions in, for example, a crystalline silicon than in amorphous silicon. Silicon-oxygen bonds in a gate dielectric layer on a surface of the substrate may be more easily broken by the fluoride ions. Oxygen ions separated from the broken silicon-oxygen bonds may oxidize the substrate silicon near the gate dielectric layer, which increases thickness of the gate dielectric layer.

[0022] As previously described, the equation defines the body effect parameter:

$$\gamma = \sqrt{2\epsilon_0 q N_a} / C_{ox}$$

[0023] An increase in the thickness of the gate dielectric layer will lead to a reduction of C_{ox} , i.e., the capacitance per unit area of the gate dielectric layer. Therefore, the body effect, and thus the threshold voltage, can be improved by increasing the thickness of the gate dielectric layer.

[0024] Moreover, as boron fluoride ions are heavier than boron ions, they may block subsequent boron ions from diffusing, so as to control horizontal diffusion of boron. Such limiting of horizontal diffusion may further improve the body effect, and thus the threshold voltage.

[0025] Fig. 1 illustrates a flow chart of a method for forming an ultra-shallow junction structure according to an embodiment of the present disclosure. The method includes:

[0026] Step S101: providing a semiconductor substrate;

[0027] Step S102: implanting first ions into the semiconductor substrate, to form a first implantation region;

[0028] Step S103: implanting second ions into the first implantation region, to amorphize the first implantation region;

[0029] Step S104: implanting third ions into the amorphized first implantation region, to form an ultra-shallow junction structure.

[0030] Fig. 2 to Fig. 6 are schematic cross-sectional views of a device in various stages of the method for forming an ultra-shallow junction structure according to an embodiment of the disclosure. The present embodiment is described with an example by which a Lightly Doped Drain (LDD) of a PMOS transistor is formed as an ultra-shallow junction structure.

[0031] As shown in Fig. 2, a semiconductor substrate 101 is provided. The

semiconductor substrate 101 may be monocrystalline silicon or silicon-germanium, or Silicon On Insulator (SOI). Alternatively, the semiconductor substrate 101 may include other materials such as III- V compound semiconductors, e.g., gallium arsenide.

5 [0032] An N-type well and a channel region (not shown) are formed in the semiconductor substrate 101. An isolation structure (not shown) may also be formed in the semiconductor substrate 101. Such an isolation structure may be, for example, a LOCOS region formed by local oxidation, or a shallow trench isolation structure.

10 [0033] As shown in Fig. 3, a gate dielectric layer 102 is formed on a surface of the semiconductor substrate 101. The gate dielectric layer 102 may be silicon oxide, silicon nitride or a High-k dielectric material. The gate dielectric layer 102 may have a thickness ranging from tens of Ångströms to hundreds of Ångströms. The gate dielectric layer 102 may be formed by, for example, thermal oxidation, Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), or Plasma Enhanced Chemical Vapor Deposition (PECVD).

15 [0034] Referring to Fig. 3, a gate electrode layer 103 is formed over the gate dielectric layer 102. The gate electrode layer 103 may be polycrystalline silicon, having a thickness ranging from hundreds of Ångströms to thousands of Ångströms. The gate electrode layer 103 may be formed by Low Pressure Chemical Vapor Deposition (LPCVD).

20 [0035] Next, the gate dielectric layer 102 and the gate electrode layer 103 are patterned using a resist mask, to form a gate structure. The gate structure includes the gate dielectric layer 102 and the gate electrode layer 103. The region of the substrate 101 on opposite sides of and separated by the gate structure are referred to herein as a source region and a drain region of the semiconductor substrate 101.

25 [0036] As shown in Fig. 4, a first implantation 105 is performed to implant first ions into the source region and the drain region using the gate structure as a mask. The first implantation may be performed with an accelerating energy ranging from 10 Kev to 30 Kev and a dose ranging from $1\text{E}15/\text{cm}^2$ to $3\text{E}15/\text{cm}^2$. A first implantation region 104 is formed by the first implantation. In one embodiment, the first ions may be boron
30 fluoride ions.

[0037] As shown in Fig. 5, a second implantation 106 is performed to implant second ions into the first implantation region 104 using the gate structure as a mask. The second implantation may be performed with an accelerating energy ranging from 30 Kev to 60 Kev and a dose ranging from $1\text{E}15/\text{cm}^2$ to $9\text{E}15/\text{cm}^2$, so as to amorphize the
35 first implantation region 104. The second ions may be tetravalent ions. In one

embodiment, the second ions may be silicon or germanium.

[0038] The second implantation is performed to cause amorphization in the first implantation region, so that crystal structures in the first implantation region may be disordered, which may limit diffusion of subsequent-implanted ions.

5 [0039] As an example, the amorphization may be performed using silicon ions with an energy of 40 Kev and a dose of $9E15/cm^2$.

[0040] Next, as shown in Fig. 6, a third implantation 107 is performed to implant third ions into the amorphized first implantation region 104 using the gate structure as a mask. The third implantation may be performed with an accelerating energy ranging from 5
10 Kev to 12 Kev and a dose ranging from $1E13/cm^2$ to $1E14/cm^2$. The third ions may be boron ions. As a result, an ultra-shallow junction structure is formed.

[0041] As an example of the third implantation 107, the energy of boron ions may be 10 Kev, and the dose may be $5.0E13/cm^2$.

15 [0042] As shown in Fig. 7, a method is provided according to an embodiment for forming a PMOS transistor. The method includes:

[0043] Step S201: providing a semiconductor substrate;

[0044] Step S202: forming a gate structure on the semiconductor substrate, which defines a source region and a drain region of the substrate separated by the gate structure and on respective sides thereof;

20 [0045] Step S203: performing a first implantation to implant first ions into the source region and the drain region by using the gate structure as a mask, to form a first implantation region;

[0046] Step S204: performing a second implantation to implant second ions into the first implantation region by using the gate structure as a mask, to amorphize the first
25 implantation region;

[0047] Step S205: performing a third implantation to implant third ions into the amorphized first implantation region by using the gate structure as a mask, thereby forming an ultra-shallow junction structure;

[0048] Step S206: forming sidewall spacers on both sides of the gate structure;

30 [0049] Step S207: heavily-doping the source region and the drain region, to form a source and a drain;

[0050] Step S208: performing thermal processing of the semiconductor substrate, to

form a PMOS transistor.

[0051] The method for forming the ultra-shallow junction structure in the PMOS transistor is similar to the embodiment described above with respect to Figs. 2-6. For example, steps S203 through S205 generally correspond to steps S102 through S104, respectively. Accordingly, the description of the method for forming a PMOS in accordance with the second embodiment does not repeat the description of the previously described steps for forming an ultra-shallow junction, but assumes previous performance of those steps. Accordingly, the method for forming the PMOS transistor of the present embodiment may start with an ultra-shallow junction structure similar to the ultra-shallow junction structure in Fig. 6.

[0052] As shown in Fig. 8, sidewall spacers 106 are formed on both sides of the gate structure formed of the gate dielectric layer 102 and the gate electrode 103. The method for forming the sidewall spacers 106 may include: forming a dielectric layer (not shown) on the semiconductor substrate 101 and etching back the dielectric layer. The dielectric layer (not shown) may be formed by Low Pressure Chemical Vapor Deposition (LPCVD). The dielectric layer may have a thickness greater than the height of the gate electrode 103, for facilitating the etch back. The dielectric layer may be silicon oxide, or have an Oxide-Nitride-Oxide (ONO) structure. The sidewall spacers 106 may be used for protecting the gate electrode 103.

[0053] As shown in Fig. 9, a source 111 and a drain 112 are formed by implanting ions into the source region and the drain region using the gate structure as a mask. In one embodiment, the implanted ions are P-type, e.g., boron or arsenic ions. The implantation may be performed at a dose having an order of magnitude in the range of 10^{14} - $10^{15}/\text{cm}^2$, and an energy in the range of 10-100 keV.

[0054] After the implantation in Fig. 9, thermal processing would be performed on the semiconductor substrate to complete forming the PMOS transistor.

[0055] The thermal processing may include performing spike annealing of the semiconductor substrate structure. The spike annealing may activate dopant ions, and recover crystal structure of the semiconductor substrate damaged due to ion implantation. The spike annealing may include: heating the semiconductor substrate to a certain temperature; maintaining the temperature for a period of time; rapidly increasing the temperature; and immediately cooling down when a peak temperature is reached. Key parameters of the spike annealing include the peak temperature of a temperature curve, dwell time of the peak temperature, and temperature divergence (i.e., time of the annealing temperature maintained near to the peak temperature). In one

embodiment, the peak temperature of spike annealing may range from 1000 to 1100 ° C.

5 [0056] Tests have shown that with the method according to the present disclosure, the body effect parameter of the PMOS transistor can be doubled, thereby doubling the threshold voltage of the PMOS transistor.

10 [0057] Embodiments described above are not to limit the scope of the invention. Those skilled in the art may use the methods and technical disclosure described herein to make various alternations and modifications to the disclosure without departing from the spirit and scope of the invention. Therefore, any simple modifications, equivalents or adjustments to the embodiments above based on the technical essence of the disclosure and without departing from the technical solution of the present disclosure should be considered to be included in the scope of the invention.

CLAIMS

1. A method for forming an ultra-shallow junction, comprising:

implanting first ions into a semiconductor substrate, to form a first implantation region;

5 implanting second ions into the first implantation region to amorphize the first implantation region; and

implanting third ions into the amorphized first implantation region, to form an ultra-shallow junction structure.

10 2. The method according to claim 1, wherein the implanting the first ions comprises implanting boron fluoride ions.

15 3. The method according to claim 1, wherein the implanting the first ions comprises implanting the first ions with energy in a range from 10 Kev to 30 Kev, and a dose in a range from $1\text{E}15/\text{cm}^2$ to $3\text{E}15/\text{cm}^2$.

4. The method according to claim 1, wherein the implanting the second ions comprises implanting tetravalent ions.

20 5. The method according to claim 1, wherein the implanting the second ions comprises implanting the second ions with energy in a range from 30 Kev to 60 Kev, and a dose in a range from $1\text{E}15/\text{cm}^2$ to $9\text{E}15/\text{cm}^2$.

25 6. The method according to claim 1, wherein the implanting the third ions comprises implanting boron ions.

7. The method to claim 1, wherein the implanting the third ions comprises implanting the third ions with energy in a range from 0.5 Kev to 12 Kev, and a dose in a range from $1\text{E}13/\text{cm}^2$ to $1\text{E}14/\text{cm}^2$.

30

8. A method for forming a PMOS transistor, comprising:

forming a gate structure on a semiconductor substrate, wherein a source region and a drain region are defined in the substrate on opposite sides of the gate structure;

5 implanting first ions into the source region and the drain region by using the gate structure as a mask, to form a first implantation region;

implanting second ions into the first implantation region by using the gate structure as a mask, to amorphize the first implantation region; and

implanting third ions into the amorphized first implantation region by using the gate structure as a mask, to form an ultra-shallow junction structure.

10

9. The method according to claim 8, wherein the implanting the first ions comprises implanting boron fluoride ions.

15 10. The method according to claim 8, wherein the implanting the first ions comprises implanting the first ions with energy in a range from 10 Kev to 30 Kev, and a dose in a range from $1\text{E}15/\text{cm}^2$ to $3\text{E}15/\text{cm}^2$.

11. The method according to claim 8, wherein the implanting the second ions comprises implanting tetravalent ions.

20

12. The method according to claim 8, wherein the implanting the second ions comprises implanting the second ions with energy in a range from 30 Kev to 60 Kev, and a dose in a range from $1\text{E}15/\text{cm}^2$ to $9\text{E}15/\text{cm}^2$.

25 13. The method according to claim 8, wherein the implanting the third ions comprises implanting boron ions.

30 14. The method according to claim 8, wherein the implanting the third ions comprises implanting the third ions with energy in a range from 0.5 Kev to 12 Kev, and a dose in a range from $1\text{E}13/\text{cm}^2$ to $1\text{E}14/\text{cm}^2$.

15. An ultra-shallow junction, comprising:

a semiconductor substrate; and

a junction structure in the substrate, the junction structure including a first ion implantation region including an amorphized structure; and second ions implanted into the amorphized structure.

16. The ultra-shallow junction according to claim 15, further comprising third ions implanted to form the amorphized structure into the first implantation region.

17. A method for manufacturing a PMOS transistor, comprising:

implanting first ions into a source region and a drain region of a substrate ;

implanting second ions into regions of the first ion implanting; and

implanting third ions into regions of the second ion implanting.

18. The method according to claim 17, wherein the implanting second ions includes implanting tetravalent ions.

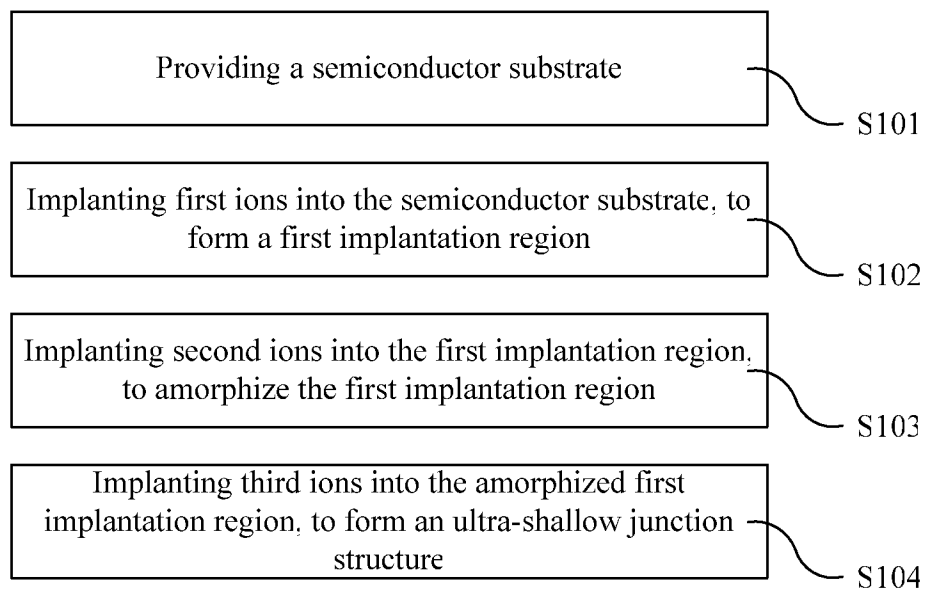
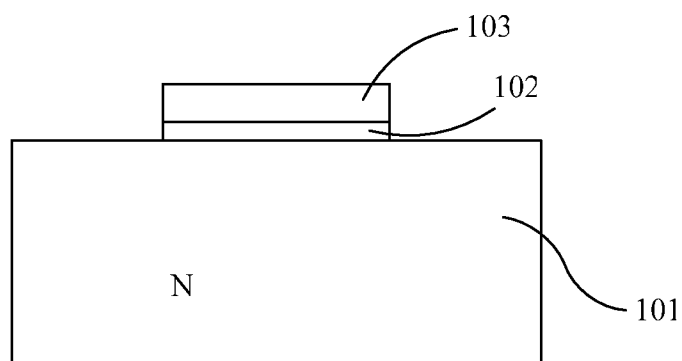
19. The method according to claim 17, further comprising:

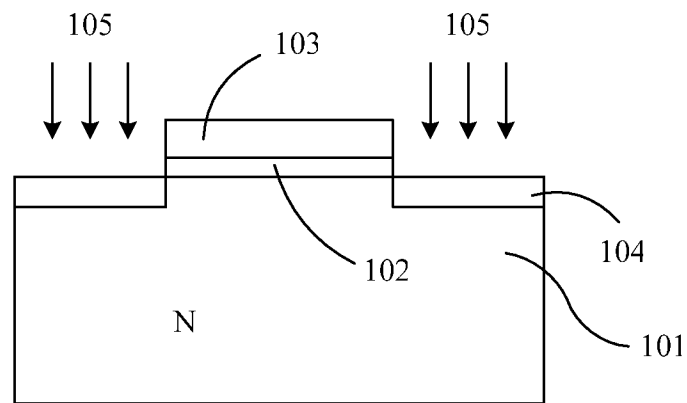
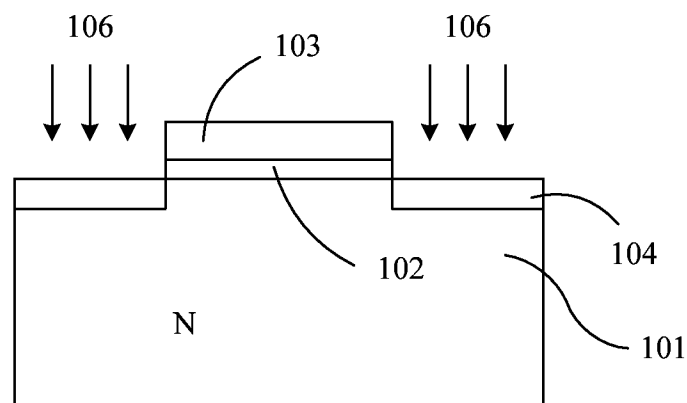
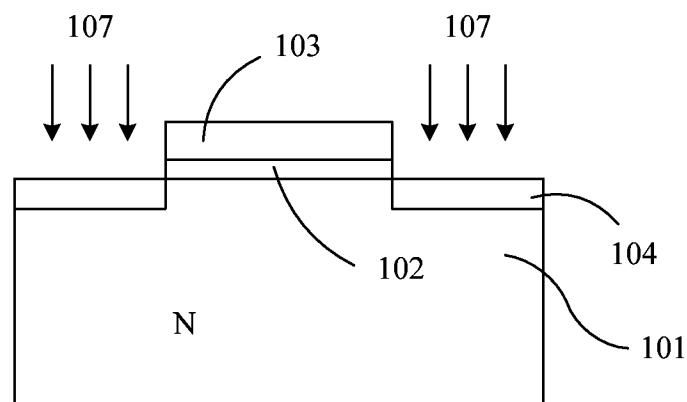
forming a gate structure on the substrate, wherein

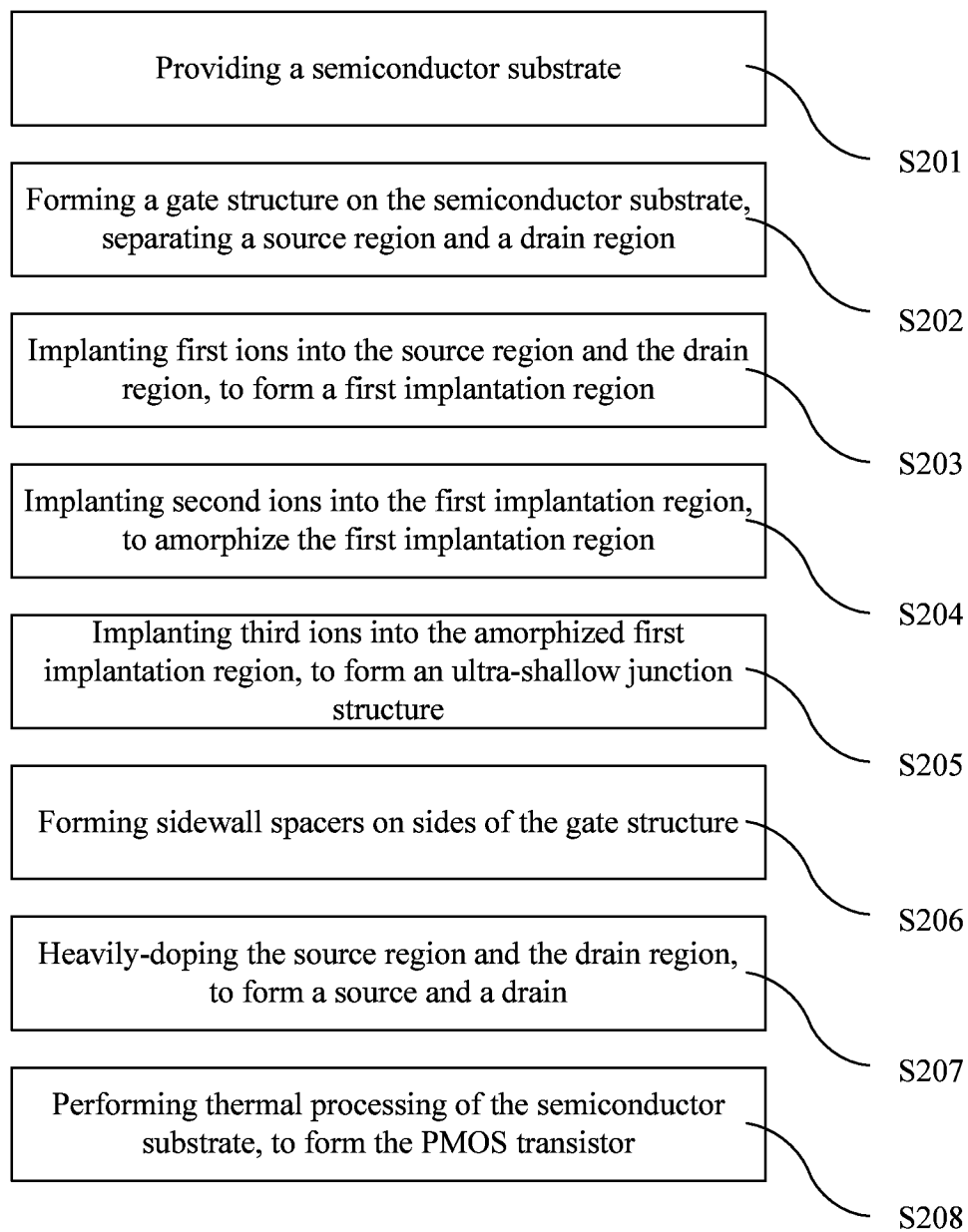
the source region and the drain region are formed in the substrate on opposite sides of the gate structure;

wherein the implanting the second ions includes amorphizing the first ion implanted regions; and

wherein the implanting the third ions includes implanting the third ions into the amorphized first ion implanted regions.

**FIG. 1****FIG. 2****FIG. 3**

**FIG. 4****FIG. 5****FIG. 6**

**FIG. 7**

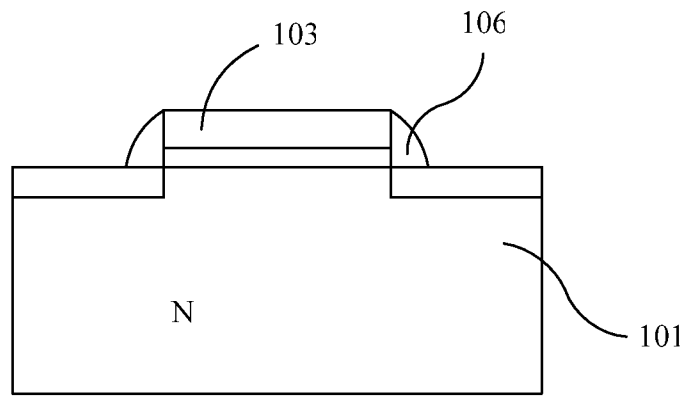


FIG. 8

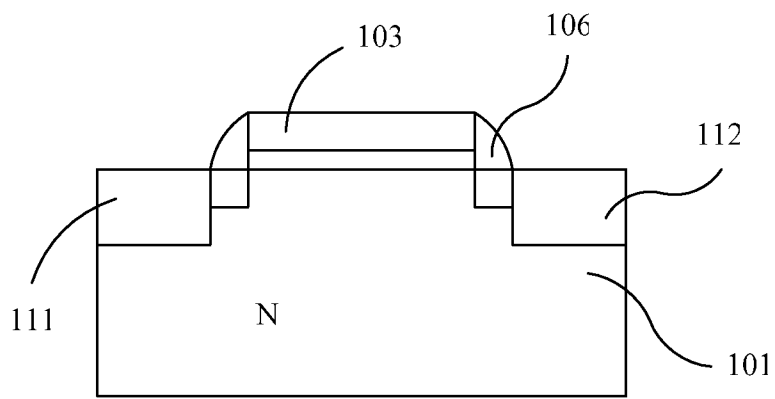


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2010/079240

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L 21/-; H01L 27/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI; EPODOC; CPRS; CNKI and KEYWORDS: ultra, shallow, junction, implantation, ion, injection, gate, energy, dose, MOS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN1744291A(SHANGHAI HONGLI SEMICONDUCTOR MFR CO LTD) 08 Mar.2006 (08.03.2006) page 2,line 10-page 3,line 5 of description, figs.1-3	1-19
X	CN1397987A(WANGHONG ELECTRONICS CO LTD) 19 Feb.2003(19.02.2003) page 4,line 2-page 5,line 3 of description, figs.6-10	1-19
X	CN101459081A(SEMICONDUCTOR MFG INT SHANGHAI CORP) 17 Jun.2009(17.06.2009) page 4,line 8-page 8,line 8 of description, figs.5-9	1-19
X	US2008/0160710A1(OH) 03 Jul.2008(03.07.2008) paragraphs [0016]-[0034] of description	1-19
A	US2007/0093033A1(WANG et al.)26 Apr.2007(26.04.2007) the whole document	1-19
A	US6727136B1(BULLER et al.)27 Apr.2004(27.04.2004) the whole document	1-19

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 11 Feb.2011(11.02.2011)	Date of mailing of the international search report 24 Feb. 2011 (24.02.2011)
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
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INTERNATIONAL SEARCH REPORT

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CLASSIFICATION OF SUBJECT MATTER

H01L 21/265 (2006.01) i

H01L 21/336 (2006.01) i