



(43) International Publication Date
28 June 2012 (28.06.2012)

- (51) International Patent Classification:
H01L 29/06 (2006.01) *H01L 21/336* (2006.01)
H01L 29/78 (2006.01)
- (21) International Application Number:
PCT/CN2011/083110
- (22) International Filing Date:
29 November 2011 (29.11.2011)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
201010603278.X 23 December 2010 (23.12.2010) CN
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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

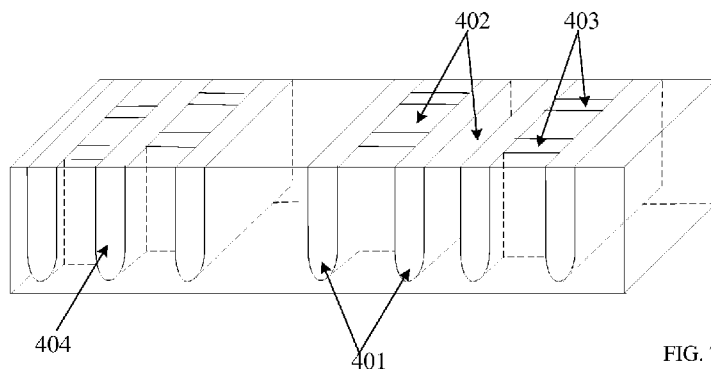


FIG. 7

(57) Abstract: A semiconductor device includes a substrate, an active region located in the substrate, a plurality of field limiting rings (402) formed in the substrate and located outside the active region, a plurality of isolation trenches (401) formed between the field limiting rings (402), and a connection channel (403) electrically connecting at least two adjacent isolation trenches (401).



Description

Title of Invention: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

[1] TECHNICAL FIELD

[2] The present disclosure relates to manufacturing of a semiconductor component and, more particularly, to a semiconductor device and a method for fabricating a semiconductor device.

[3] BACKGROUND

[4] High-voltage power semiconductor devices, such as Trench MOS (Trench Metal-Oxide Semiconductor) devices, VDMOS devices, IGBT devices, etc., are widely used due to their special features such as high frequency, high switching speed, and high controlling efficiency. Blocking capability is a factor for evaluating the level of development of high-voltage power semiconductor devices. Depending on its application, a breakdown voltage of high-voltage power semiconductor device can be in a range from 25V to 6000V. However, modern planar-structured semiconductor devices usually have a shallow junction depth and a curved junction edge, resulting in a decreased voltage capability and a poor voltage stability. Such devices have a narrow safe working range and are easy to break down. In order to increase the voltage capability of a device, besides adjusting the parameters of the device, one may also need to properly treat the PN junction ending at the device surface, thus improving the electric field distribution, reducing the concentration of surface electric field, and increasing the voltage capability and the stability of the device.

[5] A conventional method to increase the voltage capability and the stability of a device includes placing a field limiting ring (FLR) at a periphery of the device. This method is suitable for vertical current MOS devices, such as Trench MOS, VDMOS, etc., as they have a higher current processing capability and current gain. The field limiting ring can reduce the concentration of surface electric field, thus increasing the voltage capability. In addition, the field limiting ring is compatible to the low voltage IC process and is thus suitable for smart power IC's (SPIC's) and discrete high-voltage devices. Furthermore, the field limiting ring located at an edge of a depletion region of a device can serve as a high voltage sensor to drive a protection circuit in an SPIC, thus increasing the sensitivity of the SPIC.

[6] There are two conventional methods to form the field limiting ring, which will be described in greater details while taking a Trench MOS as an example.

[7] FIGS. 1 and 2 illustrate a method for fabricating field limiting rings according to a first conventional method. FIG. 1 is a top view of a semiconductor chip fabricated

using the first conventional method, and FIG. 2 is a cross-sectional view of the chip. According to the first conventional method, field limiting rings 104 are formed at an edge of the chip by implantation. The voltage capability of the chip is increased since the field limiting rings 104 take a portion of the applied voltage.

[8] As shown in FIG. 2, the field limiting rings 104 are formed by the following process. First, after main junctions 102 of an active region and trenches 103 are formed in a substrate 101, a photoresist is spin-coated on a surface of the substrate 101 and processed to form a photoresist layer 105 having a pattern corresponding to field limiting rings. Then, the field limiting rings 104 are formed by ion implantation using the photoresist layer 105 as a mask. In other words, this method needs a separate photolithography process to define an implantation area for forming the field limiting rings 104. Due to this extra photolithography step, cost is increased.

[9] FIGS. 3 and 4 illustrate a method for fabricating field limiting rings according to a second conventional method. FIG. 3 is a top view of a semiconductor chip fabricated using the second conventional method, and FIG. 4 is a cross-sectional view of the chip. Some commercial low-voltage MOS's are formed using the second conventional method. In this method, to reduce cost, the field limiting rings are formed using a trench isolation implantation method to omit the extra photolithography step employed in the first conventional method.

[10] As shown in FIG. 4, field limiting rings 205 are formed by the following process. First, trenches 202 in an active region and isolation trenches 204 for isolating the field limiting rings are formed in a substrate 201. Then, main junctions 203 in the active region and the field limiting rings 205 are formed by ion implantation. Although the cost of the second conventional method is lower than that of the first conventional method, the field limiting rings formed according to the second conventional method usually have a poor voltage dividing capability and thus the voltage capability of the chip is limited. The reasons are as follows.

[11] In the second conventional method, since the field limiting rings are formed by trench isolation implantation, a maximum width of a depletion region of each field limiting ring 205 equals a width of one isolation trench 204, which is very small. Therefore, the voltage-dividing capability of the field limiting rings 205 cannot reach an optimum voltage-dividing capability corresponding to a doping concentration in the field limiting rings 205. When a voltage is applied, a region between neighboring field limiting rings 205 is quickly depleted, That is, before one field limiting ring 205 reaches its optimum voltage-dividing capability, the depletion region may have extended to its neighboring field limiting ring 205. Since the electrical potential within the field limiting rings 205 is identical, the regions in the field limiting rings 205 are not depleted. In other words, in the chip fabricated by the second conventional method,

a total width of the depletion region of all the field limiting rings is the sum of the widths of the isolation trenches 204. Therefore, the voltage dividing capability of the field limiting rings 205, and thus the voltage capability of the chip, are limited.

- [12] One way to extend the depletion region of the field limiting rings 205 is to increase the widths of the isolation trenches 204. However, the widths of the isolation trenches 204 may not be increased as much as desired, because they are limited by a subsequent gate material (such as polysilicon) filling process (usually a thin film deposition process). The maximum widths of the isolation trenches 204 usually should not be larger than about 1.2 times of the thickness of the polysilicon film to prevent gaps from occurring during the deposition process. Such maximum widths are still smaller than the width that the field limiting rings 205 required to achieve their optimum voltage-dividing capability.

[13] SUMMARY

- [14] In accordance with the present disclosure, there is provided a semiconductor device. The semiconductor device includes a substrate, an active region located in the substrate, a plurality of field limiting rings formed in the substrate and located outside the active region, a plurality of isolation trenches formed between the field limiting rings, and a connection channel electrically connecting at least two adjacent isolation trenches.

- [15] Also in accordance with the present disclosure, there is provided a method for fabricating a semiconductor device. The method includes providing a substrate, and simultaneously forming an active region trench, a plurality of isolation trenches, and a connection trench in the substrate. The connection trench electrically connects at least two adjacent isolation trenches. The method further includes simultaneously forming an active region main junction and a plurality of field limiting rings. The field limiting rings are formed between the isolation trenches.

- [16] Also in accordance with the present disclosure, there is provided a method for fabricating a semiconductor device. The method includes providing a substrate having an active region, and forming, in the substrate, a plurality of field limiting rings outside the active region and a plurality of isolation trenches between the field limiting rings, forming a dielectric layer over the substrate, and forming a via in the dielectric layer. The via extends to the isolation trenches. The method further includes filling the via with a metal, and forming a metal layer over the dielectric layer. The metal in the via and the metal layer form a connection channel connecting at least two adjacent isolation trenches.

- [17] Features consistent with the present disclosure will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the present disclosure. Such features will be realized and

attained by means of the elements and combinations particularly pointed out in the appended claims.

[18] BRIEF DESCRIPTION OF THE DRAWINGS

[19] The components in the drawings are not necessarily drawn to scale, but merely to illustrate the concept of the present disclosure. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the views.

[20] FIG. 1 is a schematic top view of a semiconductor device fabricated according to a first conventional method;

[21] FIG. 2 is a schematic cross-sectional view of the semiconductor device fabricated according to the first conventional method;

[22] FIG. 3 is a schematic top view of a semiconductor device fabricated according to a second conventional method;

[23] FIG. 4 is a schematic cross-sectional view of the semiconductor device fabricated according to the second conventional method;

[24] FIG. 5 is a schematic cross-sectional view of a semiconductor device consistent with an embodiment of the present disclosure;

[25] FIG. 6 is a schematic top view of a semiconductor device consistent with another embodiment of the present disclosure;

[26] FIG. 7 is a schematic perspective view of the semiconductor device shown in FIG. 6;

[27] FIGS. 8-14 show a method for fabricating a semiconductor device according to an embodiment of the present disclosure;

[28] FIG. 15 is a schematic cross-sectional view of a semiconductor device consistent with a further embodiment of the present disclosure.

[29] DETAILED DESCRIPTION

[30] The disclosure is illustrated by way of examples and not by way of limitation in the accompanying drawings, in which like references indicate same or similar elements. It should be noted that references to 'an' or 'one' embodiment in this disclosure are not necessarily to the same embodiment, and such references mean at least one.

[31] FIG. 5 is a schematic cross-sectional view of a semiconductor device consistent with embodiments of the present disclosure.

[32] The semiconductor device shown in FIG. 5 includes a substrate 301. In some embodiments, the substrate 301 may be formed of an elementary semiconductor material, such as monocrystalline, polycrystalline, or amorphous silicon or silicon-germanium (Si-Ge). In some embodiments, the substrate 301 may be formed of a compound semiconductor material, such as silicon carbide, indium antimonide, lead telluride, gallium arsenide, indium phosphide, gallium arsenide, gallium antimonide, semiconductor alloy, or any combination thereof. In some embodiments, the substrate 301 may be a silicon on insulator (SOI). Alternatively, the substrate 301 may include a multi-layered

structure including an epitaxial layer or a buried layer. Although several examples of materials suitable for the substrate 301 are described, any materials that can be used as the substrate 301 fall within the spirit and scope of the present disclosure.

- [33] As shown in FIG. 5, the semiconductor device also includes an active region 310 formed in the substrate 301, a plurality of field limiting rings 305 formed outside the active region, and a plurality of isolation trenches 304 are located between the plurality of field limiting rings 305. Trenches 302 are formed in the active region. As shown in FIG. 5, among the isolation trenches 304, at least two adjacent ones are electrically connected by a connection channel 306. The field limiting ring located between two connected isolation trenches may have a same induction potential as the electrical potential of the connected isolation trenches.
- [34] Consistent with embodiments of the present disclosure, the connection channel 306 may be implemented in many ways, such as connection trench, metal, etc.
- [35] Consistent with embodiments of the present disclosure, the plurality of field limiting rings 305 are formed as follows. First, active region trenches 302 and isolation trenches 304 configured for isolating field limiting rings are formed in the substrate 301. Then, a main junction 303 of the active region and a plurality of field limiting rings 305 are formed simultaneously by ion implantation.
- [36] When forming the semiconductor device consistent with embodiments of the present disclosure, since the plurality of field limiting rings 305 and the main junction 303 of the active region are formed simultaneously, the photolithography step required in the first conventional method is not needed. Therefore, the cost is reduced. In some embodiments, the field limiting rings 305 and the main junction 303 of the active region may have the same doping state.
- [37] When a reverse bias voltage applied to the main junction 303 increases, an edge electric field of the semiconductor device increases. If the edge electric field reaches a critical electric field, the main junction 303 will be broken down. However, in the device consistent with embodiments of the present disclosure, before avalanche breakdown in the main junction 303 occurs, the depletion region of the main junction 303 has already extended to a ring junction of the field limiting rings. That is, the depletion region of the PN junction extends through the field limiting rings 305, and thus the depletion layer of the main junction 303 and the depletion layer of the ring junction of the field limiting rings 305 are connected with each other. As a result, a ring junction electric field is inductively created adjacent to the field limiting rings 305. Since the ring junction electric field of the field limiting rings 305 and the main junction electric field have the same direction, the total electric field is a superposition of these two electric fields. Thus, the electrical potential difference borne by the main junction 303 is decreased. When the applied voltage further increases, the field limiting

rings 305 bear the additional voltage, such that the increase of voltage on the main junction 303 may be limited.

- [38] In other words, the field limiting rings 305 may function as a voltage divider disposed at the edge of the planar power device, distributing the applied voltage to a longer range. Therefore, breakdown of the main junction 303 due to high applied voltage may be avoided.
- [39] The width of the depletion region of the field limiting rings 305 may affect their voltage dividing capability. In the device consistent with embodiments of the present disclosure, since a set of adjacent isolation trenches 304 are electrically connected, the inductive electric potential of the field limiting ring 305 located between the set of connected isolation trenches 304 may be the same as the electrical potential of the set of connected isolation, and thus this field limiting ring 305 is shielded by the set of connected isolation trenches 304. Therefore, the width of the depletion region of a single field limiting ring 305 equals the sum of a horizontal width of the set of connected isolation trenches 304 and a horizontal width of the field limiting ring 305 located between the set of connected isolation trenches 304. In contrast, in the device fabricated by the second conventional method, the width of the depletion region of a single field limiting ring is the horizontal width of a single isolation trench. Therefore, in the device consistent with embodiments of the present disclosure, the voltage dividing capability of the field limiting rings 305 is improved.
- [40] It is understood that, the number of the field limiting rings 305 and that of the isolation trenches 304 are not limited to a specific number. In addition, the number of isolation trenches 304 in the set of connected isolation trenches 304 is also not limited to a specific number. In some embodiments, two or three isolation trenches 304 may be connected, depending on features that may affect the breakdown voltage and the voltage dividing capability, such as the amount of surface charges of the semiconductor device (generally, for a bipolar device, the more the surface charges are, the lower is the breakdown voltage), the doping concentration in the substrate (generally, the lower the doping concentration is, the higher is the breakdown voltage), the junction depth (generally, the breakdown voltage increases as the junction depth increases), and the thickness of the substrate.
- [41] FIGS. 6 and 7 show a semiconductor device consistent with embodiments of the present disclosure. FIG. 6 is a top view and FIG. 7 is a perspective view. The semiconductor device shown in FIGS. 6 and 7 has a similar structure as that shown in FIG. 5.
- [42] In the semiconductor device shown in FIGS. 6 and 7, each isolation trench 401 is connected, with one of its neighboring isolation trenches 401 by connection trenches 403. The connection trenches 403 serve as the connection channel 306 shown in FIG.

5.

- [43] Consistent with embodiments of the present disclosure, the connection trenches 403, the isolation trenches 401, and active region trenches 404 are formed by the same photolithography process. Accordingly, the connection trenches 403, the isolation trenches 401, and the active region trenches 404 may have a same doping state.
- [44] The doping state includes doping concentration and impurity type. Having a same doping state means having a same doping concentration and a same impurity type.
- [45] In some embodiments, a substrate of the device shown in FIGS. 6 and 7 may include an epitaxial layer, and the isolation trenches 401, the connection trenches 403, field limiting rings 402, and the active region are formed in the epitaxial layer. The main filling material for the isolation trenches 401, the connection trenches 403, and the active region trenches 404 may be polysilicon. In some embodiments, an isolation oxide layer may be formed on the sidewall of the trenches before filling in the polysilicon. The isolation oxide layer may be formed together with gate oxide in a cellular region.
- [46] The semiconductor device shown in FIGS. 6 and 7 is a trench MOS device. The field limiting rings 402 and main junction of the active region of the trench MOS device are formed by the same implanting process, and thus have the same doping state.
- [47] It is to be noted that, the number of the connection trenches 403 between the connected isolation trenches 401 and the distance between the connection trenches 403 are not limited, for they depend on the conditions such as doping state, junction depth, substrate thickness, etc.
- [48] FIGS. 8-14, show a method for fabricating a semiconductor device consistent with embodiments of the present disclosure. The method includes the following steps.
- [49] First, a substrate 501 is provided. The substrate 501 may include an epitaxial layer, which may be an N-type epitaxial layer or a P-type epitaxial layer grown on a wafer using CVD method. A thickness of the epitaxial layer may be determined based on application. In some embodiments, the substrate 501 may be a silicon substrate.
- [50] Referring to FIG. 8, an oxide layer is then formed on the substrate 501 as a barrier layer 502. In some embodiments, the barrier layer 502 may be a silicon oxide layer formed using tetraethyl orthosilicate (TEOS) and may be formed by low-pressure CVD (LPCVD) method.
- [51] Next, a photoresist layer 503 is spin coated on a surface of the barrier layer 502. In some embodiments, in order to ensure exposure accuracy, an anti-reflection layer may be formed between the photoresist layer 503 and the barrier layer 502, to reduce unnecessary reflection. After that, the photoresist layer 503 is exposed using a mask having a pattern of active region trenches, isolation trenches, and connection trenches. After developing the exposed photoresist layer 503, a pattern of the active region

trenches, the isolation trenches, and the connection trench is formed thereon (not shown). Next, the barrier layer 502 is dry etched or wet etched using the photoresist layer 503 having the pattern of the active region trenches, the isolation trenches, and the connection trenches as a mask and a pattern of the active region trenches, the isolation trenches, and the connection trenches is formed on the barrier layer 503, as shown in FIG. 9.

- [52] Referring to FIG. 10, the substrate 501 is etched by, for example, a dry etching method or any other suitable etching method, using the barrier layer 502 as a hard mask, such that pattern openings of the active region trenches, the isolation trenches, and the connection trenches are formed in the substrate 501. Then, the photoresist layer 503 and the barrier layer 502 are removed by wet chemical cleaning method.
- [53] Referring to FIG. 11, an oxide layer (not shown) is grown on an inner surface of the pattern openings. Next, a gate material is deposited on a surface of the substrate 501 and filled in the pattern openings.
- [54] In some embodiments, the gate material may be deposited by chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), high density plasma-enhanced chemical vapor deposition (HD-PECVD), or physical vapor deposition (PVD). In some embodiments, the gate material may be undoped polysilicon (which may be doped in later processes) or doped polysilicon.
- [55] Next, referring to FIG. 12, the gate material outside the pattern openings is removed. The gate material left in the pattern openings form active region trenches 504, isolation trenches 505, and connection trenches (not shown).
- [56] In some embodiments, the gate material outside the pattern openings may be removed by CMP, so as to flatten the substrate surface. In some embodiments, the gate material outside the pattern openings may be removed by an etch-back process using a silicon oxide film formed on the surface of the substrate as an etch stop layer, such that a surface of the active region trenches 504, the isolation trenches 505, and the connection trenches is coplanar with the surface of the substrate 501. After that, the silicon oxide film may be removed by wet etching or other method.
- [57] Active region main junction and field limiting rings between the isolation trenches 505 are formed in the substrate 501, simultaneously, by, for example, ion implantation, as shown in FIGS. 13 and 14.
- [58] Referring to FIG. 13, a thin oxide layer is formed on the substrate 501 to serve as an implantation oxide layer. The implantation oxide layer may reduce the damage to the surface of the active region during the ion implantation. It may also prevent the impurity atoms or ions from diffusing out of the substrate. The implant oxide layer may be formed by CVD or thermal oxidation. Then, ion implantation is performed. For an N-type MOSFET, P-type impurities are implanted. Doping ions may be boron ions

and dosage of the implantation may be $1\text{E}13\text{cm}^{-3}$.

- [59] Referring to FIG. 14, after the ion implantation is performed, a high temperature drive-in process is performed to diffuse and activate the implanted ions. During the high temperature drive-in process, implanted ions may be driven deeper into the substrate 501 and form a junction having an expected depth (i.e. diffusion level). The implanted ions may be bonded to the silicon atoms in the lattice. This process activates the implanted ions and forms the active region main junction 506 and the field limiting rings 507.
- [60] In some embodiments, the high temperature drive-in diffusion process may be performed at a temperature in a range from about 1000°C to about 1150°C . In some embodiments, temperature ranges other than the above-noted one may also be employed, depending on actual situations. Thus, the temperature and the time of the high temperature drive-in process are not limited in the present disclosure.
- [61] The implant oxide layer may be kept or may be removed by, for example, wet chemical cleaning method.
- [62] FIG. 15 shows another semiconductor device consistent with embodiments of the present disclosure. The semiconductor device of FIG. 15 includes a substrate 601 and an active region located in the substrate 601. The semiconductor device also includes a plurality of field limiting rings 602 located outside the active region and a plurality of isolation trenches 603 are located between the plurality of field limiting rings 602. Trenches 604 are formed in the active region.
- [63] As shown in FIG. 15, a dielectric layer 605 is formed over the substrate 601. In some embodiments, the dielectric layer 605 may be an interlayer dielectric layer or a pre-metal dielectric layer. A metal layer 606 is formed over the dielectric layer 605. Vias 607 are formed in the dielectric layer 605 and are connected to the metal layer 606. The vias 607 are filled with metal, such as tungsten or copper.
- [64] In the semiconductor device shown in FIG. 15, the metal layer 606 serves as the connection channel 306 shown in FIG. 5. The metal layer 606 is connected to the vias 607 connected to the isolation trenches 603, such that at least two adjacent isolation trenches 603 are electrically connected and have the same electrical potential, as shown in FIG. 15.
- [65] Since the vias 607 positioned above the isolation trenches 603 and the vias positioned above the active region are formed by the same photolithography process, the metal in the vias 607 and the metal plugs in the active region are formed by the same deposition process, and the metal layer 606 above the isolation trenches 603 and the metal layer above the active region are formed by the same photolithography process, no extra photolithography process is necessary. Therefore, cost is reduced.
- [66] In some embodiments, the vias 607 may merely penetrate through the dielectric layer

605. In some embodiments, the vias 607 may further extend into the isolation trenches 603, such that the metal in the vias 607 may provide better connection between the isolation trenches 603 and the metal layer 606.

[67] The semiconductor device shown in FIG. 15 may be formed by a method described below.

[68] First a substrate is provided. Then, an active region, a plurality of field limiting rings outside the active region, and a plurality of isolation trenches between the plurality of field limiting rings are formed in the substrate.

[69] Next, a dielectric layer is formed on the substrate. Vias are then formed in the dielectric layer, exposing the plurality of isolation trenches. The dielectric layer may be an interlayer dielectric layer or a pre-metal dielectric layer.

[70] As described above, the vias positioned above the isolation trenches and the vias positioned above the active region are formed by the same photolithography process. Specifically, a photoresist layer is spin-coated on the dielectric layer. The photoresist layer is then exposed using a mask having a pattern of the vias. After developing, a pattern of the vias is formed in the photoresist layer. Next, the dielectric layer is etched using the photoresist layer as a mask to form the vias in the dielectric layer, including the vias above the isolation trenches and the vias above the active region.

[71] Next, the vias above the isolation trenches and the vias above the active region are filled with metal in a same deposition step. In some embodiments, the metal may be tungsten, and may be deposited using a PVD method. Specifically, a thin titanium layer may first be formed on the dielectric layer. The titanium layer may also be formed on bottoms and sidewalls of the vias as an adhesive for retaining tungsten. A thin titanium nitride may then be formed on the titanium layer as a diffusion stop layer to prevent the diffusion of titanium atoms. Next, tungsten is formed on the titanium nitride using the CVD method, so as to fill the vias. Finally, the tungsten outside the vias is removed by a CMP method, so as to flatten the dielectric layer.

[72] Next, a metal layer is formed on the dielectric layer, forming a connection channel connecting adjacent isolation trenches.

[73] The metal layer above the isolation trenches and the metal layer above the active region are formed during the same photolithography process. Specifically, a metal layer having a sandwich structure is first formed on the dielectric layer. Then, a desired pattern is formed in the metal layer by photolithography and etching processes. Adjacent isolation trenches are connected via the metal in the vias and the metal layer.

[74] Other embodiments of the present disclosure will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following

claims.

Claims

- [Claim 1] A semiconductor device, comprising:
a substrate;
an active region located in the substrate;
a plurality of field limiting rings formed in the substrate and located outside the active region;
a plurality of isolation trenches formed between the field limiting rings;
and
a connection channel electrically connecting at least two adjacent isolation trenches.
- [Claim 2] The semiconductor device according to claim 1, wherein the connection channel is a connection trench.
- [Claim 3] The semiconductor device according to claim 2, further comprising an active region trench formed in the active region,
wherein the connection trench, the isolation trenches, and the active region trench are formed by a photolithography process at a same time.
- [Claim 4] The semiconductor device according to claim 2, wherein the connection trench, the isolation trenches, and the active region trench have a same doping state.
- [Claim 5] The semiconductor device according to claim 1, further comprising a dielectric layer formed over the substrate, the dielectric layer having a via formed therein,
wherein the connection channel comprises:
a metal filled in the via, and
a metal layer formed over the dielectric layer,
wherein the metal filled in the via connects the at least two adjacent trenches to the metal layer.
- [Claim 6] The semiconductor device according to any one of claim 1 to claim 5, wherein the semiconductor device is a trench MOS device, the semiconductor device further comprising a main junction,
wherein the plurality of field limiting rings and the main junction are formed by a same implantation process, and have a same doping state.
- [Claim 7] A method for fabricating a semiconductor device, comprising:
providing a substrate;
simultaneously forming an active region trench, a plurality of isolation trenches, and a connection trench in the substrate, the connection trench electrically connecting at least two adjacent isolation trenches; and

simultaneously forming an active region main junction and a plurality of field limiting rings, the field limiting rings being formed between the isolation trenches.

[Claim 8] The method according to claim 7, wherein the active region main junction and the plurality of field limiting rings are formed by ion implantation.

[Claim 9] A method for fabricating a semiconductor device, comprising:
providing a substrate having an active region;
forming, in the substrate, a plurality of field limiting rings outside the active region, and a plurality of isolation trenches between the field limiting rings;
forming a dielectric layer over the substrate;
forming a via in the dielectric layer, the via extending to the isolation trenches;
filling the via with a metal; and
forming a metal layer over the dielectric layer,
wherein the metal in the via and the metal layer form a connection channel connecting at least two adjacent isolation trenches.

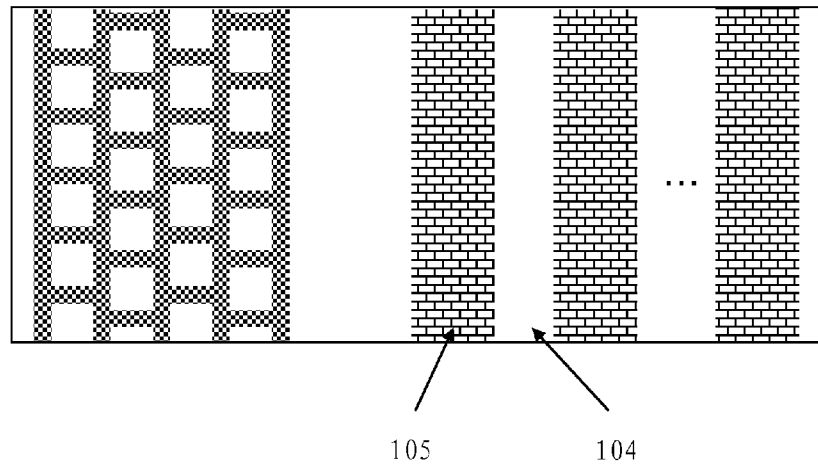


FIG. 1

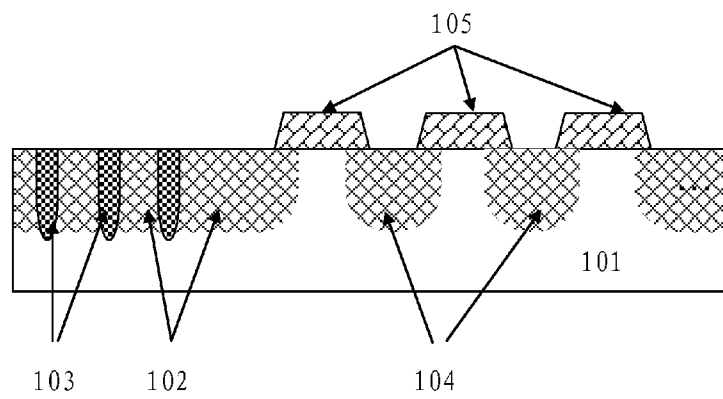


FIG. 2

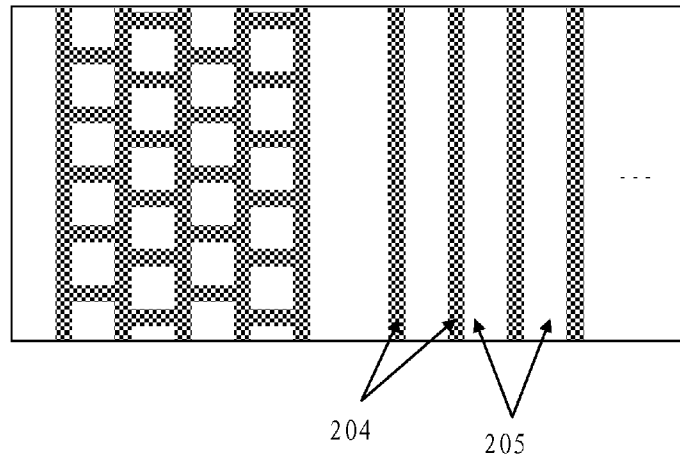


FIG. 3

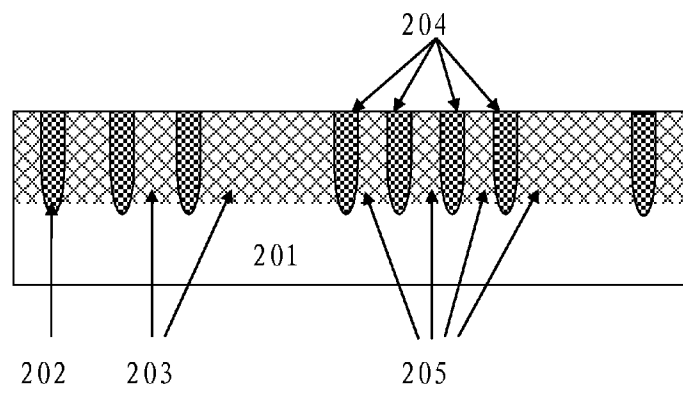


FIG. 4

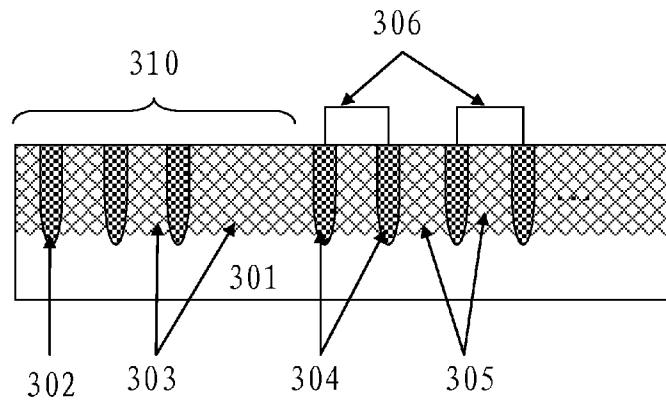


FIG. 5

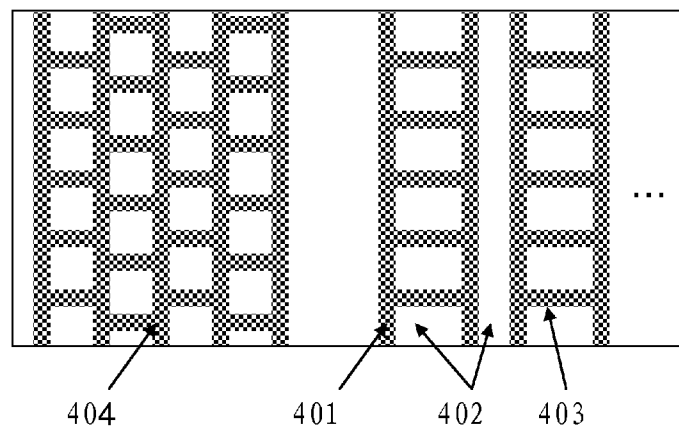


FIG. 6

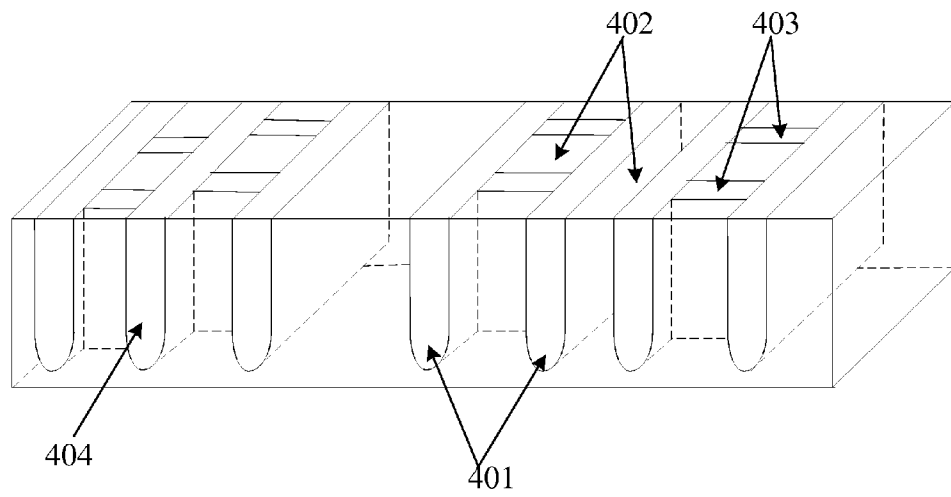


FIG. 7

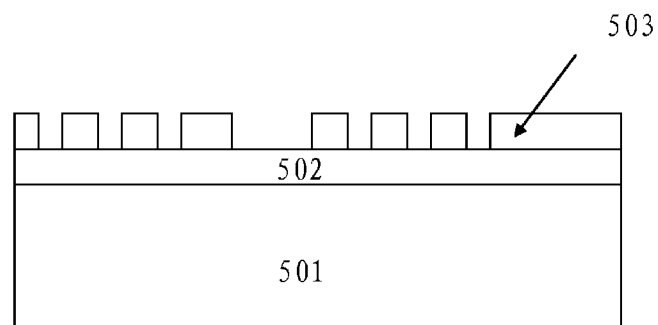


FIG. 8

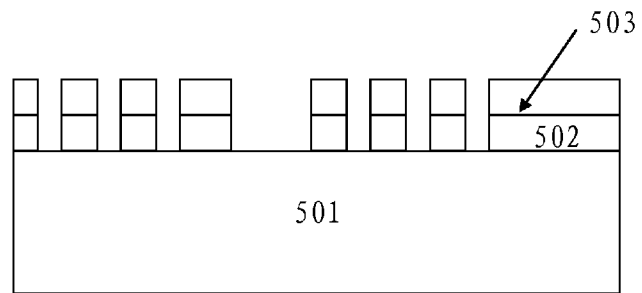


FIG. 9

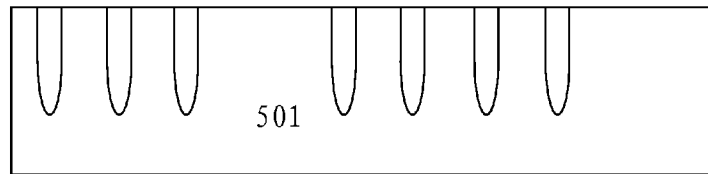


FIG. 10

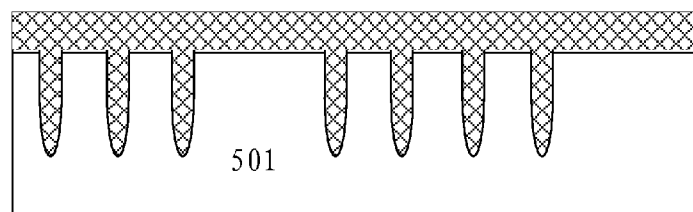


FIG. 11

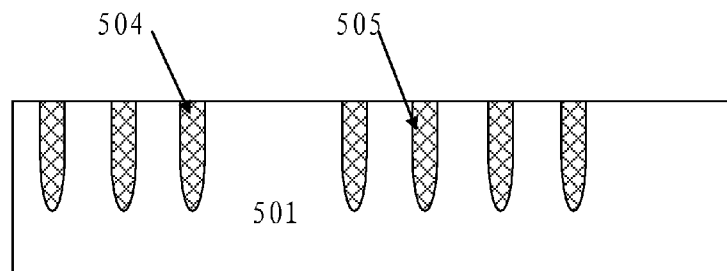


FIG. 12

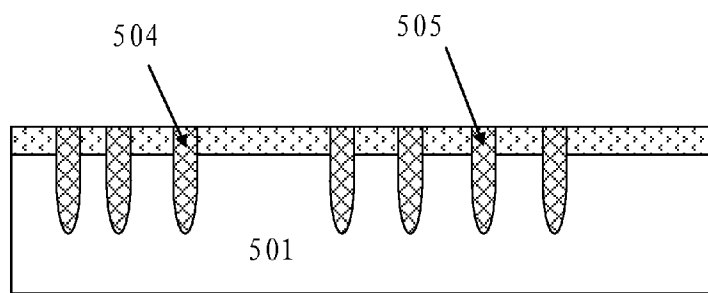


FIG. 13

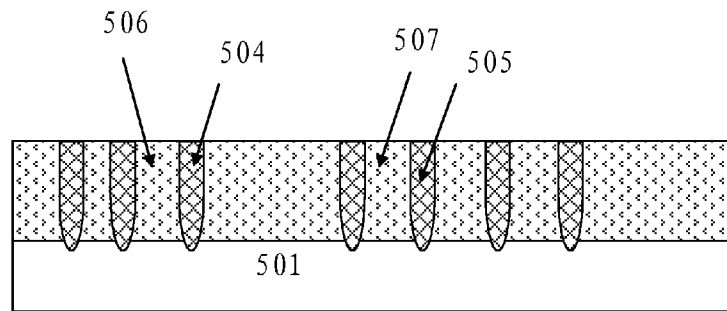


FIG. 14

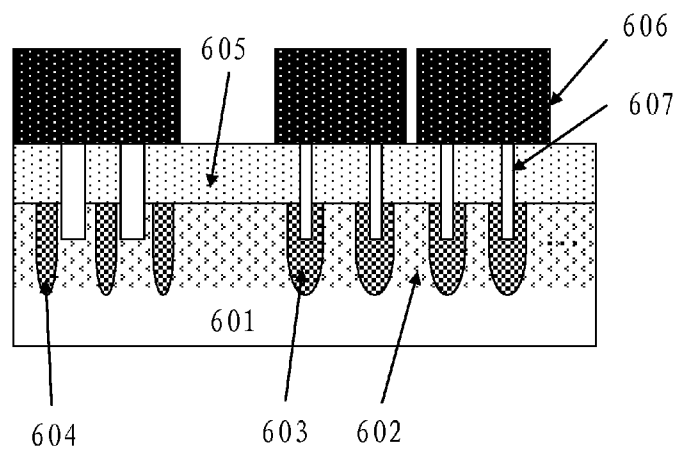


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/083110

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
CNPAT,WPLEPODOC: power, semiconductor, trench, termina+, field, limiting, ring, trench wring, plate, trench w MOS, voltage, +connect+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US2009/0294892A1 (MAXPOWER SEMICONDUCTOR INC.) 03 Dec. 2009 (03.12.2009) paragraphs [0026]-[0030], fig.1a	1
Y		6
Y	US2008/0179662A1 (FORCE-MOS TECHNOLOGY CORPORATION) 31 Jul. 2008 (31.07.2008) paragraphs [0023]-[0027], fig.2A, 4A-4E	6
A		1-5,7-9
A	US2002/0179950A1 (KONINKLIJKE PHILIPS ELECTRONICS N.V.) 05 Dec. 2002 (05.12.2002) THE WHOLE DOCUMENT	1-9
A	CN1799144A (KONINK PHILIPS ELECTRONICS N.V.) 05 Jul. 2006 (05.07.2006) THE WHOLE DOCUMENT	1-9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&”document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 03 Feb. 2012 (03.02.2012)	Date of mailing of the international search report 15 Mar. 2012 (15.03.2012)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer CHE,Xiaolu Telephone No. (86-10)62411843

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/083110

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US2009/0294892A1	03.12.2009	WO2009148695A2	10.12.2009
		WO2009148695A3	04.03.2010
		US7911021B2	22.03.2011
US2008/0179662A1	31.07.2008	US7800185B2	21.09.2010
US2002/0179950A1	05.12.2002	WO02097876A2	05.12.2002
		KR20030023718A	19.03.2003
		US6620669B2	16.09.2003
		EP1407485A2	14.04.2004
		JP2004520724A	08.07.2004
		JP4261335B2	30.04.2009
		WO2004107449A1	09.12.2004
CN1799144A	05.07.2006	EP1634337A1	15.03.2006
		KR20060036393A	28.04.2006
		JP2006526287A	16.11.2006
		US2008116520A1	22.05.2008
		CN100442537C	10.12.2008

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/083110

Continuation of : **CLASSIFICATION OF SUBJECT MATTER**

H01L 29/06 (2006.01) i

H01L 29/78 (2006.01) i

H01L21/336 (2006.01) i