United States Patent

Rosener

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[54] CIRCULAR INTERPOLATION SYSTEM

[72] Inventor: **Harvey J. Rosener**, Dayton, Ohio

[73] Assignee: **Allen-Bradley Company**, Milwaukee, Wis.

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Related U.S. Application Data

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[51] **Int. Cl.**.....**G06f 7/38**, G06f 15/34, G06j 1/02

[58] **Field of Search**.....235/152, 150.31, 156, 92 NT

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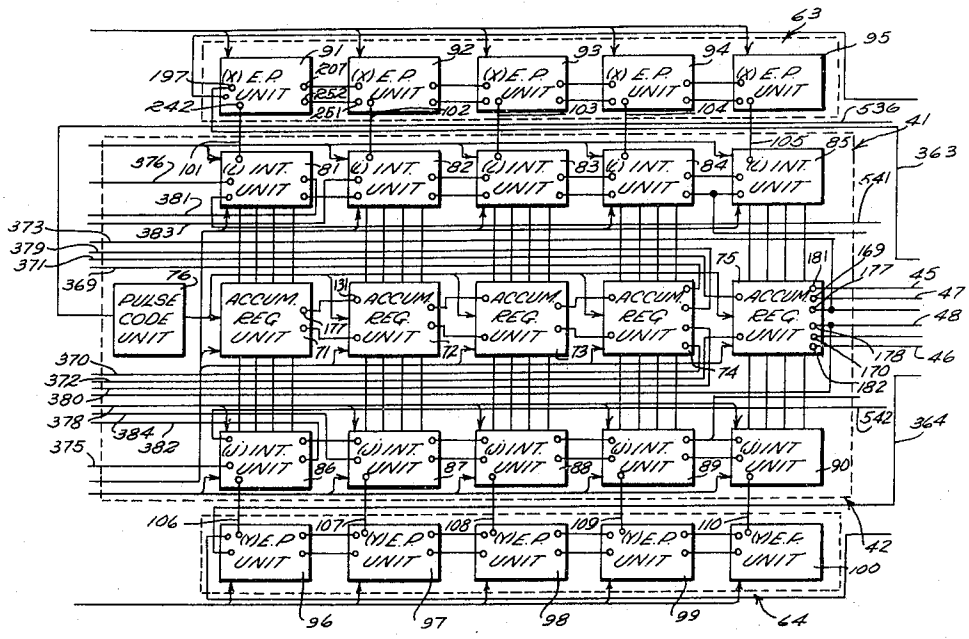
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Primary Examiner—Eugene G. Botz
Assistant Examiner—James F. Gottman
Attorney—Arnold T. Ericsen and Richard C. Steinmetz, Jr.

[57] **ABSTRACT**

An operational integrator comprising an integrand register and an accumulator register, a pulse code unit for supplying four series of pulses and a carry pulse to transfer the numbers stored in respective integrand decades to respective associated accumulator decades in parallel, with provision for carry between successive accumulator decades in response to the carry pulse. The number in the integrand register can be selectively changed in a positive or negative direction to provide for circular interpolation, for example.

10 Claims, 4 Drawing Figures



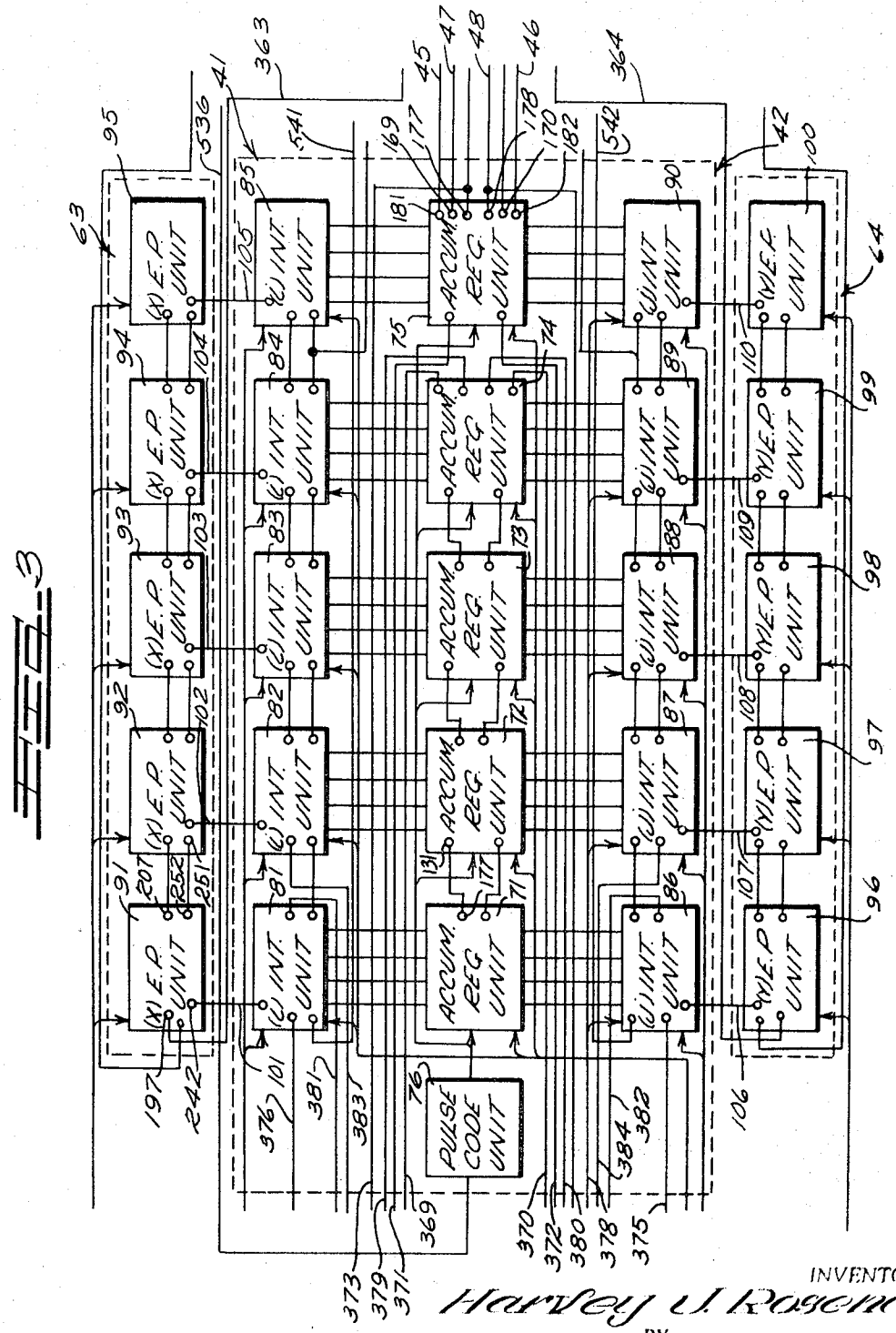
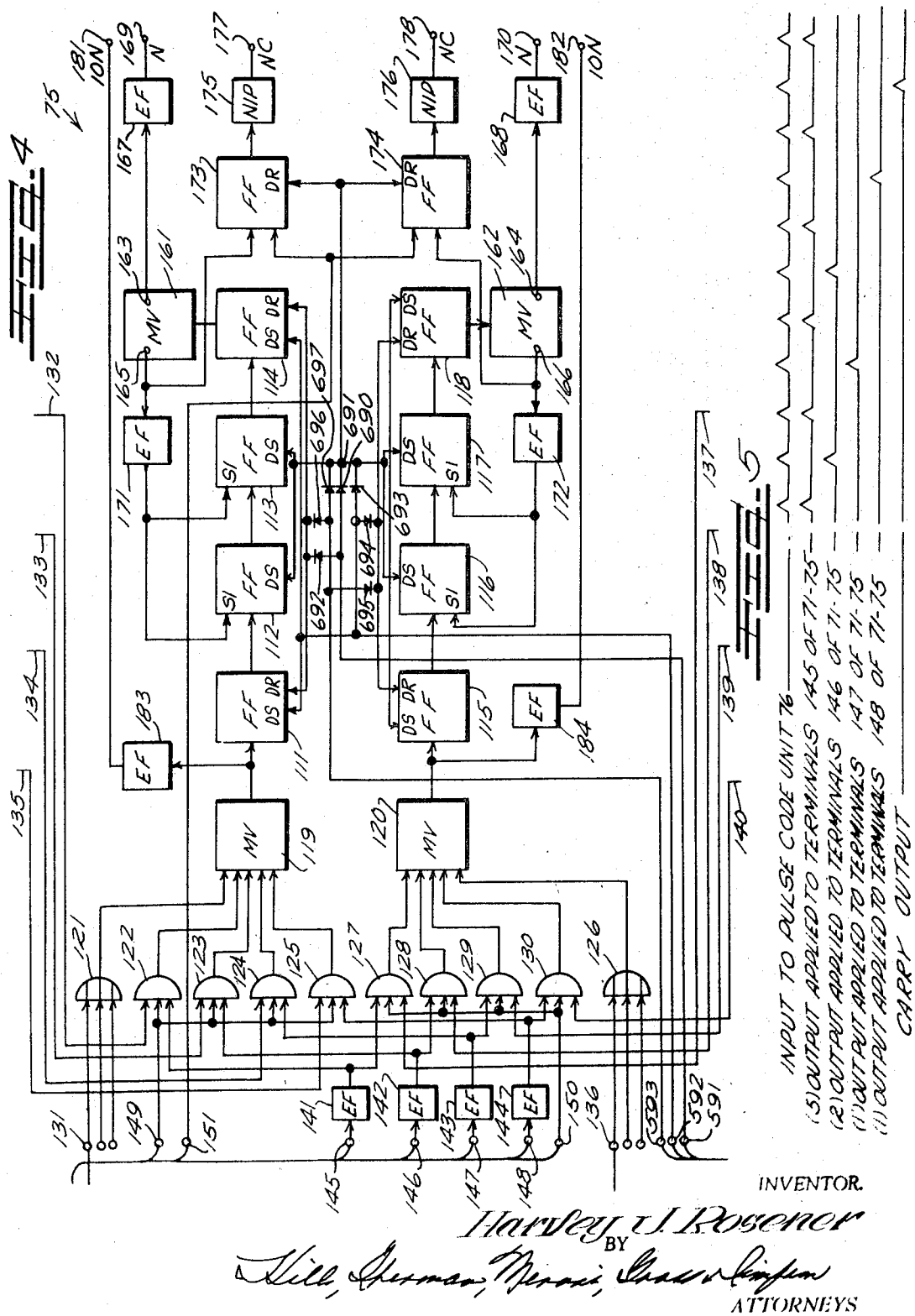


FIG. 3

INVENTOR.
Harvey U. Rosencr
BY
Hill, Sherman, Meroni, Gross & Simpson
ATTORNEYS



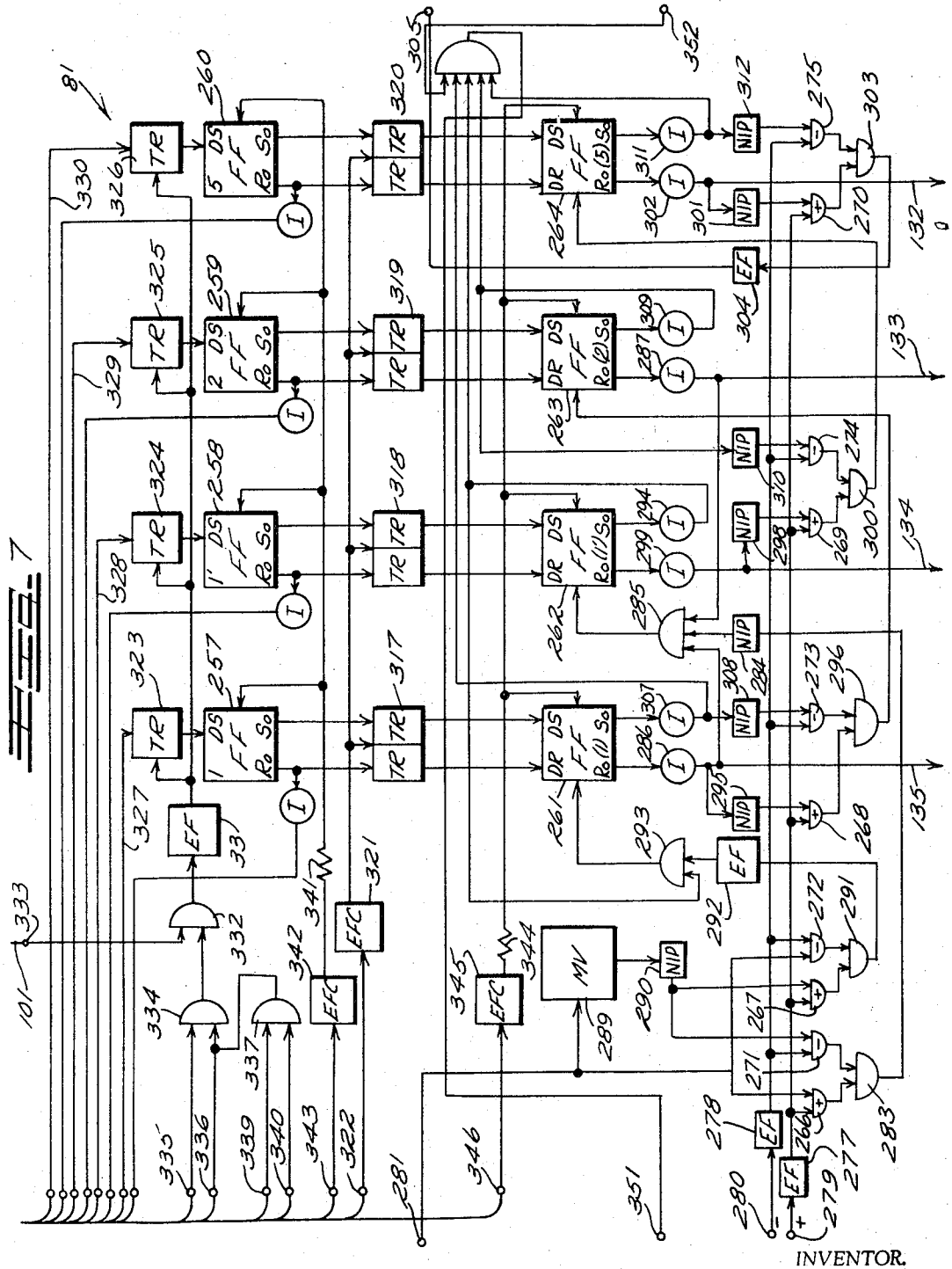
INVENTOR.

Harvey U. Rosener

BY

Hill, Sherman, Meroni, Gross & Simpson

ATTORNEYS



INVENTOR.

Harvey J. Rosener

BY

Hill, Sherman, Meroni, Gross & Simpson

ATTORNEYS

CIRCULAR INTERPOLATION SYSTEM

CROSS-REFERENCE TO RELATED APPLICATION

This application is a division of my pending application Ser. No. 341,958 filed Feb. 3, 1964, now U.S. Pat. No. 3,506,812 issued Apr. 14, 1970.

The disclosure of said U.S. Pat. No. 3,506,812 is incorporated herein by reference.

SUMMARY OF THE INVENTION

A pair of operational integrators are provided each including an integrand register and an accumulator register, each including a plurality of serially connected units with parallel connections between units of the accumulator register and units of the integrand register. Means are provided for simultaneously operating all of the accumulator register units through an addition cycle to cause each unit to add a number stored therein at the beginning of a cycle to a number supplied in parallel from the associated integrand register unit, and also to cause transmission of pulses serially from each accumulator register unit to a succeeding unit. With this arrangement, the addition operation can be carried out at a high rate of speed. In addition, information can be readily applied initially to the integrand registers, which are preferably decade units, and most preferably are units having four flip-flops each, to which information may be applied using a 5, 2, 1′, 1 code.

According to a specific feature of the invention, each accumulator register unit comprises a decade having an input connected to four gates which are selectively enabled from signals applied directly from an associated integrand register unit, and such gates are connected to a pulse code unit which operates through a cycle of operation to apply four series of pulses in each cycle of operation with the number of pulses in the four series being selectively addable to produce any number from one through nine. Preferably, the 5, 2, 1′, 1 code is used, five pulses being applied in each cycle to one gate, two pulses to a second gate, and one pulse each to the other two gates, the pulses being noncoincident. In addition, a storage means in the form of a flip-flop is provided for storing a carry pulse from the decade, and the stored carry pulse is controllably released by a carry pulse from the pulse code unit, the carry pulse from the pulse code unit being noncoincident with other pulses produced thereby.

With this arrangement, an addition operation may be performed with application of only 10 input pulses to the pulse code unit. In addition, the information applied in parallel from the integrand units may be modified during the carry time of the pulse code unit, so as not to interfere with the addition operation. Additional advantages are that the input can be stopped at any time without loss of information in the integrand and accumulator registers, and a variable-frequency input may be used, to obtain any desired feed rate.

Additionally, pulses may be supplied to output lines from different units of the accumulator register, as desired, and pulses may also be feed back from such units to the first or other units of the integrand register, and various different modes of both linear and circular interpolation operation may be obtained. In addition, the system can be readily used in variable lead thread cutting operation.

Another important feature of the invention is in the construction of the integrand unit to which information can be readily applied initially in parallel, and which can thereafter be modified serially in an up-counting or down-counting operation as required to generate the proper output signals.

BRIEF DESCRIPTION OF FIGS. 3–5 AND 7

FIG. 3 is a block diagram of operational integrators and end point storage registers of the system of FIG. 1 of parent U.S. Pat. No. 3,506,812 incorporated herein by reference;

FIG. 4 is a block diagram of one of five dual channel accumulator register units of the operational integrators of FIG. 3;

FIG. 5 is a graph showing the timed relationship of pulses produced by a pulse code unit of the integrators of FIG. 3; and

FIG. 7 is a block diagram of one of 10 integrand register units of the system.

DETAILED DESCRIPTION OF FIGS. 3–5 AND 7

OPERATIONAL INTEGRATORS 41 AND 42

Referring to FIG. 3, the operational integrators 41 and 42 are in the form of digital differential analyzers each including accumulator and integrand registers. The accumulator registers include five dual channel units 71–75 each of which contains circuits of both the operational integrator 41 and the operation integrator 42. The units 71–75 are supplied with signals from a pulse code unit 76, operative in a manner as described below.

Five integrand register units 81–85 form the integrand register of the integrator 41, while five integrand register units 86–90 form the integrand register of the integrator 42. As also shown in FIG. 3, the end point storage unit 63 comprises five register units 91–95 while the end point storage circuit 64 comprises five register units 96–100.

In both linear and circular interpolation, an x number or word is entered into the end point register units 91–95, the least significant digit being entered in the unit 95. Similarly, a y is entered into the register units 96–100.

In linear interpolation, such x and y numbers are also entered into the integrand units 81–85 and the integrand units 86–90, through lines 101–105 and 106–110. The x and y numbers so stored in the integrand units 81–85 and 86–90 are cyclically added through the operation of the dual channel accumulator register units 71–75, and output pulses are developed on lines 45 and 46, connected to the final unit 75, at rates proportional to the numbers stored in the integrand units 81–85 and 86–90. Output pulses are also developed on lines 47 and 48 at rates which are one-tenth the rates at which they are developed on the lines 45 and 46.

In normal linear interpolation, the lines 45 and 46 are connected through the switching and control circuit 43 to the output lines 25 and 26, respectively, and the servosystems 27 and 28 move the machine parts 21 and 22 in proportion thereto.

As an example of such linear interpolation operation, assume that it is desired to move a cutter relative to a workpiece along the linear path 30 from the point 31 to the point 32 as illustrated in FIG. 2 (as shown in U.S. Pat. No. 3,506,812). The numbers 30,000 and 40,000 would be entered into the integrand units 81–85 and 86–90 and in a given interval of time, 30,000 and 40,000 pulses would be developed on the lines 45 and 46, connected to the lines 25 and 26, respectively. After development of such pulses, the integrators 41 and 42 would be stopped in response to signals from the end point storage circuits 63 and 64, assuming normal linear interpolation operation. In long dimension linear interpolation 10 times as many pulses would be developed before stopping, as explained below, whereby 10 times as many pulses would be developed with the same numbers entered into the units.

In circular interpolation, x and y numbers or words are entered into the end point register units 91–95 and 96–100, while i and j words are entered into the integrand units 81–85 and 86–90, as above indicated. In such circular interpolation operation, however, the connections are reversed in the signal switching and combining circuit 43 such that in normal circular interpolation operation, the lines 45 and 46 or the lines 47 and 48 are connected to the lines 26 and 25, respectively, and the initial rate of generation of pulses on the line 25 is determined by the number entered into the j integrand 86–90 while the initial rate of generation of pulses on the line 26 is determined by the number entered into the i integrator units 81–85. In circular interpolation, feedback connections are provided in the feedback switching unit 55, such that the numbers stored in the integrand units 81–85 and 86–90 are changed in response to output pulses, in a manner such as to vary the rates of generation of the pulses, and to cause relative movements of the parts in a circular path, rather than a linear path.

ACCUMULATOR REGISTER UNITS 71–75

FIG. 4 illustrates the circuit of the final dual channel accumulator register unit **75**, the circuits of the other four register units **71–74** being identical thereto. In general, each register unit has an operating cycle in which it adds a number initially stored therein to a number stored in a corresponding integrand unit, and to supply the results of such addition to a subsequent unit or other circuit.

The register unit **75** comprises a divide-by-10 register or decade counter for each channel, including four flip-flops **111–114** for the *i* channel and four flip-flops **115–118** for the *j* channel. The inputs of the first flip-flops **111** and **115** are connected to the outputs of monostable multivibrators **119** and **120** each of which has five input terminals, connected to an OR-gate in the input circuit of the multivibrator. One input of the multivibrator **119** is connected to the output of an OR-gate **121**, and the other four inputs are connected to the outputs of AND-gates **122–125**.

Similarly, the inputs of the multivibrator **120** are connected to the outputs of an OR-gate **126** and four AND-gates **127–130**. The OR-gate **121** has one input connected to an input terminal **131** and to additional inputs which are not used in the illustrated system, but are provided as auxiliaries. The input terminal **131** is connected to an output from a preceding decade to receive carry pulses in a manner to be described. The AND-gates **122–125** have inputs connected through lines **132–135** to outputs from the corresponding *i* integrand unit, in this case the unit **85**. Similarly, the OR-gate **126** has an input connected to an input terminal **136** and the AND-gates **127–130** have inputs connected through lines **137–140** to the corresponding *j* integrand unit, in this case the unit **90**.

Four emitter followers **141–144** are provided having inputs connected to input terminals **145–148** and having output terminals connected to inputs of the gates **122–125** and also to inputs of the gates **127–130**. In addition, inputs of all four gates **122–125** are connected to a terminal **149**, while inputs of all four gates **127–130** are connected to an input terminal **150**. Enabling signals are applied to the terminals **149** and **150**, to render the units operative.

The input terminals **145–148** and also an input terminal **151** are connected to outputs of the pulse code unit, which is a decade unit of a type known in the art, operative to supply pulses with a 5, 2, 1′, 1 code, in response to supply of input pulses thereto. The timed relation of such pulses is shown in FIG. 5. In response to a cycle of operation wherein 10 input pulses are applied to the pulse code unit, five pulses are developed at a first output which is connected to the terminal **145**, and to like terminals of the other units. That output is designated as the (5) output and it will be noted that the five pulses are developed coincident with the first, third, fifth, seventh and ninth input pulses of a cycle. A (2) output, connected to terminal **146**, develops two pulses coincident with the second and sixth pulses of each cycle, a (1′) output, connected to terminal **147**, developes one output pulse coincident with the fourth input pulse of each cycle, and a (1) output, connected to the terminal **148**, also develops one output pulse coincident with the eighth pulse of each cycle. In addition, the unit **76** developes a carry output pulse, coincident with the 10th or final pulse of each cycle, such being applied to the terminal **151**.

In operation, the decade counter which includes the flip-flops **111–114** is advanced in count in response to each series of 10 input pulses to the pulse code unit, according to which of the gates **122–125** is enabled from signals applied from the corresponding integrand unit. By way of example, if the flip-flops **111–114** are initially in a zero-count condition and if enabling signals are applied to the (5) and (2) input lines **132** and **133**, the decade counter formed by the flip-flops will be advanced to a count of seven in response to a cycle of operation wherein 10 pulses are applied from the pulse code unit **76**. With enabling signals applied to the (2) input **133**, the (1′) input **134** and the (1) input **135** in the next cycle the decade counter would be advanced by a count of four in response to the series of 10 input pulses of the next cycle. It would, however, reset at the count of 10 so that in this example, the counter would register one after two cycles with a total of 20 input pulses.

Accordingly, an addition operation is performed by each accumulator register unit during each cycle wherein 10 input pulses are applied to the pulse code unit **76**, the number stored in the corresponding integrand unit during one cycle being added to the number stored in the accumulator register unit during the preceding cycle.

With respect to the operation of the decade counters in the accumulator register units, reset outputs of the flip-flops **111–113** and **115–117** are respectively connected to binary inputs of flip-flops **112–114** and **116–118**. Reset outputs of the flip-flops **114** and **118** are connected to inputs of monostable multivibrators **161** and **162** having output terminals **163** and **164** at which output signals are developed immediately upon triggering of the multivibrators and having additional output terminals **165** and **166** at which output signals are developed after a certain delay, preferably on the order of 2 microseconds. Output terminals **163** and **164** are connected through emitter-followers **167** and **168** to output terminals **169** and **170**. Output terminals **165** are connected through emitter-followers **171** and **172** to inputs of flip-flops **112**, **113** and **116**, **117**. Such output terminals **165** and **166** are additionally connected to inputs of a pair of carry pulse storage flip-flops **173** and **174** having reset inputs connected to the terminal **151** and having set outputs connected to the inputs of negative input pulsers **175** and **176**, the outputs of which are connected to output terminals **177** and **178**.

In operation of the *i* decade including flip-flops **111–114** (which is the same as that of the *j* decade), the flip-flops **111** and **114** may be assumed to be initially in the reset condition, while flip-flops **112** and **113** may be assumed to be in a set condition. The first pulse applied from the multivibrator **119** sets the flip-flop **111**. The second pulse resets the flip-flop **111** which resets the flip-flop **112**, which resets the flip-flop **113**, which sets the flip-flop **114**. The third pulse sets the flip-flop **111**. The fourth pulse resets the flip-flop **111** and sets the flip-flop **112**. The fifth pulse sets the flip-flop **111**. The sixth pulse resets the flip-flop **111** which resets the flip-flop **112**, which sets the flip-flop **113**. The seventh pulse sets the flip-flop **111**. The eighth pulse resets the flip-flop **111** which sets the flip-flop **112**. The ninth pulse sets the flip-flop **111**. The tenth pulse resets the flip-flop **111**, which resets the flip-flop **112**, which resets the flip-flop **113**, which resets the flip-flop **114**. When the flip-flop **114** is reset, the monostable multivibrator **161** is operated and after a certain delay, on the order of 2 microseconds, a signal is developed at the output terminal **165** which is applied through the emitter follower **171** to the set inputs of flip-flops **112** and **113** to place the same in a set condition. The counter is then in its initial condition with the flip-flops **111** and **114** being reset and with the flip-flops **112** and **113** being set.

When the delayed signal is developed at the output terminals **165** of the delay multivibrator **161**, the carry pulse storage flip-flop **173** is placed in a set condition. Thereafter, when the next carry pulse is applied from the pulse code unit, the flip-flop **173** is reset, and the negative input pulser **175** develops an output signal at the terminal **177**.

The output signal at the terminal **177** is referred to herein as a normal controlled carry signal or "NC" signal and it is applied to the input terminal **131** of the next succeeding accumulator register unit. In the case of the final unit **75**, the terminal **177** and also the terminal **178** are not connected to a succeeding accumulator unit, but may be connected to an integrand unit through the feedback switching circuit **65** in a manner to be described. However, the input terminals **131** and **136** of the final unit **75** are connected to the normal controlled carry output terminals **177** and **178** of the preceding accumulator register unit **75**.

It is important to note that the controlled carry signal is generated in synchronism with the carry signal from the pulse code unit and therefore it is not in time coincidence with other output signals from the pulse code unit **176**. Accordingly, the signals applied to the multivibrators **119** and **120** from the terminals **131** and **136** are not coincident with, and do not interfere with, the signals applied thereto from gates **122–125** and **127–130**. Also, as will be clarified hereinafter, feedback switching signals applied from the controlled carry output terminals **177** and **178** to integrand units **86** and **81** or **87** and **82** cause operation of the integrand units and change the signals which may be applied on lines **132–135** and **137–140**, at a time which is not coincident with code pulses applied from the pulse code unit **76** to input terminals **145–148**.

The output terminals **169** and **170** are referred to herein as normal or N outputs. An addition pair of output terminals **181** and **182** are provided, designated as "Ten Normal" or "10 N" terminals. Pulses are developed at such terminals at a rate equal to 10 times the rate of generation of pulses at the N terminals **169** and **170**. In particular, terminals **181** and **182** are connected to the outputs of the monostable multivibrators **119** and **120**. Thus, the input pulses to the decade counters are applied through the emitter-followers **183** and **184** to the output terminals **181** and **182**.

Accordingly, each of the accumulator register units performs an addition operation during each cycle of operation of the pulse code unit **76**, the number stored in the corresponding integrand units being added to the numbers stored in the two channels of the accumulator register unit during the preceding cycle. Three pairs of outputs are developed by each accumulator register unit. First, the "Normal" output pulses are developed at the "N" output terminals **169** and **170**, developed upon resetting of the decade counters of the unit. Secondly, each unit develops "Normal Controlled" pulses at the NC output terminals **177** and **178**, equivalent to the Normal pulses stored in the flip-flops **173** and **174**, and generated in synchronism with the carry pulse from the pulse code unit **76**. Thirdly, each unit develops the "Ten Normal" pulses at the 10 N terminals **181** and **182**.

As above indicated, the NC output terminals **177** and **178** of each unit are connected to the input terminals **131** and **136** of the succeeding unit. The NC output terminals **177** and **178** of the final unit, also the N output terminals **169** and **170** and the 10 N output terminals **181** and **182** of the final unit **75**, and in some cases those terminals of the fourth unit **74**, are connected in various modes of operation, as will be clarified hereinafter. First, however, the construction and operation of the integrand register units, and also the end storage register units, will be described.

INTEGRAND REGISTER UNITS

FIG. 7 illustrates the circuit of the integrand register unit **81**, the circuits of the other units **82–90** being substantially identical thereto. In general the integrand register units operate to selectively energize the 5, 2, 1′, 1 code lines **132–135** (or **137–140**) to the accumulator register units, in accordance with stored information which can be serially increased or decreased.

Illustrated unit **81** is similar to the end point storage unit **91** of FIG. **6** of parent U.S. Pat. No. 3,506,812, and comprises an intermediate or buffer storage section including four flip-flops **257–260** and a final or active storage section including four flip-flops **261–264**. The intermediate storage section operates in substantially the same manner as that of the end point unit, and the final storage section also operates in generally the same manner, in storing information according to the 5, 2, 1′, 1 code, and having a storage which may be serially diminished in response to application of input pulses. However, the integrand register unit additionally incorporates circuitry for selectively increasing rather than decreasing the stored information in response to input pulses.

In particular, five "plus" gates **266–270** and five "minus" gates **271–275** are provided, inputs of such plus and minus gates being respectively connected to outputs of emitter-followers **277** and **278** having inputs connected to terminals **279** and **280**.

With a signal applied to the plus terminal **279**, the gates **266–270** are enabled, and application of input pulses to an input terminal **281** causes the stored number to be increased by a count of one in response to each pulse. Similarly, with the signal applied to the minus terminal **280**, the gates **271** and **275** are enabled and application of each pulse to the terminal **281** reduces the stored number by a count of one.

The diminishing or subtraction operation performed with the gates **271–275** enabled, is substantially the same as that of the end point storage unit of FIG. **6**, as above described. To accommodate the addition operation with the gates **266–270** enabled, additional circuitry is provided including a plurality of negative input pulsers which permit the change between plus and minus operation without destroying the stored information.

The flip-flops **261–264** are respectively (1), (1′), (2) and (5) storage elements, operating in this respect in the same way as the flip-flops **191–194** of the end point storage units. For the addition operation, it may be assumed that flip-flops **261–264** are initially in a reset condition, so that a zero is stored, and also a "high" signal is applied to the plus terminal **279** to enable the gates **266–270**.

A first input pulse applied to terminal **281** passes through the gate **266**, an OR-gate **283** and an emitter-follower **284** to an input of a gate **285** which, however, is blocked through the connection of another input thereof through an inverter **286** to the reset output of the flip-flop **261**, and it is also blocked by the connection of another input thereof through an inverter **287** to the reset output of the flip-flop **263**. The first input pulse is, however, applied to the input of a monostable multivibrator **289** having an output connected to the input of a negative input pulser **290** which develops an output pulse delayed with respect to the input pulse, by a certain time interval which is preferably on the order of 3 microseconds. The first delayed pulse passes through the gate **267** through an OR-gate **291**, an emitter-follower **292** and an AnD-gate **293** to the binary input of the flip-flop **261** which is then switched from its reset condition to a set condition. Gate **293** is enabled by connection of a second input through an inverter **294** to the set output of flip-flop **262**. A count of one is then stored.

The second input pulse from terminal **281** passes through gate **266**, gate **283** and emitter-follower **284** to the gate **285** which, however, is still blocked by the connection of an input thereof through the inverter **287** to the reset output of the flip-flop **263**. The second delayed pulse at the output of the negative input pulser **290** passes through the gate **267**, the OR-gate **291**, the emitter-follower **292** and the AND-gate **293** to the binary input of flip-flop **261** to reset the flip-flop **261**. When flip-flop **261** is reset, an output pulse is developed at the output of a negative input pulser **295** connected to the output of the inverter **286**, and the pulse so developed is applied through the gate **268** and through an OR-gate **296** to the binary input of the flip-flop **263** to place the flip-flop **263** in a set condition. A count of two is then stored.

The third input pulse passes through gate **266**, gate **283** and emitter-follower **284** but is blocked at gate **285** through the connection of an input thereof through an inverter **286** to the reset output of the flip-flop **261**. The third delayed pulse at the output of the negative input pulser **290** passes through gate **267**, gate **291**, emitter-follower **292** and the gate **293** to set the flip-flop **261**. It is noted that this action enables gate **285** but without any immediate effect, because of the delay obtained from the multivibrator **289** and the negative input pulser **290**. At this point, a count of three is stored.

A fourth input pulse passes through gate **266**, gate **283**, emitter-follower **284** and the gate **285** to set the flip-flop **262** through its binary input. The fourth delayed pulse at the output of pulser **292** is the gate **293** but is blocked by the connec-

tion of an input of the gate **293** through the inverter **294** to the set output of the flip-flop **262**. A count of four is then stored.

The fifth input pulse passes through gate **266**, gate **283**, emitter-follower **284** and gate **285** to reset flip-flop **262**. The fifth delayed pulse passes through gate **267**, gate **291**, emitter-follower **292** and gate **293** to reset flip-flop **261**. An output pulse is then developed by the negative input pulser **295** which passes through gate **268** and gate **296** to reset the flip-flop **263**. When flip-flop **262** is reset in response to the fifth input pulse as above described, a signal is developed at the output of a negative input pulser **298**, connected through an inverter **299** to the reset output of the flip-flop **262**. The pulse so developed is applied through the AND-gate **269** and an OR-gate **300** to the binary input of the flip-flop **264**, to set flip-flop **264**. Thus flip-flops **261**, **262** and **263** are reset, while flip-flop **264** is set, and a count of five is stored.

The sixth, seventh, eighth and ninth input pulses perform operations similar to those performed by the first, second, third and fourth pulses respectively.

The tenth pulse produces an operation similar to that of the fifth input pulse but is different in that the flip-flop **264** is reset. When flip-flop **264** is reset, an output pulse is developed by a negative input pulser **301**, connected through an inverter **302** to the reset output of the flip-flop **264**, and is applied through AND-gate **270**, an OR-gate **303** and an emitter-follower **304** to an output terminal **305** which is connected to the input terminal **281** of the next unit. The pulse so applied operates as a carry pulse in the addition operation. In the subtraction operation, a borrow pulse is developed at the terminal **305**.

With respect to the subtraction operation, reference is made to the foregoing discussion of the operation of the end point storage unit of FIG. **6** of parent U.S. Pat. No. 3,506,812. With the minus gate **271–275** enabled by application of a signal to the input terminal **280**, the connection of circuit component is substantially the same as that described above. It is noted that for such operation, the set output of the flip-flop **261** is connected through an inverter **307** to a negative input pulser **308**, the signal being developed at the output of the pulser **308** when the flip-flop **261** is set. Similarly, the set output of the flip-flop **263** is connected through an inverter **309** to a negative input pulser **310** connected to the gate **274**, and the set output of the flip-flop **264** is connected through an inverter **311** to a negative input pulser **312** connected to an input of the gate **275**. When the flip-flops **263** and **264** are set, corresponding signals are developed at the outputs of the pulsers **310** and **312**.

It is noted that the lines **132–135** are respectively connected to the outputs of the inverters **302**, **287**, **299** and **286** connected to the reset outputs of the flip-flops **264**, **263**, **262** and **261** are high when the respective flip-flops are set.

Reset and set inputs of the flip-flops **261–264** are connected to dual transfer circuits or units **317–320** having inputs connected to reset and set outputs of the flip-flops **257–260**. The transfer signal is applied to the units **317–320** from a complementary emitter-follower **321** connected to an input terminal **322**. Set inputs of the flip-flops **257–260** are connected to transfer units **323–326** having inputs connected to (1), (1'), (2) and (5) data input lines **327–330** from the coded tape reader. A transfer pulse is applied to the unit **323–326** from a complementary emitter-follower **331** having an input connected to the output of an OR-gate **332** having a first input connected to an input terminal **333** and a second input connected to the output of a gate **334** having a first input connected to a terminal **335** and a second input connected to a terminal **336** and also to the output of a gate **337** having inputs connected to terminals **339** and **340**.

Reset inputs of the flip-flops **257–260** are connected through a resistor **341** to the output of a complementary emitter-follower **342** having an input connected to a terminal **343**. Similarly, reset outputs of the flip-flops **261–264** are connected through a resistor **344** to the output of a complementary emitter-follower **345** having an input connected to a terminal **346**.

In operation, a reset signal may be applied to terminal **346** to place the final storage flip-flops **261–264** in a reset condition. A transfer pulse may then be applied to the terminal **332** to transfer to the flip-flops **261–264** information which was previously stored in the flip-flops **257–260**. A reset signal may then. be applied to the terminal **343** to reset the flip-flops **357–360** and suitable signals may be applied from the tape reader to the terminal **336** or to the terminals **339** and **340**, after which a data insert signal may be applied to the terminal **335** to cause operation of the transfer units **323–326** and to store information applied from the lines **327–330**.

In linear interpolation, as discussed above, the same information is applied to the integrand unit as applied to the end point storage units, and terminals **333** of each integrand unit may be connected to the terminal **242** of the corresponding end point storage unit. Thus, data inputs **327–330** may be connected in parallel with the date inputs **227–330**.

The integrand unit of FIG. 7 incorporates a zero sensing system similar to that of the end point storage unit of FIG. **6**. In particular, a gate **350** is provided having an output connected to a terminal **351** and having five inputs, one of which is connected to a terminal **352**. The other four inputs of the gate **330** are connected to the output of the inverter **307**, to the output of the inverter **294**, to the output of the inverter **309** and to the output of the inverter **311**, to develop an output at the terminal **351** when an input signal is applied to the terminal **352** and when all four of the flip-flops **261–264** are reset. Input terminal **352** is connected to the output terminal **351** of the next higher significant unit, or to a signal source in the case of the first unit, an output terminal **351** of the final unit is connected to the start-stop control and end point correction circuit **61**.

It will be understood that modifications and variations may be effected without departing from the spirit and scope of the novel concepts of this invention.

I claim as my invention:

1. A digital computer system,

a. a pulse code unit **76** having an input **536** for receiving a series of 10 input pulses (FIG. **5**) in each cycle of operation, said pulse code unit **76** having four noncarry outputs **145–148** and a carry output **151** and being operable in each cycle of operation to produce respective series of noncarry pulses (FIG. **5**) at the respective four noncarry outputs and produce a carry pulse (FIG. **5**) at said carry output, with the numbers of noncarry pulses in said series being selectively addable to produce any number from one through nine and with the noncarry pulses of each series being noncoincident with the carry pulse and with the noncarry pulses of each of the other series,

b. a series of accumulator register decade units **71–75** for storing respective decimal digits therein and connected in cascade for representing successive decimal orders, and including a lowest order accumulator register decade unit, a highest order accumulator register decade unit and intervening order accumulator register decade units representing decimal orders intervening between the lowest order and the highest order of said successive decimal orders, each accumulator register decade unit comprising a decade counter **111–114** having a decade counter input circuit **119** and a decade counter output circuit **161**,

c. respective sets of four gates **122–125** having outputs connected to the respective decade counter input circuits **119** of the respective accumulator register decade units **71–75**, each set of four gates **122–125** having at least two inputs per gate, one such input being connected to a respective one of the noncarry outputs **145–148** and other such input being controlled by a respective bit of a plural order coded decimal signal having respective weights at its successive bit positions corresponding to the numbers of noncarry pulses of the respective series and having respective orders corresponding to the successive decimal orders represented by said series of accumulator register decade units, said sets of gates **122–125** thereby

being controllable to supply numbers of noncarry pulses to the decade counter input circuits **119** of the respective accumulator register decade units simultaneously in accordance with said plural order coded decimal signal, in each cycle of operation of said pulse code unit,

d. said accumulator register decade units **71–75** each including a carry storage circuit **173** connected with the decade counter output circuit **161** thereof for assuming an active condition in response to a decade carry pulse from such decade counter output circuit **161** at a count of 10 of the decade counter **111–114** thereof, without transmission of said decade carry pulse to the input circuit **119** of the next succeeding accumulator register decade unit,

e. said carry storage circuits **173** of the respective accumulator register decade units being all connected with the carry output **151** of said pulse code unit **76** for receipt of the carry pulse therefrom, said carry storage circuits **173** when in said active condition being responsive to a carry pulse from said pulse code unit **76** to transmit an effective carry pulse to the decade counter input circuit **119** of the next succeeding accumulator register decade unit to provide for the counting of such effective carry pulses, and whereby said plural order coded decimal signal may be altered during the time of the carry pulses from the carry output **151** of said pulse code unit **76**.

2. In a digital computer system,

a. an operational integator **41** comprising an integrand register **81–85** and an accumulator register **71–75** including, respectively, serially connected integrand decade units **261–264**, and serially connected accumulator decade units **111–114**, with bistable carry storage circuits **173** interposed between the output **161** of each accumulator decade unit and the input **119** of the next succeeding accumulator decade unit,

b. a parallel transfer circuit **317–320** operative with a 1, 1′, 2, 5 code for applying information in parallel to respective stages **261**, **262**, **263**, and **264** of each decade unit of said integrand register **81–85**, with the successive stages **261–264** thus representing weights of 1, 1, 2 and 5, respectively,

c. respective sets of gates **122–125** connected with the inputs **119** of the respective accumulator decade units, each set of gates **122–125** being operatively controlled in parallel by respective stages **264**, **263**, **262**, and **261** of a corresponding integrand decade unit in such 1, 1′, 2, 5 code, and

d. a 5, 2, 1′, 1 pulse code unit **76** having noncarry outputs **145–148** connected to the respective gates **122–125** of each of said sets of gates **122–125**, and having a carry output **151**, said pulse code unit **76** being responsive, during a cycle of operation thereof, to a series of 10 input pulses (FIG. **5**) to generate at a first noncarry output **145** five noncarry pulses, at a second noncarry output **146** two noncarry pulses, at a third noncarry output **147** one noncarry pulse, and at a fourth noncarry output **148** one noncarry pulse, respectively, and to generate a carry pulse at said carry output **151** which is subsequent to said noncarry pulses, with transmission by each set of gates **122–125** to the input **119** of the associated accumulator decade unit of a number of noncarry pulses corresponding to the digit registered by the associated integrand decade unit in said 1, 1′, 2, 5 code, said pulse code unit **76** being responsive to said series of 10 input pulses to simultaneously operate all of said accumulator decade units **71–75** through an addition cycle to cause each accumulator decade unit to add to a number stored therein at the beginning of each cycle of operation of said pulse code unit **76**, a number corresponding to the number of noncarry pulses supplied thereto by the associated set of gates **122–125** during said cycle of operation, and corresponding to the number registered by the associated integrand decade unit, any decade carry pulses caused by a count of 10 of the respective accumulator decade units **72–75** serving to set the respective associated bistable carry storage circuit **173** without transmission of such decade carry pulses to the input **119** of the following accumulator decade unit,

e. said bistable carry storage circuits **173** being connected to the carry output **151** of said pulse code unit **76** to receive said carry pulse therefrom and being responsive to such carry pulse, when in set condition, to transmit an effective carry pulse to the input **119** of the next succeeding accumulator decade unit for counting thereby, whereby the number registered by said integrand register **81–85** may be changed during the output of the carry pulse from the carry output **151** of the pulse code unit **76** without spuriously affecting the number of noncarry pulses transmitted by said sets of gates **122–125**.

3. In a digital computer system,

a. an operational integator **41** comprising an integrand register **81–85** and an accumulator register **71–75** including, respectively, serially connected integrand decade units **81–85**, and serially connected accumulator decade units **71–75**, with bistable carry storage circuits **173** interposed between the output **161** of each accumulator decade unit and the input **119** of the next succeeding accumulator decade unit,

b. respective sets of gates **122–125** connected with the inputs **119** of the respective accumulator decade units, each set of gates **122–125** being operatively controlled in parallel by respective stages **264**, **263**, **262**, and **261** of a corresponding integrand decade unit, and

c. a pulse code unit **76** having noncarry outputs **145–148** connected to the respective gates **122–125** of each of said sets of gates **122–125** and having a carry output **151**, said pulse code unit **76** being responsive, during a cycle of operation thereof, to a series of 10 input pulses to produce four series of noncarry pulses at the respective noncarry outputs **145–148** and a carry pulse at the carry output **151**, with the numbers of noncarry pulses in said series being selectively addable by control of said gates **122–125** to produce at the inputs **119** of the respective accumulator decade units any number of noncarry pulses from 1 through 9, and with the noncarry pulses of each series being noncoincident with the carry pulse and noncoincident with the noncarry pulses of each of the other series, with transmission by each set of gates **122–125** to the input **119** of the associated accumulator decade unit of a number of noncarry pulses corresponding to the digit registered by the associated integrand decade unit, said pulse code unit **76** being responsive to said series of 10 input pulses to simultaneously operate all of said accumulator decade units **71–75** through an addition cycle to cause each accumulator decade unit to add to a number stored therein at the beginning of each cycle of operation of said pulse code unit **76**, a number corresponding to the number of noncarry pulses supplied thereto by the associated set of gates **122–125** during said cycle of operation, any decade carry pulses caused by a count of 10 of the respective accumulator decade units **71–75** serving to set the respective associated bistable carry storage circuit **173** without transmission of such decade carry pulses to the input **119** of the following accumulator decade unit,

d. said bistable carry storage circuits **173** being connected to the carry output **151** of said pulse code unit **76** to receive said carry pulse therefrom and being responsive to such carry pulse, when in set condition, to transmit an effective carry pulse to the input **119** of the next succeeding accumulator decade unit for counting thereby, whereby the number registered by said integrand register **81–85** may be changed during the output of the carry pulse from the carry output **151** of the pulse code unit **76** without interfering with the transmission of noncarry pulses by said sets of gates **122–125**.

4. In a digital computer system,

a. an operational integator **41** comprising an integrand register **81–85** and an accumulator register **71–75** including, respectively, serially connected integrand decade units **81–85**, and serially connected accumulator decade units **71–75**, with bistable carry storage circuits **173** interposed between the output **161** of each accumulator decade unit and the input **119** of the next succeeding accumulator decade unit,

b. respective sets of gates **122–125** connected with the inputs **119** of the respective accumulator decade units, each set of gates **122–125** being operatively controlled in parallel by respective stages **264**, **263**, **262**, and **261** of a corresponding integrand decade unit,

c. a pulse code unit **76** having noncarry outputs **145–148** connected to the respective gates **122–125** of each of said sets of gates **122–125** and having a carry output **151**, said pulse code unit **76** being responsive, during a cycle of operation thereof, to a series of 10 input pulses to produce four series of noncarry pulses at the respective noncarry outputs **145–148** and a carry pulse at the carry output **151**, with the numbers of noncarry pulses in said series being selectively addable by control of said gates **122–125** to produce at the inputs **119** of the respective accumulator decade units any number of noncarry pulses from 1 through 9, and with the noncarry pulses of each series being noncoincident with the carry pulse and noncoincident with the noncarry pulses of each of the other series, with transmission by each set of gates **122–125** to the input **119** of the associated accumulator decade unit of a number of noncarry pulses corresponding to the digit registered by the associated integrand decade unit, said pulse code unit **76** being responsive to said series of 10 input pulses to simultaneously operate all of said accumulator decade units **71–75** through an addition cycle to cause each accumulator decade unit to add to a number stored therein at the beginning of each cycle of operation of said pulse code unit **76**, a number corresponding to the number of noncarry pulses supplied thereto by the associated set of gates **122–125** during said cycle of operation, any decade carry pulses caused by a count of 10 of the respective accumulator decade units **71–75** serving to set the respective associated bistable carry storage circuit **173** without transmission of such decade carry pulses to the input **119** of the following accumulator decade unit,

d. said bistable carry storage circuits **173** being connected to the carry output **151** of said pulse code unit **76** to receive said carry pulse therefrom and being responsive to such carry pulse, when in set condition, to transmit an effective carry pulse to the input **119** of the next succeeding accumulator decade unit for counting thereby, whereby the number registered by said integrand register **81–85** may be changed during the output of the carry pulse from the carry output **151** of the pulse code unit **76** without interfering with the transmission of noncarry pulses by said sets of gates **122–125**, and

e. a serial connection circuit **266–275** for connecting said integrand decade units **261–264** in series for serially counting pulses supplied to an input **281** of said integrand register **81–85**, and said integrand register **81–85** being responsive to pulses supplied to its input **281** during the time of generation of said carry pulse at said carry output **151** of said pulse code unit **76** to provide for serial modification of the number stored in aid integrand register without interfering with the transmission of noncarry pulses by said sets of gates **122–125**.

5. In a digital computer system in accordance with claim **4**, said serially connected integrand decade units **81–85** each comprising four flip-flops **261–264** respectively representing digits selectively addable to produce any digit from 1 through 9, each integrand decade unit **81–85** including a delay circuit **289** connected with said input **281** for responding to said input pulses to produce delayed pulses, and said serial connection circuit **266–275** comprising gates **266**, **272** and **267**, **271** for selectively applying said input and delayed pulses to said flip-flops **261–264**, said integrand register being operable to respond to each input pulse and associated delayed pulse for shifting by one the count stored therein.

6. In a digital computer system in accordance with claim **4**, said serially connected integrand decade units **81–85** each comprising four flip-flops **261–264** respectively representing digits selectively addable to produce any digit from 1 through 9, said serial connection circuit **266–275** being operable in a countdown mode to respond to each input pulse at said input **281** of said integrand register to reduce by one the count stored therein, means **312** associated with said serial connection circuit **266–275** for generating a borrow pulse when all of said flip-flops **261–264** are reset to represent a zero count, and means **305** connecting said integrand decade units **81–85** in series to apply a borrow pulse from each integrand decade unit to the input **281** of a succeeding integrand decade unit.

7. In a digital computer system in accordance with claim **4**, said integrand decade units **81–85** each comprising four flip-flops **261**, **262**, **263**, and **264** with a zero count being represented by a reset condition of all four of said flip-flops **261–264**, an AND-gate **350** in each unit having five inputs **352**, **307**, **294**, **309** and **311** and an output **351**, means connecting one **352** of said inputs to the output **351** of the succeeding integrand decade unit of next higher significance, and means connecting the other four **307**, **294**, **309** and **311** of said five inputs to said four flip-flops **261–264** to develop an output from said gate **350** in response to concurrence of a reset condition of all four of said flip-flops **261–264** and a signal from the output **351** of the gate **350** of the succeeding integrand decade unit.

8. In a digital computer system,

a. a pulse code unit **76** having noncarry outputs **145–148** and a carry output **151**, and operable through a cycle of operation in response to application of 10 input pulses thereto for producing at the respective noncarry outputs **145–148** first, second, third and fourth series of noncarry pulses and for producing at the carry output **151** a carry pulse, said first series comprising five noncarry pulses coincident with the first, third, fifth, seventh and ninth of said 10 input pulses, said second series comprising two noncarry pulses coincident with the second and with the sixth of said 10 input pulses, said third series comprising one noncarry pulse coincident with the fourth of said 10 input pulses, said fourth series comprising one pulse coincident with the eighth of said 10 input pulses, and said carry pulse being coincident with the 10 th pulse of said 10 input pulses,

b. a plurality of accumulator register units **71–75** connected in cascade and each comprising a decade counter **111–114** having an input **119** and an output **161**, and having a bistable carry storage circuit **173** connected between the output **161** of each decade counter and the input **119** of the next succeeding decade counter,

c. respective sets of first, second, third and fourth gates **122–125** connected with the respective noncarry outputs **145–148** of said pulse code unit **76** for respectively applying said first, second, third and fourth series of noncarry pulses to the input **119** of each of said decade counters,

d. means **81–85** for selectively controlling said gates **122–125** in accordance with respective bits of a plural order coded decimal number weighted according to a 5, 2, 1′, 1 code so as to supply in parallel and simultaneously to the inputs **119** of the respective decade counters numbers of noncarry pulses from the pulse code unit in accordance with the respective digits of the plural order coded decimal number, during application of said 10 input pulses to said pulse code unit **76**,

e. said bistable carry storage circuits **173** being operable for storing a decade carry pulse from the decade counters **111–114** in response to a count of 10 of said decade counters **111–114**, and

f. said carry output **151** of said pulse code unit **76** being connected to a reset input of each of said bistable carry storage circuits **173** to cause an effective carry pulse to be transmitted from the bistable carry storage circuit **173** to the input **119** of the next decade counter, when a decade carry pulse has caused the previous setting of the bistable carry storage circuit, the effective carry pulses being generated in response to the carry pulse from the pulse code unit **76**.

9. In a digital computer system in with claim **8**, said means **81–85** for selectively controlling said gates **122–125** comprising an integrand register **81–85** having successive integrand decade counters each comprising four flip-flops **261–264** respectively representing digits in a 1, 1′, 2, 5 code, input means **281** for connection to a source of input pulses synchronized with the carry pulse from said carry output **151** of said pulse code unit **76**, pulse-channelling means including gates **268–270** and **273–275** and **285** and **293** controlled by said flip-flops **261–264** for selectively triggering said flip-flops **261–264** in response to said input pulses for shifting by one the count stored in said integrand register **81–85** in response to each input pulse, and means **277**, **278**, **266–275** for selectively operating said pulse-channelling means in an addition mode wherein each input pulse increases the stored count by one and in subtraction mode wherein each input pulse decreases the stored count by one.

10. In a digital computer system in accordance with claim **8**, said means **81–85** for selectively controlling said gates **122–125** comprising a series of integrand decade counters each comprising four flip-flops **261–264** respectively representing weights of 1, 1, 2 and 5, input means **281** for connection to a source of input pulses synchronized with the carry pulse from the carry output **151** of said pulse code unit **76**, signal-channelling means including gates **268–270**, **273–275**, **285** and **293** controlled by said flip-flops **261–264** for selectively triggering said flip-flops **261–264** in response to input pulses for shifting by one the counts stored in said integrand register units **81–85** in response to each input pulse, and four output lines **132–135** respectively connected to the outputs of said four flip-flops **264**, **263**, **262** and **261** and connected to respective gates **122–125** of each of said sets of gates **122–125**.

* * * * *

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,644,723 Dated February 22, 1972

Inventor(s) Harvey J. Rosener

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 8, Line 17	"date" should read --data--
Column 8, Line 38	Before "A" insert --In--
Column 11, Line 65	"aid" should read --said--
Column 13, Line 10	After "in" insert --accordance-- (second occurrence)

Signed and sealed this 25th day of July 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents