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(72) Inventeurs/Inventors:

Duhamel, Pierre, FR;
Mahieux, Yannick, FR

(73) Propriétaire/Owner:

FRANCE TELECOM, FR

(74) Agent: GOUDREAU GAGE DUBUC

(54) Titre : METHODE ET APPAREIL DE CODAGE-DECODAGE DE SIGNAUX NUMERIQUES

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$$Y_{2k} = \sum_{n=0}^{N-1} y_n \cdot \cos(2\pi / (4N) \cdot (2n+1) \cdot (4k+1) + (4+1) \cdot \pi / 4) \quad (I)$$

$$Y_{2k+N/4+j} Y_{2k} = \sum_{n=0}^{N/4-1} ((y'_n - y''_{n+N/4}) + j(y''_n + y'_{n+N/4})) \cdot W_{4N}(4k+1)(4n+1) \quad (II)$$

$$z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1} \cdot \sum_{n=0}^{N/4-1} (z_n \cdot W_N^n) \cdot W_{N/4}^{nk} \quad (III)$$

(57) Abrégé/Abstract:

The invention relates to a method and to apparatus for encoding-decoding a digital signal comprising a sequence of samples $x(n)$. After a windowing operation $h(n)$ performed by space-time weighting of the samples, the method and the apparatus consists in performing or enabling to be performed a modified discrete cosine transform of the samples to calculate the even order transformation coefficients: (see formula I) for $k \in [0, \dots, N/2-1]$ with $Y_{N-k} = -Y_{k-1}$. The coefficient Y_{2k} are expressed in the form of an invertible complex transformation: (see formula II) for $k = 0, \dots, N/4-1$ with $y'_n = x_{2n} \cdot h_{2n}$; $y''_n = x_{N-2n-1} \cdot h_{N-2n-1}$; $W_{4N} = \cos(2\pi / 4N) + j \cdot \sin(2\pi / 4N)$. The invertible complex transformation is calculated using an auxiliary calculation equation: (see formula III) with $z_n = (y_{2n} - y_{N/2-1-2n}) + j(y_{N-1-2n} + y_{N/2+2n})$. The invention is applicable to encoding and decoding digital audio or video signals.



A B S T R A C T

The invention relates to a method and to apparatus for encoding-decoding a digital signal comprising a sequence of samples $x(n)$. After a windowing operation $h(n)$ performed by space-time weighting of the samples, the method and the apparatus consists in performing or enabling to be performed a modified discrete cosine transform of the samples to calculate the even order transformation coefficients:

10

$$Y_{2k} = \sum_{n=0}^{N-1} y_n \cdot \cos(2\pi/(4N) \cdot (2n+1) \cdot (4k+1) + (4+1) \cdot \pi/4)$$

for $k \in [0, \dots, N/2-1]$ with $Y_{N-k} = -Y_{k-1}$

The coefficient Y_{2k} are expressed in the form of an invertible complex transformation:

15

$$Y_{2k+N/4+jY_{2k}} = \sum_{n=0}^{N/4-1} (-1)^{k+1} \cdot W_8^{-1} \cdot ((y'_n - y''_{n+N/4}) + j(y''_n + y'_{n+N/4})) \cdot W_{4N}(4k+1)(4n+1)$$

20

for $k = 0, \dots, N/4-1$

with $y'_n = x_{2n} \cdot h_{2n}$

$$y''_n = x_{N-2n-1} \cdot h_{N-2n-1}$$

$$W_{4N} = \cos(2\pi/4N) + j \cdot \sin(2\pi/4N)$$

The invertible complex transformation is calculated using an auxiliary calculation equation:

25

$$Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1} \cdot \sum_{n=0}^{N/4-1} (z_n \cdot W_N^n) \cdot W_{N/4}^{nk}$$

with:

30

$$z_n = (y_{2n} - y_{N/2-1-2n}) + j(y_{N-1-2n} + y_{N/2+2n})$$

The invention is applicable to encoding and decoding digital audio or video signals.

35

A METHOD AND APPARATUS FOR ENCODING-DECODING A DIGITAL SIGNAL

The invention relates to a method and to apparatus for encoding-decoding a digital signal for the purpose of reducing the bit rate it requires for transmission or the space it requires for storage.

One of the highest-performance encoding-decoding techniques known at present is frequency transform coding. In coders of that type, the digital signal is initially subjected to time-frequency transformation and it is the coefficients of the frequency transform which are encoded and transmitted.

For identical transmitted signal quality, the saving in transmission rate depends on the choice of transformation used for encoding, with the inverse transformation being performed on decoding. Thus, a modified discrete cosine transform (MDCT) based on time domain aliasing cancellation (TDAC, i.e. eliminating distortion in the time domain), is particularly effective compared with conventional transforms such as the discrete Fourier transform (DFT) or the discrete cosine transform (DCT). For a comparison of the relative performance of these types of processing, reference may be made to the article "Analysis/synthesis filter bank design based on time domain aliasing cancellation" published by J.P. Princen and A.B. Bradley in IEEE Transactions on ASSP, Vol. 34, pp. 1153-1161, October 1986.

When compared with encoding techniques using banks of filters, that technique of processing and encoding appears to be much more robust. Furthermore, although the above-mentioned encoding technique does not appear to be significantly better for relatively low compression ratios (e.g. for a high quality digital audio signal whose data rate is reduced to 128 kbits/s instead of a higher bit rate), use thereof would appear to be practically inevitable at much greater compression ratios. However, under such circumstances, such compression performance gives rise to increased complexity.

To enable coding algorithms that use MDCT to operate in real time, i.e. to enable corresponding dedicated coding processors to be implemented under satisfactory conditions of

cost and reliability in operation, it is essential to establish a fast coding and calculation method for said transform, in order to significantly facilitate not only installation and implementation, but also real time operation of the above-mentioned processors.

In the above-mentioned method described by Princen and Bradley, the transform coefficients are defined by:

$$(1) \quad y(m,k) = \sum_{n=0}^{N-1} x_m(n) \cdot h(N-1-n) \cdot \cos(2\pi \cdot (k+1/2)(n+N_0)/N)$$

with $k=0, \dots, N-1$.

In that equation, N is the size or number of samples $x(n)$ in the transform block, $h(n)$ is the block weighting window obtained by space or time weighting, m is the number of the transformation block, and $x_m(n)$ indicates the n -th signal sample in the m -th block under consideration. The phase shift N_0 is required for perfect reconstruction of the original signal.

Because of the relationship $y(k-1) = -y(N-k)$, the number of independent coefficients $y(m,k)$ in the frequency domain is equal to $N/2$. The inverse transform MDCT^{-1} required for reconstructing or synthesizing the original audio signal cannot therefore deliver the original sequence. Sampling, being imperfect in the frequency domain, gives rise to distortion in the time domain known as "aliasing".

The synthesis can nevertheless be expressed with the aid of a block transform in which consecutive blocks overlap. For signal synthesis of block m_0 , the n -th sample of the reconstituted audio signal $x_{r_{m_0}}(n)$ is written:

$$x_{r_{m_0}}(n) = f(n+N/2) \cdot X_{m_0-1}(n+N/2) + f(n) \cdot X_{m_0}(n)$$

for $n = 0, \dots, N/2-1$.

In the above equation, $f(n)$ is the synthesis window and $X_{m_0}(n)$ is the inverse transform of the transform coefficient $y(m_0,k)$, i.e.: $X_{m_0}(n) = \text{MDCT}^{-1}y(m_0,k)$, i.e.:

$$(2) \quad X_m(n) = (1/N) \sum_{k=0}^{N-1} y(m,k) \cdot \cos(2\pi \cdot (k+1/2)(n+N_0)/N)$$

The original signal is accurately reconstructed, i.e. $x_{rmo}(n) = x_{mo}(n)$ by imposing conditions on the analysis window $h(n)$ and on the synthesis window $f(n)$, and also on the phase shift term N_0 .

5 Thus, the aliasing terms from one block to another have the same modulus and opposite sign, and therefore cancel, providing the analysis and synthesis windows $h(n)$ and $f(n)$ are identical, of equal length, symmetrical about $N/2$ and satisfy the following equations:

10 (3) $f(n+N/2) \cdot h(n) - f(n) \cdot h(N/2+n) = 0$

(4) $f^2(n+N/2) + f(n) = 2$

for $n = 0, \dots, N/2-1$

(5) $n_0 = N/4 + 1/2$

For example, the following analysis and synthesis windows have
15 a 50% inter-block overlap and satisfy the above conditions:

(6) $h(n) = f(n) = \sqrt{2} \cdot \sin(\pi \cdot (n+1/2)/N)$

for $n = 0, \dots, N-1$.

The main advantage of MDCT lies in the fact that it is possible to use the above-mentioned high-performance windows in
20 the frequency domain without reducing the bit-rate available per coefficient to be encoded. MDCT in association with the above-mentioned windows ensures proper separation of the signal components and thus provides better energy concentration. This improvement in the spectrum representation also facilitates
25 taking account of perceptual phenomena because of the major reduction in spectrum spread, which is not the case when a rectangular window is used, for example.

The MDCT defined above in equation (1) can be calculated by means of a fast Fourier transform (FFT) of the same size,
30 with the above-mentioned MDCT being written:

(7) $y(m,k) =$

$$\operatorname{Re}[e^{j2\pi(k+1/2)n_0/N} \cdot \sum_{n=0}^{N-1} x_m(n) \cdot h(N-1-n) \cdot e^{j2\pi(k+1/2)n}]$$

35 where $\operatorname{Re}[\dots]$ designates the real portion of the complex expression between brackets, i.e.:

$$(8) \quad y(m,k) = \text{Re}[e^{j2\pi(k+1/2)no/N} \cdot \text{DFT}(x_m(n) \cdot h(N-1-n) \cdot e^{j\pi n/N})]$$

It will nevertheless be observed that direct application of above equation (8) requires the following number of
 5 calculation operations:

calculation of $x(n) \cdot e^{j\pi n/N}$, i.e. N real and imaginary products;

an FFT of length N ; and

10 calculation of the real portion of the term-by-term product of two complex vectors of length N .

For $N=2^p$ and for the most efficient calculation algorithm presently known such as that described in the article

"Implementation of split Radix FFT algorithms for complex, real and real symmetric data" by Pierre Duhamel, published in IEEE
 15 on ASSP, Vol. 34, pp. 285-295, April 1986, calculating equation (8) requires $2N+N \cdot (p-3+4)+2N$ multiplications and $3N(p-1)+4+N$ additions, i.e. a total of $N(4p-1)+8$ operations, ignoring the space-time weighting operations required for the windowing.

These numbers which are large when the size of the transform
 20 blocks is large, e.g. $N = 1024$ for encoding-decoding a digital audio signal, can penalize the use of MDCT in an encoding-decoding method for use in real time.

An object of the method and apparatus for encoding-decoding a digital signal (x) represented by digital samples
 25 $x(n)$ of the present invention is to remedy the above-mentioned drawbacks.

Another object of the present invention is to implement a method and apparatus for encoding-decoding a digital signal in which the number of operations required for encoding is
 30 substantially reduced.

Another object of the present invention is to implement a method of encoding-decoding a digital signal which, because of the simplification in the processing procedure, makes it possible for such a processing procedure to be installed in a
 35 dedicated processor under conditions of cost and reliability that are compatible with real time operation.

The method of the invention for encoding a digital signal(s) represented by digital samples $x(n)$ is applied to samples lumped together in blocks of N successive samples.

Said method is remarkable in that following a windowing operation consisting in space or time weighting of the samples as a function of the position n of each sample in the block, $y(n) = x(n) \cdot h(N-1-n)$ where $h(N-1-n)$ represents a determined weighting law, a modified discrete cosine transform (MDCT) is performed at sample block level to calculate the even order coefficients of the following transformation:

$$(9) \quad Y_{2k} = \sum_{n=0}^{N-1} y_n \cdot \cos(2\pi/(4N) \cdot (2n+1) \cdot (4k+1) + (4k+1) \cdot \pi/4)$$

for $k \in [0, \dots, N/2-1]$ with $Y_{N-k} = -Y_{k-1}$
 the phase shift term being distributed as a function of the order k of the above-mentioned coefficient. The calculated even order transformation coefficients Y_{2k} are expressed in the form of an invertible complex transformation:

$$(10) \quad Y_{2k+N/4} + jY_{2k} = \sum_{n=0}^{N/4-1} ((y'_n - y''_{n+N/4}) + j(y''_n + y'_{n+N/4})) \cdot W_{4N}(4k+1)(4n+1) \cdot (-1)^{k+1} \cdot W_8^{-1}$$

for $k = 0, \dots, N/4-1$
 with $y'_n = x_{2n} \cdot h_{2n}$
 $y''_n = x_{N-2n-1} \cdot h_{N-2n-1}$
 $W_{4N} = \cos(2\pi/4N) + j \cdot \sin(2\pi/4N)$
 $W_8 = W_{4N}$ for $N=2$

The above invertible complex transformation is then calculated using the auxiliary calculation equation

$$(11) \quad Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1} \cdot \sum_{n=0}^{N/4-1} (z_n \cdot W_N^n) \cdot W_{N/4}^{nk}$$

where:

$$(12) \quad z_n = (y_{2n} - y_{N/2-1-2n}) + j(y_{N-1-2n} + y_{N/2+2n})$$

and $W_N = \cos(2\pi/N) + j \cdot \sin(2\pi/N)$

The apparatus for encoding a digital signal (x) represented by digital samples $x(n)$ lumped in blocks of N

successive samples is remarkable in that it comprises first and second input memories each enabling $N/2$ successive samples to be stored, the second input memory serving to store samples that are delayed by $N/2$. Following a windowing operation on said samples, which law consists in space sampling the samples $y_n = x(n) \cdot h(N-1-n)$ where $h(N-1-n)$ represents a determined weighting law, a calculation circuit makes it possible to perform a modified discrete cosine transform MDCT so as to calculate the even order transform coefficients of the form:

$$Y_{2k} = \sum_{n=0}^{N-1} y_n \cdot \cos(2\pi/(4N) \cdot (2n+1) \cdot (4k+1) + (4k+1) \cdot \pi/4)$$

for $k \in [0, \dots, N/2-1]$ with $Y_{N-k} = -Y_{k-1}$

the phase shift term being distributed as a function of the order k of the coefficient under consideration, using an invertible complex transformation

$$Y_{2k+N/4+j} Y_{2k}$$

from an auxiliary calculation equation

$$Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1} \cdot \sum_{n=0}^{N/4-1} (z_n \cdot W_N^n) \cdot W_{N/4}^{nk}$$

where:

$$z_n = (y_{2n} - y_{N/2-1-2n}) + j(y_{N-1-2n} + y_{N/2+2n})$$

for $n = 0, \dots, N/4-1$.

The method and the apparatus for decoding a digital signal x represented by digital samples $x(n)$, said samples being lumped in blocks of N samples and being encoded by the coding method of the invention consists in or allows, in succession: permutating the real portions $Y_{N/4+2k}$ and the imaginary portions Y_{2k} of the transmitted transformation coefficients, subjecting the permuted coefficients to an encoding processing procedure by calculating the complex portion of the forward MDCT, of the form $\text{Re}[Z_k]$, $\text{Im}[Z_k]$, in permutating the real and imaginary portions of the complex portion, and then in performing an overlap calculation to reconstitute the samples $x(n)$.

The method and apparatus of the present invention are suitable for use in reducing the bit-rate required for

transmission or the space required for storage of digital audio or video signals.

A more detailed description is given below in a description that refers to the drawings, in which:

5 Figure 1 is a general flow chart showing how the method of the invention is implemented for encoding;

 Figure 2 is a flow chart of a particularly advantageous but non-limiting implementation of the essential steps in the implementation of Figure 1;

10 Figure 3 is a flow chart of an implementation of the method of the invention, at decoding level;

 Figure 4 is a block diagram of one embodiment of apparatus of the present invention for encoding a digital signal;

15 Figure 5a is a block diagram of apparatus for decoding a digital signal encoded using the encoding apparatus of the invention as shown in Figure 4;

 Figure 5b shows a detail of the embodiment of Figure 5a; and

20 Figure 6 is a block diagram of an embodiment of apparatus for encoding or decoding, in which the calculation operations relating to windowing or space-time overlap of the samples is integrated in the calculation of a complex product, thereby eliminating the cost (in terms of number of operations) of windowing or overlapping.

25 The method of the invention is initially described with respect to encoding a digital signal x represented by digital samples $x(n)$.

 The samples are lumped together in blocks of N successive samples.

30 In conventional manner, the encoding method of the invention, as shown in Figure 1, consists initially in performing a windowing operation by space or time weighting of the samples as a function of sample position n within the block under consideration.

35 In Figure 1, a first step marked A consists in an operation of inputting the samples of a block of N samples under consideration, said inputting operation corresponding

substantially to storing the samples under consideration under special conditions that are described below.

Above step A is followed by a step B consisting in the above-mentioned windowing operation for converting each sample
5 $x(n)$ into a weighted sample written:

$$y_n = x(n) \cdot h(N-1-n)$$

In the above equation, $h(N-1-n)$ represents a determined weighting law. Naturally, said weighting law satisfies the above-specified conditions, and said weighting law may have the
10 form specified in above equation (6).

As represented by operation C in Figure 1, the encoding method of the invention then consists in performing a modified discrete cosine transform MDCT on the blocks of samples, essentially on the weighted samples obtained from step B, to
15 calculate the even order coefficients of the transformation of the form:

$$Y_{2k} = \sum_{n=0}^{N-1} y_n \cdot \cos(2\pi/(4N) \cdot (2n+1) \cdot (4k+1) + (4k+1) \cdot \pi/4)$$

20 In an advantageous aspect of the method of the invention, the above even order transformation is calculated for:

$$k \in [0, \dots, N/2-1]$$

It is necessary to calculate the even terms only because of antisymmetry:

$$25 \quad k \in [0, \dots, N/2-1] \quad \text{with } Y_{N-k} = -Y_{k-1}$$

It may be observed in above equation (2) that the phase shift term is distributed as a function of the position k of the transformation coefficient under consideration.

In a particularly advantageous aspect of the encoding
30 method of the present invention, the above-mentioned even order transformation coefficients are expressed in the form of an invertible complex transformation at step D in Figure 1.

This invertible complex transformation satisfies the equation:

$$35 \quad Y_{2k+N/4} + jY_{2k} = \sum_{n=0}^{N/4-1} ((y'_n - y''_{n+N/4}) + j(y''_n + y'_{n+N/4})) \cdot w_{4N}(4k+1)(4n+1) (-1)^{k+1} \cdot w_8^{-1}$$

The above equation is calculated for

$k = 0, \dots, N/4-1$.

In this equation, the following expressions have the values given below:

$$\begin{aligned} 5 \quad y'_n &= x_{2n} \cdot h_{2n} \\ y''_n &= x_{N-2n-1} \cdot h_{N-2n-1} \\ W_{4N} &= \cos(2\pi/4N) + j \cdot \sin(2\pi/4N) \end{aligned}$$

It should be observed, in particular, that the expression W_{4N} designates the $4N$ -th root of unity.

10 As also shown in Figure 1, the above invertible complex transformation is calculated using the following auxiliary calculation equation:

$$15 \quad Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1} \cdot \sum_{n=0}^{N/4-1} (z_n \cdot W_N^n) \cdot W_N^{4nk}$$

In which the term z_n designates:

$$z_n = (y_{2n} - y_{N/2-1-2n}) + j(y_{N-1-2n} + y_{N/2+2n})$$

With said equation likewise being calculated for $n = 0, \dots, N/4-1$.

20 In general, it is considered that in a particularly advantageous aspect of the encoding method of the present invention, the invertible complex transformation as established at step D of Figure 1 can then be calculated very efficiently in the following step E using the above equation.

25 A particularly advantageous calculation procedure for calculation steps E and D as described above with reference to Figure 1 is described below in greater detail with reference to Figure 2.

30 In Figure 2, the above-mentioned invertible complex transformation is calculated by the following successive steps:

step a: calculate z_n using equation (12) for $n = 0, \dots, N/4-1$; i.e. at an effective cost of $N/2$ real additions

step b: calculate

$$35 \quad (13) \quad z'_n = z_n \cdot W_N^n$$

for $n = 0, \dots, N/4-1$

which step requires $N/4-1$ complex multiplications, since the expression W_N^n satisfies the equation:

$$WN^n = \cos(2\pi \frac{n}{N}) + j.\sin(2\pi \frac{n}{N})$$

step c: inverse fast Fourier transform on the variable $z'n$ obtained above in step b to obtain:

$$(14) Z'k = FFT^{-1}.z'n$$

5 It may be observed that the fast Fourier transform is a Fourier transform of size $N/4$, with such an operation making use of known processing techniques.

Step c is then followed by step d, as shown in Figure 2, which consists in calculating the equation:

$$10 (15) Zk = ((-1)^{k+1}.W8^{-1}.W4N^{4k+1}.Z'k)$$

for $k = 0, \dots, N/4-1$.

In the above equation, it should be observed that $W8$ designates the 8-th root of unity, and that $W4N^{4k+1}$ designates the $4N$ -th root of unity raised to the power $4k+1$.

15 The above equation is calculated for $k = 0, \dots, N/4-1$; step e: successively determining the even order transformation coefficients given by the following equations:

$$(16) Y2k \varepsilon \text{Im}[Zk] \quad \text{imaginary portion of } Zk$$

$$(17) Y2k+N/4 \varepsilon \text{Re}[Zk] \quad \text{real portion of } Zk$$

20 It will thus be observed that the even order coefficients are given by the imaginary portion and by the real portion of the above-mentioned equation Zk .

step f: transmitting the transformation coefficients obtained above at step e instead of the digital samples $x(n)$ constituting the digital signal. This transmission is performed by transmission in the form of an encoded signal.

It may be observed that an identical step for determining the odd order transformation coefficients after the even order coefficients have been determined is not necessary since said odd coefficients are given by the antisymmetry relationship based on the even order coefficients:

$$(18) Y2K+1 = -Y2k$$

$$(19) Y2k+1+N/4 = -Y2k+N/4$$

35 In order to perform step c of the fast Fourier transform calculation, it is preferable to use the calculation method described by Pierre Duhamel in the publication entitled "Implementation of Split-Radix FFT algorithms for complex real

and real symmetric data" specified above in the introduction to the description.

Under such circumstances, the number of calculation operations required for performing the encoding method of the present invention can be evaluated as follows:

total number of multiplications:

$N/4(q+1)$ real multiplications with $N=2^q$; and

total number of additions:

$N/4(3q-1)$ real additions.

Adding together the total number of real operations, it can be seen that the minimum total number of operations required for implementing the encoding method of the present invention is exactly equal to $N.q$. In evaluating the above number of operations, it has been assumed in conventional manner that in terms of calculation difficulty, a complex multiplication is equivalent to three real multiplications plus three real additions.

It would also be possible to evaluate equivalence using four real multiplications and two real additions, but that gives rise to equations that are much more complicated. In any event the total number of operations $N.q$ remains unchanged. The encoding method of the present invention thus provides an improvement by a factor of 4 relative to the prior art encoding method described in the introduction to the description of the present patent application.

In particular, it may be observed that the above-defined term for calculation difficulty is compatible with the best FFT coding methods. The relationship between this type of FFT coding process and equations (11) and (12) defining the expression Z_k given in step E of the coding method of the present invention are bilateral and one-to-one. In an article entitled "Algorithms meeting the lower bound on the multiplicative complexity of length $2n$ DFT's and their connection with practical algorithms" published in the journal IEEE trans on ASSP, Vol. 38, pp. 1504-1511, in September 1990, the same author Pierre Duhamel has shown that the active portion of a split radix type fast Fourier transform corresponding to size N

5 The term "compatibility" must thus be understood as the fact that the improvement of the processing by the split radix type fast Fourier transform would obtain a better modified discrete cosine transform (MDCT) process, but the improvement of the modified discrete cosine transform (MDCT) process as
0 proposed in the coding method of the present invention also provides a better way of processing using the fast Fourier transform (FFT) than those presently known.

In the implementation of the coding process shown in Figure 2, it is possible to modify above-described steps b and d by taking multiplication by $W8^{-1}$ from step d and including it in above-mentioned step b. Such an operation changes the symmetries in the sine and cosine tables, i.e. tables of values required for implementing the coding method of the present invention.

In addition, with the equation for the auxiliary calculation of Z_k being expressed in the form:

steps b and d of Figure 2 can be interchanged. Complex multiplications by $W_{4N}^{(4n+1)}$ are then placed at the beginning or at the end of the calculation. Which end is chosen is determined as a function of minimum calculation time.

A method of decoding a digital signal x represented by digital samples $x(n)$ lumped into blocks and encoded using the above-described encoding method is now described with reference to Figure 3.

5 In Figure 3, following a step A' in which the previously transmitted real and imaginary portions $Y_{N/4+2k}$ and Y_{2k} are received after being encoded by the method of the invention, the decoding method consists in a step B' in permutating the real and imaginary portions $Y_{N/4+2k}$ and Y_{2k} of the transmitted
10 transformation coefficients.

 In a particularly advantageous aspect of the encoding and decoding method of the present invention, the method further consists during decoding in a step C' as shown in Figure 3, where the above-mentioned permuted coefficients are subjected
15 to an encoding process by calculating the complex portion of the forward MDCT of the form $\text{Re}[Z_k]$, $\text{Im}[Z_k]$.

 The operation consisting in subjecting the permuted coefficients to an encoding process by calculating the complex portion of the forward MDCT is justified by the fact that the
20 set of steps b, c, and d as described above with reference to Figure 2 forms an invertible complex transformation. Consequently, the inverse of the transform constituted by the above-specified steps constitutes the core of an inverse modified discrete cosine transform or inverse MDCT, said MDCT
25 being calculated by means of the corresponding forward MDCT, after the real and imaginary portions of the input signal have been interchanged, such interchanging having the effect for any input signal of complex form $z = a+jb$ of generating an inverted complex signal of form $z^* = b+ja$, thereby generating inverted
30 input signals, after which the forward MDCT is performed on the inverted input signals to generate output signals written Y^*k . It will naturally be observed that interchanging the real and imaginary portions of the output signals Y^*k makes it possible to generate the inverse output signals Y_k , which reduces to
35 permutating the real and imaginary portions of the complex portion of the above-mentioned MDCT.

The decoding method of the present invention is then followed by a step G' in which the block overlap is calculated in order to reconstruct the samples $x(n)$.

In the decoding method of the present invention, the processing constituted by steps C', D', and E' of Figure 3 where the complex portion of the forward MDCT is performed is identical to the processing performed during encoding and, like the encoding method, comprises the following calculations but performed on the permuted real and imaginary portions as received after transmission: at C', calculating $z'n = z_n \cdot W_N^n$ for $n = 0, \dots, N/4-1$; at D' calculation using the inverse fast Fourier transform FFT^{-1} of size $N/4$, i.e. $Z'k = FFT^{-1}.z'n$; then at E', calculating the expression given by the following equation:

$$(15) \quad Z_k = ((-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1}) \cdot Z'k$$

for $k = 0, \dots, N/4-1$.

Apparatus for encoding a digital signal in accordance with the present invention is described in greater detail with reference to Figure 4.

In Figure 4, using samples as described above lumped into blocks of N successive samples, the apparatus comprises first and second input memories 111 and 112 each capable of storing $N/2$ successive samples. By way of non-limiting example, the second input memory 112 serves to store samples delayed by $N/2$. In another variant embodiment, the first input memory serves to store $N/2$ even order points or samples by addressing, while the second input memory 112 serves to store $N/2$ odd order samples or points.

Calculation circuits referenced 1, 2, 3, and 4 in Figure 4 serve respectively to perform the following:

- calculate z_n in compliance with equation (12);
- calculate $z'n$ satisfying equation (13);
- calculate the inverse fast Fourier transform FFT^{-1} of $N/4$ using equation (14); and
- calculate Z_k using equation (15).

Naturally, by way of non-limiting example, following the above-mentioned windowing operation constituting space or time

weighting of the samples, the calculation circuits 1, 2, 3, and 4 thus perform a modified discrete cosine transform MDCT making it possible, in particular, to establish successively an invertible complex transformation $Y_{2k+N/4} + jY_{2k}$ satisfying equations (16) and (17) using the auxiliary calculation expression.

Thus, the above-mentioned circuits 1, 2, 3, and 4 for calculating the invertible complex transformation comprise in succession and in cascade the encoding apparatus of the present invention, a complex calculation circuit 1 for calculating z_n , a complex multiplication circuit 2 for calculating $z'_n = z_n \cdot W_N^n$ for $n = 0, \dots, N/4-1$, an inverse fast Fourier transform calculation circuit 3 for calculating $FFT^{-1} \cdot z'_n$, i.e. the expressions Z'_k satisfying equation (14), and a third circuit 4 for calculating the expression Z_k satisfying equation (15) for $k = 0, \dots, N/4-1$. This third circuit 4 thus serves to determine in succession the even and odd order coefficients of the transformation, as described above.

As shown in Figure 4, the first complex calculation circuit z_n comprises first and second summing circuits referenced 121 and 122, connected to the first and second input memory circuits 111 and 112.

The first summing circuits receive firstly the weighted sample value y_{2n} directly from the first input memory, and secondly the weighted sample value $y_{N/2-1-2n}$ from the second input memory 112 via a multiplier referenced 123 for multiplying by -1. The second summing circuits 122i receive firstly the weighted sample $y_{N/2+2n}$ from the first input memory 111, and secondly the weighted sample y_{N-1-2n} from the second input memory. It will naturally be observed that the first and second summing circuits 121 and 122 may in fact be constituted by elementary summing circuits referenced 121i, 122i, with each elementary summing circuit receiving the above-mentioned pairs of weighted sample values so as to build up the set of complex values z_n . Naturally, each first summing circuit 121i is connected to the second input memory 112 via a circuit for multiplying by -1, referenced 123i. Thus, the first summing

circuits 121 may be formed by $N/2$ elementary summing circuits 121i. The same applies to the second summing circuits 122, made up of elementary summing circuits 122i.

5 The number of elementary components such as the elementary summing circuits 121i and 122i can be determined so as to establish a compromise between processing speed and memory capacity.

10 Furthermore, the first complex calculation circuit 1 includes first and second auxiliary memories for storing $N/4$ values, these first and second auxiliary memories referenced 131 and 132 being connected to the outputs of the first and second adding circuits 121 and 122, and in particular to the elementary adding circuits that make them up.

15 The auxiliary memories 131 and 132 enable the real portion and the imaginary portion respectively of z^n to be stored.

In the same manner, and as shown in Figure 4, the second circuits 2 for complex multiplication to calculate z^n include circuits referenced 20a and 20b for storing constant values, namely the constants WN^n . These memory circuits may be
20 constituted by RAM type memory circuits suitable for fast read access, and themselves being loaded from read-only memories (ROM) containing the above-mentioned constant values.

In addition, first multiplier circuits referenced 21a and 22a are provided to receive firstly the real portion a of $z^n = a+jb$, and secondly either the real portion $\cos 2\pi \frac{n}{N}$ or the
25 imaginary portion $\sin 2\pi \frac{n}{N}$ of WN^n . These first multiplier circuits deliver the products $a \cdot \cos 2\pi \frac{n}{N}$ and $a \cdot \sin 2\pi \frac{n}{N}$.

In the same way, second multiplier circuits referenced 21b and 22b receive firstly the imaginary portion b of z^n , and
30 secondly the real portion $\cos 2\pi \frac{n}{N}$ or the imaginary portion $\sin 2\pi \frac{n}{N}$ of WN^n . These second multiplier circuits 21b and 22b deliver the products $b \cdot \cos 2\pi \frac{n}{N}$ and $b \cdot \sin 2\pi \frac{n}{N}$.

As also shown in Figure 4, first summing circuits 23 receive the product $a \cdot \cos 2\pi \frac{n}{N}$ from the first multiplier circuit
35 21a and also the product $b \cdot \sin 2\pi \frac{n}{N}$ from the second multiplier 22b via a multiplier by -1 referenced 23a. The first summing circuit 23 thus delivers the real portion of $z^n = a'+jb'$ with $a' = a \cdot \cos 2\pi \frac{n}{N} - b \cdot \sin 2\pi \frac{n}{N}$.

Similarly, second summing circuit 24 is provided which receives firstly the product $a.\sin 2\pi\frac{n}{N}$ from the first multiplier circuit 22a and secondly the product $b.\cos 2\pi\frac{n}{N}$ from the multiplier circuit 21b. This second summing circuit 24

5 delivers the imaginary portion of z_n ,

$$b' = a.\sin 2\pi\frac{n}{N} + b.\cos 2\pi\frac{n}{N}$$

The notation i in the multiplier circuits and in the summing circuits indicates that there may be a multiplicity of them up to a possible maximum number $N/4$ under the conditions indicated above.

In addition, first and second auxiliary memories 25 and 26 serve respectively to store the values of the real portion a' and of the imaginary portion b' of z'_n . It may be observed that the above-mentioned auxiliary memories are RAM type memories, each capable of storing $N/4$ values.

The calculation circuit 3 serves to perform an inverse fast Fourier transform FFT^{-1} of the expression

$$Z'_k = FFT^{-1}.z'_n$$

This may be performed by a dedicated circuit implementing the calculation method described by Pierre Duhamel in the above-mentioned article.

Finally, as also shown in Figure 4, third complex multiplier circuits 4 of the expression Z_k may include circuits referenced 40a and 40b for storing the real and imaginary portions of the constants W_8^{-1} and $W_{4N^{4k+1}}$. It may be observed that in general the permanent memories for constants such as 20a, 20b, or 40a, 40b are omitted from the drawings of the corresponding calculation circuits in order to avoid overcrowding the drawings.

30 As can be seen in Figure 4, the third complex multiplication circuit 4 comprises components analogous to those of the second complex multiplication circuit 2. In particular, it comprises first multiplier circuits 41a and 42a receiving firstly the real portion of the expression Z'_k and secondly the real portion and the imaginary portion respectively of the constants W_8^{-1} and $W_{4N^{4k+1}}$ from the memory circuits 40a and 40b.

The first multiplier circuits deliver the corresponding products.

In addition, second multiplier circuits 41b and 42b receive firstly the imaginary portion of the expression Z^k and secondly the real portion and the imaginary portion respectively of the constants $W8^{-1}$ and $W4N^{4k+1}$ from the same memory circuits 40a and 40b. They deliver the corresponding products.

In addition, first and second summing circuits 43 and 44 are provided. The first summing circuit 43 receives the product delivered by the first multiplier circuit 41a and the product delivered by the second multiplier circuit 42b via a multiplier by -1 referenced 43a. It delivers the real portion of the expression Z_k , such that:

$$\text{Re}[Z_k] = Y_{N/4+2k}$$

The second summing circuit 44 receives firstly the product delivered by the first multiplier circuit 42a, and secondly the product delivered by the second multiplier circuit 41b, and it delivers the imaginary portion of the expression Z_k :

$$\text{Im}[Z_k] = Y_{2k}$$

A more detailed description of apparatus for decoding a digital signal x represented by samples $x(n)$, said samples having been coded using the above-described encoding method, is now given with reference to Figure 5a.

As shown in Figure 5a, the decoding apparatus comprises a circuit 5 for storing and reading the transmitted transformation coefficients as established by the encoding circuit of Figure 4, said coefficients being written:

$$Y_{N/4+2k} = \text{Re}[Z_k] \text{ and } Y_{2k} = \text{Im}[Z_k]$$

The circuit 5 for storing and reading makes it possible to permute the transmitted transformation coefficients as stored by appropriate addressing on reading, said permutation being represented in Figure 5a by crossing over the real and imaginary stored portions.

In addition, the decoding apparatus includes a circuit 6 for calculating the complex portion of the forward MDCT, which circuit includes in cascade: a complex multiplier circuit 62

for calculating Z^k , and a circuit 63 for performing the corresponding inverse Fourier transform FFT^{-1} . A circuit 64 serves to calculate the equation Z_k :

$$Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_4 N^{4k+1} \cdot Z^k$$

5 It may be observed that the circuit 6 for calculating the complex portion of the forward MDCT includes modules 62, 63, and 64 which are respectively identical to the modules 2, 3, and 4 of the encoding apparatus. Consequently, these modules are not described in greater detail.

10 In addition, as shown in Figure 5a, the decoding apparatus includes, after interchanging or permutating the real and imaginary portions of Z_k by read addressing in manner analogous to the permutation performed with the above-described input module 5, a module referenced 7 for calculating overlap and
15 described below.

It will be understood that the module 6 for calculating the complex portion of the forward MDCT by means of above-described modules 62, 63, and 64 in which data is processed in an inverse procedure, finally delivers a complex variable
20 written Z_n and having the form:

$$Z_n = (x_{2n} \cdot h_{2n} - x_{N/2-2n-1} \cdot h_{N/2-2n-1}) \\ + j(x_{N-2n+1} \cdot h_{N-2n+1} - x_{N/2+2n} \cdot h_{N/2+2n})$$

In this equation, the real portion is delayed by half a block relative to the imaginary portion, i.e. by $N/2$ samples.

25 In the above-mentioned equation, it is assumed that the weighting window in the encoding process and the window used in the decoding process are identical.

After compensating for the above-mentioned delay, the above equation can be written in the form:

30
$$Z_n = (x_{2n} + jx_{N/2-2n+1})(h_{2n} + jh_{N/2+2n})$$

The above-mentioned conditions that enable the original samples to be perfectly reconstructed then enable the sequence of samples $x(n)$ to be reconstructed merely by complex multiplication of the above-mentioned equation for z_n by the
35 expression:

$$h_{2n} - jh_{N/2+2n}$$

As shown in Figure 5b, the module 7 for calculating

overlap comprises first and second memories 71a and 71b for storing $N/2$ samples enabling the samples corresponding to blocks m and $m-1$ respectively to be stored so as to compensate for the $N/2$ sample delay of the real portion relative to the
5 corresponding imaginary portion in the above-mentioned expression. The $N/2$ samples of the imaginary portion of block m are stored in a memory 72.

In addition, as described above when describing complex multiplier circuits such as 2 and 4 or 62 and 64, for example,
10 the module 7 for calculating overlap includes multipliers 73ai, 73bi, 74ai, 74bi, a sign inverter 75ai, and two summing circuits 75i and 76i.

The multiplying coefficients h_{2n} and $h_{N/2+2n}$ are stored in memories 70a and 70b. It will naturally be understood that in
15 the embodiment shown in Figure 5b, the multiplying circuits and the summing circuits of index i are shown merely by way of example so as to avoid overcrowding the drawing, and the number of multiplying circuits and summing circuits may be equal to $N/2$ so as to perform the corresponding operations on the
20 corresponding stored $N/2$ values.

The summing circuits 75i and 76i then deliver corresponding reconstituted samples x_{2n} and $x_{N/2-2n-1}$.

In an improved embodiment for implementing the encoding and decoding method and apparatus of the present invention,
25 said method and apparatus may advantageously enable windowing and overlap to be taken into account directly in the calculation process.

It may be observed firstly that the structure of the calculation process shows that the window enabling perfect
30 reconstruction does in fact perform a rotation of the two sample portions of even rank or odd rank respectively in the sequence of input samples $x(n)$. In addition, with respect to the overlap calculation, when reconstructing samples in the decoder, the property of perfect reconstruction due solely to
35 the $N/2$ sample overlap between blocks of samples makes it possible after compensating for the $N/2$ sample delay to obtain the sequence of reconstructed samples x_{2n} by complex multiplication by the expression:

$$h_{2n} - jh_{N/2+2n}$$

Using a window such as that defined by equation (6) then makes it possible to simplify the encoding process or the decoding process as the case may be as implemented by the present invention very considerably by taking account of the observation, whereby the operator defined by equation (6) defining the weighting window applied to the samples during the operation of weighting the input samples $x(n)$ or the operation or reconstructing the output samples x_{2n} is none other than the operation of taking the $4N$ -th root of unity to the power $4n+1$, i.e. W_{4N}^{4n+1} .

In both the encoding process and the decoding process it can be seen that the equation (15) is obtained by a similar rotation operation applied to the coefficients Z^k obtained after processing 3 using the inverse fast Fourier transform FFT^{-1} .

Thus, the windowing 1 and the complex multiplication 2 for calculating z^n in the processing technique with

$$c = \cos 2\pi \frac{4n+1}{4N} \quad \text{and} \quad s = \sin 2\pi \frac{4n+1}{4N}$$

can be expressed by the equation:

$$(18) \quad z^n = ((x_{2n}.c - x_{N/2-1-2n}.s) + j.zo^{-N/2}.(x_{2n}.s + x_{N/2-2n-1}.c)).(c + js))$$

i.e.:

$$(19) \quad z^n = zo^{-N/2}.(x_{2n}.s^2 + x_{N/2-1-2n}.cs) + j(x_{2n}.cs - x_{N/2-1-2n}.c^2)$$

the identity $c^2 = 1 - s^2$ makes it possible to deduce:

$$(20) \quad z^n = (x_{2n} - j.x_{N/2-1-2n}) + (-(x_{2n}.s^2 + x_{N/2-2n-1}.cs) + j(x_{2n}.cs + x_{N/2-1-2n}.c^2)) + zo^{-N/2}.((x_{2n}.s^2 + x_{N/2-2n-1}.cs) + j(x_{2n}.cs + x_{N/2-2n-1}.c^2))$$

In the above equations, it is recalled that $zo^{-N/2}$ represents the $N/2$ sample delay operator applied to the current order n samples or values.

Thus, the above-mentioned process as described takes account of the special windowing while causing only two new

quantities to be included in each block of N samples, namely the quantities

$$(x_{2n}.s^2 + x_{N/2-2n-1}.cs) \quad \text{and} \\ (x_{2n}.cs + x_{N/2-2n-1}.c^2)$$

5 Thus, by storing N/4 additional values, it is possible in an embodiment of an encoder or a decoder of the present invention as described with reference to Figure 6 to reduce the number of operations from 3N as required for said operations comprising two rotations, windowing performed upstream from the
10 process 1 for calculating z_n , and the complex multiplication at 2 for calculating z'_n in Figure 4, where said two rotation processes together require 3N operations, to N multiplications and N additions, i.e. to 2N operations, such that the cost in number of operations relating to windowing thus appears to be
15 eliminated.

It may be observed that in the encoding process as shown in Figure 6, the apparatus implementing such a process includes a module 8 for windowing and calculating z'_n which replaces the windowing module (not shown), the module 1 for calculating z_n ,
20 and the module 2 for complex multiplication to calculate z'_n in Figure 4. The module 8 is followed by the module 3 for calculating the inverse fast Fourier transform FFT^{-1} of size N/4, which is itself followed by a module 9 for calculating the even coefficients of the transform Y_{2k} and then respective odd
25 coefficients $Y_{N/2-2k-1}$.

Figure 6 shows the above-mentioned modules 8, 3, and 9 in succession. It may be observed that in application of the above-established convention, any operator (multiplication or summing) is given a general numerical reference which, when
30 associated with an index $\underline{i}$, corresponds to an elementary operator with a plurality of such elementary operators serving to build up the above-mentioned operator. Thus, in the modules 8 and 9 of Figure 6, all of the indices $\underline{i}$ indicate that there may in fact be a plurality of N/4 corresponding elementary
35 operators, thereby enabling an encoding apparatus or a decoding apparatus to be implemented that is capable of operating in real time with optimized memory capacity.

As shown in Figure 6, the module 8 for windowing and calculating z^n comprises a first input memory 81a and a second input memory 81b serving to store odd samples and even samples $x(n)$, respectively.

5 First multipliers 82a and 82b receive respectively the stored samples x_{2n} delivered by the memory 81b and the odd samples $x_{N/2-1-2n}$ delivered by the memory 81a. The above-mentioned first multipliers also receive respectively via an auxiliary memory 80a the value of the constant c mentioned
10 above via an inverter 821i and directly.

In addition to receiving the even samples x_{2n} and the odd samples $x_{N/2-1-2n}$, second multipliers, referenced 83a and 83b, receive the value of the above-mentioned constant c from an auxiliary memory referenced 80b, respectively directly and via
15 a multiplier by -1 referenced 89.

First summing circuits 84a and 84b receive firstly the product delivered by the first multiplier 82a and by the second multiplier 83a, and secondly the product delivered by the first multiplier 82b and the product delivered by the second
20 multiplier 83b.

Second summing circuits are referenced 86a and 86b. Second summing circuit 86a receive the sum delivered by the first summing circuit 84a together with the same sum delayed by an $N/2$ value delay line 85a after inversion in an inverter
25 referenced 861i. Similarly, the second summing circuit 86b receives the sum delivered by the first summing circuit 84b, together with the same sum delayed by $N/2$ values by a delay line 85b.

Third summing circuits are referenced 87a and 87b and they
30 receive the sums delivered by the second summing circuits 86a and 86b respectively. The third summing circuit 87a also receives the value of the odd sample $x_{N/2-1-2n}$ after inversion by an inverter referenced 871i, while the third summing circuit 87b receives the value of the even sample x_{2n} . The third
35 summing circuits 87a and 87b thus deliver values corresponding to z^n , with the third summing circuits 87a delivering the real portions of z^n and with the third summing circuit 87b

delivering the imaginary portions of z^n . It may be observed that the memories 88a and 88b may advantageously be constituted by RAM type memories each capable of storing $N/4$ values.

5 The module 3 for calculating the inverse fast Fourier transform FFT^{-1} is identical to the module 3 in Figure 4.

The module 9 for calculating the transform coefficients Y_k then serves to calculate the values of the even coefficients Y_{2k} and of the odd coefficients $Y_{N/2-2k-1}$ on the basis of the values of the above-mentioned fast Fourier transform.

10 As shown in Figure 6, the module 9 comprises first multipliers referenced 91, 91b, 91c, and 91d. The first multipliers respectively receive the following: the real portion of the results of the fast Fourier transform written $Re[Z^{N/8-k}]$; the corresponding imaginary portion written
15 $Im[Z^{N/8-k}]$; the real portion $Re[Z^{N/8+k}]$; and finally the corresponding imaginary portion $Im[Z^{N/8+k}]$. The above-mentioned first multipliers also receive the above-mentioned value c from an auxiliary memory 90a.

The module 9 for calculating the transform coefficients
20 further includes second multipliers respectively referenced 92a, 92b, 92c, and 92d. The second multipliers respectively receive the following: the products of the inverse fast Fourier transform in the same manner as the above-mentioned first multipliers, and also the above-mentioned value s from an
25 auxiliary memory written 90b. The second multipliers deliver the corresponding products.

First summing circuits 93a, second summing circuits 93b, third summing circuits 93c, and fourth summing circuits 93d receive the values of the products of the first and second
30 multipliers with and without inversion, respectively as follows: first multiplier 91a and second multiplier 92b; second multiplier 92a via an inverter 93b, and first multiplier 91b; first multiplier 91c and second multiplier 92d via an inverter 94c; and second multiplier 92c and first multiplier 91d. The
35 sums delivered by the first and third summing circuits 93a and 93c are stored in an auxiliary memory 95a which constitutes a memory for the odd coefficients $Y_{N/2-2k-1}$ of the transform,

while an auxiliary memory 95b receives the values delivered by the second and fourth summing circuits 93b and 93d, thereby storing the even coefficients Y_{2k} of the transform.

5 It will thus be understood that the encoding module as shown in Figure 6 enables a particularly advantageous gain in calculation time to be achieved since, as mentioned above, the number of operations is reduced from $3N$ operations to $2N$ operations, with a number of operations corresponding to those required for windowing in the embodiment of Figure 4 thus being
10 omitted.

It will naturally be observed that a decoder may be implemented using the same configuration as shown in Figure 6 by applying the invertible transformation principle as already described with reference to Figures 4 and 5a. A detailed
15 description of such a decoder is therefore not given since, in practice, it suffices merely to substitute the corresponding input and output variables, providing the procedure terminates with the series of multiplications by the above-mentioned rotation values c and s .

20 In an appendix to the present description, there follows a source code listing of a program for processing the samples $x(n)$ both during encoding and during decoding. In the example given, the processing corresponds to that performed by the apparatus of Figure 6. The above-mentioned source code program
25 is written in the C language, together with comments in English.

30

35

APPENDIX TO THE DESCRIPTION

```

5      /* forward TDAC. declarations are omitted */

      /* *****initialisations***** */
      if(init == 0)
      {
          for (i = 0; i < N/4; i++)
          {
10             /* Twiddle factors for the FFT (size N/4) */
               rw1[i] = cos(8.0*pi*(float)i/(float)N);
               rw2[i] = sin(8.0*pi*(float)i/(float)N);
            /* constants for the input and output rotations */
               theta = 2.0*pi*(4*(float)i+1)/(4.0*(float)N);
               cc[i] = cos(theta)*cos(theta);
               cs[i] = cos(theta)*sin(theta);
            }
          for (i=1; i<N/8+1; i++)
15             {
               theta = 2.0*pi*(float)i/(float)N;
               wcos[i] = cos(theta);
               wsine[i] = sin(theta);
            }
            init = 1;
        }
        /* ***** Fast Algorithm ***** */
        for (i = 0; i < N/4; i++)
20             {
               A = x[2*i]*cs[i] - x[N/2-1-2*i]*cc[i];
               B = x[2*i]*(1.0-cc[i]) - x[N/2-1-2*i]*cs[i];
               ycr[i] = memr[i] - x[N/2-1-2*i] - A;
               yci[i] = memi[i] + x[2*i] - B;
               memr[i] = A;
               memi[i] = B;
            }
25             sign = -1;
               fft(ycr,yci,rw1,rw2,N/4,sign);
               for(k = 1; k < N/8+1; k++)
            {
               A = ycr[N/8-k];
               ycr[N/8-k] = A*wcos[k]+yci[N/8-k]*wsine[k];
               yci[N/8-k] = yci[N/8-k]*wcos[k]-A*wsine[k];
               A = ycr[N/8+k];
               ycr[N/8+k] = A*wcos[k]-yci[N/8+k]*wsine[k];
30               yci[N/8+k] = yci[N/8+k]*wcos[k]+A*wsine[k];
            }
            for(k = 0; k < N/4; k++)
            {
               y[2*k] = -yci[k];
               y[N/2-2*k-1] = ycr[k];
            }

35

```

CLAIMS

1/ A method of encoding a digital signal (x) represented by digital samples $x(n)$, said samples being lumped into blocks of N successive samples, the method being characterized in that,
 5 following a windowing operation consisting in space or time weighting of the samples as a function of the position n of each sample within the block such that:

$$y_n = x(n) \cdot h(N-1-n)$$

where $h(N-1-n)$ represents a determined weighting law, the
 10 method consists in:

performing a modified discrete cosine transform on the blocks of samples to calculate the even order transformation coefficients of the form:

$$15 \quad Y_{2k} = \sum_{n=0}^{N-1} y_n \cdot \cos(2\pi/(4N) \cdot (2n+1) \cdot (4k+1) + (4k+1) \cdot \pi/4)$$

for $k \in [0, \dots, N/2-1]$ with $Y_{N-k} = -Y_{k-1}$

the phase shift term being distributed as a function of the order k of the above-mentioned coefficient;

20 expressing said calculated even order coefficients Y_{2k} in the form of an invertible complex transformation

$$25 \quad Y_{2k+N/4} + jY_{2k} = \sum_{n=0}^{N/4-1} ((y'_n - y''_{n+N/4}) + j(y''_n + y'_{n+N/4})) \cdot W_{4N}^{(4k+1)(4n+1)}$$

for $k = 0, \dots, N/4-1$ with

$$y'_n = x_{2n} \cdot h_{2n}$$

$$y''_n = x_{N-2n-1} \cdot h_{N-2n-1}$$

$$W_{4N} = \cos(2\pi/4N) + j \cdot \sin(2\pi/4N); \text{ and}$$

30 calculating said invertible complex transformation on the basis of the following auxiliary calculation equation:

$$Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1} \cdot \sum_{n=0}^{N/4-1} (z_n \cdot W_N^n) \cdot W_{N/4}^{nk}$$

35 where:

$$z_n = (y_{2n} - y_{N/2-1-2n}) + j(y_{N-1-2n} + y_{N+2+2n})$$

for $n = 0, \dots, N/4-1$.

2/ A method according to claim 1, characterized in that said invertible complex transform is calculated by the following successive steps:

- a) calculating z_n for $n = 0, \dots, N/4-1$;
- 5 b) calculating $z'_n = z_n \cdot W_N^n$ for $n = 0, \dots, N/4-1$;
- c) calculating the corresponding coefficients Z'_k by the inverse fast Fourier transform FFT^{-1} of size $N/4$:
 $Z'_k = FFT^{-1}.z'_n$;
- d) calculating the equation
 10 $Z_k = ((-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1}) \cdot Z'_k$
 for $k = 0, \dots, N/4-1$;
- e) successively determining the even order transformation coefficients

Y_{2k}	$Im[Z_k]$	imaginary portion of Z_k
15 $Y_{2k+N/4}$	$Re[Z_k]$	real portion of Z_k ;
- f) transmitting said transformation coefficients Y_{2k} , $Y_{2k+N/4}$ in the form of a coded signal instead of the digital sample $x(n)$ constituting the digital signals.

20 3/ A method according to claim 2, characterized in that with the auxiliary calculation equation being expressed in the form:

$$Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_N^k \cdot \sum_{n=0}^{N/4-1} (z_n \cdot W_{4N}^{(4n+1)} \cdot W_{N/4}^{nk})$$

25 steps b) and d) are interchanged, with complex multiplications by $W_{4N}^{(4n+1)}$ being placed at the beginning or the end of the calculation.

30 4/ A method of decoding a digital signal (x) represented by digital samples $x(n)$, said samples being lumped into blocks of N samples, and being encoded according to claim 1, the decoding being characterized in that it consists in:

permutating the real and imaginary portions $Y_{N/4 + 2k}$, Y_{2k} of the transmitted transformation coefficients;

35 subjecting said permuted coefficients to an encoding process by calculating the complex portion of the forward MDCT, of the form $Re[Z_k]$, $Im[Z_k]$;

permutating the real and imaginary portions of said complex portion; and

performing an overlap calculation to reconstruct said samples $x(n)$.

5

5/ A method according to claim 4, characterized in that said process identical to the encoding process by calculating said forward MDCT complex portion comprises:

calculating

10

$z'n = zn.WN^n$ for $n = 0, \dots, N/4-1$;

calculating $Z'k$ by the inverse fast Fourier transform FFT^{-1} of size $N/4$

$Z'k = FFT^{-1}.z'n$; and

calculating the expression

15

$Zk = ((-1)^{k+1}.W8^{-1}.W4N^{4k+1}).Z'k$

for $k = 0, \dots, N/4-1$.

6/ A method according to claim 5, characterized in that with the set of steps b), c), and d) forming an invertible complex transformation, the inverse of the transform constituted by the above steps constitutes the core of an inverse modified discrete cosine transform (inverse MDCT), which inverse MDCT is calculated by means of a corresponding forward MDCT following:

20

interchanging the reel and imaginary portions of the input signals, $z = a+jb \Rightarrow z^* = b+ja$ to generate inverted input signals;

25

calculating the forward MDCT of the inverted input signals to generate output signals Y^*k ; and

interchanging the real and imaginary portions of the output signals Y^*k to generate inverted output signals Yk .

30

7/ Apparatus for encoding a digital signal (x) represented by digital samples $x(n)$ lumped into blocks of N successive samples, the apparatus being characterized in that it include:

35

first and second input memories each serving to store $N/2$ successive samples, said second input memory enabling said samples to be stored with a delay of $N/2$; and

calculation means following a windowing operation on said samples which consists in performing space weighting of the samples $y_n = x(n) \cdot h(N-1-n)$ where $h(N-1-n)$ represents a determined weighting law, with a modified discrete cosine transform MDCT so as to calculate the even order transform coefficients of the form:

$$Y_{2k} = \sum_{n=0}^{N-1} y_n \cdot \cos(2\pi/(4N) \cdot (2n+1) \cdot (4k+1) + (4k+1) \cdot \pi/4)$$

for $k \in [0, \dots, N/2-1]$
with $Y_{N-k} = -Y_{k-1}$

the phase shift term being distributed as a function of the order k of the coefficient under consideration,

the even order coefficients Y_{2k} being obtained from an invertible complex transform $Y_{2k+N/4} + jY_{2k}$ using an auxiliary calculation equation:

$$Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1} \cdot \sum_{n=0}^{N/4-1} (z_n \cdot W_N^n) \cdot W_{N/4}^{nk}$$

where:

$$z_n = (y_{2n} - y_{N/2-1-2n}) + j(y_{N-1-2n} + y_{N/2+2n})$$

for $n = 0, \dots, N/4-1$.

8/ Apparatus according to claim 7, characterized in that said means for calculating the invertible complex transformation $Y_{2k+N/4} + jY_{2k}$ comprise successively and in cascade:

first complex calculation means enabling z_n to be calculated;

second complex calculation means for calculating $z'_n = z_n \cdot W_N^n$ for $n = 0, \dots, N/4-1$;

inverse fast Fourier transform calculation means to calculate $FFT^{-1} \cdot z'_n$; and

third complex calculation means for calculating the expression:

$$Z_k = (-1)^{k+1} \cdot W_8^{-1} \cdot W_{4N}^{4k+1} \cdot Z'_k$$

for $k = 0, \dots, N/4-1$

and for successively determining even order transformation coefficients:

y_{2k}	$\text{Im}[z_k]$	imaginary portion of z_k
$y_{2k+N/4}$	$\text{Re}[z_k]$	real portion of z_k .

9/ Apparatus according to claim 7, characterized in that said
 5 first complex calculation means for calculating z_n comprise,
 connected to said first and second input memories:

first and second summing means, said first summing means
 receiving firstly directly from said first input memory the
 weighted sample value y_{2n} , and secondly from said second input
 10 memory via a multiplier by -1, the weighted sample value
 $y_{N/2-1-2n}$, said second summing means receiving firstly from
 said first input memory the weighted sample $y_{N/2+2n}$, and
 secondly from said second input memory the weighted sample
 y_{N-1-2n} ; and

15 first and second auxiliary memories of capacity $N/4$
 connected respectively to the outputs of the first and second
 adders and serving to store the real portion and the imaginary
 portion respectively of

$$z_n = (y_{2n} - y_{N/2-1-2n}) + j(y_{N-1-2n} + y_{N/2+2n})$$

20

10/ Apparatus according to claim 7, characterized in that said
 second complex multiplication means for calculating z'_n
 comprise:

memory means for storing the constants

25 $WN^n = \cos 2\pi \frac{n}{N} + j \sin 2\pi \frac{n}{N}$

first multiplier means receiving firstly the real portion
 a of $z_n = a + jb$ and secondly the real portion $\cos 2\pi \frac{n}{N}$ or the
 imaginary portion $\sin 2\pi \frac{n}{N}$ of WN^n , and delivering the products
 $a \cdot \cos 2\pi \frac{n}{N}$ and $a \cdot \sin 2\pi \frac{n}{N}$;

30 second multiplier means receiving firstly the imaginary
 portion b of $z_n = a + jb$ and secondly the real portion $\cos 2\pi \frac{n}{N}$ or
 the imaginary portion $\sin 2\pi \frac{n}{N}$ of WN^n , and delivering the
 products $b \cdot \cos 2\pi \frac{n}{N}$ and $b \cdot \sin 2\pi \frac{n}{N}$;

first summing means receiving firstly from the first
 35 multiplier means the product $a \cdot \cos 2\pi \frac{n}{N}$ and secondly from the
 second multiplier means the product $b \cdot \sin 2\pi \frac{n}{N}$ via a multiplier
 by -1, to deliver the real portion of $z'_n = a' + jb'$,

$$a' = a \cdot \cos 2\pi \frac{n}{N} - b \cdot \sin 2\pi \frac{n}{N};$$

second summing means receiving firstly from the first multiplier means the product $a \cdot \sin 2\pi \frac{n}{N}$ and secondly from the second multiplier means the product $b \cdot \cos 2\pi \frac{n}{N}$ and delivering the
 5 imaginary portion of $z'n = a' + jb'$

$$b' = a \cdot \sin 2\pi \frac{n}{N} + b \cdot \cos 2\pi \frac{n}{N}; \text{ and}$$

first and second auxiliary memories for storing the values of the real and imaginary portions a' and b' respectively of $z'n$.

10 11/ Apparatus according to claim 7, characterized in that said calculation means for performing complex multiplication on $Z'k$ comprise:

means for storing the real and imaginary portions of the constants $W8^{-1}$ and $W4N^{4k+1}$;

15 first multiplier means receiving firstly the real portion of the expression $Z'k$ and secondly the real portion or the imaginary portion of said constants $W8^{-1}$, $W4N^{4k+1}$ from the memory means, and delivering the corresponding products;

second multiplier means receiving firstly the imaginary
 20 portion of the expression $Z'k$ and secondly the real portion or the imaginary portion of said constants $W8^{-1}$ and $W4N^{4k+1}$ from the memory means, and delivering the corresponding products;

first summing means receiving firstly the product
 25 delivered by the first multiplier means and secondly the product delivered by the said second multiplier means via a multiplier by -1 , and delivering the real portion of the expression for Zk such that:

$$\text{Re}[Zk] = YN/4 + 2k; \text{ and}$$

30 second summing means receiving firstly the product delivered by the first multiplier means and secondly the product delivered by the second multiplier means, and delivering the imaginary portion of the expression Zk , such that:

35 $\text{Im}[Zk] = Y2k.$

12/ Apparatus for decoding a digital signal (x) represented by

digital samples $x(n)$ lumped into blocks of N successive samples, said samples being encoded by means of the encoding apparatus according to claim 7, the decoding apparatus being characterized in that it includes:

5 means for storing and reading the transmitted transformation coefficients

$$Y_{N/4+2k} = \text{Re}[Z_k] \text{ and } Y_{2k} = \text{Im}[Z_k]$$

said read means enabling said stored transmitted transformation coefficients to be permutated; and

10 means for calculating the complex portion of the forward MDCT comprising successively and in cascade complex multiplication means for calculating $z'n$, means for calculating the inverse fast Fourier transform $\text{FFT}^{-1}.z'n$, and means for calculating the expression

15
$$Z_k = (-1)^{k+1}.W_8^{-1}.W_{4N}^{4k+1}.Z'_k.$$

13/ Apparatus according to claim 12, characterized in that said means for calculating the complex portion of the forward MDCT comprise modules that are identical to respective modules of
20 the encoder apparatus.

14/ Apparatus for encoding and decoding a digital signal (x) represented by samples $x(n)$ lumped into blocks of N successive samples, the apparatus being characterized in that it
25 comprises:

first means for calculating by complex multiplication an equation

$$z'n = ((x_{2n}.c - x_{N/2-1-2n}.s) + j.z_0^{-N/2}.(x_{2n}.s + x_{N/2-2n-1}.c)).(c+js)$$

30 on the basis of even samples x_{2n} and odd samples $x_{N/2-1-2n}$ where:

$$c = \cos 2\pi \frac{4n+1}{4N} \text{ and } s = \sin 2\pi \frac{4n+1}{4N}$$

35 means for applying the inverse fast Fourier transform FFT^{-1} to the expression $z'n$ to deliver the expressions

$z'(N/8-k) = \text{FFT}^{-1}.z'n$; and

second calculation means for performing complex multiplication to calculate the even coefficients Y_{2k} and the odd coefficients $Y_{N/2-2k-1}$ of the transform.

5

15/ Apparatus according to claim 14, characterized in that said first means for calculation by complex multiplication comprise:

first and second input memories for storing odd and even samples $x_{N/2-1-2n}$ and x_{2N} respectively;

10 first and second permanent memories for storing the above-mentioned values of c and s ;

first multiplier means receiving firstly the even samples x_{2n} or the odd samples $x_{N/2-1-2n}$ and secondly the value c via a multiplier by -1 or directly;

15 second multiplier means receiving firstly the even samples or the odd samples, and secondly, from the memory, the value of the constant s either directly or via a multiplier by -1 ;

first summing means receiving the products delivered by respective ones of said first and second multipliers;

20 second summing means receiving firstly directly the sums delivered by the first summing means and secondly the sums delivered thereby via respective delay lines with and without an inverter;

25 third summing means receiving firstly the odd samples via an inverter or the even samples directly and secondly the sums delivered by respective ones of the second summing means, said third summing means delivering the real and imaginary portions respectively of $z'n$; and

30 first and second RAM type memories respectively receiving said real and imaginary portions of $z'n$.

16/ Apparatus according to claim 14, characterized in that said second calculation means using complex multiplication to obtain the even coefficient Y_{2k} and the odd coefficients $Y_{N/2-2k-1}$ of the transform comprise:

35

first and second permanent memories for storing the values of c and s ;

first multipliers receiving in order: the real portion $\text{Re}[Z'N/8-k]$, the imaginary portion $\text{Im}[Z'N/8-k]$, the real portion $\text{Re}[Z'N/8+k]$, and the imaginary portion $\text{Im}[Z'N/8+k]$ of the inverse fast Fourier transform of $z'n$, $\text{FFT}^{-1}.z'n$, said

5 first multiplier means also receiving the value of $\underline{c}$ from the first memory;

second multiplier means receiving in order: the real portion $\text{Re}[Z'N/8-k]$, the imaginary portion $\text{Im}[Z'N/8-k]$, the real portion $\text{Re}[Z'N/8+k]$, and the imaginary portion $\text{Im}[Z'N/8+k]$ of the inverse fast Fourier transform of $z'n$, $\text{FFT}^{-1}.z'n$, said

10 second multiplier means also receiving the value $\underline{s}$ from the second memory;

first, second, third, and fourth summing means respectively receiving products from the first and second

15 multipliers as follows: directly from the first multiplier and from the second multiplier; from the second multiplier via an inverter and directly from the first multiplier; directly from the first multiplier and from the second multiplier via an inverter; and directly from the second multiplier and from the

20 first multiplier; and

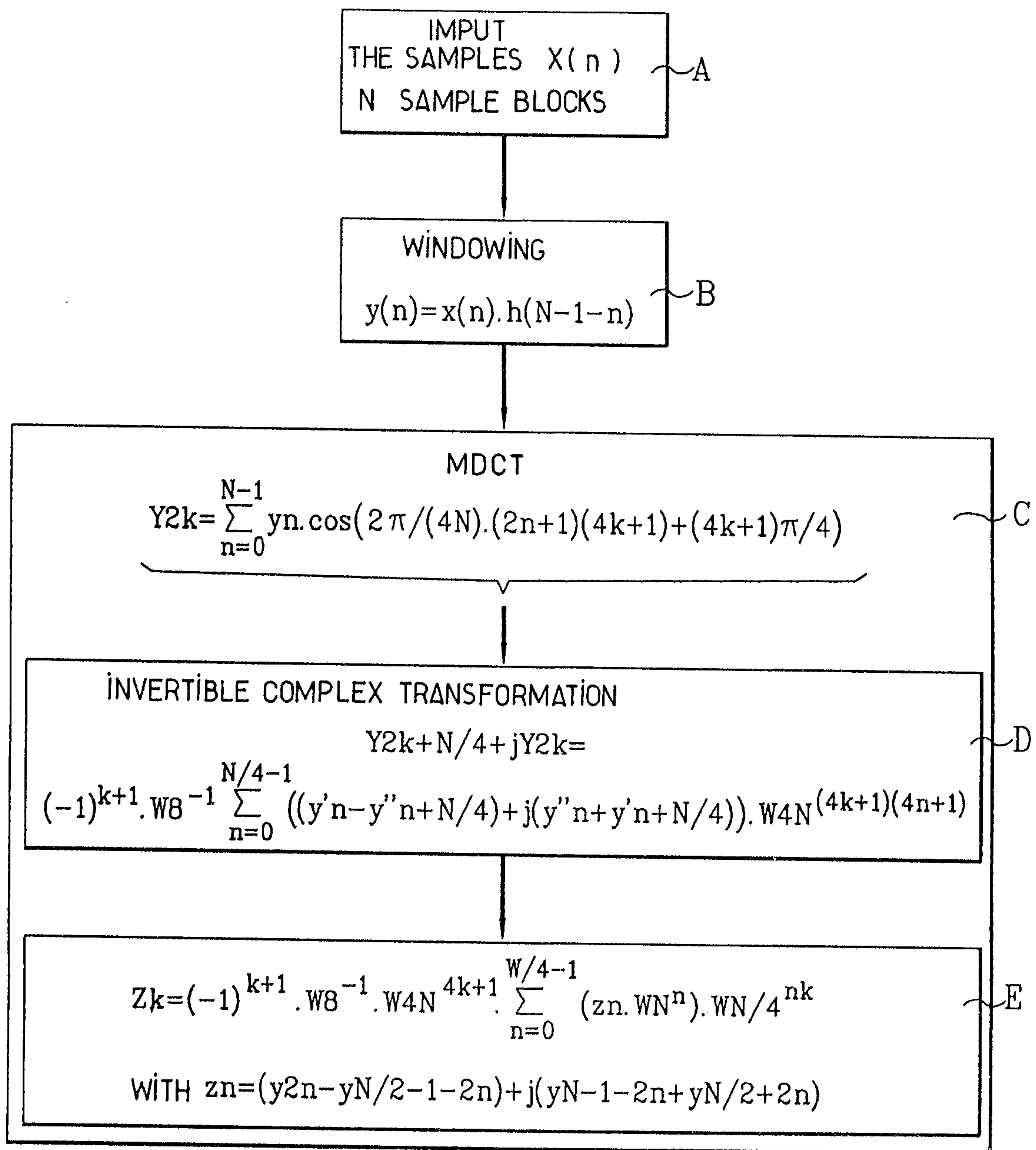
first and second auxiliary memories respectively storing the sums delivered by the first and second or by the third and fourth summing circuits, said stored sums corresponding to the odd coefficient $Y_{N/2-2k-1}$ and to the even coefficients Y_{2k} of

25 the transform, respectively.

30

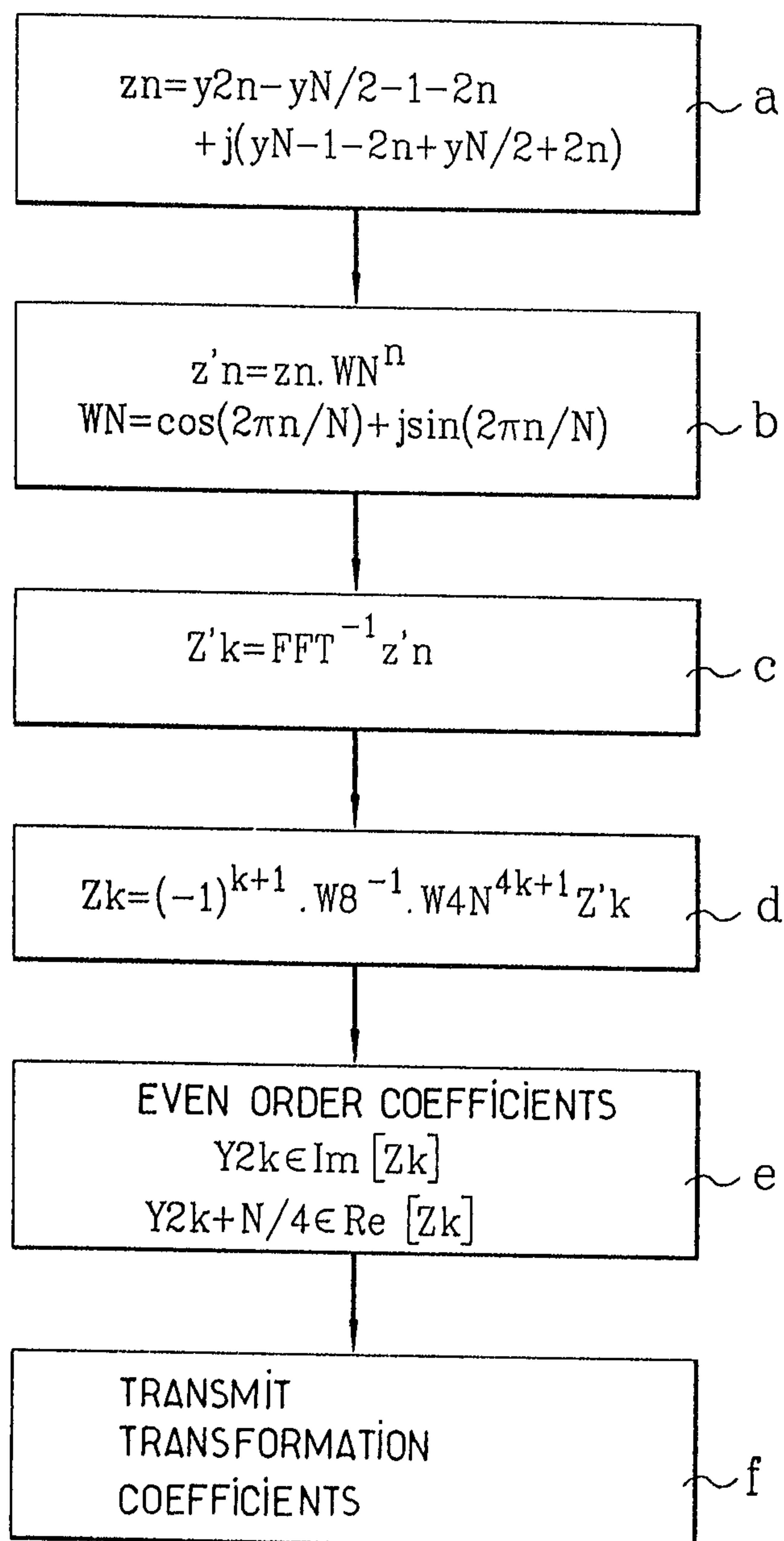
35

FIG.1.



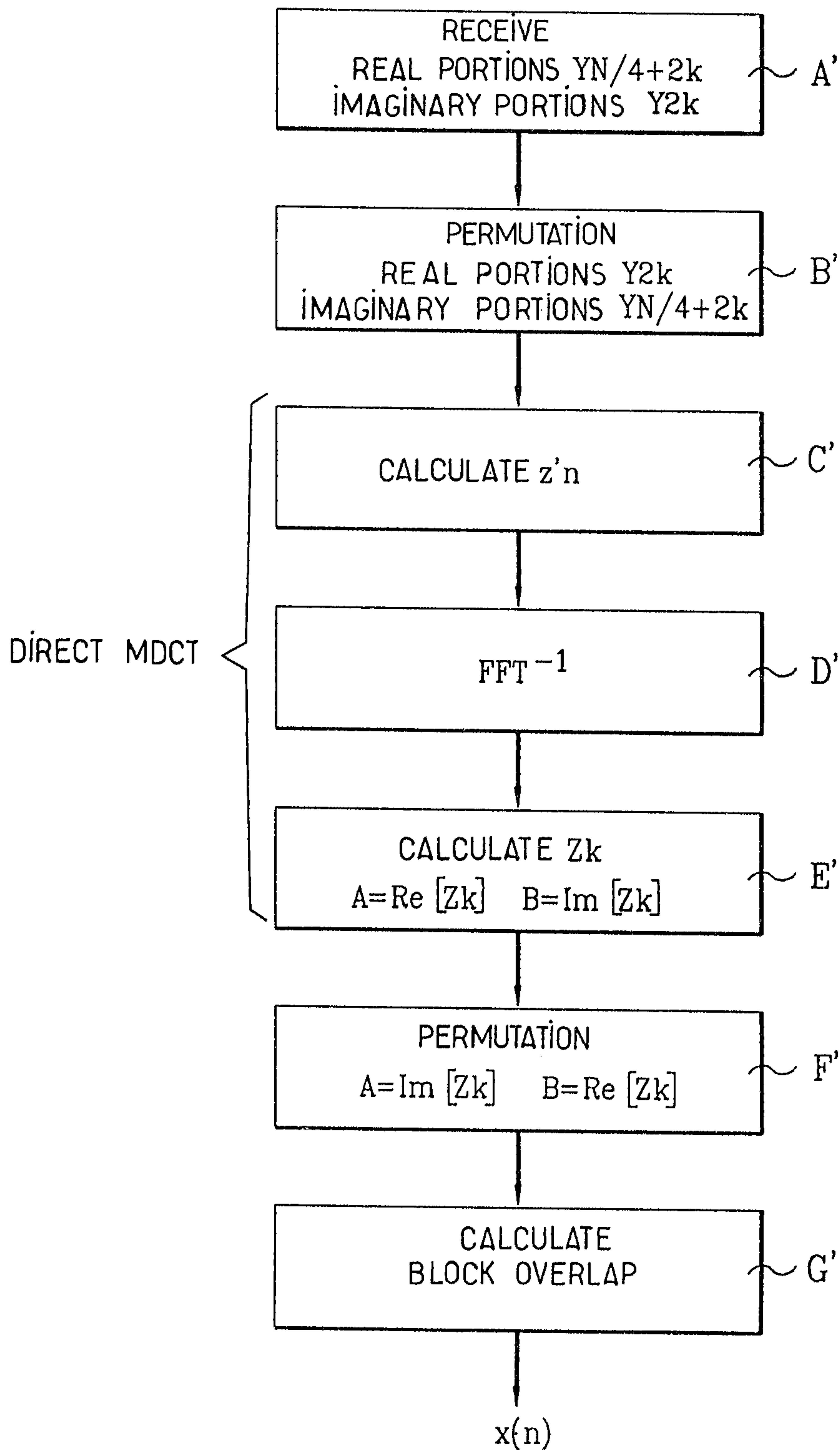
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FIG. 2.



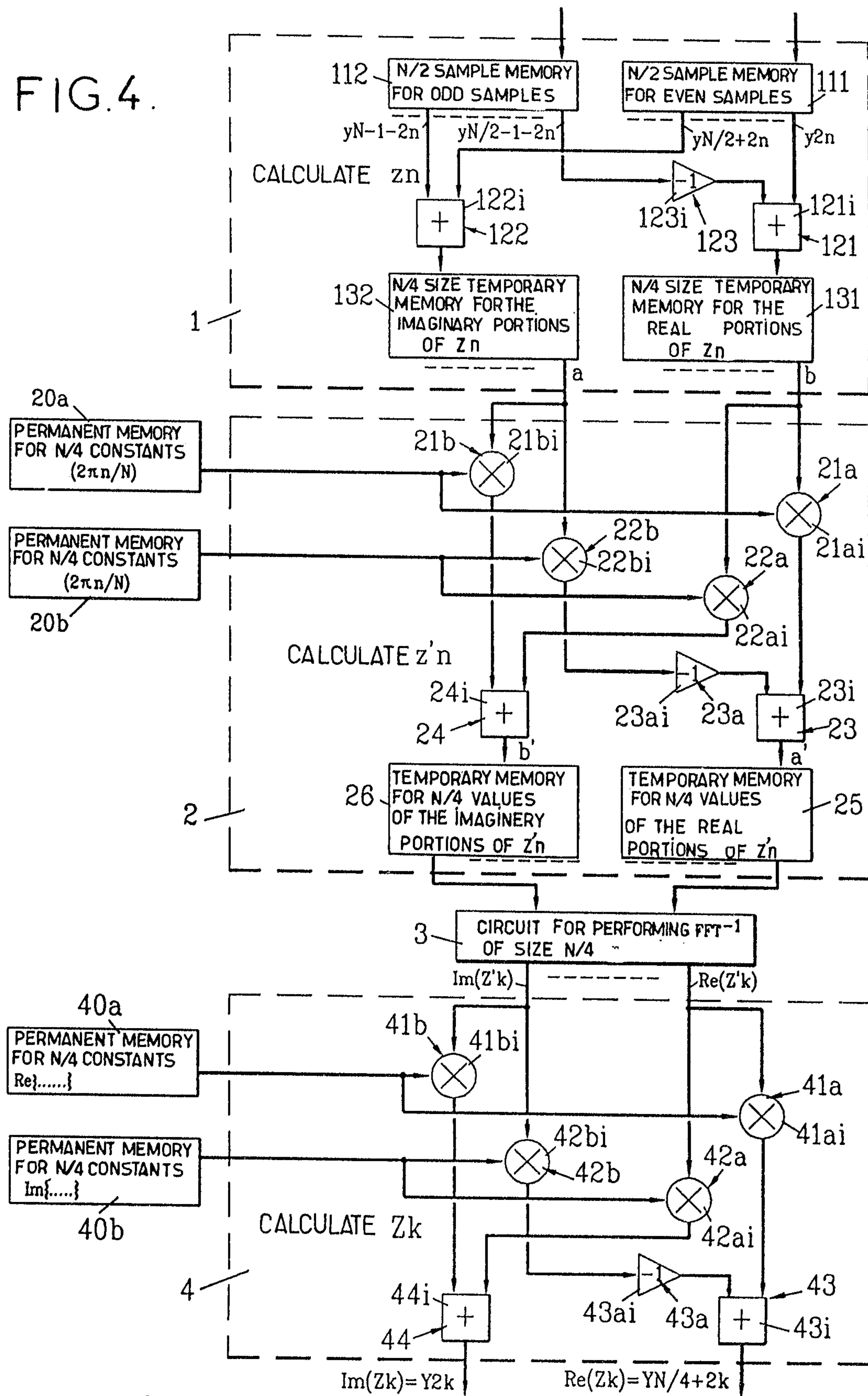
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FIG. 3.



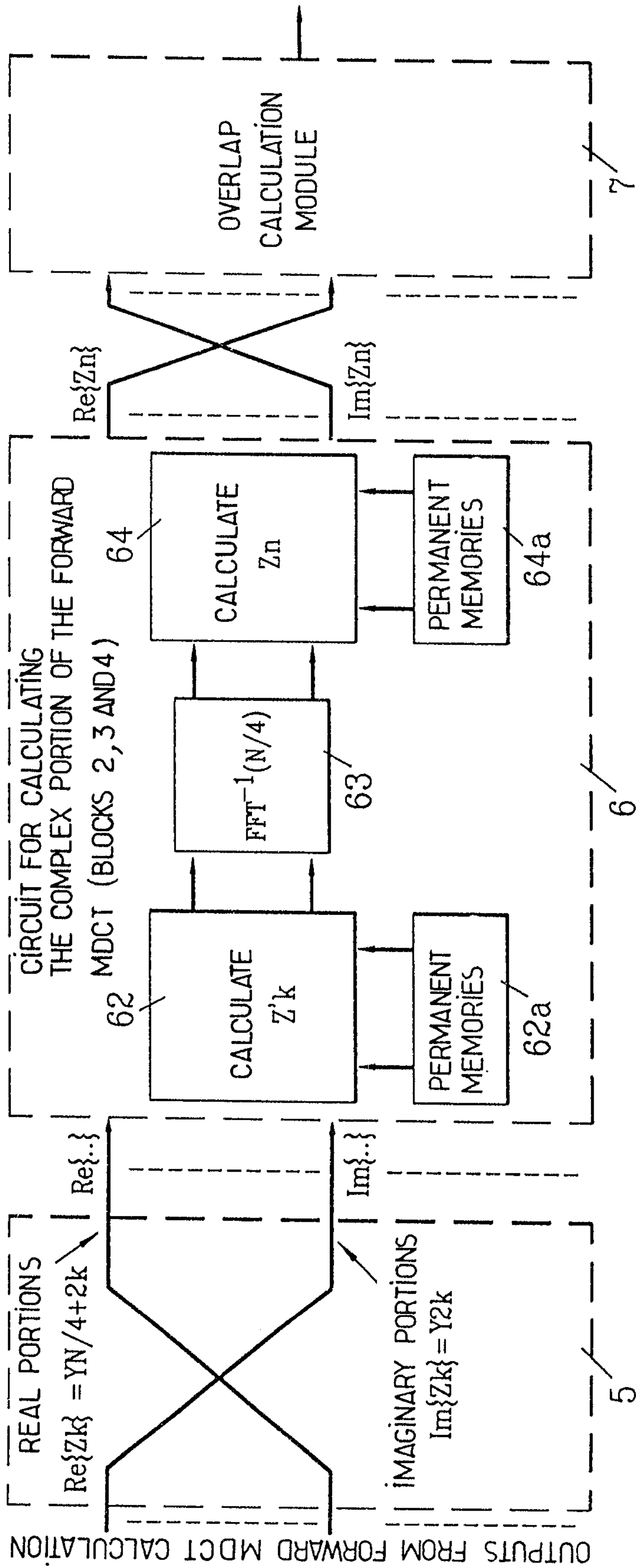
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FIG. 4.

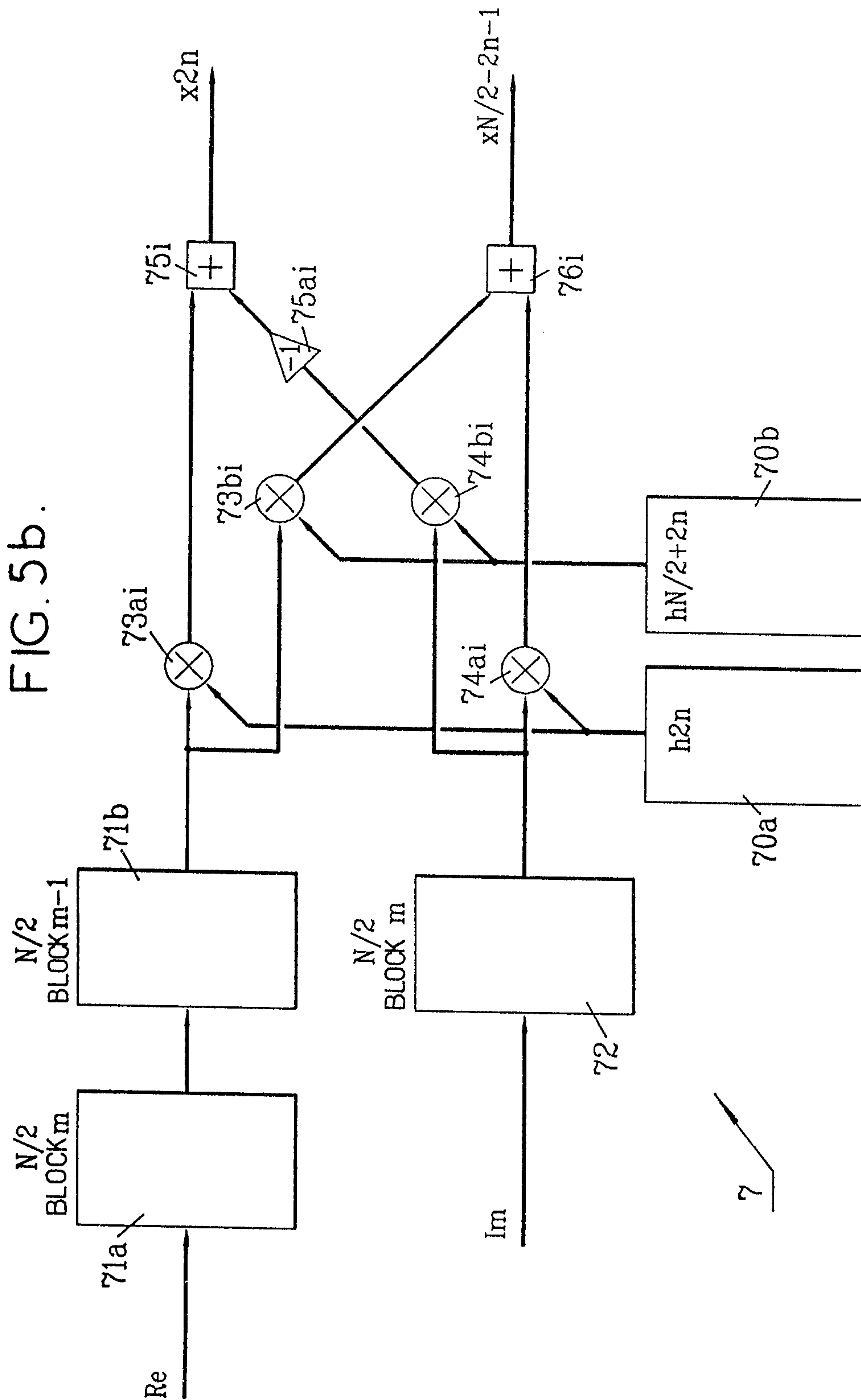


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FIG. 5a.

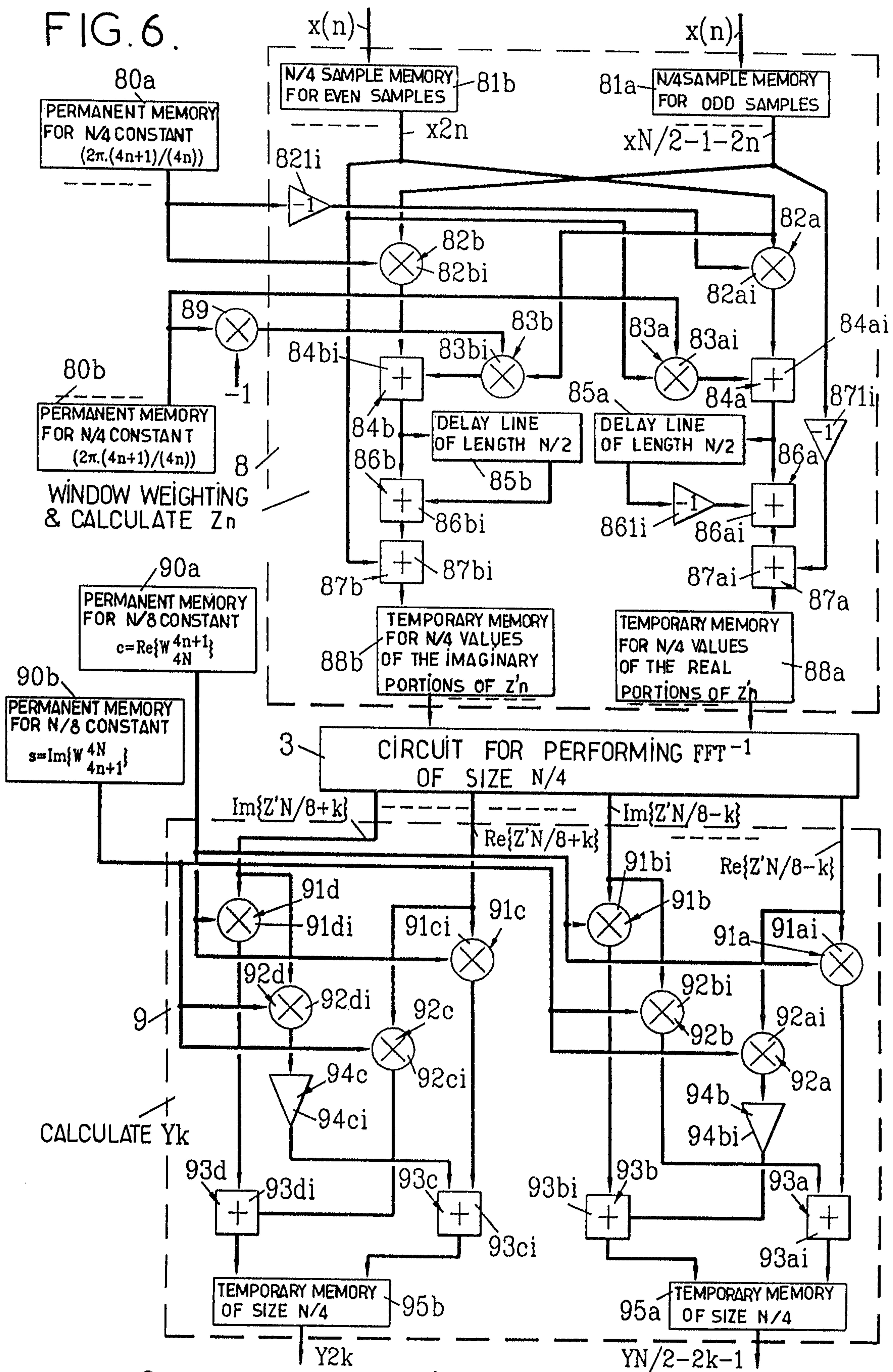


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FIG. 6.



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$$Y_{2k} = \sum_{n=0}^{N-1} y_n \cdot \cos(2\pi / (4N) \cdot (2n+1) \cdot (4k+1) + (4+1) \cdot \pi / 4) \quad (\text{I})$$

$$Y_{2k+N/4+j} Y_{2k} = \sum_{n=0}^{N/4-1} ((y'_n - y''_{n+N/4}) + j(y''_n + y'_{n+N/4})) \cdot w_{4N}(4k+1)(4n+1) \cdot (-1)^{k+1} \cdot w_8^{-1} \quad (\text{II})$$

$$Z_k = (-1)^{k+1} \cdot w_8^{-1} \cdot w_{4N}^{4k+1} \cdot \sum_{n=0}^{N/4-1} (z_n \cdot w_N^n) \cdot w_{N/4}^{nk} \quad (\text{III})$$