(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 May 2013 (23.05.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/074680 A1

(51) International Patent Classification:
H01L 29/73 (2006.01) *G01R 31/26* (2006.01)
H04B 1/00 (2006.01)

(21) International Application Number:
PCT/US2012/065090

(22) International Filing Date:
14 November 2012 (14.11.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/560,400 16 November 2011 (16.11.2011) US

(71) Applicant: **SKYWORKS SOLUTIONS, INC.** [US/US]; 20 Sylvan Road, Woburn, MA 01801 (US).

(72) Inventors: **CISMARU, Cristian**; 3843 Calle Alta Vista, Newbury Park, CA 91320 (US). **ZAMPARDI, Peter, J., Jr.**; 3995 Maurice Drive, Newbury Park, CA 91320 (US).

(74) Agent: **CHRISTENSEN, Michael, R.**; Knobbe Martens Olson & Bear LLP, 2040 Main Street, Fourteenth Floor, Irvine, CA 92614 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

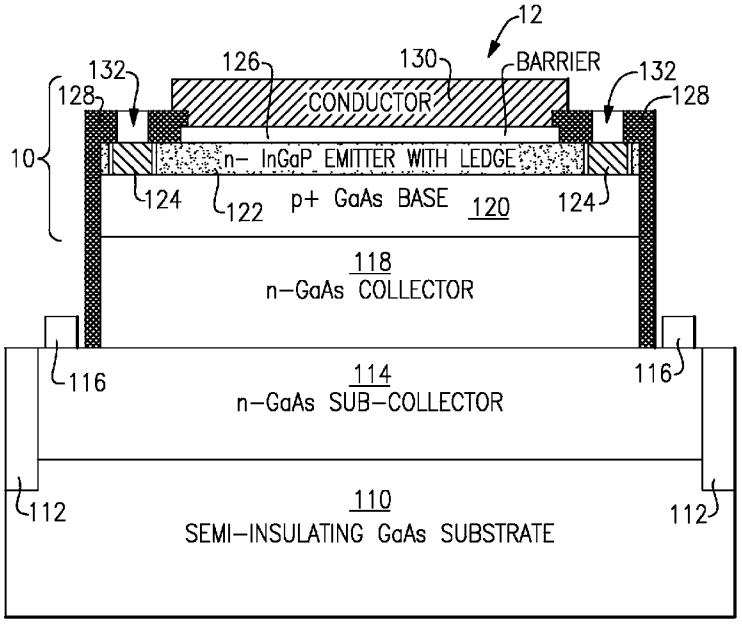
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report (Art. 21(3))*

[Continued on next page]

(54) **Title**: DEVICES AND METHODS RELATED TO A BARRIER FOR METALLIZATION IN HETEROJUNCTION BIPOLAR TRANSISTOR PROCESSES



(57) **Abstract**: Disclosed are structures and methods related to a barrier layer for metallization of a selected semiconductor such as indium gallium phosphide (InGaP). In some embodiments, the barrier layer can include tantalum nitride (TaN). Such a barrier layer can provide desirable features such as barrier functionality, improved adhesion of a metal layer, reduced diffusion, reduced reactivity between the metal and InGaP, and stability during the fabrication process. In some embodiments, structures formed in such a manner can be configured as an emitter of a gallium arsenide (GaAs) heterojunction bipolar transistor (HBT) or an on-die high-value capacitance element. In some embodiments, some of the foregoing structures can be configured as a capacitance element having a capacitance value representative of the thickness of the emitter layer. Accordingly, monitoring of such a capacitance value during various HBT processes allows monitoring of the integrity of the emitter layer.

WO 2013/074680 A1

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

DEVICES AND METHODS RELATED TO A BARRIER FOR METALLIZATION IN HETEROJUNCTION BIPOLAR TRANSISTOR PROCESSES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Application No. 61/560,400 filed November 16, 2011 and entitled "DEVICES AND METHODOLOGIES RELATED TO TaN BARRIER FOR METALLIZATION OF InGaP," which is expressly incorporated by reference herein in its entirety.

BACKGROUND

Field

[0002] The present disclosure generally relates to structures and fabrication processes associated with bipolar transistors.

Description of the Related Art

[0003] A bipolar junction transistor (BJT) typically includes two back-to-back p-n junctions formed by a base region disposed between an emitter region and a collector region. Such junctions can include a PNP configuration or an NPN configuration. The bipolar functionality results from its operation involving both electrons and holes.

[0004] A heterojunction bipolar transistor (HBT) is a type of BJT, where different semiconductor materials are utilized for the emitter and base regions to yield a heterojunction. Such a configuration can allow HBTs to be particularly useful in radio-frequency (RF) applications, including high-efficiency RF power amplifiers.

SUMMARY

[0005] According to a number of implementations, the present disclosure relates to a metallization structure that includes a selected semiconductor layer and a tantalum nitride (TaN) layer formed over the selected semiconductor layer. The selected semiconductor includes wide bandgap semiconductor lattice-matched to

gallium arsenide (GaAs). The structure further includes a metal layer formed over the TaN layer, such that the TaN layer forms a barrier between the metal layer and the selected semiconductor layer.

[0006] In some embodiments, the selected semiconductor layer can include indium gallium phosphide (InGaP). In some embodiments, the TaN layer can be configured to reduce the likelihood of the metal layer contacting the InGaP layer and behaving in an ohmic manner.

[0007] In some embodiments, the structure can further include a first gallium arsenide (GaAs) layer underneath the InGaP layer. In some embodiments, the structure can further include a metal contact disposed relative to the first GaAs layer so as to facilitate electrical connection with the first GaAs layer. The InGaP layer can be dimensioned such that the metallization structure provides a capacitance density of at least 2.0 $fF/\mu m^2$ when capacitance is measured between the metal layer and the metal contact.

[0008] In some embodiments, the first GaAs layer can be part of a base of a heterojunction bipolar transistor (HBT) and the InGaP layer can be part of an emitter of the HBT. The structure can further include a second GaAs layer configured as a collector of the HBT, and a semi-insulating GaAs substrate. In some embodiment, the HBT can be configured as an NPN or PNP transistor.

[0009] In some implementations, the present disclosure relates to a packaged module having a packaging substrate configured to receive a plurality of components. The module further includes a gallium arsenide (GaAs) die mounted on the packaging substrate and has an integrated circuit (IC). The die includes a GaAs substrate and a selected semiconductor layer formed over the GaAs substrate. The selected semiconductor includes wide bandgap semiconductor lattice-matched to GaAs. The die further includes a metallization assembly having a tantalum nitride (TaN) layer formed over the selected semiconductor layer, and a metal layer formed over the TaN layer. The TaN layer forms a barrier between the metal layer and the selected semiconductor layer.

[0010] In some embodiments, the selected semiconductor layer can include indium gallium phosphide (InGaP). In some embodiments, the metallization

assembly, the InGaP layer, and the GaAs substrate can form an on-die high-value capacitance element. Such an on-die capacitance element can be part of, for example, a power amplifier circuit, a tuning network circuit, or a power supply bypass circuit.

[0011] In some embodiments, the InGaP layer can be configured as an emitter of a heterojunction bipolar transistor (HBT). Such an HBT can be part of, for example, a power amplifier circuit configured to amplify a radio-frequency (RF) signal. In such an example context, the module can be a power amplifier module.

[0012] In accordance with some implementations, the present disclosure relates to a radio-frequency (RF) device having an antenna and a transceiver coupled to the antenna and configured to process a radio-frequency (RF) signal. The RF device also has an integrated circuit (IC) that is coupled to or is part of the transceiver and configured to facilitate the processing of the RF signal. The IC is implemented on a gallium arsenide (GaAs) die. The die includes a GaAs substrate and a selected semiconductor layer formed over the GaAs substrate. The selected semiconductor includes wide bandgap semiconductor lattice-matched to GaAs. The die further includes a metallization assembly having a tantalum nitride (TaN) layer formed over the selected semiconductor layer, and a metal layer formed over the TaN layer. The TaN layer forms a barrier between the metal layer and the selected semiconductor layer.

[0013] In some embodiments, the RF device can be a wireless device. In some embodiments, the IC can be part of a power amplifier configured to amplify the RF signal.

[0014] In a number of teachings, the present disclosure relates to a method for fabricating a metallization structure. The method includes providing or forming an underlying semiconductor layer, and forming a selected semiconductor layer over the underlying semiconductor layer. The method further includes forming a tantalum nitride (TaN) layer over the selected semiconductor layer, and forming a metal layer over the TaN layer.

[0015] In some implementations, the present disclosure relates to a gallium arsenide (GaAs) die that includes a GaAs substrate and a selected

semiconductor layer formed over the GaAs substrate. The selected semiconductor includes wide bandgap semiconductor lattice-matched to GaAs. The die further includes a metallization assembly having a tantalum nitride (TaN) layer formed over the selected semiconductor layer, and a metal layer formed over the TaN layer. The TaN layer forms a barrier between the metal layer and the selected semiconductor layer.

[0016] In some embodiments, the selected semiconductor layer can include indium gallium phosphide (InGaP). In some embodiments, the metallization assembly, the selected semiconductor layer, and the GaAs substrate can form a high-value capacitance element. In some embodiments, the selected semiconductor layer can be configured as an emitter of a heterojunction bipolar transistor (HBT). In such a configuration, the GaAs substrate can include a first GaAs layer configured as a base and a second GaAs layer configured as a collector of the HBT.

[0017] According to some implementations, the present disclosure relates to a method for fabricating a heterojunction bipolar transistor (HBT). The method includes providing or forming a gallium arsenide (GaAs) substrate, and forming a collector layer, a base layer, and an emitter layer over the GaAs substrate. The method further includes forming a barrier layer over the emitter layer, forming a metal layer over the barrier layer, and measuring capacitance between the metal layer and the base layer, with the capacitance being representative of a thickness of the emitter layer.

[0018] In some embodiments, the emitter layer can include indium gallium phosphide (InGaP). In some embodiments, the emitter layer can include a ledge. In some embodiments, the collector layer, the base layer, and the emitter layer can be configured as an NPN transistor. In some embodiments, the barrier layer can include tantalum nitride (TaN). In some embodiments, the method can further include forming a metal contact on the base layer. In some embodiments, the method can further include adjusting a process parameter so that the capacitance is within a selected range.

[0019] In a number of implementations, the present disclosure relates to a system for monitoring a heterojunction bipolar transistor (HBT) fabrication process. The system includes a process assembly configured to form an emitter layer over a base layer, a barrier layer over the emitter layer, and a metal layer over the barrier layer. The system further includes a monitoring assembly configured to measure capacitance between the metal layer and the base layer, with the measured capacitance being representative of a thickness of the emitter layer.

[0020] In some embodiments, the emitter layer can include indium gallium phosphide (InGaP). In some embodiments, the emitter layer can include a ledge. In some embodiments, the barrier layer can include tantalum nitride (TaN).

[0021] In some embodiments, the process assembly can be further configured to form a metal contact on the base layer. In some embodiments, the system can further include a process control assembly configured to adjust a process parameter so that the capacitance is within a selected range.

[0022] According to some teachings, the present disclosure relates to a method for monitoring a semiconductor fabrication process. The method includes providing or forming an underlying semiconductor layer, and forming a selected semiconductor layer over the underlying semiconductor layer. The selected semiconductor includes wide bandgap semiconductor lattice-matched to gallium arsenide (GaAs). The method further includes forming a tantalum nitride (TaN) layer over the selected semiconductor layer, and forming a metal layer over the TaN layer. The method further includes measuring capacitance between the metal layer and the underlying semiconductor layer to obtain an estimate of a thickness of the selected semiconductor layer.

[0023] In some embodiments, the method can further include adjusting a process parameter if the measured capacitance is outside of a selected range.

[0024] In some embodiments, the thickness of the selected semiconductor layer can be calculated from the measured capacitance based on an approximation that the metal layer behaves as a portion of a parallel-plate capacitor. In some embodiments, the selected semiconductor layer can include indium gallium phosphide (InGaP). In some embodiments, the underlying semiconductor layer can

include gallium arsenide (GaAs). In some embodiments, the InGaP layer and the GaAs layer can be emitter and base, respectively, of a heterojunction bipolar transistor (HBT). In some embodiments, the metal layer, the TaN layer, the InGaP layer, and the GaAs layer form a high-value capacitor having a capacitance density is at least 2.0 $fF/\mu m^2$.

[0025] According to a number of implementations, the present disclosure relates to a metallization structure that includes a first-type gallium arsenide (GaAs) layer and a second-type indium gallium phosphide (InGaP) layer disposed over the GaAs layer, with the second-type being different than the first type. The metallization structure further includes a tantalum nitride (TaN) layer disposed over the InGaP layer, and a metal layer disposed over the TaN layer.

[0026] In some embodiments, the TaN layer can be configured as a barrier layer between the metal layer and the InGaP layer to reduce the likelihood of the metallization structure behaving in an ohmic manner. The first-type GaAs layer can include a p-type GaAs layer; and the second-type InGaP layer can include an n-type InGaP layer. The metal layer includes an M1 metal layer.

[0027] In some embodiments, the metallization structure can further include a metal contact disposed relative to the GaAs layer so as to facilitate electrical connection with the GaAs layer. The InGaP layer can be dimensioned such that the structure provides a capacitance density greater than or equal to a selected value when capacitance is measured between the metal layer and the metal contact. Such a selected value of capacitance density can be at least 2.0 $fF/\mu m^2$.

[0028] In some embodiments, the first-type GaAs layer can be part of a base of a heterojunction bipolar transistor (HBT), and the second-type InGaP layer can be part of an emitter of the HBT. In some embodiments, the emitter can have a ledge.

[0029] In some implementations, the present disclosure relates to a heterojunction bipolar transistor (HBT) having a semi-insulating gallium arsenide (GaAs) substrate, a collector layer disposed over the substrate, a first-type GaAs base layer disposed over the collector, and a second-type indium gallium phosphide

(InGaP) emitter layer disposed over the base layer, with the second-type being different than the first type. The HBT further includes a tantalum nitride (TaN) layer disposed over the emitter layer, and a metal layer disposed over the TaN layer.

[0030] In some embodiments, the HBT can further include a sub-collector layer disposed between the collector layer and the GaAs substrate. The sub-collector layer can include n+ GaAs, the collector layer can include n- GaAs, the base layer can include p+ GaAs, and the emitter layer can include n- InGaP.

[0031] In a number of implementations, the present disclosure relates to a gallium arsenide (GaAs) die having an integrated circuit (IC). The die includes a metallization structure that includes a first-type GaAs layer; a second-type indium gallium phosphide (InGaP) layer disposed over the GaAs layer, with the second-type being different than the first type; a tantalum nitride (TaN) layer disposed over the InGaP layer; and a metal layer disposed over the TaN layer.

[0032] In some embodiments, the metallization structure can be part of a capacitor. In some embodiments, the metallization structure can be part of a heterojunction bipolar transistor.

[0033] In accordance with some implementations, the present disclosure relates to a packaged module that includes a packaging substrate and a gallium arsenide (GaAs) die mounted on the packaging substrate and having an integrated circuit (IC). The die includes a metallization structure that includes a first-type GaAs layer; a second-type indium gallium phosphide (InGaP) layer disposed over the GaAs layer, with the second-type being different than the first type; a tantalum nitride (TaN) layer disposed over the InGaP layer; and a metal layer disposed over the TaN layer.

[0034] According to some implementations, the present disclosure relates to a radio-frequency (RF) device that includes an antenna and a transceiver coupled to the antenna and configured to process RF signals. The RF device further includes an integrated circuit (IC) that is coupled to or is part of the transceiver. The IC is implemented on a gallium arsenide (GaAs) die, and IC includes a metallization structure that includes a first-type GaAs layer; a second-type indium gallium phosphide (InGaP) layer disposed over the GaAs layer, with the second-type

different than the first type; a tantalum nitride (TaN) layer disposed over the InGaP layer; and a metal layer disposed over the TaN layer.

[0035] In a number of implementations, the present disclosure relates to a method for fabricating a metalized semiconductor structure. The method includes forming or providing a first-type gallium arsenide (GaAs) layer, and forming a second-type indium gallium phosphide (InGaP) layer over the GaAs layer, with the second-type being different than the first type. The method further includes forming a tantalum nitride (TaN) layer over the InGaP layer, and forming a metal layer over the TaN layer.

[0036] In some implementations, the present disclosure relates to a method for fabricating a heterojunction bipolar transistor (HBT). The method includes providing or forming a semi-insulating gallium arsenide (GaAs) substrate, forming a collector layer over the substrate, forming a first-type GaAs base layer over the collector, and forming a second-type indium gallium phosphide (InGaP) emitter layer over the base layer, with the second-type being different than the first type. The method further includes forming a tantalum nitride (TaN) layer over the emitter layer, and forming a metal layer over the TaN layer. In some embodiments, such an HBT can include an NPN HBT.

[0037] According to some implementations, the present disclosure relates to a system for monitoring a heterojunction bipolar transistor (HBT) fabrication process. The system includes a component configured to metalize an emitter with a ledge that includes indium gallium phosphide (InGaP). The system further includes a monitoring component configured to measure capacitance associated with the metalized emitter, where the measured capacitance is representative of thickness of the emitter.

[0038] In some embodiments, the thickness of the emitter can be calculated from the measured capacitance based on an approximation that the metalized emitter behaves as a parallel-plate capacitor. In some embodiments, the system can further include a process control component configured to adjust at least a part of the HBT fabrication process if the measured capacitance or the calculated emitter thickness is outside of a desired range.

[0039] In a number of implementations, the present disclosure relates to a method for monitoring a heterojunction bipolar transistor (HBT) fabrication process. The method includes metalizing an emitter by providing or forming an indium gallium phosphide (InGaP) emitter; forming a tantalum nitride (TaN) layer and a metal layer so that the TaN layer acts as a barrier layer between the metal layer and the emitter. The method further includes measuring capacitance associated with the metalized emitter to obtain an estimate of a thickness of the emitter.

[0040] In some implementations, the present disclosure relates to a metallization structure that includes a selected semiconductor layer, a metal layer, and a tantalum nitride (TaN) layer disposed between the metal layer and the selected semiconductor layer so as to act as a barrier layer. The selected semiconductor includes wide bandgap semiconductor lattice-matched to gallium arsenide (GaAs). In some embodiments, the selected semiconductor layer can include an indium gallium phosphide (InGaP) layer.

[0041] For purposes of summarizing the disclosure, certain aspects, advantages and novel features of the inventions have been described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment of the invention. Thus, the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0042] Figures 1A and 1B schematically depict a capacitor such as a high-value capacitor and a heterojunction bipolar transistor (HBT) having one or more features as described herein.

[0043] Figure 2 shows that in some implementations, an integrated circuit (IC) can include the capacitor and/or the HBT of Figure 1.

[0044] Figure 3 shows that one or more ICs of Figure 2 can be implemented on a semiconductor die.

[0045] Figure 4A schematically shows that in some implementations, a packaged module can include one or more ICs of Figure 2.

[0046] Figures 4B and 4C show different views of a more specific example of the packaged module of Figure 4A.

[0047] Figure 5A schematically shows that in some implementations, a radio-frequency (RF) device such as a wireless device can include the module of Figure 4.

[0048] Figure 5B shows a more specific example of a wireless device.

[0049] Figure 6 shows an example configuration of an HBT having a barrier layer such as a tantalum nitride (TaN) layer disposed between an emitter having a ledge and an M1 conductor.

[0050] Figure 7 shows a portion of the example HBT of Figure 6 that can function as a high-value capacitor.

[0051] Figures 8A and 8B show layout and side sectional views of the example capacitor of Figure 7.

[0052] Figure 9 shows that the example metallization structure of Figures 7 and 8 can behave as a diode and not in an ohmic manner.

[0053] Figure 10 shows examples of capacitance values measured for the metallization structure of Figures 7 and 8 having different areas for the TaN layer.

[0054] Figures 11 and 12 shows additional details of the capacitance values, where active and implanted configurations can extend ranges of voltages having desired capacitance.

[0055] Figure 13 shows a process that can be implemented to fabricate the example metallization structure of Figures 7 and 8.

[0056] Figure 14 shows a process that can be implemented to fabricate the example HBT structure of Figure 6.

[0057] Figure 15 shows a process that can be implemented as a more specific example of the process of Figure 14.

[0058] Figure 16 schematically depicts an HBT process monitoring system capable of monitoring formation of an InGaP emitter with a ledge.

[0059] Figure 17 shows a process that can be implemented to fabricate the InGaP emitter and metallization thereon, test the wafer to determine thickness of the emitter, and perform process control based on the test.

[0060] Figure 18 shows an example distribution of measured capacitance density ($fF/\mu m^2$) across an example wafer being tested.

[0061] Figure 19 shows an example distribution of ledge thickness (angstrom) calculated from the measured capacitance.

[0062] Figure 20 shows an example of averaged ledge thickness variation across the example wafer.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

[0063] The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

[0064] InGaP (indium gallium phosphide)/GaAs (gallium arsenide) heterojunction bipolar transistors (HBT) are widely used for wireless applications since they have excellent features such as high power density and high efficiency. InGaP emitter structures can offer significant performance advantages over AlGaAs emitter structures. For example, InGaP emitter HBTs can exhibit improvements in temperature and bias stability, as well as significantly enhanced reliability. Further InGaP emitter HBTs can also be easier to fabricate.

[0065] Performance and reliability of an HBT can be greatly influenced by an emitter and the effectiveness of its ledge. Such a ledge typically reduces the recombination current to thereby provide better device scaling and improved reliability. Such effectiveness in desirable functionality can be based on the thickness of the emitter/ledge.

[0066] For the purpose of description herein, it will be assumed that an emitter of an HBT includes a ledge feature. Such a combination is sometimes referred to as an "emitter/ledge" or simply as an "emitter." It will be understood, however, that one or more features of the present disclosure can also be implemented in HBTs where an emitter does not include a ledge.

[0067] Given the importance of the HBT's emitter thickness, monitoring the quality of such a thickness can allow for better in-line quality control and wafer screening. In an AlGaAs HBT process, a ledge monitor can be achieved by using a first interconnect metal (M1) layer as a top electrode. The metal layer, such as a Ti/Pt/Au stack, can be deposited directly on the AlGaAs passivation ledge to form a MIS (metal-insulator-semiconductor) capacitor between M1 and the HBT base (e.g., p+ base). In-line capacitance measurements of such a structure can allow for the monitoring of the AlGaAs ledge thickness and quality. However, with the InGaP HBT processes, such a metallization structure does not work, since the metal applied to InGaP does not form a high quality Schottky contact. In some situations, application of the metal (used in the foregoing AlGaAs HBT process) in the InGaP HBT process can result in the metal punching through the InGaP ledge and behave in an ohmic manner.

[0068] Described herein are devices and methodologies related to a metallization structure that allows effective way of monitoring of InGaP ledges. As described herein, such an InGaP ledge can be part of a GaAs HBT, and/or a high-value capacitor.

[0069] In some implementations, TaN (tantalum nitride) can be utilized as a barrier between a first metal (M1) and the InGaP layer. Properties or functionalities that can be provided by a TaN layer in such a configuration can include, for example, barrier functionality, improved adhesion, reduced diffusion, reduced reactivity with metals or dielectrics, and/or stability during fabrication process. Although described in the context of TaN material, it will be understood that materials having similar properties can also be utilized. For example, TiN (titanium nitride) and NbN (niobium nitride) are metal nitride materials that can also be utilized in similar applications, including GaAs processes. In the context of TaN material, a TaN barrier layer between M1 and InGaP layer can be formed using deposition methods such as physical vapor deposition (PVD) such as sputtering, evaporation, chemical vapor deposition (CVD), metal organic CVD (MOCVD), plasma assisted CVD (PACVD), and metal organic atomic layer deposition (MOALD). Such a TaN barrier layer can have a thickness in a range of, for

example, 10 nm to 200 nm, 20 nm to 100 nm, 30 nm to 70 nm, or 40 nm to 60 nm. In the various examples described herein, the TaN barrier layer has a thickness of about 50 nm.

[0070] Similarly, although described in the context of InGaP semiconductor and process, it will be understood that one or more features of the present disclosure can also be implemented in other semiconductor materials and processes, including other HBT processes. For the purpose of description herein, semiconductor materials such as InGaP are sometimes referred to as selected semiconductors. InGaP is an example of wide bandgap semiconductor lattice-matched to gallium arsenide (GaAs). Accordingly, selected semiconductors can include wide bandgap semiconductors that are lattice-matched, substantially lattice-matched, or capable of being lattice-matched to GaAs.

[0071] Figure 1A schematically shows that one or more features related to metallization of InGaP (such as an InGaP emitter) with a barrier (such as a TaN layer) can be implemented in a capacitor 10. In some embodiments, such a capacitor can have a relatively high-value capacitance density of about 3 $fF/\mu m^2$ at about zero volt, which is about twice as much as that of a similarly sized stack capacitor. In some embodiments, a capacitor having metalized InGaP with a TaN barrier as described herein can have a capacitance density that is at least 2.8 $fF/\mu m^2$, 2.5 $fF/\mu m^2$, or 2.0 $fF/\mu m^2$.

[0072] Figure 1B schematically shows that one or more features related to the metallization of InGaP as described herein can be implemented in an HBT 12. In some embodiments, such an HBT can have an InGaP emitter whose quality (such as thickness) can be monitored during fabrication. Examples of such ledge monitoring are described herein in greater detail.

[0073] Figure 2 shows that in some embodiments, a capacitor 10 and/or an HBT 12 having one or more features as described herein can be implemented in an integrated circuit (IC) 20. In the context of the HBT 12, the IC 20 can include circuits that utilize HBTs. For example, the IC 20 can include radio-frequency (RF) related circuits where high power efficiency is desired. More specifically, the IC 20 can include circuits for RF power amplifiers configured for wireless devices. In the

context of the capacitor 10, the IC 20 can include circuits where high capacitance density is desired. More specifically, power amplifiers, tuning networks, and power supply bypass circuits are examples where one or more of such capacitors can provide beneficial functionalities.

[0074] Figure 3 shows that in some embodiments, one or more ICs of Figure 2 can be implemented as part of a semiconductor die 30. In the example shown, a first IC 20 is depicted as including a high-value capacitor 10; and a second IC 20 is depicted as including an HBT 12. As described in reference to Figure 2, it will be understood that each of the example ICs can include either or both of the capacitor 10 and the HBT 12.

[0075] In some implementations, the die 30 can include a GaAs die. In some embodiments, the die 30 can be configured for mounting onto a substrate such as a laminate to accommodate wirebond or flip-chip connections.

[0076] Figure 4A schematically shows that in some embodiments, an IC 20 having a capacitor 10 and/or an HBT 12 as described herein can be implemented in a packaged module 40. In some embodiments, such an IC can be implemented on a die (e.g., die 30 of Figure 3). The module 40 can further include one or more packaging structures 44 that provide, for example, a mounting substrate and protection for the IC 20 of the die 30. The module 40 can further include connection features 42 such as connectors and terminals configured to provide electrical connections to and from the IC 20.

[0077] Figures 4B and 4C show a plan view and a side view of a module 40 that can be a more specific example of the module 40 of Figure 4A. The example module 40 can include a packaging substrate 44 that is configured to receive a plurality of components. In some embodiments, such components can include an HBT die 20 having one or more featured as described herein. For example, the die 20 can include an HBT and/or a capacitor having one or more features described herein. In some embodiments, such an HBT and/or a capacitor can be part of a power amplifier 12. A plurality of connection pads 45 formed on the die 20 can facilitate electrical connections such as wirebonds 42 to connection pads 46 on the substrate 44 to facilitate passing of various signals to and from the die 20.

[0078] In some embodiments, the components mounted on the packaging substrate 44 or formed on or in the packaging substrate 44 can further include, for example, one or more surface mount devices (SMDs) (e.g., 47) and one or more matching networks (not shown). In some embodiments, the packaging substrate 44 can include a laminate substrate.

[0079] In some embodiments, the module 40 can also include one or more packaging structures to, for example, provide protection and facilitate easier handling of the module 40. Such a packaging structure can include an overmold 43 formed over the packaging substrate 44 and dimensioned to substantially encapsulate the various circuits and components thereon.

[0080] It will be understood that although the module 40 is described in the context of wirebond-based electrical connections, one or more features of the present disclosure can also be implemented in other packaging configurations, including flip-chip configurations.

[0081] Figure 5A schematically shows that in some embodiments, a component such as the module 40 of Figure 4 can be included in an RF device 50. Such an RF device can include a wireless device such as a cellular phone, smart phone, tablet, or any other portable device configured for voice and/or data communication. In Figure 5A, the module 40 is depicted as including a capacitor 10 and/or an HBT 12 as described herein. The RF device 50 is depicted as including other common components such an antenna 54, and also configured to receive or facilitate a power supply 52 such as a battery.

[0082] Figure 5B shows a more specific example of how the wireless device 50 of Figure 5A can be implemented. In Figure 5B, an example wireless device 50 is shown to include a module 40 (e.g., a PA module) having one or more features as described herein. For example, the PA module 40 can include a plurality of HBT power amplifiers 12 configured to provide amplifications for RF signals associated with different bands and/or modes.

[0083] In the example wireless device 50, the PA module 40 can provide an amplified RF signal to the switch 66 (via a duplexer 64), and the switch 66 can route the amplified RF signal to an antenna 54. The PA module 40 can receive an

unamplified RF signal from a transceiver 65 that can be configured and operated in known manners. The transceiver 65 can also be configured to process received signals. The transceiver 65 is shown to interact with a baseband sub-system 63 that is configured to provide conversion between data and/or voice signals suitable for a user and RF signals suitable for the transceiver 65. The transceiver 65 is also shown to be connected to a power management component 62 that is configured to manage power for the operation of the wireless device 50. Such a power management component can also control operations of the baseband sub-system 63 and other components of the wireless device 50.

[0084] The baseband sub-system 63 is shown to be connected to a user interface 60 to facilitate various input and output of voice and/or data provided to and received from the user. The baseband sub-system 63 can also be connected to a memory 61 that is configured to store data and/or instructions to facilitate the operation of the wireless device, and/or to provide storage of information for the user.

[0085] In some embodiments, the duplexer 64 can allow transmit and receive operations to be performed simultaneously using a common antenna (e.g., 54). In Figure 5B, received signals are shown to be routed to "Rx" paths (not shown) that can include, for example, a low-noise amplifier (LNA).

[0086] The example duplexer 64 is typically utilized for frequency-division duplexing (FDD) operation. It will be understood that other types of duplexing configurations can also be implemented. For example, a wireless device having a time-division duplexing (TDD) configuration can include respective low-pass filters (LPF) instead of the duplexers, and the switch (e.g., 66 in Figure 5B) can be configured to provide band selection functionality, as well as Tx/Rx (TR) switching functionality.

[0087] A number of other wireless device configurations can utilize one or more features described herein. For example, a wireless device does not need to be a multi-band device. In another example, a wireless device can include additional antennas such as diversity antenna, and additional connectivity features such as Wi-Fi, Bluetooth, and GPS.

[0088] Figure 6 shows an example of an HBT 12 structure having an InGaP emitter (with a ledge) 122 (such as an n- InGaP) metalized with a conductor 130 (such as an M1 layer) over a barrier layer 126 (such as a TaN layer). Such a metalized emitter is shown to be disposed over a base layer 120 (such as a p+ GaAs layer). Base contacts 124 are shown to be disposed over the base layer 120 so as to facilitate electrical connection with the base layer 120. For the purpose of description, an assembly that includes the M1 layer 130, the TaN barrier layer 126, the InGaP emitter 122, the base layer 120, and the base contacts 124 can be considered to be a high-value capacitor 10. Additional details concerning such a capacitor are described herein.

[0089] Figure 6 further shows that the foregoing assembly that can act as the capacitor 10 can be disposed over a collector layer 118 (such as an n- GaAs layer). The collector layer 118 can, in turn, be disposed over a sub-collector layer 114 (such as an n+ GaAs layer). Collector contacts 116 can also be disposed over the sub-collector layer 114. The sub-collector layer 114 can, in return, be disposed over a semi-insulating substrate 110 (such as a semi-insulating GaAs substrate).

[0090] Figure 6 further shows that a passivation structure 128 can be formed about the emitter 122 and the base 120. Access to the base contacts 124 is shown to be provided by openings 132 defined by the passivation structure 128. The HBT 12 can further include isolation structures 112 configured to provide isolation for the HBT 12.

[0091] Although the example HBT structure 12 is described in the context of an NPN GaAs configuration, other configurations such as PNP GaAs can also benefit from one or more features as described herein. Further, a concept of metalizing an emitter layer of an HBT with a barrier layer such as a TaN layer can also be implemented in other types of HBTs.

[0092] Figure 7 shows an enlarged view of the capacitor structure 10 described in reference to Figure 6. In the example configuration shown, a TaN layer can be used as the barrier layer 126, and an M1 metal layer can be used as the conductor 130. An assembly formed in the foregoing manner can yield a diode configuration 150 having a Schottky behavior (depicted as 152) for the M1 electrode

130, leading to a desired MIS capacitor formation. The junction between the base layer 120 and the emitter layer 122 can behave as a diode 154 as shown.

[0093] In some embodiments, as described in reference to Figure 6, the capacitor structure 10 can be a part of an HBT (12) structure. In some embodiments, the capacitor structure 10 can be utilized as a high-value capacitor without being associated with an HBT.

[0094] Figures 8A and 8B show layout and side sectional views of an example capacitor structure 10 that can be implemented based on the examples of Figures 6 and 7. A base layer 120 is depicted as being a rectangular shaped region formed over an underlying layer 202. An emitter (with a ledge) 122 is depicted as being a rectangular region formed over and within the area of the base layer 120. An opening 132 for providing electrical connections to base contacts 124 (not shown in Figure 8A) is depicted as a via having a footprint in an inverted-U shape. As shown in Figure 8B, the base contacts 124 are shown to be connected to an M1 metal layer 204 through conductors 206. The example M1 metal layer 204 is depicted as also having an inverted-U shaped footprint.

[0095] Figures 8A and 8B further show that a TaN barrier layer 126 can be formed over the emitter 122 and have a rectangular shaped footprint. Such a rectangle can be dimensioned (length L and width W) so as to be nested within the inverted-U shape of the M1 metal layer 204. The TaN barrier layer 126 is also depicted as having a thickness (208 in Figure 8B). An M1 metal layer 130 is shown to be formed over the TaN barrier layer 126 and have an inverted-T shaped footprint. The TaN layer 126 can be dimensioned so that the leg portion of the T-shape covers the TaN barrier 126 and also be nested within the inverted-U shape of the M1 metal layer 204.

[0096] Figure 9 shows I-V curves for the capacitor structure 10 (Figures 7 and 8) having different values of the TaN layer area. The measured (between the emitter terminal 130 and the base terminal 204) I-V curves show that the devices tested have a desired Schottky behavior indicative of desired InGaP ledge thicknesses and quality. If the InGaP ledge is too thin, such an I-V curve can

behave almost like a tunnel diode (with very low turn-on voltage due to the thin InGaP layer) between the TaN layer and the p-type base layer.

[0097] Figure 10 shows capacitance curves (measured between the emitter terminal 130 and the base terminal 204) as a function of voltage for the capacitor structure 10 (Figures 7 and 8) having different values of the TaN layer area. Since the capacitor structure 10 can be approximated as a parallel-plate capacitor (where capacitance C is proportional to area), the measured capacitance values increase as the area increases, as expected. Since the parallel-plate capacitance C is also inversely proportional to the gap distance between the electrodes, a measured capacitance value will be approximately inversely proportional to the thickness of the emitter for a given TaN layer area. Accordingly, such capacitance measurement can provide information about the emitter thickness. An example application of such thickness determination is described herein in greater detail.

[0098] Figure 10 further shows that one or more layers of the capacitor structure 10 can be configured to adjust its operating voltage range. For example, each of the area cases shown, data points include those belonging to “active” and “implanted” configurations. In the plots, the "implanted" data points generally start from the left side (less than -2V), and the "active" data points generally start from about -1.5V. For the purpose of description herein, an active configuration refers to epitaxial layers as grown; and an implant configuration refers to a damage implant in a process meant to disrupt the crystal lattice and thus provide electrical isolation between devices. In the context of the example of Figure 10, the implant may damage both the emitter and the base, although its target is much deeper. The active cases are shown to have a desirable operating range (where capacitance is generally flat) between about -1V to about +4V, while the implanted cases generally operate between about -2V to about +3V.

[0099] Figures 11 and 12 show more pronounced deviations from the desired flatness response. Figure 11 shows a plot of area capacitance density ($F/\mu m^2$) for active and implanted cases; and Figure 12 shows a plot of fringe (peripheral) capacitance ($F/\mu m$) of the emitter. By characterizing various area and

periphery configurations, one can obtain the area component of capacitance separately from the periphery component. As described herein, both of the area and the periphery contributions can provide relatively flat response over a voltage range of interest. The foregoing methodology also allows one to better estimate capacitance of larger devices where the area component dominates.

[0100] In Figure 11, the implanted case's deviation at about +3V is readily apparent, while the active case extends out to about +4V. In Figure 12, the active case's deviation at about -1V is also readily apparent, while the implanted case extends out to about -2V. Accordingly, the examples in Figures 10-12 show that the operating voltage range can be adjusted as needed or desired. For example, if it is desired to have an extended range in the negative voltage side, implantation can provide such an extension. In another example, if it is desired to have an extended range in the positive voltage side, maintaining an active configuration can provide such an extension.

[0101] Figure 13 shows a process 300 that can be implemented to fabricate a capacitor structure having one or more features as described herein. In block 302, an active layer can be formed or provided. In some implementations, such an active layer can include a p+ GaAs layer. In block 304, an InGaP layer can be formed over the active layer. In block 306, a TaN layer can be formed over the InGaP layer. In block 308, a metal layer can be formed over the TaN layer, such that the TaN layer acts as a barrier layer between the metal layer and the InGaP layer. In block 310, an electrical contact for the active layer can be formed. In some implementations, the metal layer and the electrical contact can act as electrodes if the capacitor structure is utilized as a capacitor element.

[0102] Figure 14 shows a process 320 that can be implemented to fabricate an HBT structure having one or more features as described herein. In block 322, a substrate can be formed or provided. In some embodiments, such a substrate can include a semi-insulating GaAs substrate. In block 324, a collector can be formed over the substrate. In some implementations, such a collector can include an n+ GaAs sub-collector layer formed over the substrate, and an n- GaAs collector layer formed over the sub-collector layer. In block 326, a base can be

formed over the collector. In some implementations, such a base can include a p+ GaAs base layer formed over the collector layer. In block 328, an emitter having a ledge can be formed over the base. In some implementations, such an emitter can include an n- InGaP emitter layer formed over the base layer. In block 330, a barrier can be formed over the emitter. In some implementations, such a barrier can include a TaN barrier layer formed over the emitter layer. In block 332, a metal structure can be formed over the barrier so that the barrier is between the metal structure and the emitter. In some implementations, such a metal structure can include an M1 metal layer formed over the barrier layer. Other structures such as contacts for the base and the collector can also be formed at appropriate stages.

[0103] Figure 15 shows a process 340 that can be implemented as a more specific example of the process 320 of Figure 14. In block 342, a semi-insulating GaAs substrate can be provided. In block 344, an n+ GaAs sub-collector layer can be formed over the substrate. In block 346, an n- GaAs collector layer can be formed over the sub-collector layer. In block 348, a p+ GaAs base layer can be formed over the collector layer. In block 350, an n- InGaP emitter layer can be formed over the base layer. In block 352, a TaN barrier layer can be formed over the emitter layer. In block 354, an M1 metal layer can be formed so that the TaN barrier layer is between the M1 layer and the InGaP emitter layer.

[0104] Figure 16 shows that in some implementations, one or more features described herein can be utilized in an HBT process monitoring system 400. Such a system can include, for example, a component 402 configured to form InGaP emitters. In some implementations, such emitters can be formed on a wafer so as to facilitate fabrication of a plurality of HBT devices. The system 400 can also include a component 404 configured to perform capacitance measurements. Such a component can perform measurements of capacitance of a capacitor structure described herein, where the thickness of the emitter can influence capacitance. The system 400 can also include a component 406 configured to perform process control. Such a component can monitor the thickness of emitters being formed based on the capacitance measurements, and perform maintenance or adjustment

to the emitter-formation process so as to yield emitters having desired properties such as a desired thickness.

[0105] Figure 17 shows a process 410 that can be performed by, or to facilitate, the HBT process monitoring system 400 of Figure 16. The process 410 can generally include a sub-process (e.g., 412 to 420) for partial fabrication of an HBT device, a sub-process (e.g., 430 and 432) for measurement of such a device, and a sub-process (e.g., 450) for process control based on such a measurement. It will be understood that the foregoing example sub-processes can be performed at a single facility, or at two or more different facilities.

[0106] In block 412, a base layer (e.g., p+ GaAs) can be formed on a wafer. In some implementations, such a wafer can already include other HBT components (e.g., sub-collector and collector layers). In block 414, an InGaP emitter can be formed over the base layer. In block 416, an electrical connection can be formed for the base layer. In some implementations such an electrical connection can include base contacts (e.g., 124 in Figure 6). In block 418, a TaN layer can be formed over the InGaP emitter. In block 420, a metal layer (e.g., M1 metal layer) can be formed over the TaN layer.

[0107] In block 430, capacitance can be measured between the metal layer associated with the InGaP emitter and the electrical connection associated with the base layer. In block 432, thickness of the InGaP emitter can be calculated based on the measured capacitance. An example of how such thickness can be calculated is described herein in greater detail.

[0108] In block 450, process control can be performed based on the calculated thickness of the InGaP emitter. Such process control can include, for example, maintenance or adjustment to the InGaP emitter formation process so as to yield emitters having a thickness within a desire range.

[0109] Figures 18-20 show examples of measurements and calculated values associated with InGaP emitters formed at various locations on a sample wafer. Figure 18 shows a normal quantile plot of capacitance density measurements as well as a distribution of the capacitance density values. As shown, the average capacitance density is about 3.00 $fF/\mu m^2$.

[0110] Figure 19 shows a normal quantile plot of emitter ledge thickness values calculated from the capacitance measurements as well as a distribution of the thickness values. As described herein, various capacitor structures described herein can be approximated as a parallel-plate capacitor. Accordingly, capacitance C can be expressed as $C = \frac{\varepsilon_r \cdot \varepsilon_0 A}{d}$, where ε_r represents relative permittivity or dielectric constant (about 11.75 for InGaP), ε_0 represents electric constant (approximately 8.854×10^{-12} F/m), A represents area, and d represents thickness. Thus, thickness (d) values can be calculated from capacitance density (C/A) values.

[0111] A distribution of emitter thickness values across the sample wafer is depicted as a contour plot in Figure 20. In the example shown, the center area has smaller thickness values (e.g., about 330 angstroms); and the edge portions have larger thickness values (e.g., about 350 angstroms).

[0112] Based on the foregoing, a number of process verifications and/or adjustments can be achieved. For example, suppose that an acceptable range of emitter thickness includes all of the monitored thickness values. Then, the monitoring process has verified that at least the emitter formation portion is being achieved in a desirable manner. In another example, suppose that substantially all of the monitored thickness values are outside of the acceptable range. Then, there may be some systematic problem that needs to be identified and fixed. In yet another example, suppose that thickness values are too small at one location of the wafer and/or too large at another location. Then, it may be possible to refine the emitter deposition technique to obtain a more uniform distribution of thickness values across the wafer.

[0113] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when

used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0114] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0115] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0116] While some embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover

such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A metallization structure comprising:

a selected semiconductor layer that includes wide bandgap semiconductor lattice-matched to gallium arsenide (GaAs);

a tantalum nitride (TaN) layer formed over the selected semiconductor layer; and

a metal layer formed over the TaN layer, the TaN layer forming a barrier between the metal layer and the selected semiconductor layer.

2. The structure of claim 1 wherein the selected semiconductor layer includes indium gallium phosphide (InGaP).

3. The structure of claim 2 wherein the TaN layer is configured to reduce the likelihood of the metal layer contacting the InGaP layer and behaving in an ohmic manner.

4. The structure of claim 2 further comprising a first gallium arsenide (GaAs) layer underneath the InGaP layer.

5. The structure of claim 4 further comprising a metal contact disposed relative to the first GaAs layer so as to facilitate electrical connection with the first GaAs layer.

6. The structure of claim 5 wherein the InGaP layer is dimensioned such that the metallization structure provides a capacitance density of at least 2.0 $fF/\mu m^2$ when capacitance is measured between the metal layer and the metal contact.

7. The structure of claim 4 wherein the first GaAs layer is part of a base of a heterojunction bipolar transistor (HBT) and the InGaP layer is part of an emitter of the HBT.

8. The structure of claim 7 wherein the emitter includes a ledge.

9. The structure of claim 7 further comprising a second GaAs layer configured as a collector of the HBT, and a semi-insulating GaAs substrate.

10. The structure of claim 9 wherein the HBT is configured as an NPN transistor.

11. A packaged module comprising:

a packaging substrate configured to receive a plurality of components; and

a gallium arsenide (GaAs) die mounted on the packaging substrate and having an integrated circuit (IC), the die including a GaAs substrate and a selected semiconductor layer formed over the GaAs substrate and including wide bandgap semiconductor lattice-matched to GaAs, the die further including a metallization assembly having a tantalum nitride (TaN) layer formed over the selected semiconductor layer, and a metal layer formed over the TaN layer, the TaN layer forming a barrier between the metal layer and the selected semiconductor layer.

12. The module of claim 11 wherein the selected semiconductor layer includes indium gallium phosphide (InGaP).

13. The module of claim 11 wherein the metallization assembly, the InGaP layer, and the GaAs substrate form an on-die high-value capacitance element.

14. The module of claim 13 wherein the on-die capacitance element is part of a power amplifier circuit, a tuning network circuit, or a power supply bypass circuit.

15. The module of claim 11 wherein the InGaP layer is configured as an emitter of a heterojunction bipolar transistor (HBT).

16. The module of claim 15 wherein the HBT is part of a power amplifier circuit configured to amplify a radio-frequency (RF) signal.

17. The module of claim 16 wherein the module is a power amplifier module.

18. A radio-frequency (RF) device, comprising:

an antenna;

a transceiver coupled to the antenna and configured to process a radio-frequency (RF) signal; and

an integrated circuit (IC) that is coupled to or is part of the transceiver and configured to facilitate the processing of the RF signal, the IC implemented on a gallium arsenide (GaAs) die, the die including a GaAs substrate and a selected semiconductor layer formed over the GaAs substrate and including wide bandgap semiconductor lattice-matched to GaAs, the die further including a metallization assembly having a tantalum nitride (TaN) layer formed over the selected semiconductor layer, and a metal layer formed over the TaN layer, the TaN layer forming a barrier between the metal layer and the selected semiconductor layer.

19. The RF device of claim 18 wherein the RF device is a wireless device.

20. The RF device of claim 19 wherein the IC is part of a power amplifier configured to amplify the RF signal.

21. A method for fabricating a heterojunction bipolar transistor (HBT), the method comprising:

providing or forming a gallium arsenide (GaAs) substrate;

forming a collector layer, a base layer, and an emitter layer over the GaAs substrate;

forming a barrier layer over the emitter layer;

forming a metal layer over the barrier layer; and

measuring capacitance between the metal layer and the base layer, the capacitance representative of a thickness of the emitter layer.

22. The method of claim 21 wherein the emitter layer includes indium gallium phosphide (InGaP).

23. The method of claim 22 wherein the emitter layer includes a ledge.

24. The method of claim 21 wherein the collector layer, the base layer, and the emitter layer are configured as an NPN transistor.

25. The method of claim 21 wherein the barrier layer includes tantalum nitride (TaN).

26. The method of claim 21 further comprising forming a metal contact on the base layer.

27. The method of claim 21 further comprising adjusting a process parameter so that the capacitance is within a selected range.

28. A system for monitoring a heterojunction bipolar transistor (HBT) fabrication process, the system comprising:

a process assembly configured to form an emitter layer over a base layer, a barrier layer over the emitter layer, and a metal layer over the barrier layer; and

a monitoring assembly configured to measure capacitance between the metal layer and the base layer, the measured capacitance representative of a thickness of the emitter layer.

29. The system of claim 28 wherein the emitter layer includes indium gallium phosphide (InGaP).

30. The system of claim 29 wherein the emitter layer includes a ledge.

31. The system of claim 28 wherein the barrier layer includes tantalum nitride (TaN).

32. The system of claim 28 wherein the process assembly is further configured to form a metal contact on the base layer.

33. The system of claim 28 further comprising a process control assembly configured to adjust a process parameter so that the capacitance is within a selected range.

34. A method for monitoring a semiconductor fabrication process, the method comprising:

providing or forming an underlying semiconductor layer;

forming a selected semiconductor layer over the underlying semiconductor layer, the selected semiconductor layer including wide bandgap semiconductor lattice-matched to gallium arsenide (GaAs);

forming a tantalum nitride (TaN) layer over the selected semiconductor layer;

forming a metal layer over the TaN layer; and

measuring capacitance between the metal layer and the underlying semiconductor layer to obtain an estimate of a thickness of the selected semiconductor layer.

35. The method of claim 34 further comprising adjusting a process parameter if the measured capacitance is outside of a selected range.

36. The method of claim 34 wherein the thickness of the selected semiconductor layer is calculated from the measured capacitance based on an approximation that the metal layer behaves as a portion of a parallel-plate capacitor.

37. The method of claim 34 wherein the selected semiconductor layer includes indium gallium phosphide (InGaP).

38. The method of claim 37 wherein the underlying semiconductor layer includes gallium arsenide (GaAs).

39. The method of claim 38 wherein the InGaP layer and the GaAs layer are emitter and base, respectively, of a heterojunction bipolar transistor (HBT).

40. The method of claim 38 wherein the metal layer, the TaN layer, the InGaP layer, and the GaAs layer form a high-value capacitor having a capacitance density is at least 2.0 $fF/\mu m^2$.

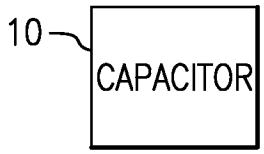


FIG.1A

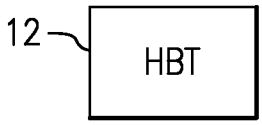


FIG.1B

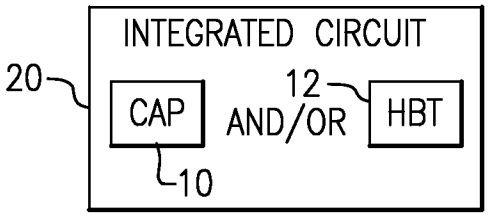


FIG.2

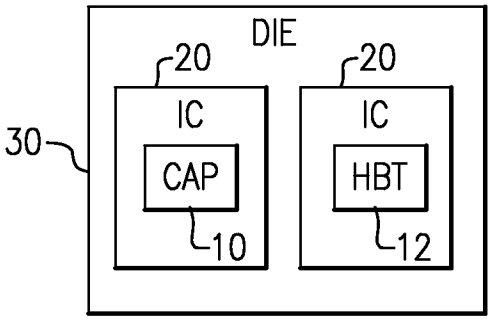


FIG.3

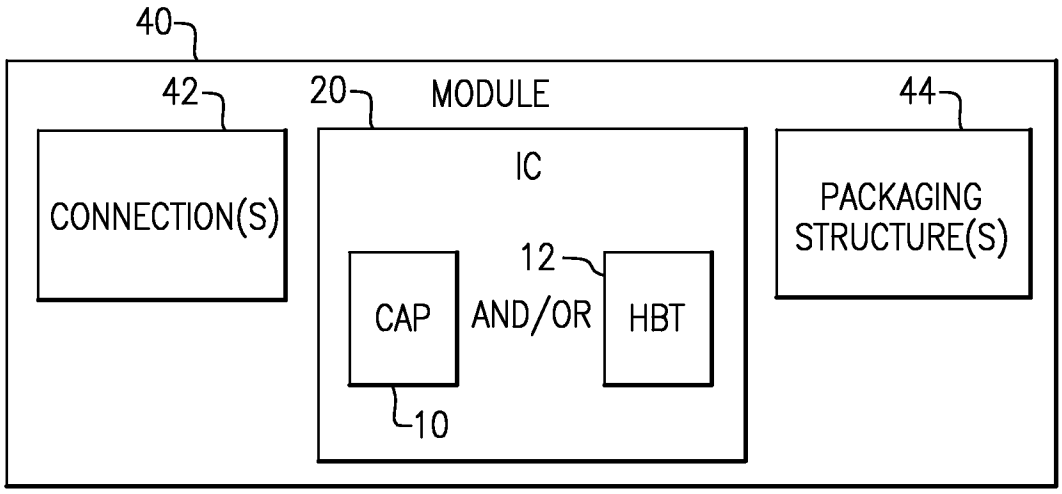


FIG.4A

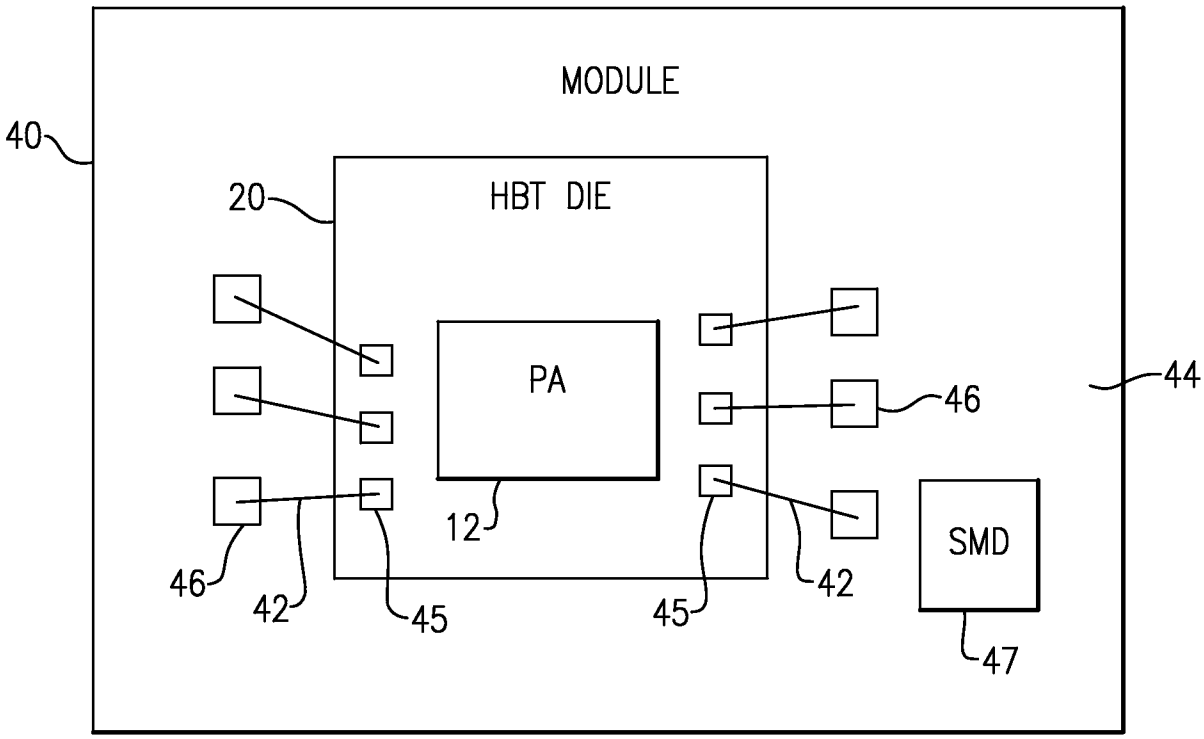

MODULE
40
20
HBT DIE
PA
12
46
44
46
42
45
45
42
SMD
47

FIG.4B

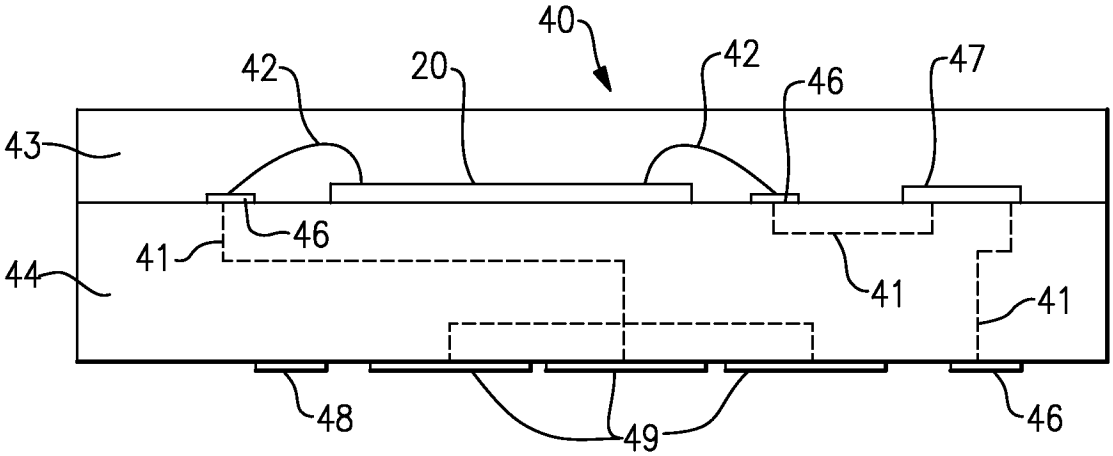

40
42
20
42
46
47
43
46
41
44
41
41
48
49
46

FIG.4C

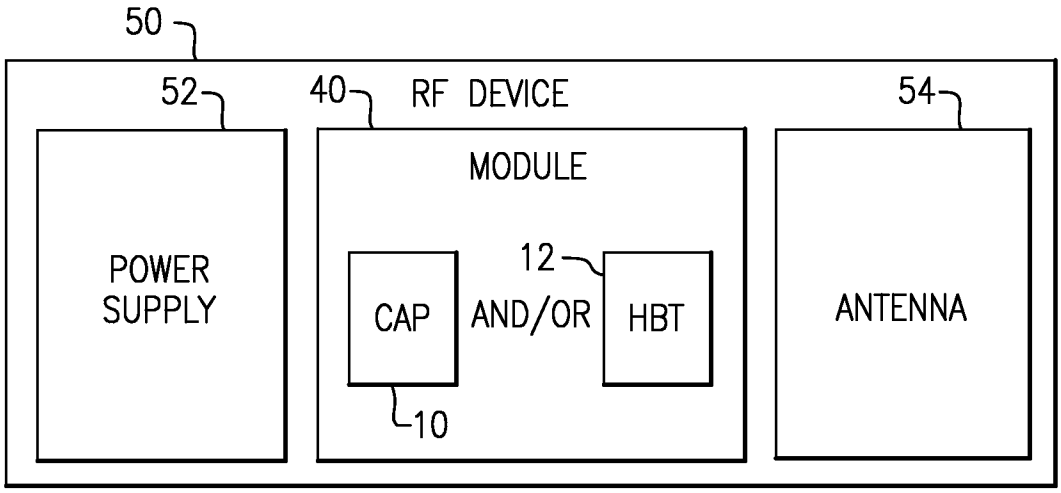

50
52
40
RF DEVICE
54
MODULE
POWER SUPPLY
12
CAP
AND/OR
HBT
ANTENNA
10

FIG.5A

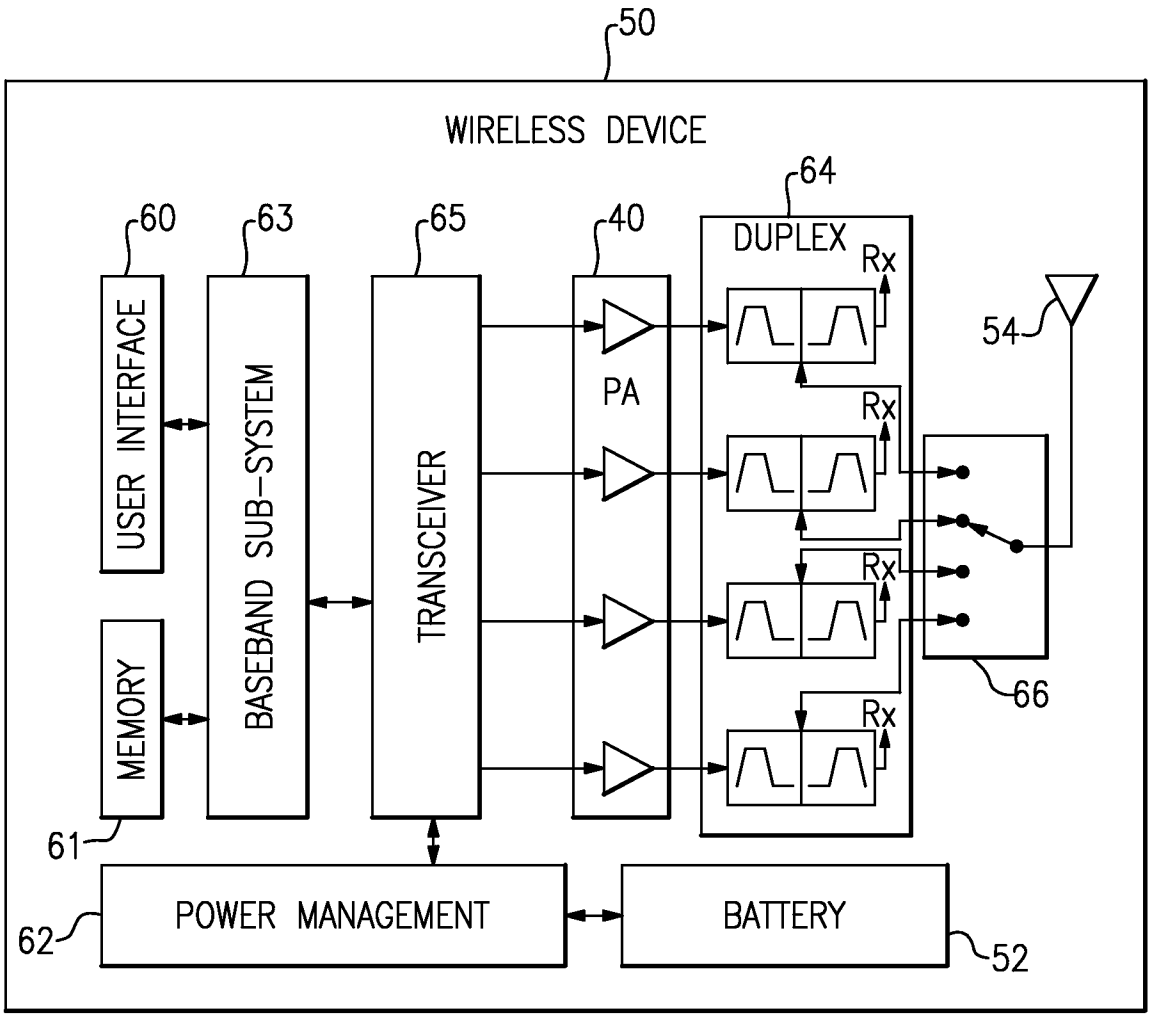

50
WIRELESS DEVICE
64
60
63
65
40
DUPLEX
Rx
54
USER INTERFACE
BASEBAND SUB-SYSTEM
TRANSCEIVER
PA
Rx
MEMORY
Rx
66
Rx
61
POWER MANAGEMENT
BATTERY
62
52

FIG.5B

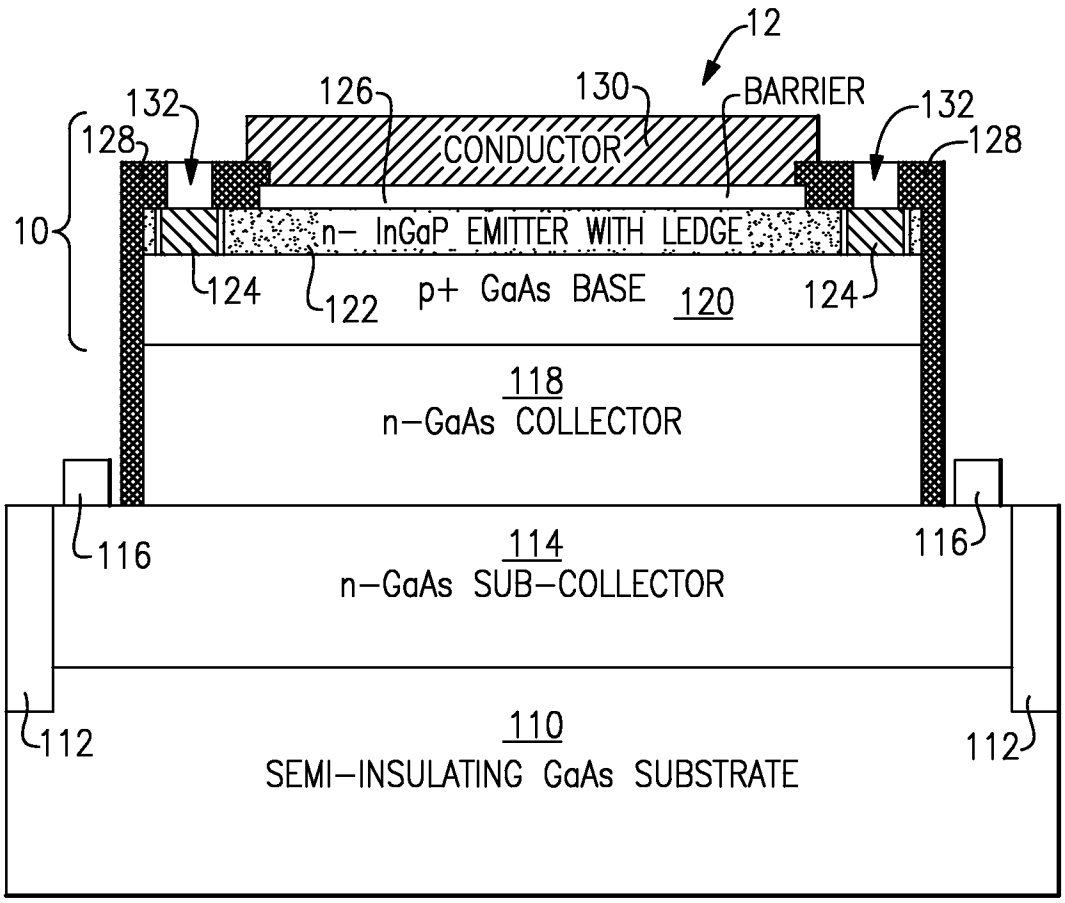

12
132
126
130
BARRIER
132
128
CONDUCTOR
128
10
n- InGaP EMITTER WITH LEDGE
124
122
p+ GaAs BASE
120
124
118
n-GaAs COLLECTOR
116
114
116
n-GaAs SUB-COLLECTOR
112
110
112
SEMI-INSULATING GaAs SUBSTRATE

FIG.6

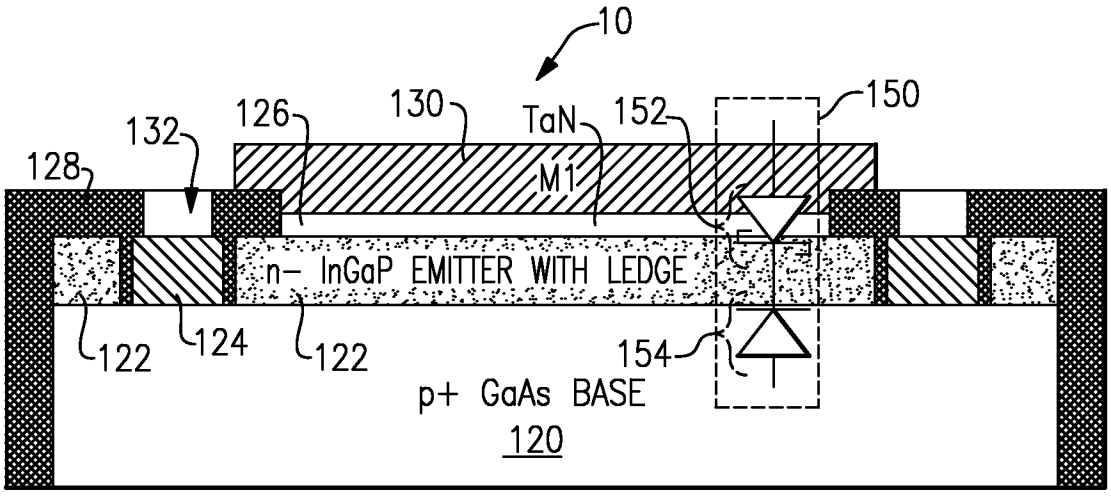

10
126
130
TaN
152
150
132
128
M1
n- InGaP EMITTER WITH LEDGE
122
124
122
154
p+ GaAs BASE
120

FIG.7

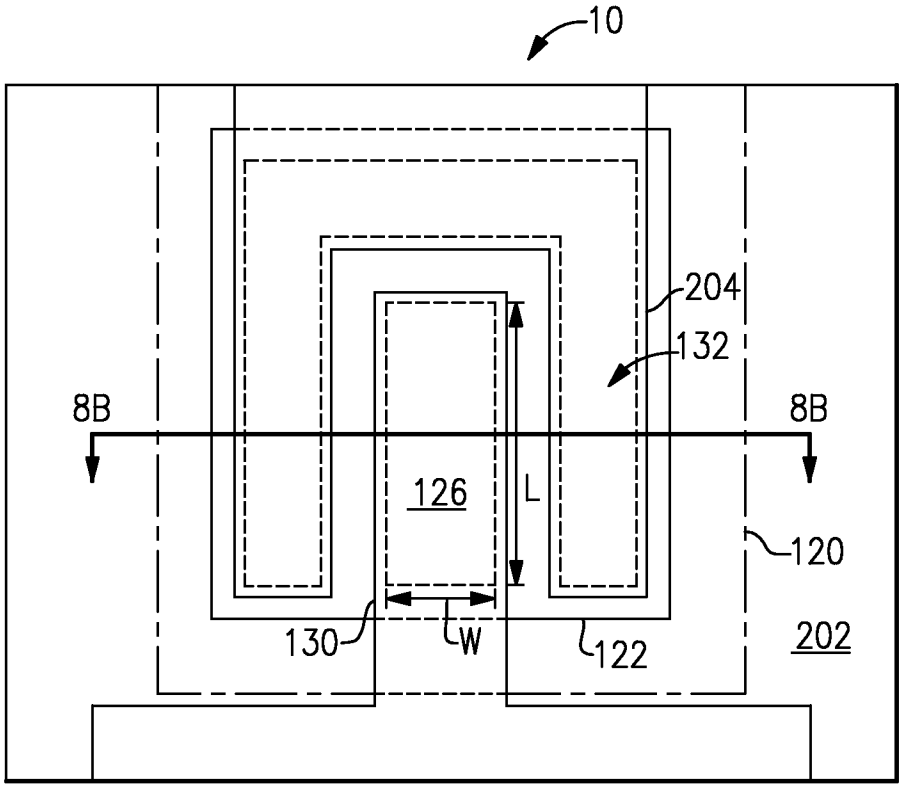

10
204
132
8B
8B
126
L
120
130
W
122
202

FIG.8A

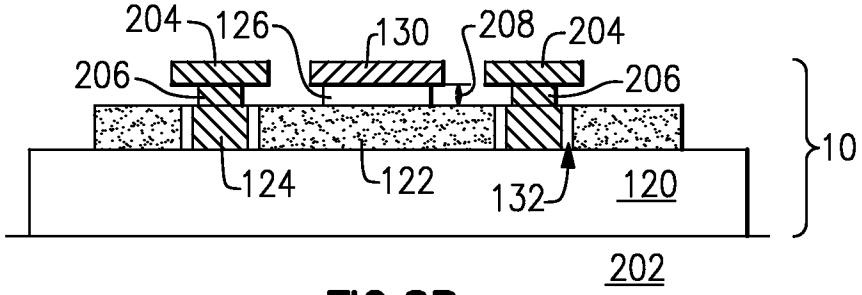

204
126
130
208
204
206
206
124
122
132
120
10
202

FIG.8B

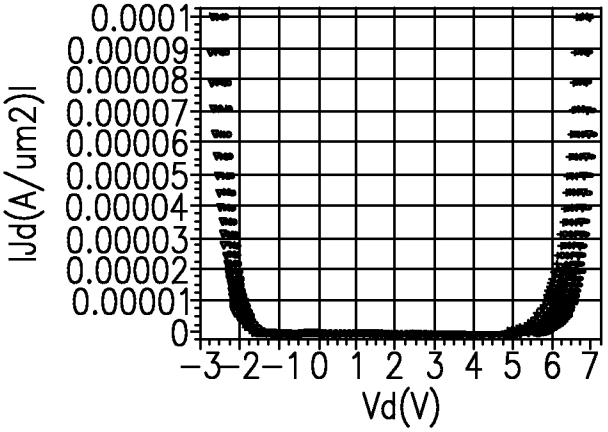

0.0001
0.00009
0.00008
0.00007
0.00006
0.00005
0.00004
0.00003
0.00002
0.00001
0
|Jd(A/um2)|
−3 −2 −1 0 1 2 3 4 5 6 7
Vd(V)

FIG.9

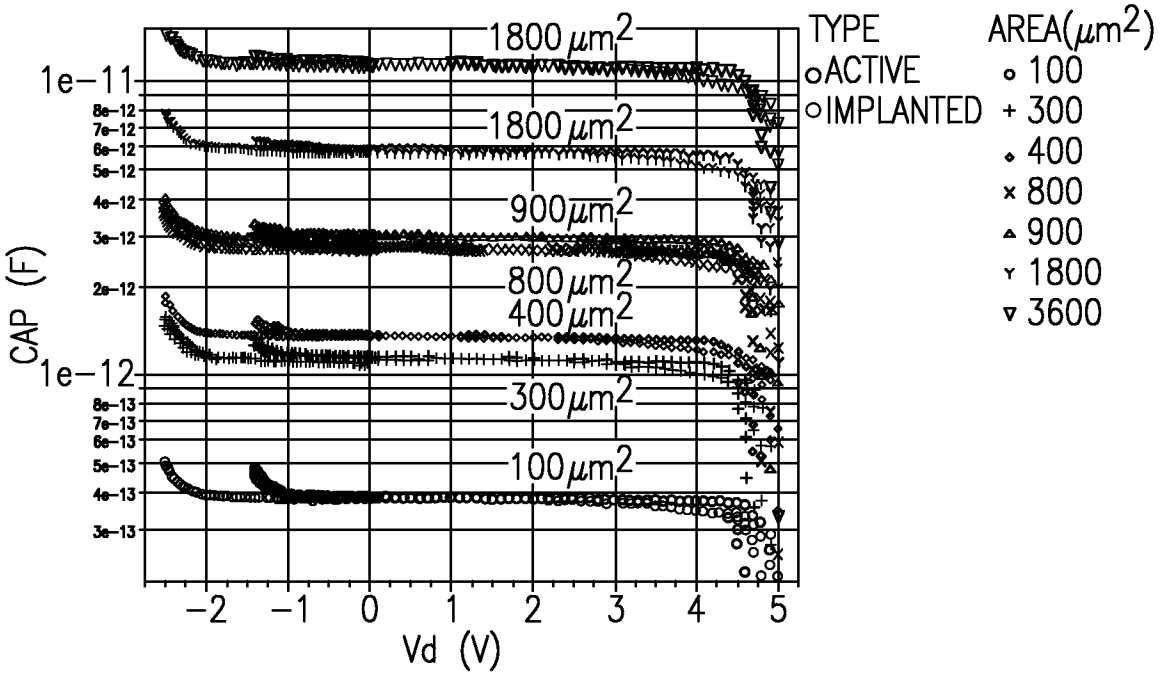

1800 μm2
1800 μm2
900 μm2
800 μm2
400 μm2
300 μm2
100 μm2
1e−11
8e−12
7e−12
6e−12
5e−12
4e−12
3e−12
2e−12
1e−12
8e−13
7e−13
6e−13
5e−13
4e−13
3e−13
CAP (F)
−2 −1 0 1 2 3 4 5
Vd (V)
TYPE
ACTIVE
IMPLANTED
AREA(μm2)
100
300
400
800
900
1800
3600

FIG.10

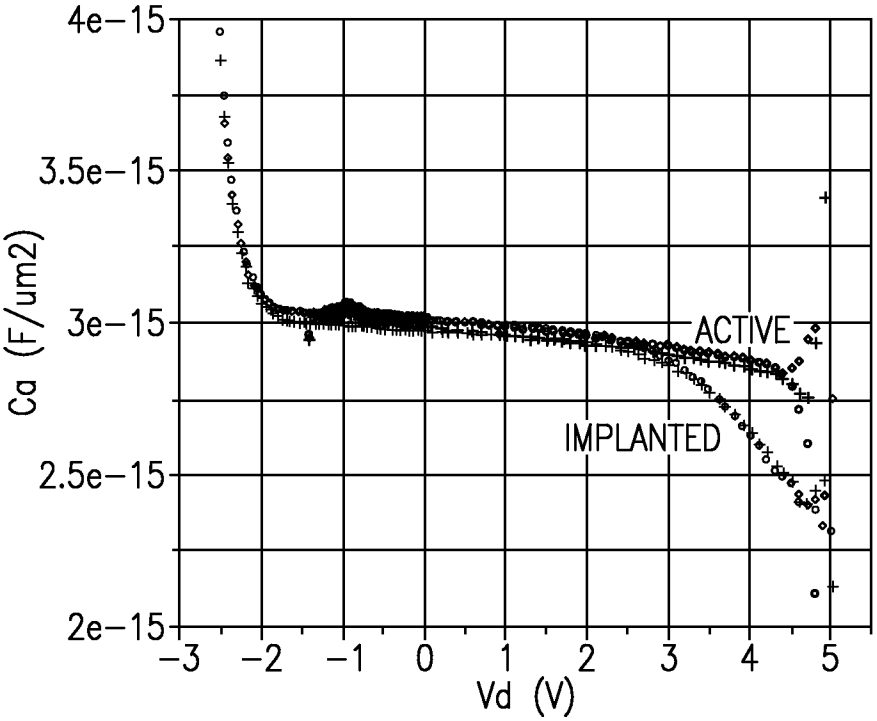

4e−15
3.5e−15
3e−15
2.5e−15
2e−15
Ca (F/um2)
ACTIVE
IMPLANTED
−3 −2 −1 0 1 2 3 4 5
Vd (V)

FIG.11

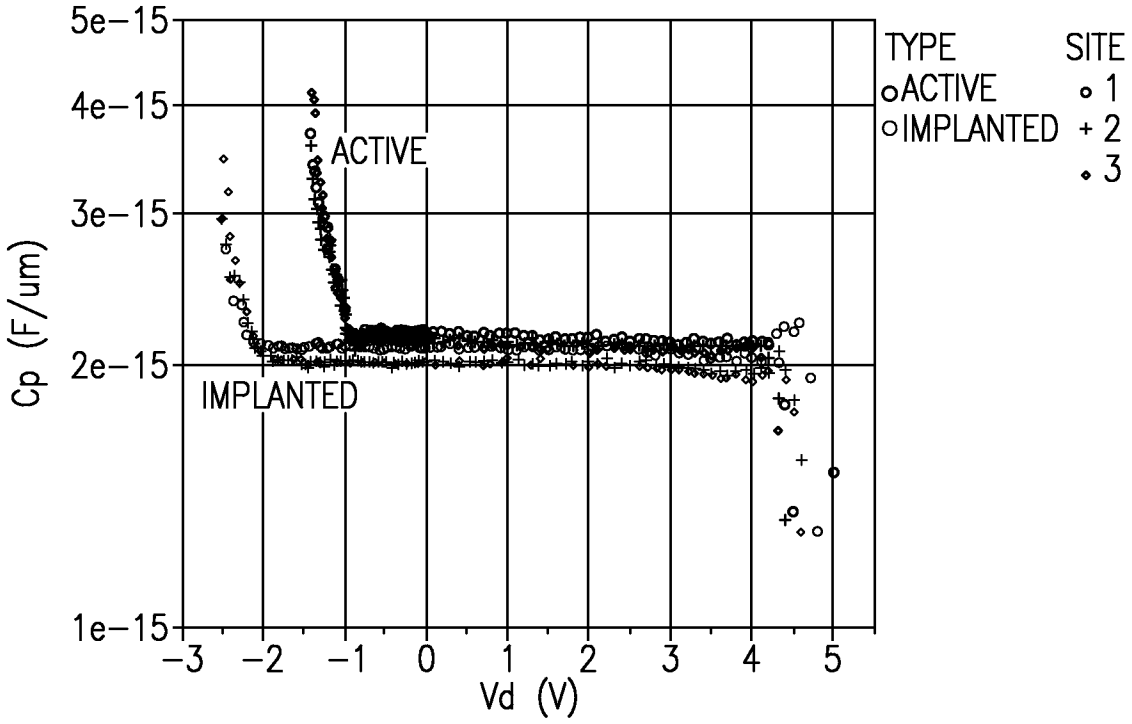

5e−15
4e−15
3e−15
2e−15
1e−15
Cp (F/um)
ACTIVE
IMPLANTED
−3 −2 −1 0 1 2 3 4 5
Vd (V)
TYPE SITE
ACTIVE 1
IMPLANTED 2
3

FIG.12

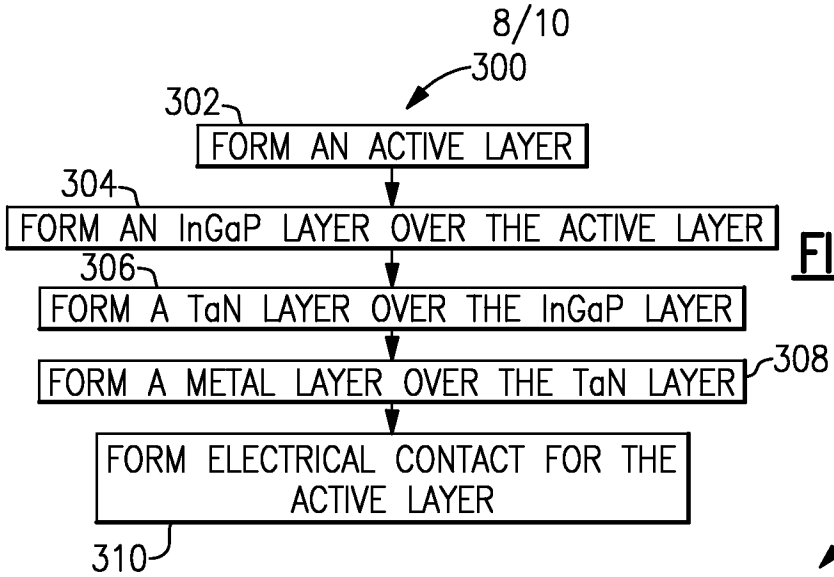


FIG.13

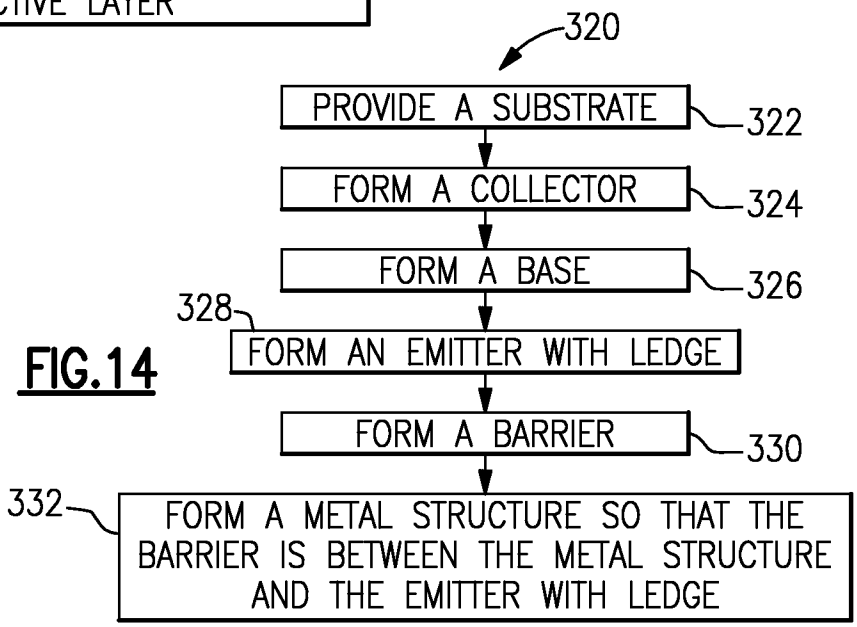


FIG.14

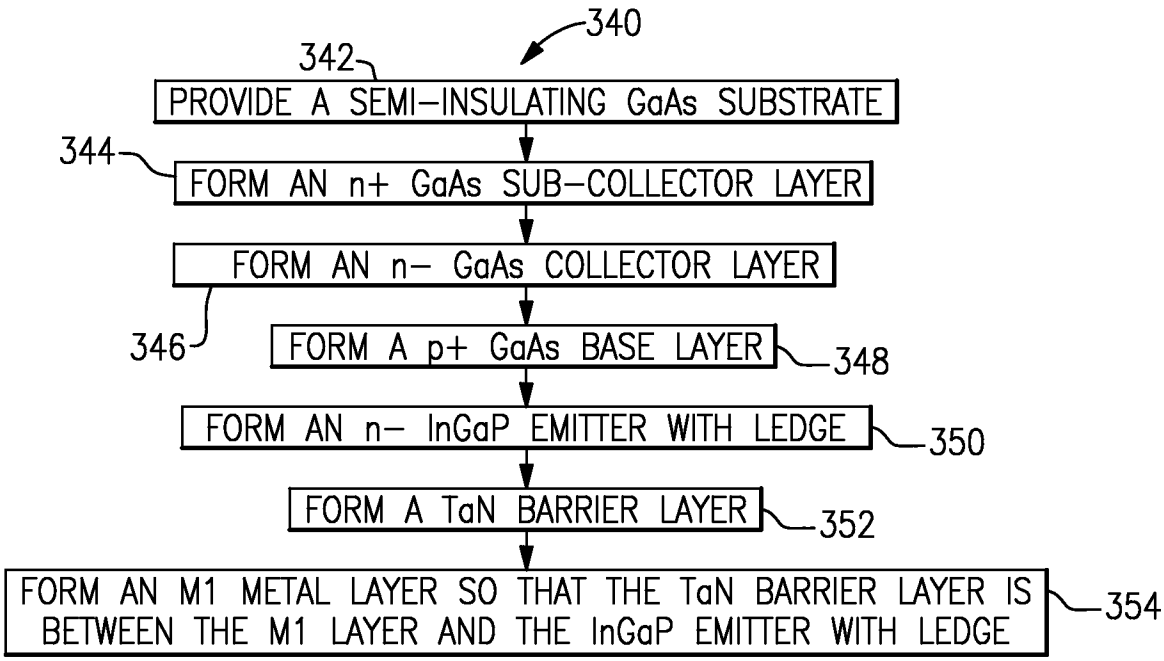


FIG.15

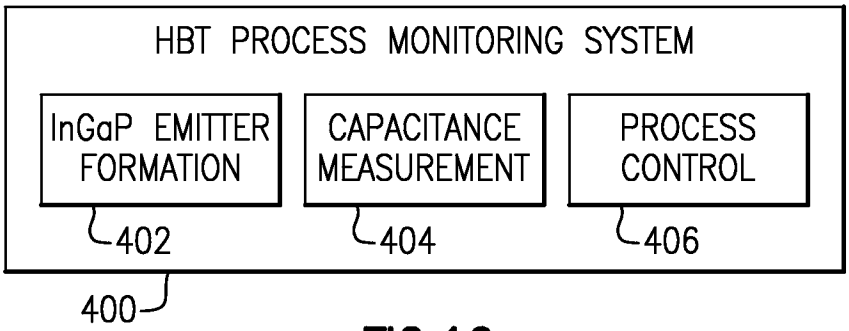

HBT PROCESS MONITORING SYSTEM
InGaP EMITTER FORMATION
CAPACITANCE MEASUREMENT
PROCESS CONTROL
402
404
406
400

FIG.16

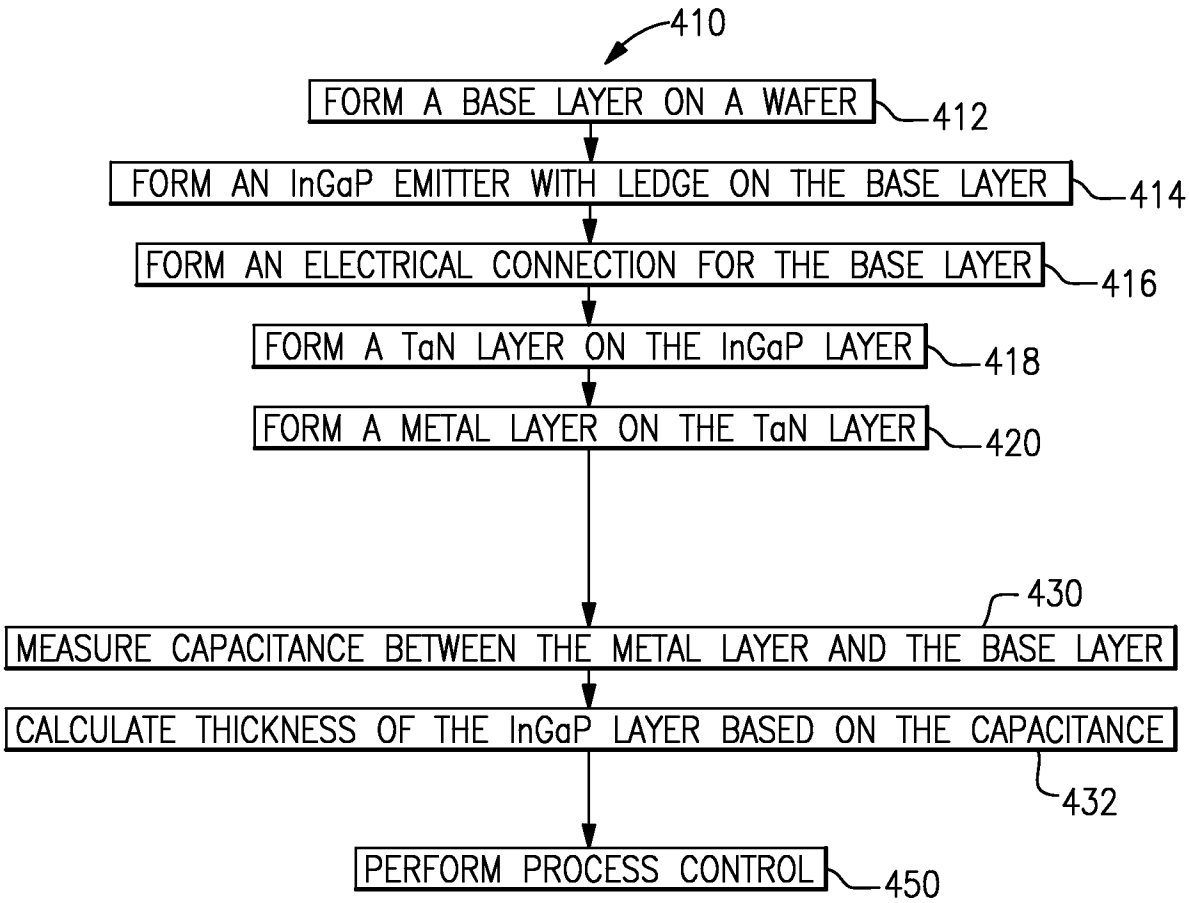

410
FORM A BASE LAYER ON A WAFER
412
FORM AN InGaP EMITTER WITH LEDGE ON THE BASE LAYER
414
FORM AN ELECTRICAL CONNECTION FOR THE BASE LAYER
416
FORM A TaN LAYER ON THE InGaP LAYER
418
FORM A METAL LAYER ON THE TaN LAYER
420
430
MEASURE CAPACITANCE BETWEEN THE METAL LAYER AND THE BASE LAYER
CALCULATE THICKNESS OF THE InGaP LAYER BASED ON THE CAPACITANCE
432
PERFORM PROCESS CONTROL
450

FIG.17

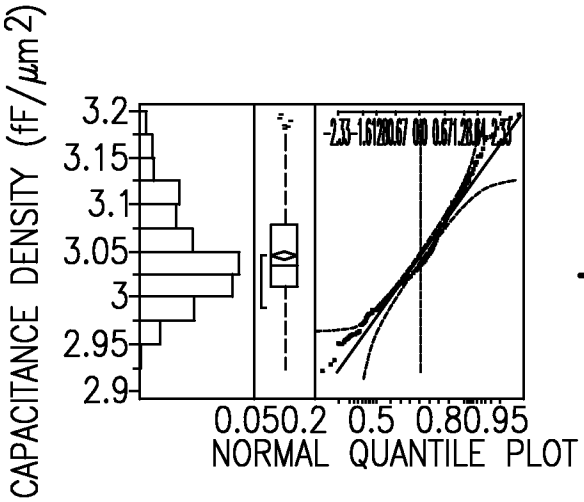


FIG.18

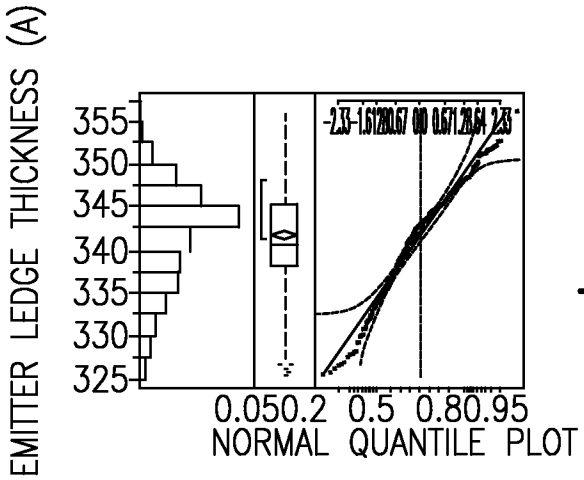


FIG.19

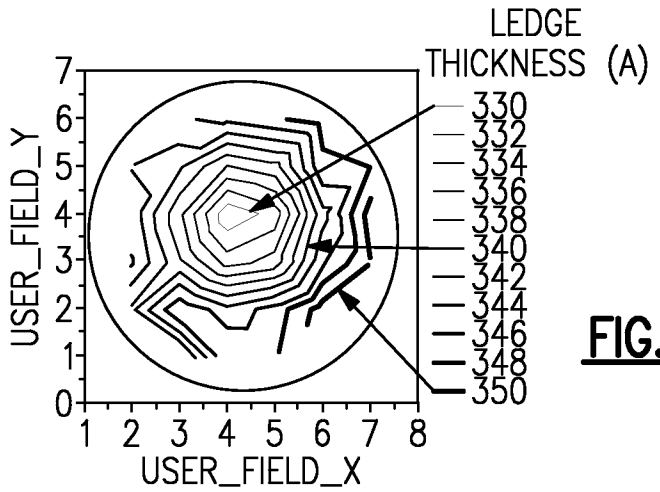


FIG.20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/065090

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/73(2006.01)i, H04B 1/00(2006.01)i, G01R 31/26(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/73; H01L 21/331; H01L 29/00; H01L; H01L 21/822; H01L 31/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: heterojunction bipolar transistor, gallium arsenide, tantalum nitride, barrier, emitter, base, collector

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0023783 A1 (ICHIRO HASE et al.) 01 February 2007 See abstract, paragraphs [0007]-[0011],[0020],[0021],[0071]-[0075],[0096],	1-33
A	[0097],[0124] and figures 1,2,15	34-40
Y	WO 2004-084272 A2 (ENECO, INC.) 30 September 2004	1-33
A	See abstract, page 11, lines 20-30 and figure 1	34-40
A	JP 2005-116773 A (JAPAN RADIO CO., LTD.) 28 April 2005 See abstract, paragraphs [0013]-[0016],[0021] and figure 1	1-40
A	US 2007-0045774 A1 (MICHAEL LEROY HUBER et al.) 01 March 2007 See abstract, paragraphs [0008],[0009],[0018]-[0023] and figure 11	1-40
A	EP 1662557 A1 (NIPPON TELEGRAPH AND TELEPHONE CORPORATION) 31 May 2006 See abstract and paragraphs [0005],[0016],[0025]	1-40

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 March 2013 (27.03.2013)	**01 April 2013 (01.04.2013)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

KIM, Tae Hoon

Telephone No. 82-42-481-8407

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/065090

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

I. Claims 1-20, 34-40 are directed to a metallization structure.
II. Claims 21-27 are directed to a method of fabricating a heterojunction bipolar transistor.
III. Claims 28-33 are directed to a system for monitoring a heterojunction bipolar transistor.

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/065090

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/065090

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