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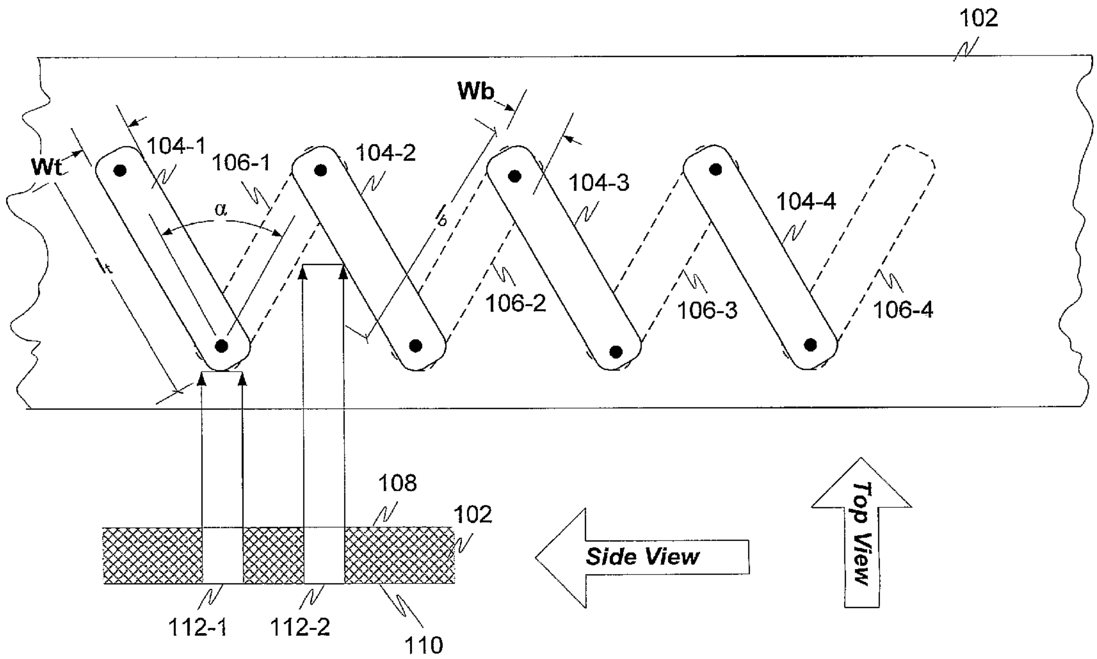
(54) Title: PRINTED MULTILAYER SOLENOID DELAY LINE



(57) Abstract: A printed solenoid inductor delay line system comprises discrete delay sections, where the inductor is implemented in the form of a printed, spiraling solenoid, with the solenoid axis in the plane of the multi-layer printed circuit board (PCB).

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TITLE OF THE INVENTION

PRINTED MULTILAYER SOLENOID DELAY LINE

CROSS REFERENCE TO RELATED APPLICATION

[0001] The present application claims the benefit under 35 USC 119(e) of U.S. Application Serial No. 60/740,637 filed November 30, 2005, the entire contents of which are herein incorporated by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to solenoid delay lines. More specifically, the invention relates to a printed multilayer solenoid delay line system.

BACKGROUND & SUMMARY OF THE INVENTION

[0003] Signal skew is a well-known characteristic in high speed communications and video signal transmission. Signal skew also occurs in multiple twisted-pair cables that are prevalent today in computer networking. Generally speaking, skew is the mismatch in arrival times of data on different signal lines where the data was originally transmitted at the same time. Skew is caused by different propagation rates through different pairs of cable. This, in turn, in the case of twisted-pair cables, is typically caused by different twist rates for the pairs of signal lines. Paired signal wires that have a tighter twist rate cause the signals to propagate over a greater distance. Cables containing twisted pair wires are intentionally designed so that different pairs have different twist rates in order to reduce the cross talk between signal wire pairs.

[0004] Details of specifying delay lines are described in "Specifying Delay Lines," by Lester Jacobson, Allen Avionics, Electronic Products Magazine, the contents of which are incorporated herein by reference.

[0005] United States Patent No. 6,377,629, titled "Twisted Pair Communications Line System," to Stewart *et al.*, issued April 23, 2002, the entire contents of which are incorporated herein by reference, illustrates a delay line formed by serpentine arrangements formed on two sides of a printed circuit board, *e.g.*, figure 3 and column 9, line 24 to column 10, line 50.

Brief Description Of The Drawings

[0006] **Fig. 1(a)** shows a printed solenoid for use in a delay line, according to embodiments of the present invention.

[0007] **Figs. 1(b), 2-7,** and **8(a)-8(c)** show alternate embodiments of the present invention.

Detailed Description Of The Invention

[0008] **Fig. 1(a)** illustrates the a solenoid delay inductor **100**, formed on two layers of a multilayer printed circuit board (PCB) **102**. The solenoid delay inductor **100** comprises a number of top portions **104-1**, **104-2**, . . ., **104-4**, (generally, top portions **104**) formed on a portion of a first layer **108** of the PCB **102** and a number of bottom portions **106-1, 106-2, . . ., 106-4**, (generally bottom portions **106**) formed on a portion of a different layer **110** of the PCB **102**. In the case of a two layer PCB, the different layer **110** will be the bottom layer of the PCB **102**.

[0009] The top portions are connected through electrical connection vias **112-1, 112-2, . . .**, (generally vias **112**) formed in the PCB **102**. Thus, as shown in **Fig. 1**, top portion **104-1** connects electrically to bottom portion **106-1** through the via **112-1**. In this manner, the top and bottom portions and their electrical connections form a solenoid delay, with the electrical connections effecting the solenoid windings.

[0010] The length l_t and width w_t of each top portion **104** may be substantially the same for each top portion, or they may differ. Similarly, the length l_b and width w_b of each bottom portion **106** may be substantially the same for each top portion, or they may differ.

[0011] Each top portion **104-*j*** forms an angle α_j with each bottom portion **106-*j*** to which it connects. The angles α_j may be the same (or substantially the same) for each top and corresponding bottom portion or they may differ.

[0012] The connected top and bottom portions form a delay solenoid with the solenoid axis in the plane of the PCB. Each top element or portion forms a portion of a delay line, as does each bottom portion or element. In the example shown, there are four top portions and four bottom portions. Those of skill in the art will immediately realize that the number and sizes of the portions depends on the amount of delay required in the line. Further, in the example shown, only two layers are shown. Those skilled in the art will realize that more than two layers can be used and are contemplated herein.

[0013] The drawings are not to scale, and the angles between corresponding elements may be adjusted in order to reduce space requirements. In addition, those skilled in the art will realize that the solenoids according to embodiments of the present invention need not be symmetric. There is no requirement, e.g., that each of the top elements **104-*j*** be the same size as the others, and similarly, there is no requirement for the lower elements **106-*k***.

[0014] **Fig. 1(b)** shows an alternate manner of forming the lower portions **104-x, 104-y**, so that the top portions **102** need not be formed at angles.

[0015] As shown in **Fig. 2**, discrete capacitors **114, 116** may be placed underneath the solenoid **100** in order to match the capacitance of some other component of a circuit (e.g., a switch, not shown). Embodiments of the present invention may use printed capacitors with a ground plane, or omit capacitors altogether, by using the inherent capacitance of switching elements.

[0016] In preferred implementations, etch width is kept fairly large to reduce losses. However, this limits the number of turns and inductance. Other sub-inductor segmentation can be implemented, rather than the long coupled solenoid design as shown, such as through non-coupled or anti-coupled designs shown in **Figs. 3** and **4**, respectively.

[0017] In the embodiments of the present invention shown in **Fig. 3**, the solenoid delay circuitry comprises three parts, denoted S1, S2 and S3.

[0018] Some embodiments of the present invention may use more-distributed capacitance, by utilizing at least one layer of the inductor closely spaced to a ground plane.

[0019] **Fig. 5** is a top view of a solenoid delay **150** according to embodiments of the present invention, with the inductor on inner layers, and the bottom layer ground plane being uniform. A row of vias connects the top and bottom ground planes. Cuts can be inserted, overlaying the inductor turn separations, to reduce any possible circulating currents.

[0020] **Fig. 6** depicts another layout of a solenoid delay according to embodiments of the present invention. As shown in the drawing, a solenoid delay **160** has a star shape (the solid lines are on a first layer of the PCB, and the dashed lines are on a second layer). The elements on the first layer connect to corresponding elements on the second layer through electrical vias (denoted as circles). The configuration shown in **Fig. 6** allows a delay line segment to complete a 180-degree turn. That is, a the segment **160** can connect to other solenoid delay segments (**166, 168**) at locations **162** and **164**.

[0021] For some embodiments of the present invention, at least a 32ns delay is needed to complete a turn. The radial or star embodiment of **Fig. 6** can make a smooth turn with 30-degree angle turns. Although this design can claim much of the end area of the PCB, as compared to implementing other types of physical delay or circuitry in this area, it is a safe way to avoid unwanted interference. This end space contains five turns, but those of skill in the art will realize the fewer or more turns could be used.

[0022] **Fig.** 7 shows an alternate configuration designed to complete a 180-degree turn, using an arrangement of two solenoids **170, 172** in series and connected centrally at the central joining ground pad **174**.

[0023] The section directly above the central joining pad **174** may be left empty of other circuitry, in order to reduce chances of interference with solenoid end-fields. Main separation between rows can be increased, to reduce capacitive coupling across sections. The two inner row sections can be staggered for lower capacitance.

[0024] In order to reduce the chance of possible coupling to the solenoid's field, an empty area should be left at each end, free of components or crossing etch; the dimensions implemented in preferred embodiments are 200 mils deep at one end, and 100 mils deep on the other end, each empty area having a width of about 100 mils. In a preferred embodiments of the present invention, the pitch between turns should be 40 mils, and spacing between left and right sections of the coil should be 65 mils. In some preferred embodiments, wider coil turns have a width of 270 mils, and the shorter turns have a width of 230 mils.

[0025] The following provides further detailed descriptions of the particular manufacturing and materials for construction of the present invention.

[0026] In some embodiments of the present invention, the PCB structure has a 59 mil rigid core center, with 1 oz. of copper mated to both sides. Thus, the center portion of the board could consist of approximately 56 mils of a common glass epoxy, such as FR4. Each side of the board has 7 mils of 7628 prepreg and a 1/2 oz of copper, which can optionally be plated up to 1oz. In some cases, 4.5 mil of 2116 prepeg may be used if more capacitance is required. However, the overall board thickness is approximately 75 mils.

[0027] The solenoid structure has a plated-through-hole (PTH) diameter of 15 mils. Additionally, the winding pitch equals about 40 mils. This is accomplished by having an outer layer of 31 mils, utilizing an 8 mil annular ring and 9 mil spacing between the pads. Further, the inner layer will be 35 mils., having a 10 mil annular ring and 5 mil spacing between the pads. Optionally, for pads staggered on a 40 mil grid, the pitch will be 56.6 mils. Consequently there will be 25.6 mils between pads on the top layer, which allows for a 9 mil run pass-through or area-fill copper, and 8 mil spaces. In order to get capacitance to ground, a 13 mil pass-through and 6 mil spaces may be utilized.

[0028] The inductors are wound on the inner layer of the solenoid, giving a 56 mil thickness of the solenoid. Additionally, the solenoid turns use 30 mil copper, allowing for 10 mil spaces (which are slightly decreased due to the angle of the turn). Further, the solenoid has one side with pads in a straight line and the other side has pads that are staggered, allowing for good top-layer ground pass-through on the staggered side.

[0029] The nominal solenoid width, consisting of the average of any staggered holes, is 250 mils. Thus, the solenoid cross-sectional area is 0.014 square inches (0.356 mm^2). Consequently, the resulting inductance is:

$$L = 4.46 \times N^2 / (0.4 \times N + 0.6) nH$$

[0030] where N is the number of turns. Consequently, for longer solenoids, the inductance is 11 nH/turn, whereas shorter solenoids have an inductance of 10 nH/turn. Thus, in one embodiment where end-inductances are added to a solenoid for impedance matching, an inductance of 10 nH/turn should be used.

[0031] The capacitance, impedance and delay details for one embodiment are as follows. A dielectric constant (E_r) of 4.7 is used for the 7628 prepreg that forms the capacitor dielectric. The capacitance of a straight, 30 mil wide run on the inner layer to an outer layer on the ground plane is then determined to be 7.44pF/in.. Thus, with the solenoid geometry as previously described, the 8 mil top layer spaces between pads and the ground plane, thus making the effective capacitor length per turn 0.0430 in. Therefore, the capacitance is about 3.2pF/turn. The impedance is calculated to be 59Ω (ohms) for long solenoids, and 56 Ω for short solenoids.

[0032] The time delay for the above value is 0.188 nS/turn. For shorter solenoids, this would be 0.179 nS/turn, which is approximately twice the delay of an equivalent length of stripline. Additionally, the delay rate is 4.7 nS/in. along the solenoid's length, and 4.5 nS/in. if short. Additionally, the individual half-turn delay sections are short enough to support high bandwidth signals.

[0033] Further, in this embodiment, the solenoid "track width" should be 0.325 in. Thus, the delay density is 14.4.nS/in^2. Additionally, the DC resistance results primarily from the 30 mil of copper. The 30 mil of copper equals 1oz of copper, and gives the entire solenoid approximately 17 mΩ/in, which correlates to 8.8 mΩ/turn and 46.8 mΩ/nS. The DC resistance reduces the signal strength, so the image colors may be affected. The pads have the main copper path width being 20 mils. The coil width is 106 mils. between centers, which allows enough space for two vias both inside and outside the "near" coil side. The coil length can be variable in order to get the proper inductance, however a square coil may be preferable in some cases.

[0034] In order to avoid a shorted turn, ground vias should not be used anywhere within a the solenoid area.

[0035] Those skilled in the art will realize that the number of turns and the length of the elements will depend on the delay needed.

[0036] It is preferable to have two turns (at signal entry and exit points) which do not have the outer ground layer covering. These turns may be used for matching where an unloaded inductance is desired.

APPLICATIONS

[0037] Solenoid delay lines according to embodiments of the present invention are applicable in a multitude of applications. However, they are particularly suited to Keyboard, Video, Mouse (KVM) applications in which video data are transmitted via twisted pairs. The invention may be incorporated into systems such as described in U.S. Patent Application No. 10/366,695, titled "Automatic Equalization of Video Signals," filed February 14, 2003, and United States Patent No. 6,377,629, titled "Twisted Pair Communications Line System," issued April 23, 2002, the entire contents of each of which are incorporated herein by reference.

[0038] While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiment, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

CLAIMS

What is claimed:

1. A solenoid delay line formed on at least two layers of a multilayer printed circuit board (PCB), comprising:

a first plurality of discrete delay elements formed on a first layer of said PCB; and

a second plurality of discrete delay elements formed on a second layer of said PCB, distinct from said first layer,

wherein each of said first discrete delay elements is electrically connected to at least one of said discrete second delay elements.

2. A solenoid delay line as in claim 1, wherein said first plurality of delay elements are disposed at an angle to said corresponding second plurality of delay elements.

3. A solenoid delay line as in claim 1, wherein said first plurality of delay elements are formed on a top portion of said PCB.

4. A solenoid delay line as in claim 1, wherein said second plurality of delay elements are formed on a bottom portion of said PCB.

5. A solenoid delay line as in claim 1, wherein corresponding ones of said first and second delay elements are connected to each other through vias formed in said PCB.

6. A solenoid delay line as in claim 1 wherein said plurality of first and second delay elements are printed on the PCB.

7. A solenoid delay line as in claim 6 wherein with the solenoid axis is formed in the plane of the PCB.

8. A solenoid delay line formed on at least two layers of a multilayer printed circuit board (PCB), comprising:

a first plurality of delay elements formed on a top portion of said PCB; and

a second plurality of delay elements formed on a bottom portion of said PCB, distinct from said top portion; and

a plurality of vias formed in said PCB;

wherein each of said first delay elements is electrically connected to at least one of said second delay elements, wherein corresponding ones of said first and second delay elements are connected to each other through said vias, and wherein said first plurality of delay elements are disposed at an angle to said corresponding second plurality of delay elements.

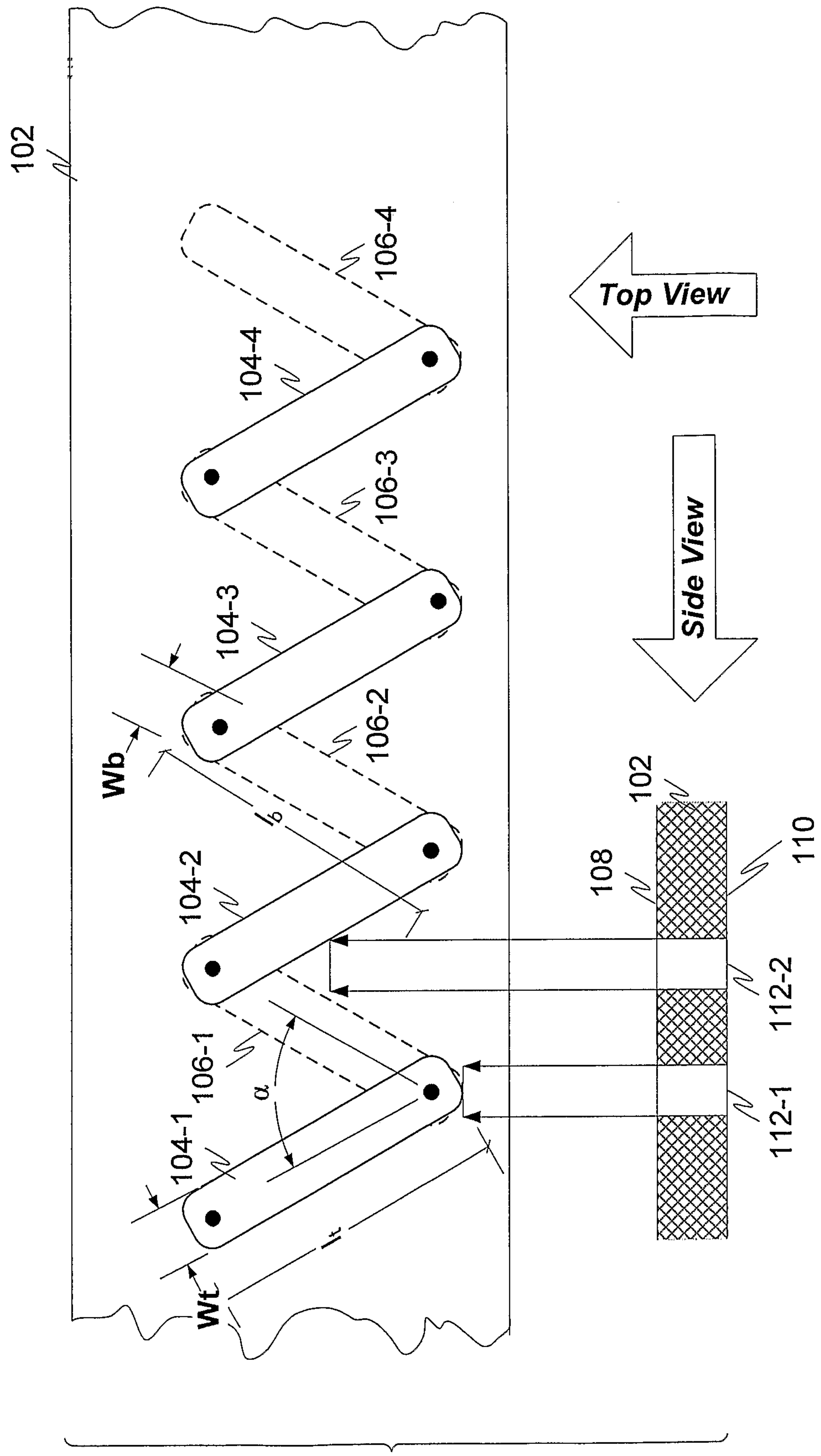
9. A method of forming a solenoid delay line on a multilayer printed circuit board (PCB), the method comprising:

forming a first plurality of delay elements on a portion of a first layer of said PCB; and

forming a second plurality of delay elements on a portion of a second layer said PCB, said second layer being distinct from said first layer; and

forming a plurality of vias in said PCB;

electrically connecting, through said vias, at least some of said first plurality of delay elements least some of said second plurality of delay elements.


102
106-4
Top View
104-4
106-3
Side View
104-3
Wb
106-2
104-2
lb
102
108
110
106-1
α
104-1
112-2
112-1
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Wt

Fig. 1(a)

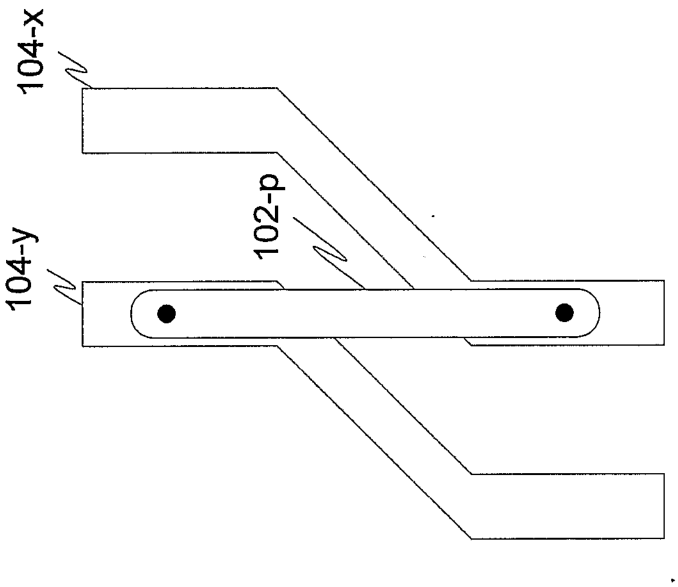

Fig. 1(b)

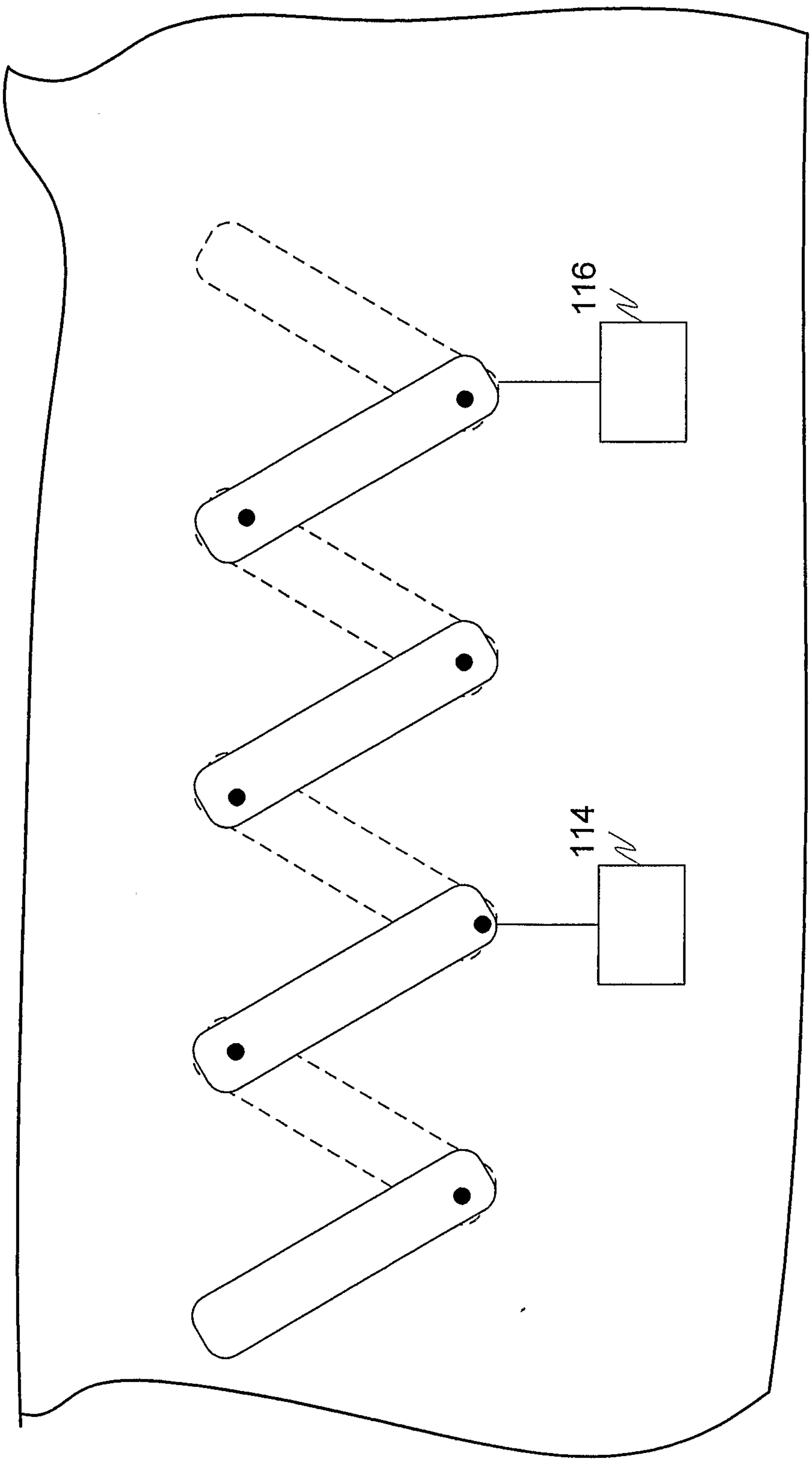

Fig. 2

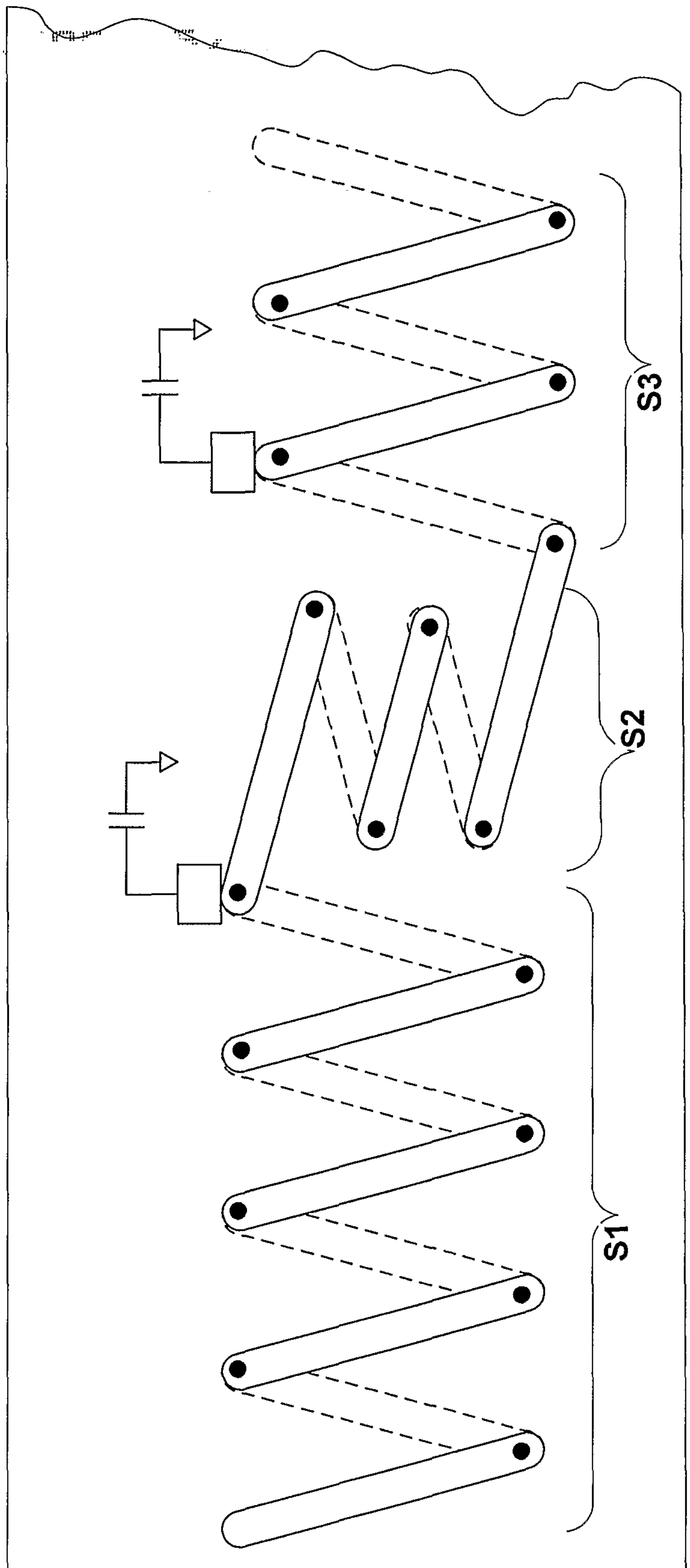

Fig. 3

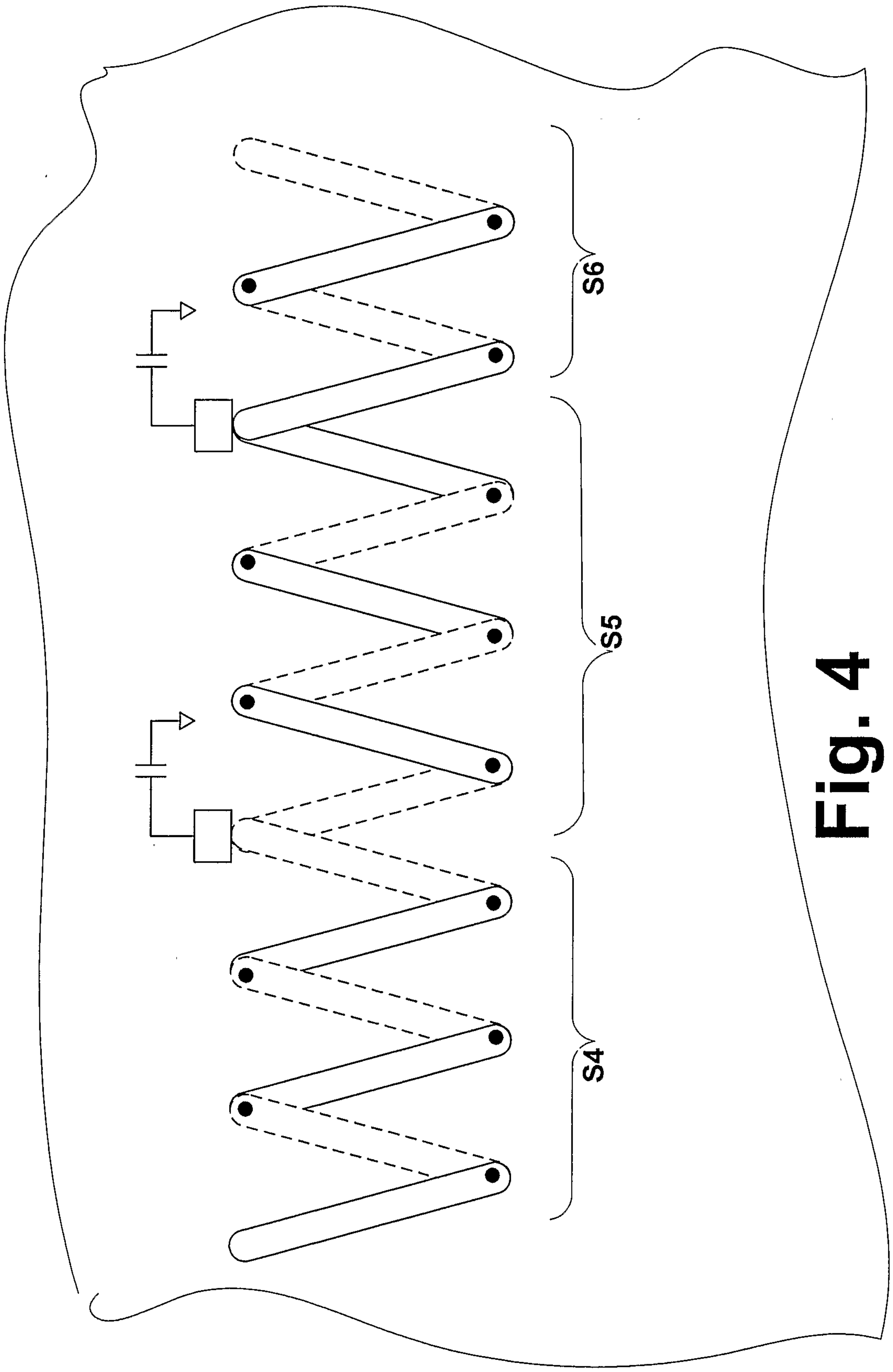

Fig. 4

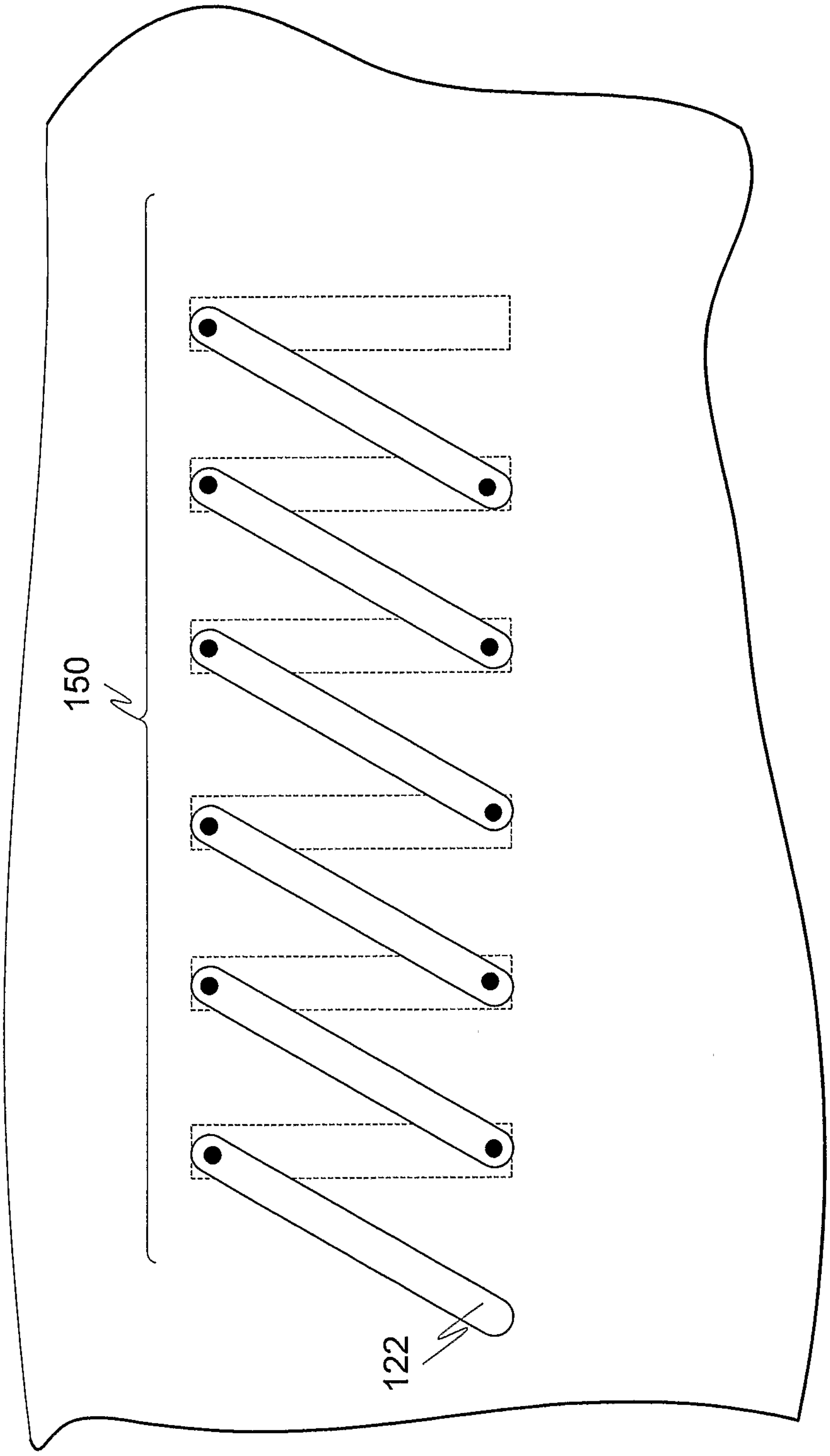

Fig. 5

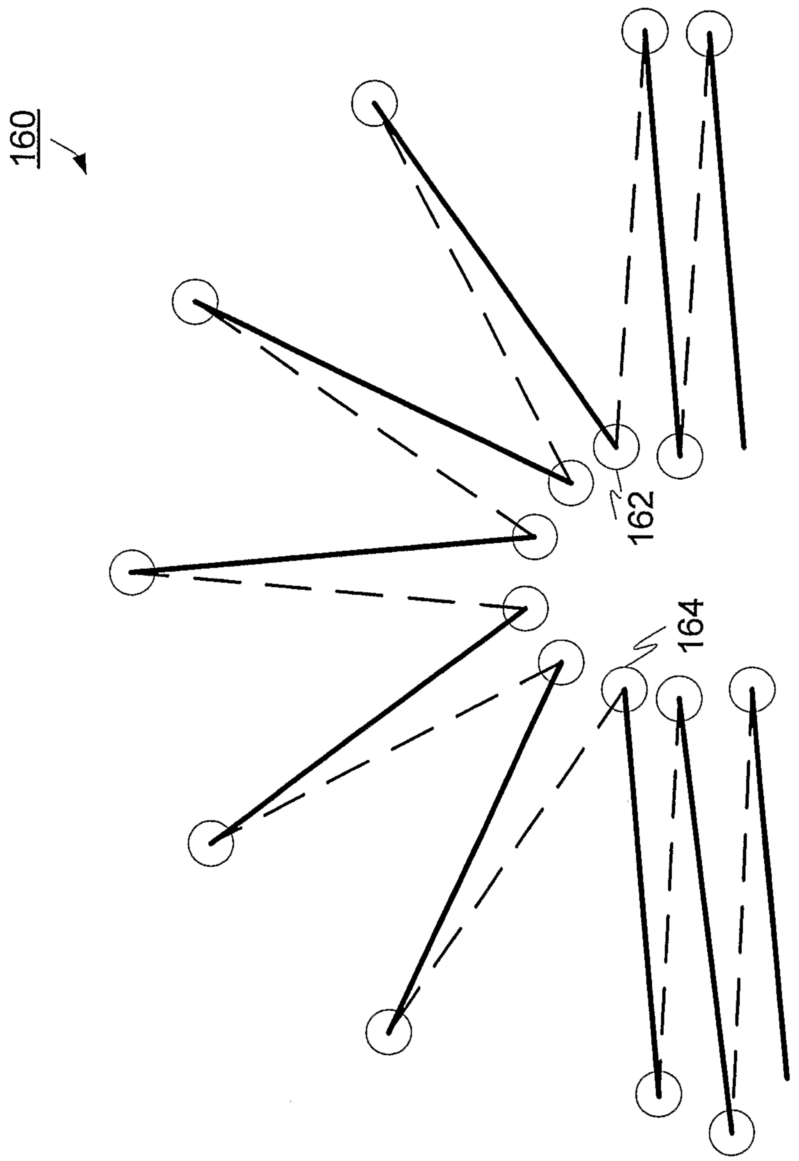

Fig. 6

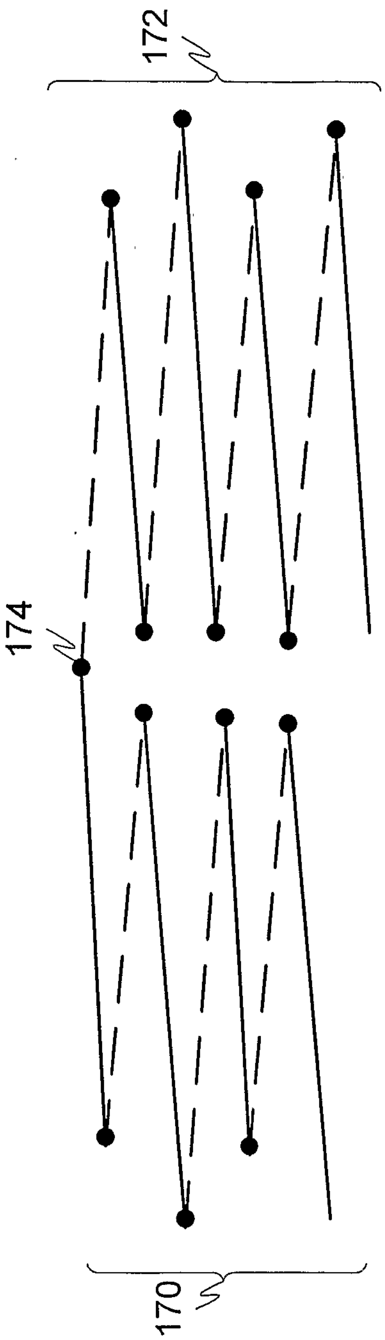

Fig. 7

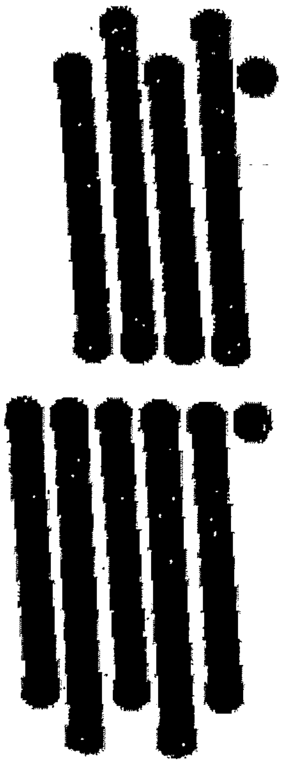

Fig. 8(a)

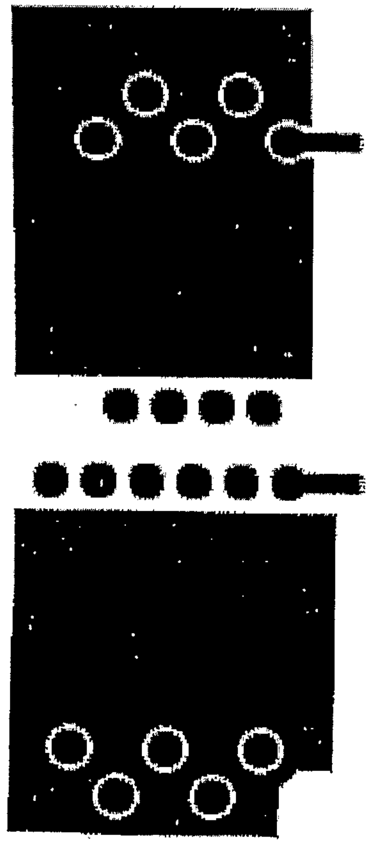

Fig. 8(b)

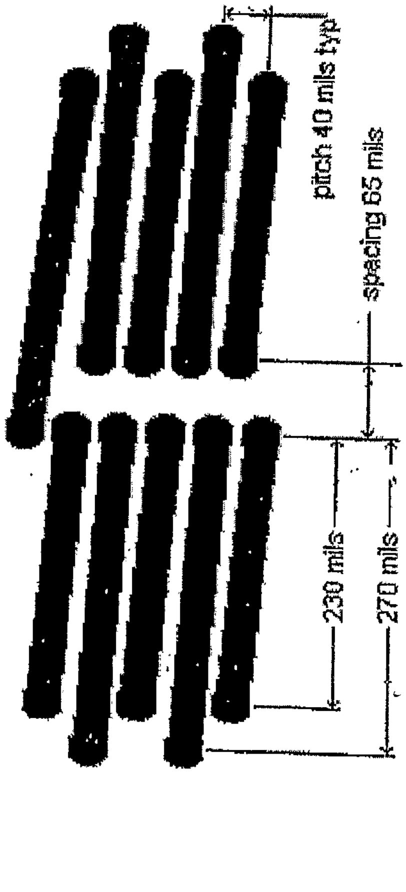

Fig. 8(c)