

Oct. 21, 1947.

P. J. HERBST

2,429,227

ELECTRONIC COMPUTING SYSTEM

Filed June 11, 1945

3 Sheets-Sheet 1

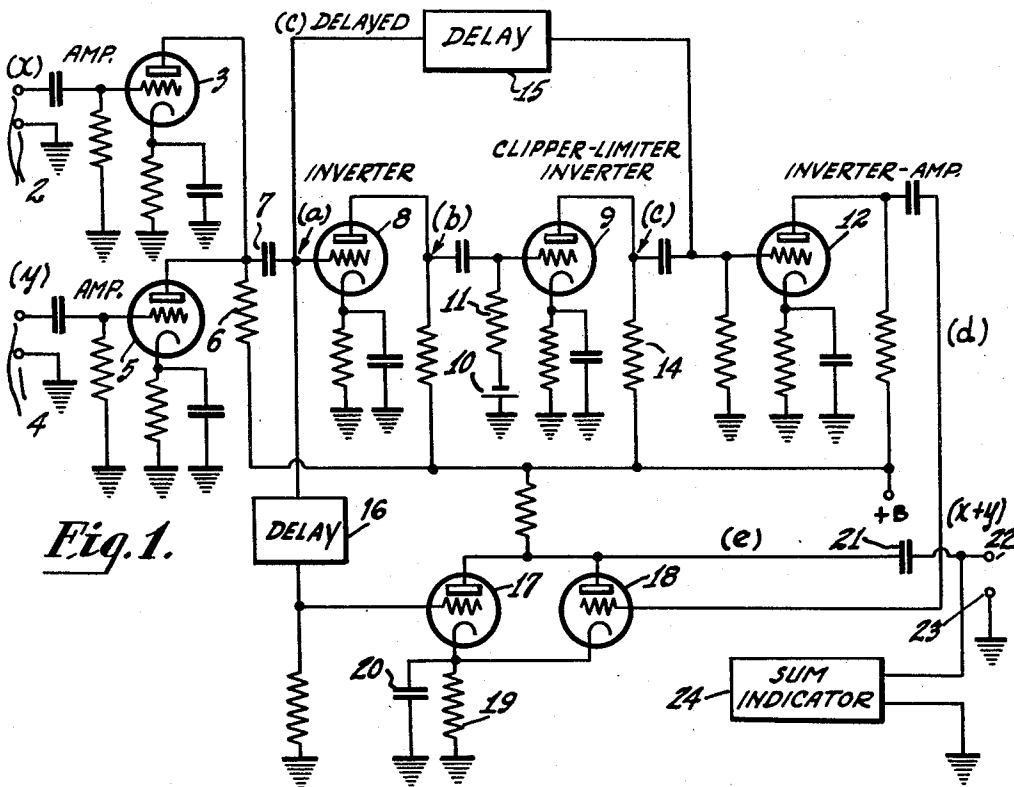
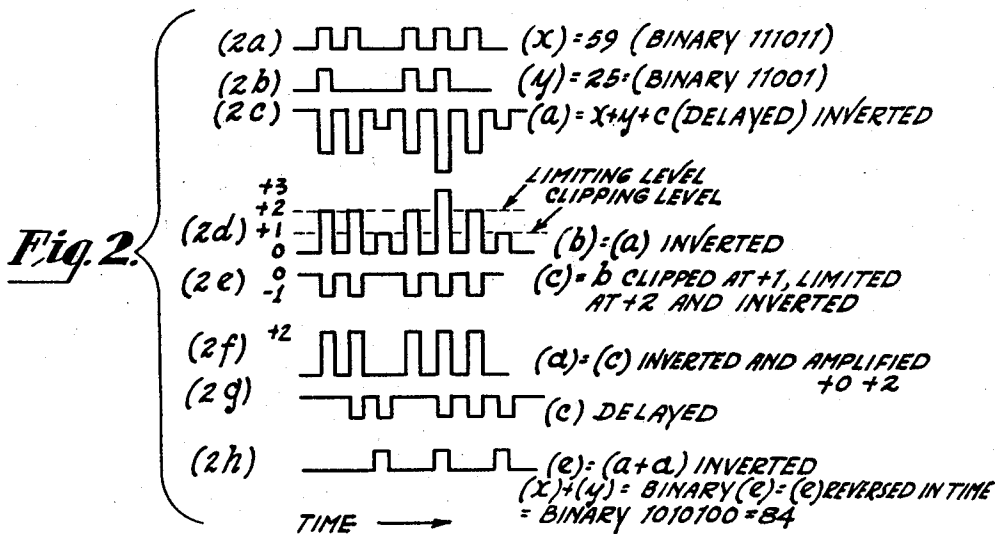


Fig. 1.



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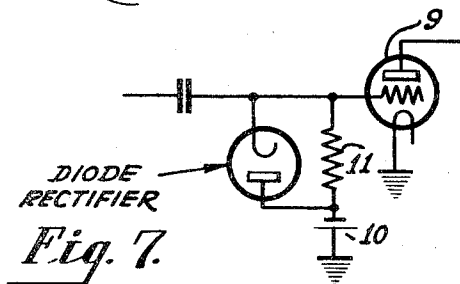
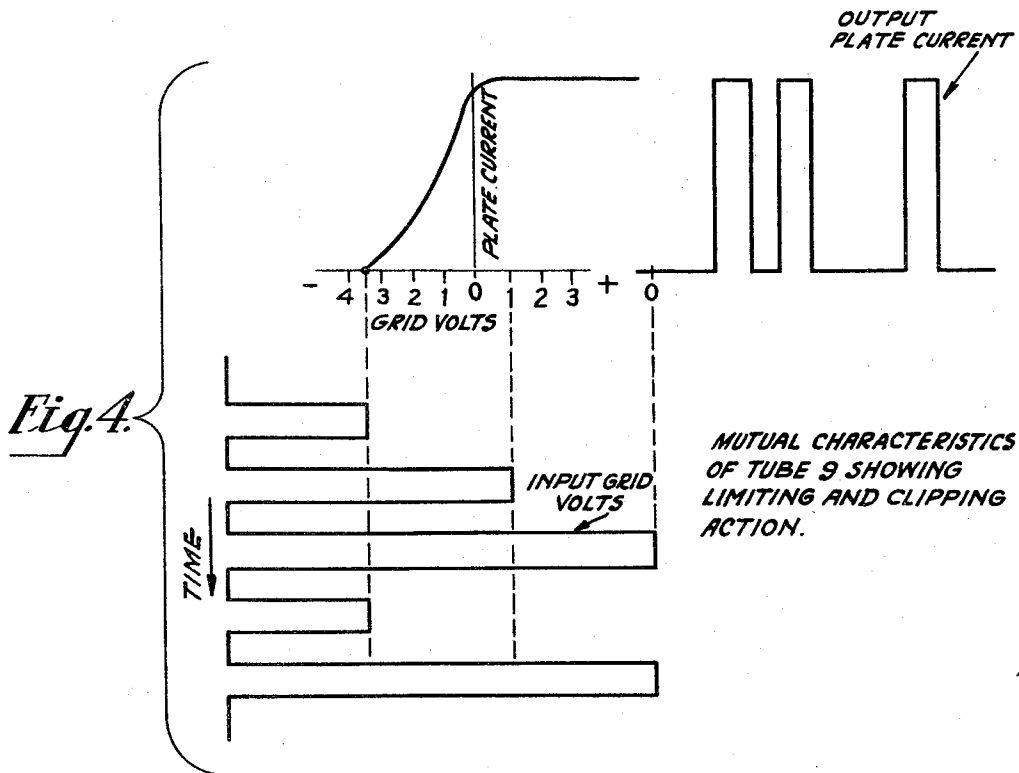
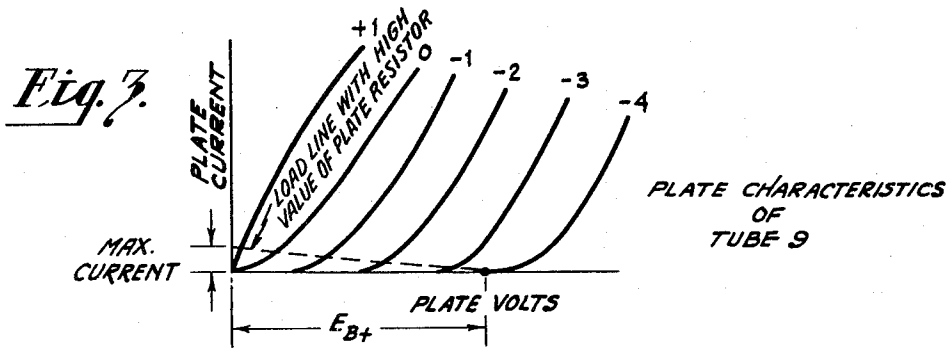
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3 Sheets-Sheet 2



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3 Sheets-Sheet 3

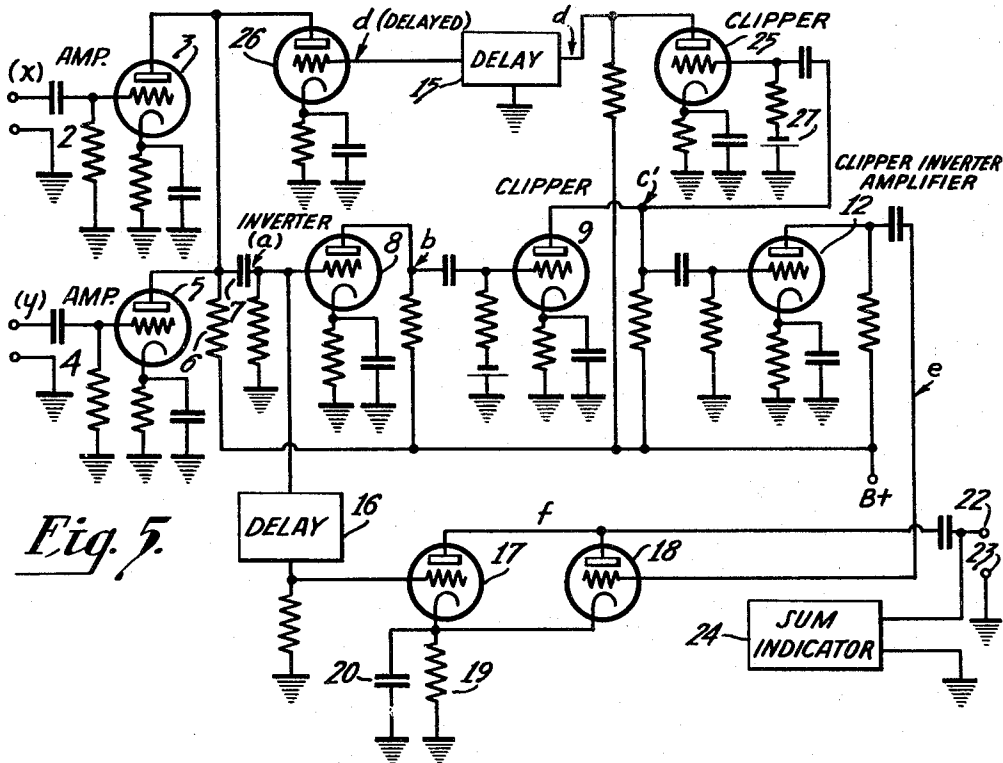


Fig. 5.

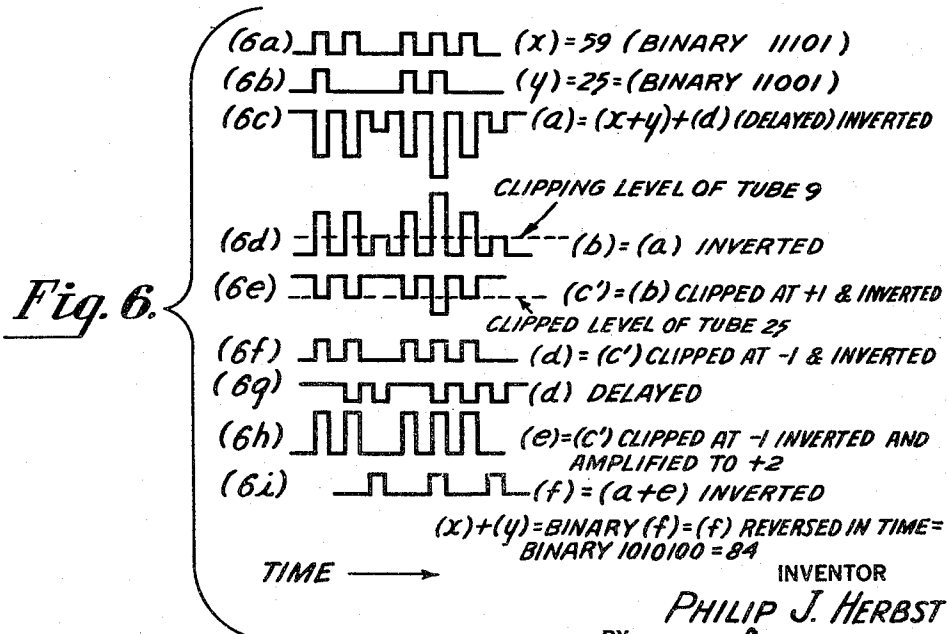


Fig. 6.

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ELECTRONIC COMPUTING SYSTEM

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Application June 11, 1945, Serial No. 598,701

7 Claims. (Cl. 235—61)

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This application is a continuation-in-part of my copending application Serial No. 485,308, filed May 1, 1943, for "Electronic computing system."

This invention relates generally to an electronic computing system, and more particularly to an electronic computer for deriving the sum of at least two quantities, each of which is represented by separate voltage pulse trains characteristic of the binary values of each of the quantities.

The binary system of computation is particularly suited to electronic computers, since a complete binary term of a binary number may be expressed in terms (a) of the conducting condition or (b) of the cut-off condition of the anode circuit of a conventional vacuum tube. A saving in the number of tubes required for a given number is also possible in a ratio of 3:1 over a numerical system utilizing a radix of 10. A description of the binary system of computation may be found in "Elementary Number Theory," by Uspenski and Heaslet.

The principle employed is the summation of the pulses representing the numbers to be added, the generation of a control pulse train having pulses whenever the pulse train representing the summation exceeds the amplitude of one pulse and in which the amplitudes of the pulses in the control train are all of the same magnitude, the delay of this control train by a time equal to the interval between pulses in the train. The addition of this delayed train to the input so as to represent the carryover from one digit to the next and the subtraction of the undelayed control train from the total sum to accomplish the cancellation of pulses of double magnitude.

Briefly, the system comprises an improved method and means for adding the magnitudes of the voltage pulses of each of the input pulse trains to derive therefrom a combined pulse train. To the combined pulse train is added a delayed pulse train representing the carry-over counts in the binary addition to derive a first control pulse train representing the binary sum but not in proper form for normal use. The first control pulse train may contain pulses of zero, unity, double or triple amplitude. The method employed consists in utilizing these amplitudes to produce a pulse train representing the binary sum in correct form as follows: Amplitudes of unity produce a count in the output pulse train but introduce no carry-over pulse in the circuit, double amplitudes produce a carry-over pulse but no count in the output train, pulses of triple amplitude produce both carry-over and count

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pulses. To accomplish this the first control pulse train is clipped at unit amplitude and limited at double amplitude to derive a second control pulse train which represents the carry-over pulses used which is delayed and added to the combined pulse train as previously described to produce the first control pulse train. The second control pulse train is amplified to derive a third control pulse train of double amplitude. The third control pulse train is combined in opposing polarity with the first control pulse train to derive a fourth pulse train which is characteristic of the sum of the binary numbers to be added. The fourth pulse train may be applied to additional computing apparatus or the sum may be indicated directly.

The two pulse trains to be added are impressed upon the input of a thermionic tube circuit having a common load, to derive therefrom the first combined pulse train. The combined pulse train is applied to the grid of a conventional amplifier stage to which the delayed pulse train representing the carry-over operation is also applied. The output of this stage constitutes the first control pulse train and is applied to a clipping-limiting stage, the output of which consists only of pulses of unit magnitude occurring whenever the magnitude of the pulses in the first control pulse train exceed unity and comprising the second control pulse train. This second control pulse train is applied to a conventional delay circuit which delays its pulses an amount equal to the time interval between pulses. The delayed pulses are combined with the combined pulse train to derive the first control pulse train as previously described. The second control pulse train is also applied to a conventional amplifier to derive a third control pulse train of double amplitude. The first and third control pulse trains are applied to the inputs of a summing stage. Since the pulses are applied in opposing polarity the pulses of the third control pulse train will tend to cancel those of the first control pulse train. However, for amplitudes of zero or unit magnitude in the first control pulse train, no pulses are present in the third, while for pulses of triple magnitude in the first, the presence of the double amplitude pulse in the third control train produces a partial cancellation which results in a pulse of unit amplitude in the output. When the pulse in the first control train is of double amplitude the cancellation is complete. The output of the summing stage is the fourth pulse train and represents the binary sum.

Among the objects of the invention is to pro-

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vide a new and improved method of and means for deriving and indicating the sum of a plurality of quantities represented by voltage pulse trains characteristic of the binary numbers corresponding to each quantity. Another object of the invention is to provide an improved method of and means for deriving the sum of at least two quantities each represented by separate voltage pulse trains characteristic of the binary values of each of said quantities, wherein the applied pulse trains are added to derive a combined pulse train, are limited, inverted, delayed and amplified to derive at least one control pulse train characteristic of carryover terms in the computation, and wherein the combined control pulse trains are combined to derive an output pulse train characteristic of the binary sum. A still further object of the invention is to provide an improved method of and means for deriving the sum of at least two quantities each represented by separate voltage pulse trains characteristic of the binary values of each of said quantities, wherein the applied pulse trains are added to derive a combined pulse train and the combined pulse train is limited to derive a control pulse train characteristic of pulses of double amplitude in the combined pulse train, and wherein the double amplitude pulses are combined with suitably delayed trains derived from the combined pulse train to derive an output pulse train characteristic of the binary sum of the quantities to be added.

The invention will be described in further detail by reference to the accompanying drawings, of which Figure 1 is a schematic circuit diagram of a preferred embodiment thereof; Figure 2 is a family of graphs characteristic of the pulse trains occurring throughout the different portions of the circuit of Fig. 1; Figures 3 and 4 are explanatory diagrams relating to the operation of the circuit of Figure 1; Figure 5 is a wiring diagram of a modified form of the invention; Figure 6 is a family of graphs characteristic of the pulse trains occurring throughout the different portions of the circuit of Figure 5; and Figure 7 illustrates a modified detail of the circuit. Similar reference numerals are applied to similar elements throughout the drawings.

Referring to the drawings, a voltage pulse train *x*, illustrated by Fig. 2a, corresponding to the number 59 expressed in terms of the binary number 111011, is applied to the input terminals 2 which are connected to the input of a first amplifier tube 3. A voltage pulse train *y*, corresponding to the quantity 25 in terms of the corresponding binary number 11001, is applied to a second group of input terminals 4 which are connected to the input of a second amplifier tube 5. The pulse trains *x*, *y* may be derived in any manner known in the art, for example, a series of delay circuits for discharging, in any predetermined sequence, the charge upon a previously charged capacitor. Such a pulse train generating circuit is disclosed in applicant's copending U. S. application Serial No. 488,801, filed May 26, 1943.

The anode circuits of the amplifier tubes 3 and 5, respectively, include a common load resistor 6 which is connected to a source of operating potential (not shown). The anodes of the first and second amplifier tubes 3, 5 are connected, through an isolating capacitor 7, to the control electrode of a third amplifier tube 8, which inverts the polarity of the combined pulse train derived from the amplifier tube 3, 5 and the out-

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put of the delay network 15. The output of the third amplifier tube 8 is applied to the control electrode of a limiter-inverter tube 9. The control electrode bias potential of tube 9 is selected so as to provide a threshold which will permit pulses of double and triple amplitude impressed on the input to produce an output in the plate circuit but discriminates against pulses of unit amplitude. The plate circuit of tube 9 is chosen so as to limit the amplitude of the pulses in the output to a fixed amplitude for all input pulses of double amplitude or greater. Figs. 3 and 4 show the mutual characteristic of tube 9 and illustrate the clipping and limiting action of this tube. The plate current limiting is realized by employing a very high resistance 14 in the plate circuit. Other methods, such as reducing the applied plate voltage could be used.

The control electrode bias potential may be derived from a battery 10 connected, through a grid resistor 11, to the control electrode of the limiter-clipper-inverter tube 9. As an added refinement to accommodate wide variation in pulse rate without shifting of the location of the pulse peaks on the mutual characteristic, a means of maintaining the base line of the input pulses may be employed. This means may take the form of a rectifier or similar "locking circuit." One form of this circuit is shown in Fig. 7. This refinement is not essential if the pulse width is small compared to the spacing or if the width of the mutual characteristic is small compared to the pulse amplitude, i. e., if the shift in the a-c axis of the pulse train is not sufficient to cause a change in the limiting clipping action of tube 9. The output of tube 9 represents the carryover count in the binary addition and will henceforth be designated as the second control pulse train *c*.

The second control pulse train *c* is applied to the control electrode of an inverter amplifier tube 12. This amplification of this tube is established by selection of the values of its associated circuit components so that the pulse train in its output signal has a constant magnitude of double amplitude. This may be further insured by providing limiter-clipper action similar to tube 9 but is not essential to the fundamental operation of the circuit. The output of tube 12 represents the cancellation terms in the binary addition and will henceforth be designated as the third control pulse train *d*.

The second control pulse train *c* also is applied, through a conventional delay circuit 15, to the control electrode of the first inverter tube 8. The delay provided in the delay circuit 15 corresponds to the period of the pulses of the applied voltage pulse trains. The resultant pulse train applied to the control electrode of the first inverter tube 8 will, therefore, represent the sum of the applied pulse trains and the delayed second control pulse train, and will hereinafter be designated as the first control pulse train *a*.

The first control pulse train *a* is applied to a delay circuit 16, which delays the pulse train an amount equivalent to the total delay in the circuits associated with the inverter and limiter tubes 8, 9 and 12. The output of the delay circuit 16 is applied to the control electrode of a triode 17. The third control pulse train *d* is applied to the control electrode of a triode 18. The triodes 17, 18, respectively, include common cathode and anode circuits and are self-biased by means of a cathode resistor 19 and cathode bypass capacitor 20 connected between the cathodes and ground.

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The anodes of the triodes 17, 18 are connected, through an output capacitor 21, to an output terminal 22. The other output terminal 23 may be connected to ground or any suitable indicator 24, for indicating the binary number corresponding to the sum of the applied quantities x , y , may be connected to the terminals 22, 23.

The indicator 24, for example, may comprise a conventional oscilloscope tube, the beam of which is normally blanked off and normally deflected just off the fluorescent screen. The pulse train to be indicated is applied to the tube control grid to unblock the cathode ray at each occurrence of a positive pulse characteristic of a binary one term. The initial pulse is applied to key a conventional sweep voltage generator to provide a relatively slower sweep voltage which may be applied to the tube deflection elements to sweep the ray across the fluorescent screen. The sweep voltage preferably should be of saw-tooth wave form, and the fluorescent screen should be of the type providing sustained fluorescence. The indications will be in the form of luminous dashes separated by relatively wide dark spaces corresponding to binary 0 terms.

Referring to Fig. 2, the first graph 2a illustrates the pulse train corresponding to the first applied quantity x . Reading from right to left, the pulses of unit amplitude, and the absence of pulses, correspond to the binary number 111011, which equals 59. 2b similarly illustrates the pulse train corresponding to the second applied quantity y . Similarly, reading from right to left, this pulse train corresponds to the binary number 11001, which equals 25. 2c illustrates the first control pulse train a , which is characteristic of the combined pulse trains $x+y+(c \text{ delayed})$. The delayed pulse train, shown at 2g, is characteristic of carryover pulses occurring whenever two or more unit pulses occur coincidentally.

2d shows the pulse train b derived from the output of the first inverter tube 8, which is equivalent to the first control pulse train a inverted in polarity. 2e represents the second control pulse train c , which is equivalent to the pulse train b clipped at an amplitude of $+1$ and limited at an amplitude of $+2$ and inverted in polarity. 2f illustrates the third control pulse train d derived from the output of the inverter tube 12, which is equivalent to double the amplitude of the second control pulse train c clipped at a magnitude of binary 1 and inverted in polarity. Pulses occur in the pulse train d only when two or more pulses coincide in the first control pulse train a . Since the a pulse train has been triple inverted, the d pulse train will be of opposite polarity thereto. When combined in the tubes 17, 18, the d pulse train will subtract double amplitude pulses from all double or triple amplitude pulses occurring in the a pulse train.

2g illustrates the delayed second control pulse train c . 2h represents the output pulse train e characteristic of the binary sum to be derived, and is equivalent to the combined, relatively delayed first and third control pulse trains $a+d$ inverted in polarity. Reading still from right to left, the graph 2h indicates a pulse train corresponding to the binary number 1010100, which equals the sum 84.

The modification of Fig. 5 differs from that of Fig. 1 in that a separate triode 25 is provided for clipping the second control pulse train c at a minus unity amplitude. In this case, the clipping and limiting of the first control pulse b to produce the second control pulse d is per-

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formed by the tubes 9 and 25 instead of the tube 9 as in the case of Fig. 1. Due to the inverting action of the tube 25, a tube 26 is provided to invert the d (delayed) pulse train before it is combined with the x and y pulse trains to form the first control pulse train b .

The graphs of Fig. 6 are for the most self-explanatory, especially in view of what has been said in connection with Fig. 2. Due to the fact that the clipping and limiting of the pulse train b is performed by separate tubes, there is in the case of Figs. 5 and 6 a pulse train c' which is clipped at one of its amplitude levels and a pulse train d which is like the pulse c of Figs. 1 and 2 except that it has to be inverted before it is combined with the x and y pulse trains.

I claim as my invention:

1. The combination of pulse train combining means, means for applying to said combining means number representative pulses of unit amplitude to derive a combined pulse train, means for deriving a unit amplitude control pulse train in which pulses occur only during such time intervals as two or more pulses are combined in said pulse combining means, means for delaying said control pulse train by a time interval equal to the period of the pulses of said trains, means for applying said delayed control pulse train to said combining means to produce a resultant pulse train of variable amplitude, and means for reducing by two units of amplitude pulses of said resultant pulse train which are of two or more units amplitude.

2. The combination of pulse train combining means, means for applying to said combining means number representative pulses of unit amplitude to derive a combined pulse train, means for deriving a unit amplitude control pulse train in which pulses occur only during such time intervals as two or more pulses are combined in said pulse combining means, means for delaying said control pulse train by a time interval equal to the period of the pulses of said trains, means for applying said delayed control pulse train to said combining means to produce a resultant pulse train of variable amplitude, a pair of triodes having common anode and cathode connections, means for applying said resultant pulse train to the control grid of one of said triodes, means for amplifying said control pulse train to double unit amplitude, and means for applying said amplified pulse train to the control grid of the other of said triodes.

3. The combination of pulse train combining means, means for applying to said combining means number representative pulses of unit amplitude to derive a combined pulse train, means for deriving a unit amplitude control pulse train in which pulses occur only during such time intervals as two or more pulses are combined in said pulse combining means, means for delaying said control pulse train by a time interval equal to the period of the pulses of said trains, means for applying said delayed control pulse train to said combining means to produce a resultant pulse train of variable amplitude, a pair of triodes having common anode and cathode connections, means for applying said resultant pulse train to the control grid of one of said triodes, means for amplifying said control pulse train to double unit amplitude, means for applying said amplified pulse train to the control grid of the other of said triodes, and an output terminal connected to the anodes of said triodes.

4. The combination of pulse train combining

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means, means for applying to said combining means number representative pulses of unit amplitude to derive a combined pulse train, means for clipping said combined pulses at unit amplitude and for limiting said combined pulses at double unit amplitude to derive a unit amplitude control pulse train in which pulses occur only during such time intervals as two or more pulses are combined in said pulse combining means, means for delaying said control pulse train by a time interval equal to the period of the pulses of said trains, means for applying said delayed control pulse train to said combining means to produce a resultant pulse train of variable amplitude, and means for reducing by two units of amplitude pulses of said resultant pulse train which are of two or more units amplitude.

5. An electronic computer for deriving the sum of two quantities each represented by separate voltage pulse trains characteristic of the binary values of each of said quantities including means for adding the magnitudes of the pulses in said pulse trains to derive a combined pulse train, means for deriving from said combined pulse train one control pulse train characteristic of carryover terms in the computation and another control pulse train of double unit amplitude, means for combining said combined pulse train and said carryover control pulse train to derive a resultant pulse train, and means for combining said resultant and double amplitude pulse trains to derive a pulse train characteristic of the binary value of the sum of said quantities.

6. An electronic computing circuit for deriving the sum of two quantities each represented by separate voltage pulse trains characteristic of the binary values of each of said quantities including means for adding the magnitudes of the pulses in said pulse trains to derive a combined pulse train, means for clipping and limiting said

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combined pulse train to derive a control pulse train of unit amplitude, means for amplifying said unit amplitude control pulse train for deriving a double unit amplitude control pulse train, means for delaying a part of said unit amplitude control pulse train an interval corresponding to the period of said pulses, means for combining said combined pulse train and said delayed pulse train to derive a resultant pulse train, means for delaying said resultant pulse train an amount to make it opposed in phase to said double amplitude control pulse train, and means for combining said resultant and double amplitude pulse trains to derive a pulse train characteristic of the binary value of the sum of said quantities.

7. An electronic computing circuit for deriving the sum of two quantities each represented by separate voltage pulse trains characteristic of the binary values of each of said quantities including a pair of thermionic tubes energized through a common load resistor for adding the magnitudes of the pulses in said pulse trains to derive a combined pulse train, means for clipping and limiting said combined pulse train to derive a unit amplitude control pulse train, means for amplifying said unit amplitude control pulse train for deriving a double amplitude control pulse train, means for delaying a part of said first unit amplitude control pulse train an interval corresponding to the period of said pulses, means for combining said combined pulse train and said delayed pulse train to derive a resultant pulse train, means for delaying said resultant pulse train an amount required to make it opposed in phase to said double amplitude pulse train, and means for combining said resultant and double amplitude control pulse trains to derive a pulse train characteristic of the binary value of the sum of said quantities.

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