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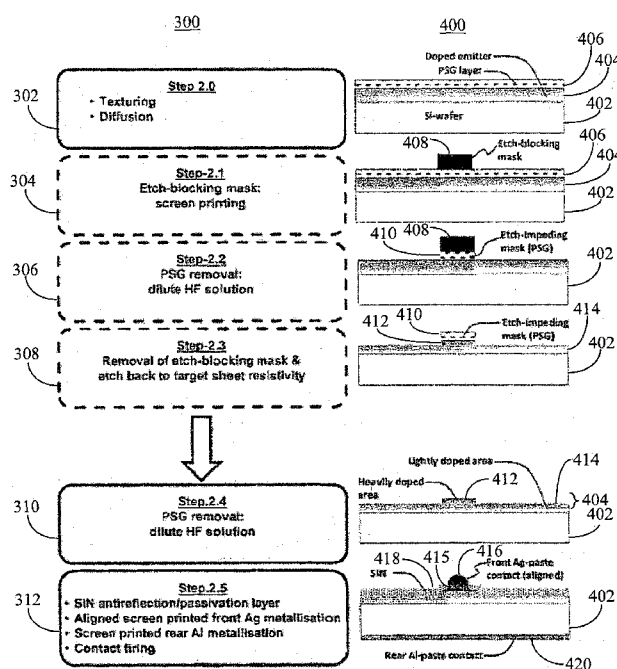
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(54) Title: MASKED ETCH-BACK METHOD AND PROCESS FOR FABRICATION OF SELECTIVE EMITTER SILICON WAFER SOLAR CELLS



(57) Abstract: A method for solar cell fabrication is provided. The method includes patterning etch-impeding material formed on an emitter surface of the silicon wafer solar cell to form an etch-impeding mask. The method also includes etching-back the emitter surface of the silicon wafer solar cell with the etch-impeding mask thereon using a solution based on alkaline and oxidising solutions which etches through the etch-impeding PSG mask at a slower rate than it etches through unmasked areas of the emitter surface to form a selective emitter on the silicon wafer solar cell. The etch-impeding material may include a silicate glass material such as phosphosilicate glass (PSG) and borosilicate glass (BSG) and the solution based on alkaline and oxidising solutions may include a solution of potassium hydroxide (KOH) and sodium hypochlorite (NaOCl) solutions. The patterning of the PSG may use an etch-blocking mask which is removed to reveal the patterned PSG before the etching-back step.



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MASKED ETCH-BACK METHOD AND PROCESS FOR FABRICATION OF SELECTIVE EMITTER SILICON WAFER SOLAR CELLS

PRIORITY CLAIM

[0001] The present application claims priority to US Patent Application No. 61/672,836, filed 18 July, 2012.

FIELD OF THE INVENTION

[0002] The present invention generally relates to solar cell manufacturing, and more particularly relates to methods and systems for masked etch-back for fabrication of selective emitter silicon wafer solar cells.

BACKGROUND OF THE DISCLOSURE

[0003] Silicon wafer solar cells are one of the dominant technologies for industrial manufacturing of photovoltaic solar cells. Current silicon wafer solar cell manufacturing techniques utilize silicon wafers and various fabrication techniques including etching of the silicon wafer solar cells. For example, chemical etching can be used during several process steps in the fabrication process of silicon wafer solar cells, such as an emitter etch-back process step.

[0004] Emitter etch-back is a process that partially removes the emitter layer on the silicon wafer. This is typically done to optimize dopant surface concentration such as

removing heavily doped surface layers, known as “surface dead layers”, that occur in inline or tube diffused phosphorous doped emitters, or dopant depleted or rich regions that occur in boron diffusion. Etch-back also allows the formation of high sheet resistance emitters from a low sheet resistance (R_{sheet}) precursor emitter in, for example, the formation of either homogenous or selective emitters. In the case of selective emitters, the etch-back is typically masked to produce selective etching to result in patterning of the sheet resistance of the emitter.

[0005] An emitter etch-back process enables partial removal of the emitter layer of a silicon wafer solar cell. This is often done to optimise surface concentration by removing surface dead layers e.g. heavily doped surface layers in tube/inline diffusion and dopant depleted regions in boron diffusion. In the case of selective emitter (SE) technology, the etch-back is applied selectively to produce high R_{sheet} values in the non-contacted areas, whilst maintaining a lower R_{sheet} value in the contacted area. The current state-of-the-art for the masked etch-back approach uses an etch-blocking mask to produce the selective patterning. The etch-blocking mask can be printed by numerous means including screen printing or inkjet printing. During the etch-back (EB), the areas under etch-blocking mask are not etched such that the diffused Si surface maintains a low R_{sheet} whereas the unmasked Si surface is etched back to a higher R_{sheet} . After etch-back the etch mask is stripped off in a mask stripping step to complete the SE structure. The low R_{sheet} under the front contact enables a low contact resistance over this area whilst the selectively etched area of higher R_{sheet} value enables better surface passivation, leading to an improved short wavelength response of the Si solar cell. All these factors attribute to a higher efficiency for the selective emitter solar cell compared to its homogeneous emitter counterpart

[0006] Emitter etch-back solutions are typically acidic and based on hydrofluoric acid-(HF), such as hydrofluoric:nitric acid (HF-HNO₃) solutions. However, these solutions represent a significant safety hazard and require complex waste disposal. In addition, these solutions also remove dielectrics such as SiN_x and SiO_x, making them incompatible for masked etching using dielectric masks.

[0007] Thus, what is needed is a solar cell fabrication process that overcomes these drawbacks of conventional emitter etch-back process steps, such as providing an etch-back solution that is compatible with dielectrics and does not have the safety hazards present in HF-based etching process steps. Furthermore, other desirable features and characteristics will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and this background of the disclosure.

SUMMARY

[0008] According to the Detailed Description, a method for silicon wafer solar cell fabrication is disclosed. The method includes patterning etch-impeding material formed on an emitter surface of the silicon wafer solar cell to form an etch-impeding mask and etching-back the emitter surface of the silicon wafer solar cell with the etch-impeding mask thereon using a solution based on alkaline and oxidising solutions which etches through the etch-impeding mask at a slower rate than it etches through unmasked areas of the emitter surface to form a selective emitter on the silicon wafer solar cell. The etch-impeding material may include a silicate glass material such as phosphosilicate glass (PSG) and borosilicate glass (BSG) and the solution based on

alkaline and oxidising solutions may include a solution of potassium hydroxide (KOH) and sodium hypochlorite (NaOCl) solutions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views and which together with the detailed description below are incorporated in and form part of the specification, serve to illustrate various embodiments and to explain various principles and advantages in accordance with a present invention.

[0010] FIG. 1, comprising FIGs. 1A and 1B, illustrates conventional diffusion techniques for silicon wafer solar cell fabrication, wherein FIG. 1A illustrates tube diffusion and FIG. 1B illustrates in-line diffusion.

[0011] FIG. 2 illustrates a conventional silicon wafer solar cell fabrication process flow.

[0012] FIG. 3 illustrates a side-by-side comparison of the conventional process flow of FIG. 2 as compared to a process flow in accordance with a present embodiment.

[0013] FIG. 4 illustrates side-by-side the process flow of FIG. 3 in accordance with the present embodiment on the left side and the device formation at each step of the process flow in accordance with the present embodiment.

[0014] FIG. 5 illustrates a graph depicting a change in average sheet resistance after etch-back for diffused monocrystalline wafers without and with the PSG etch-impeding layer in accordance with the present embodiment.

[0015] And FIG. 6 illustrates a graph depicting a change in average sheet resistance after etch-back for diffused multicrystalline wafers without and with the PSG etch-impeding layer in accordance with the present embodiment.

[0016] Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been depicted to scale. For example, the dimensions of some of the elements in the block diagrams may be exaggerated in respect to other elements to help to improve understanding of the present embodiments.

DETAILED DESCRIPTION

[0017] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any theory presented in the preceding background of the invention or the following detailed description. Chemical etching is used on several occasions during the fabrication process of silicon wafer solar cells. A present embodiment as disclosed in more detail herein enables a novel method for the fabrication of selective emitter solar cells using a masked emitter etch-back approach.

[0018] Selective emitter technology using a masked emitter etch-back is one of the key technologies in high-efficiency crystalline silicon (Si) wafer solar cells. The typical masked emitter etch-back approach uses a printed, etch-blocking mask to stop etching on selected areas of the emitter to realise the selective emitter structure. In accordance with the present embodiment, a masking method is disclosed which uses an etch-impeding mask formed of an etch-impeding material that substantially slows the etching rate of the etch-back solution on the masked region, but does not stop

etching. The present embodiment consists of using patterning of the etch-impeding material such as a silicate glass material like phosphosilicate glass (PSG) or borosilicate glass (BSG) on the emitter surface to form the etch-impeding mask. Patterning of the etch-impeding material can be achieved using several methods, including using an etch-blocking mask as the initial process step. The present embodiment uses an etch-back solution of potassium hydroxide (KOH) and sodium hypochlorite (NaOCl) solutions, which etches through the etch-impeding mask at a slower rate than the un-masked areas to realise the selective emitter. The preferred KOH-NaOCl etch-back solution also provides a controlled, slow, uniform and near-conformal silicon etching that preserves the surface texture of the wafers even after long etch-back times. Other etch solutions based on alkaline and oxidising solutions could also be used. The present embodiment has several positive impacts on both mono- and multicrystalline silicon wafer solar cell technologies as will be discussed herein, including reducing the number of process steps and potentially enhancing device performance. While the present embodiment is described in terms of using PSG for the etch-impeding material, those skilled in the art will realize that any other etch-impeding material could alternatively be used

[0019] The fabrication sequence for selective emitter solar cells using the masked etch-back approach starts with textured silicon wafers that are tube or inline diffused with a heavily doped emitter. Referring to FIGs. 1A and 1B, conventional fabrication techniques for emitters on silicon wafer solar cells typically comprise either boron or phosphorous diffusion. Batch-based tube diffusion depicted in an illustration 100 (FIG. 1A) using a high-purity phosphorus oxychloride (POCl_3) liquid dopant source is the de-facto standard for emitter formation in the photovoltaic industry. Inline-diffusion depicted in an illustration 150 (FIG. 1B) is an alternate process for emitter

formation, which uses spray-on solutions of orthophosphoric acid (H_3PO_4) as the dopant source. The illustrations 100, 150 are industry standard process illustrations from PV-Tech.org. Inline diffusion benefits from shorter diffusion times, reduced automation requirements, simpler wafer loading and low cost dopant solutions. However, the short diffusion times used for inline diffused emitters typically results in a surface dead layer (due to surface contaminants and a high dopant concentration at the surface), which tends to limit open circuit voltage (V_{oc}) and efficiency of inline diffused solar cells compared to tube-diffused. Effective reduction or removal of this heavily doped dead layer and surface contaminants is essential for achieving higher efficiencies using inline-diffusion. Various cleaning or etching processes have been developed to remove this dead layer and surface contaminants including the so called “emitter etch-back” process. One skilled in the art will recognize that tube diffused emitters also have surface dead-layers, albeit at a lower level, and therefore will also benefit from “emitter etch-back” processes.

[0020] Referring to FIG. 1A, the illustration 100 depicts conventional tube diffusion wherein a quartz tube 102 inside a furnace of radiation heaters (108) is used for batch based (i.e., vertical or horizontal wafers 104) emitter formation on the silicon wafers 104 by providing phosphorus oxychloride (POCl_3) vapour at an intake 105 by passing a nitrogen carrier gas 106 through a bubbler 107 of POCl_3 liquid. An exhaust 110 removes excess gas from the furnace 102.

[0021] Referring to FIG. 1B, the illustration 150 depicts conventional horizontal inline diffusion where phosphoric acid (H_3PO_4) 152 is sprayed over one or both surfaces of the silicon wafer 110 and then the silicon wafer 110 is driven on a belt 154 under infrared lamps and/or resistive heaters 156 in several heating zones (typically seven to ten heating zones) to form emitters on the silicon wafers 110.

[0022] Referring to FIG. 2, Referring to FIG. 2, a conventional silicon wafer solar cell fabrication process flow 200 starts with texturing and diffusing the silicon wafer at step 202 for either acidic-isotropic textured multi-crystalline silicon or alkaline-anisotropic textured mono-crystalline silicon. During diffusion 202 a layer of phosphorus glass is automatically grown on the silicon wafer surface. Then, parts of the emitter surface area (which will later be metallised) are selectively protected by an etch-blocking mask at step 204. The mask can be applied by numerous methods including ink-jet printing, screen printing, or stencil printing. The masked wafers are then etched with a dilute hydrofluoric (HF) acid solution to remove the diffusion glass from the unmasked areas at step 206. Subsequently, the unmasked heavily doped silicon surface regions are etched-back to a required high sheet resistance value using a conventional etch-back solution 208, the area under the etch-blocking mask not being etched. Finally, the etch-blocking mask is stripped in a dilute hot alkaline solution (e.g. KOH) at step 210, and the remaining diffusion glass is removed in dilute HF at step 212, thereby completing the selective emitter (SE) structure. After the PSG removal at step 212, the emitter anti-reflective coating (ARC) is deposited and final metallization is performed at step 214. The dashed outlined boxes for steps 204, 206, 208, 210 indicate the additional steps required for formation of a selective emitter solar cell.

[0023] For simplicity, edge isolation is not shown in the process flow 200 and either laser edge isolation or rear-side wet-etch junction removal (typ. HF-HNO₃) can be used for such edge isolation step. Present etch-back solutions are all acidic and HF-based (HF-HNO₃, HF-HNO₃-HAc, HF-O₃, etc.), which while etching the emitter layers also disadvantageously etches the PSG. In addition, stripping the etch mask in the hot KOH solution may further degrade the crystalline silicon wafer solar cell.

[0024] In accordance with the present embodiment, an etch-impeding mask combined with a non-acidic etch-back solution is used to provide an improved silicon wafer solar cell fabrication process. Referring to FIG. 3, a side-by-side comparison of the conventional process flow 200 and a process flow 300 in accordance with the present embodiment is presented. The process 300 begins with texturing and diffusing the silicon wafer at step 302 for either acidic-isotropic textured multi-crystalline silicon or alkaline-anisotropic textured mono-crystalline silicon. During diffusion 302, a PSG layer is automatically grown on the diffused wafer. The preferred embodiment uses the PSG to form the etch-impeding mask. Thus, the PSG layer is selectively protected by applying a patterned etch-blocking mask at step 304, the mask pattern matching the final front side metallisation pattern to be used on the solar cell. Various methods can be used to apply the etch-blocking mask at step 304 including screen printing, ink jet printing and stencil printing. Next, the un-masked PSG layer is etched by a dilute HF solution at step 306 to selectively remove the PSG, thereby forming the etch-impeding PSG mask.

[0025] Next, in accordance with the present embodiment, the wafer is immersed at step 308 in an etch-back solution based on alkaline and oxidising solutions which etches through the PSG to form a selective emitter on the silicon wafer solar cell. The etch-back solution must be selected such that it etches through the etch-impeding PSG mask at a slower rate than the un-masked areas to realise the selective emitter. Preferably, the chemical etching step 308 uses a solution of potassium hydroxide (KOH) and sodium hypochlorite (NaOCl) solutions, which etches more slowly through the PSG etch-impeding mask whilst also providing a controlled, uniform and near-conformal etching of the emitter in the non-masked areas. During the first forty to fifty seconds, the alkaline nature of the etch-back solution completely removes the

printed etch-blocking mask in parallel with commencement of the etch-back in the unprotected doped Si-area, thereby removing the need to have a separate mask stripping step (e.g. step 210 in the convention process flow 200). After the removal of the etch-blocking mask, the thin layer of PSG then acts as an etch-impeding mask, substantially slowing the etching action of the KOH-NaOCl etch-back solution. The two unequal silicon etching rates on the exposed and masked areas ultimately results in the formation of the selective emitter structure on the diffused wafer. The exposed area is etched back to a higher sheet resistance (R_{sheet}), whereas the area under the etch-impeding PSG mask is etched at a substantially slower rate resulting in a smaller change in the R_{sheet} . In addition to fewer process steps, the removal of high concentration HF from the process (i.e., the HF used for mask removal in conventional step 210) significantly lowers health and safety risks.

[0026] Finally, the remaining PSG is removed in dilute HF at step 310, thereby completing the selective emitter (SE) structure. After the PSG removal at step 310, the emitter anti-reflective coating (ARC) is deposited and final metallization is performed at step 312. In accordance with the present embodiment, contact formation on the SE structure is aligned such that the contacts are formed at the heavily doped, smaller change in R_{sheet} portions of the SE structure.

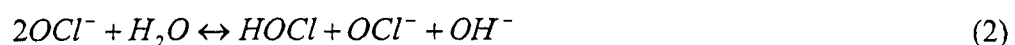
[0027] As before, the dashed outlined boxes for steps 304, 306, 308 indicate the additional steps required for formation of the selective emitter solar cell (only three steps for process flow 300 in accordance with the present embodiment as compared to the four steps required for formation of the selective emitter solar cell for conventional process flow 200). As described above, the edge isolation is also not shown in the process flow 300. Either laser edge isolation or rear-side wet-etch

junction removal (typically HF-HNO₃) can be used for the edge isolation step in the process flow 300.

[0028] Referring to FIG. 4, the process flow 300 is depicted side-by-side with en process structures 400. At step 302, after texturing and diffusion, a silicon wafer 402 has a diffused doped emitter layer 404 covered by the PSG layer. The diffused doped layer 404 is most heavily doped at a surface under the PDG layer 406. A patterned etch-blocking mask 408 is formed on the PSG layer 406 at step 304 and the unmasked portions of the PSG layer 406 are removed at step 306.

[0029] As described above, step 308 advantageously replaces conventional steps 208 and 210. In the HF/HNO₃ based process used at conventional step 208, the HNO₃ oxidises the Si surface whilst the HF removes the oxide, resulting in an etch-back of the unmasked area. In this reaction, the etch-blocking mask stops etching of the emitter in the masked area. Simultaneously, a layer of porous Si is generated on the unmasked heavily diffused Si wafer surface. The porous Si layer on the exposed Si surface is necessary to protect the exposed Si during the mask stripping in hot alkali solution at step 210. The exothermic nature of HF/HNO₃ etch-back process, which is dependent on process bath temperature, is challenging to control as it requires continuous cooling to keep the solution below 10°C. In addition, the HF/HNO₃ solution is not compatible with PSG as it also etches PSG.

[0030] Thus, in accordance with the present embodiment, the etch-back is performed by the use of KOH (or NaOH) and NaOCl solutions, where NaOCl is a strong oxidising agent. The chemical reactions are summarized in chemical formulas (1) to (3):





NaOCl ionizes in water to give hypochlorous acid (HOCl) and hypochlorite ions (OCl⁻). The silicon etching rate is very small due to the availability of hydroxyl (OH⁻). Further, silicon reacts with the hypochlorous ions to form silicon dioxide (SiO₂). The SiO₂ layer produced due to the presence of NaOCl acts as a barrier to fast silicon etching by KOH leading to a slow overall etching rate. The process bath temperature is maintained at 80°C to keep the etch rate stable. The slow etching rate and near conformal Si etching makes the process highly controllable. Because of the controllability of the etch rate, the total removal of the doped region is set by the total etch time, for a given solution composition, to reach the desired sheet resistance or surface concentration required for the solar cell being fabricated. More importantly, the KOH/NaOCl solution is compatible with PSG enabling the use of the PSG as an etch-impeding mask 410.

[0031] The process for formation of a selective emitter in accordance with the present embodiment requires selective removal of the PSG layer 406 at step 306 to form the etch-impeding mask 410. The PSG layer 406, which is automatically grown during diffusion, is selectively protected by applying the patterned etch-blocking mask 408. The pattern of the etch-block mask 408 matches the final front side metallisation pattern to be used on the solar cell. Next, the un-masked PSG layer 406 is etched away by dilute HF solution at step 306 to selectively remove the PSG, thereby forming the etch-impeding PSG mask 410 for the emitter etch-back step 308.

[0032] During the initial forty to fifty seconds of the emitter etch-back step 308, the alkalinity of the etch-back solution removes the initial etch-blocking mask 408 used to form the PSG etch-impeding mask. Once the etch-blocking mask 408 is removed, the PSG etch-impeding mask 410 inhibits the etch-back action of the KOH/NaOCl

solution in a repeatable manner. After the etch-back step 308, surface contaminants including residual PSG are removed at step 310 providing heavily doped selective emitters 412 separated by lightly doped areas 414. At step 312, the front metallization 415 is formed by, for example, screen printing the metallization 415 aligned with the selective emitters 412 and later forming a contact 416 thereon by firing the contact 416. An antireflection/passivation layer of SiN 418 is also formed on the front while a metallization layer 420 is formed on the back of the substrate 402.

[0033] The change in R_{sheet} of the diffused (both tube & inline) mono- and multicrystalline Si wafers (with or without a PSG layer) for etch-back durations of up to five minutes is shown in FIGs. 5 and 6. Referring to FIG. 5, a graph 500 depicts a change in average sheet resistance (R_{sheet}) after etch-back for diffused monocrystalline wafers without and with the PSG etch-impeding layer in accordance with the present embodiment. Time is plotted along the X-axis 502 and the change in sheet resistance is plotted along the Y-axis 504. Trace 506 depicts the change in sheet resistance over time for tube-formed monocrystalline wafers without the PSG etch-impeding layer and trace 508 depicts the change in sheet resistance over time for tube-formed monocrystalline wafers with the PSG etch-impeding layer. Similarly, trace 510 depicts the change in sheet resistance over time for inline-formed monocrystalline wafers without the PSG etch-impeding layer and trace 512 depicts the change in sheet resistance over time for inline-formed monocrystalline wafers with the PSG etch-impeding layer. All wafers had a starting sheet resistance of $\sim 45 \Omega/\text{sq}$ and were etched in the KOH/NaOCl solution for the duration of one to five minutes. The traces 506, 508, 510, 512 clearly show that a differential in R_{sheet} of $\sim 50 \Omega/\text{sq}$ can be achieved for monocrystalline, which is sufficient for forming viable selective emitter structures.

[0034] Referring to FIG. 6, a graph 600 depicts a change in average sheet resistance (R_{sheet}) after etch-back for diffused multicrystalline wafers without and with the PSG etch-impeding layer in accordance with the present embodiment. As with FIG. 5, time is plotted along the X-axis 602 and the change in sheet resistance is plotted along the Y-axis 604. Trace 606 depicts the change in sheet resistance over time for tube-formed multicrystalline wafers without the PSG etch-impeding layer and trace 608 depicts the change in sheet resistance over time for tube-formed multicrystalline wafers with the PSG etch-impeding layer. Similarly, trace 610 depicts the change in sheet resistance over time for inline-formed multicrystalline wafers without the PSG etch-impeding layer and trace 612 depicts the change in sheet resistance over time for inline-formed multicrystalline wafers with the PSG etch-impeding layer. Again, all wafers had a starting sheet resistance of $\sim 45 \text{ } \Omega/\text{sq}$ and were etched in the KOH/NaOCl solution for the duration of one to five minutes. The traces 606, 608, 610, 612 clearly show that a differential in R_{sheet} of $\sim 50 \text{ } \Omega/\text{sq}$ can be achieved for multicrystalline, which is sufficient for forming viable selective emitter structures.

[0035] One skilled in the art will recognise that other solutions using a mixture of alkaline chemicals (including NaOH, KOH, and similar alkaline chemicals) and oxidiser chemicals (NaOCl, H_2O_2 , KMnO_4 , and other oxidiser chemicals) could also be used to achieve the combined etch-back/mask-removal process in accordance with the present embodiment. The etch concentration, etch rate and etch time needs to be empirically determined for each PSG layer thickness and density in order to achieve the process target. In each case the etch-back process can be performed using batch based tube processing (i.e., vertical wafers) or horizontal in-line processing.

[0036] As seen, conventional etch-back solutions 200 are based on concentrated HF acid solutions and HF is an extremely hazardous material, resulting in a high hazard

for etch-back solutions based on HF acid. The HF-free property of the process 300 in accordance with the present embodiment significantly lowers the risk and creates an alternate, environment-friendly option for etch-back processes. HF based etch-back solutions 208 also remove the PSG/PG layers, which disallows the use of PSG as a masking layer. Because of this incompatibility, undercut etching of the mask can occur during the etch-back step 208 leading to process deviations. The process 300 in accordance with the present embodiment is compatible with the PSG layers allowing the use of PSG/PG layers as etch mask and enabling new processing routes for the fabrication of selective emitter solar cells. HF based etch-back solutions 208 typical affect textured surfaces, which limits the amount of etch-back that can be achieved without impacting the optical performance of the texture. The controlled, uniform and near-conformal Si-etching of the etch-back solution used at step 308 allows much deeper etch-backs without impact the texturing.

[0037] In the typical process 200, normally a two to four hundred micron masked area is used as a heavily doped area for contact formation. However, the present day silver contacts generally have sixty to one hundred micron finger widths. Hence, the remaining part of the heavily doped area (which is not metallised) is exposed to light. However, the heavy doping severely reduces photocurrent due to higher recombination of light generated carriers. In accordance with the present embodiment, Si-etching is still going on with a relatively slow speed under the etch-impeding PSG mask at step 308. This slow but controlled Si-etching increases the high R_{sheet} value to a small extent, enough to reduce the effect of increased recombination in the non-metallised region of the heavily doped area 412. Therefore, the process 300 provides additional potential for enhancement of solar cell efficiency.

[0038] Thus, it can be seen that a solar cell fabrication process that overcomes the drawbacks of conventional etching process steps, such as providing possible efficiency increase due to increased R_{sheet} values to a small extent underneath the etch-impeding layer during etch-back by eliminating the effect of a dead layer, has been provided. Further, a solar cell fabrication process has been provided that does not have the safety risks and hazards present in HF-based etching process steps. In addition, fabrication process flows have been provided which can reduce cost by reducing the steps required. While exemplary embodiments have been presented in the foregoing detailed description of the invention, it should be appreciated that a vast number of variations exist.

[0039] It should further be appreciated that the exemplary embodiments are only examples, and are not intended to limit the scope, applicability, operation, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing an exemplary embodiment of the invention, it being understood that various changes may be made in the function and arrangement of process steps described in the exemplary embodiment without departing from the scope of the invention as set forth in the appended claims.

CLAIMS

What is claimed is:

1. A method for silicon wafer solar cell fabrication comprising:
patterning etch-impeding material formed on an emitter surface of the silicon wafer solar cell to form an etch-impeding mask; and
etching-back the emitter surface of the silicon wafer solar cell with the etch-impeding mask thereon using a solution based on alkaline and oxidising solutions which etches through the etch-impeding mask at a slower rate than it etches through unmasked areas of the emitter surface to form a selective emitter on the silicon wafer solar cell.
2. The method in accordance with Claim 1 wherein the etching-back step comprises etching-back the emitter surface of the silicon wafer solar cell until a target sheet resistance is reached.
3. The method in accordance with either Claim 1 or Claim 2 wherein the etching-back step comprises etching-back the emitter surface of the silicon wafer solar cell using a solution of potassium hydroxide (KOH) and sodium hypochlorite (NaOCl) solutions.
4. The method in accordance any of Claims 1 to 3 wherein the patterning step comprises:
forming an etch-blocking mask on the etch-impeding material formed on the emitter surface of the silicon wafer solar cell; and

patterning the etch-impeding material through the etch-blocking mask to form the etch-impeding mask.

5. The method in accordance with Claim 4 wherein the step of forming the etch-blocking mask comprises screen printing the blocking mask on the etch-impeding material formed on the emitter surface of the silicon wafer solar cell.

6. The method in accordance with either Claim 4 or Claim 5 further comprising removing unmasked portions of the etch-impeding material from the emitter surface prior to the etching-back of the emitter surface of the silicon wafer solar cell.

7. The method in accordance with Claim 6 wherein the removing unmasked portions of the etch-impeding material step comprises removing the unmasked portions of the etch-impeding material using a dilute hydrofluoric acid (HF) solution.

8. The method in accordance with either Claim 4 or Claim 5 wherein the etching-back step comprises etching-back the emitter surface of the silicon wafer solar cell while removing the etch-blocking mask.

9. The method in accordance with any of Claims 1 to 8 wherein the etch-impeding material comprises a silicate glass material.

10. The method in accordance with Claim 9 wherein the silicate glass material is selected from the group comprising phosphosilicate glass (PSG) and borosilicate glass (BSG).

11. The method in accordance with any of Claims 1 to 10 further comprising removing surface contaminants including residual etch-impeding material after etching-back the emitter surface of the silicon wafer solar cell.

12. The method in accordance with Claim 11 wherein the removing surface contaminants step comprises removing surface contaminants including residual etch-impeding material using a dilute hydrofluoric acid (HF) solution.

13. The method in accordance with any of Claims 1 to 12 further comprising after the etching-back step:

depositing an anti-reflective coating (ARC) on an outer surface of the emitter;
and
performing final metallisation.

14. The method in accordance with Claim 13 further comprising after the final metallisation step the step of firing contacts on the silicon wafer solar cell.

1/6

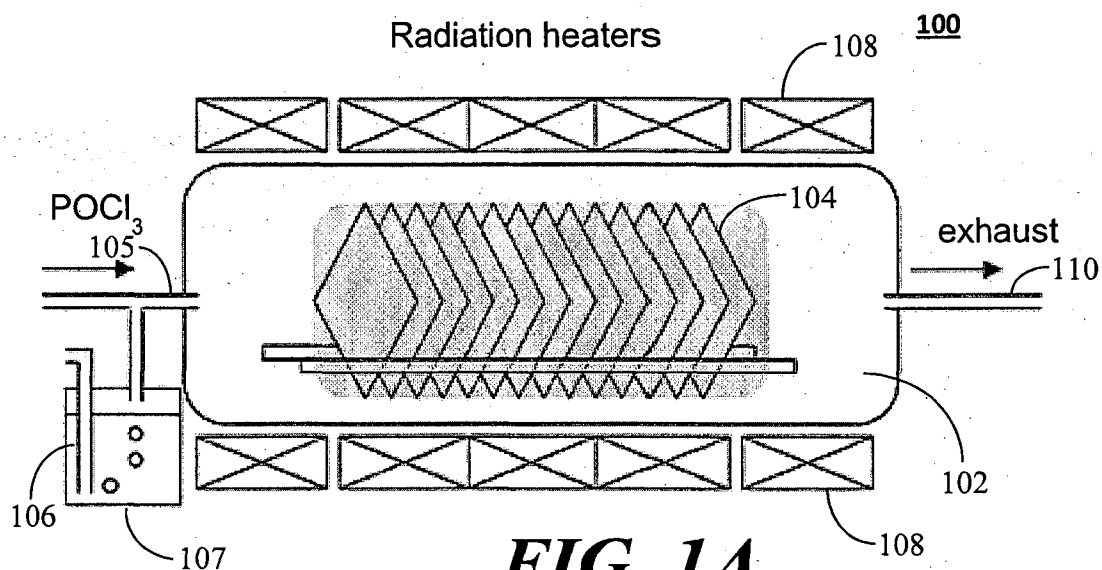


FIG. 1A
PRIOR ART

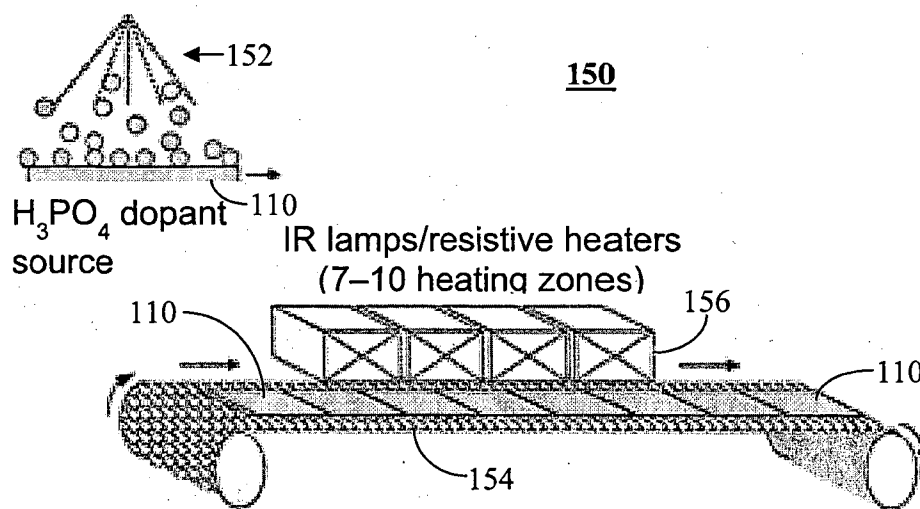


FIG. 1B
PRIOR ART

2/6

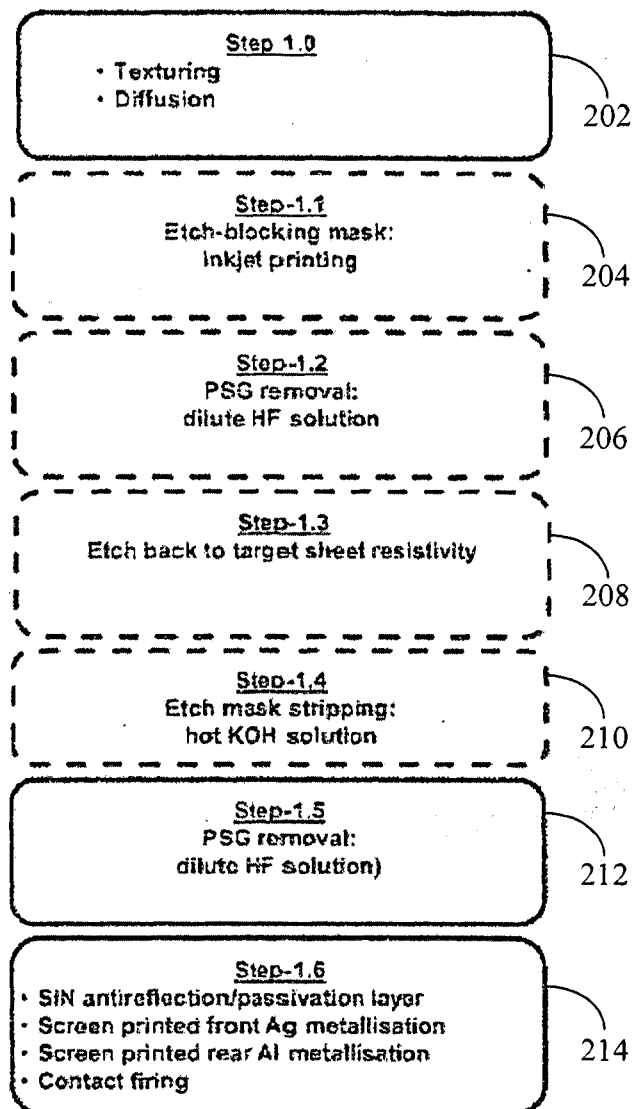
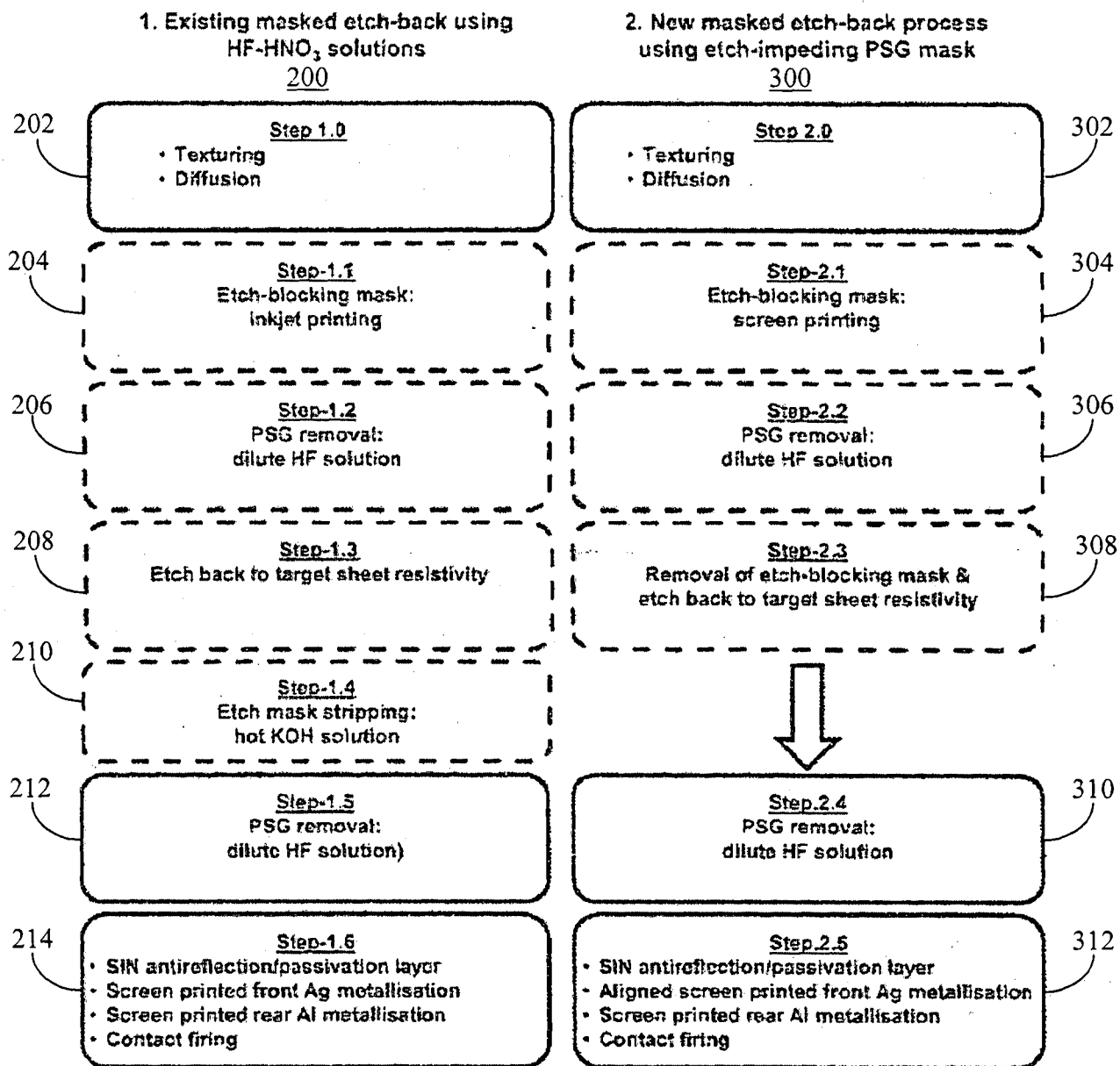
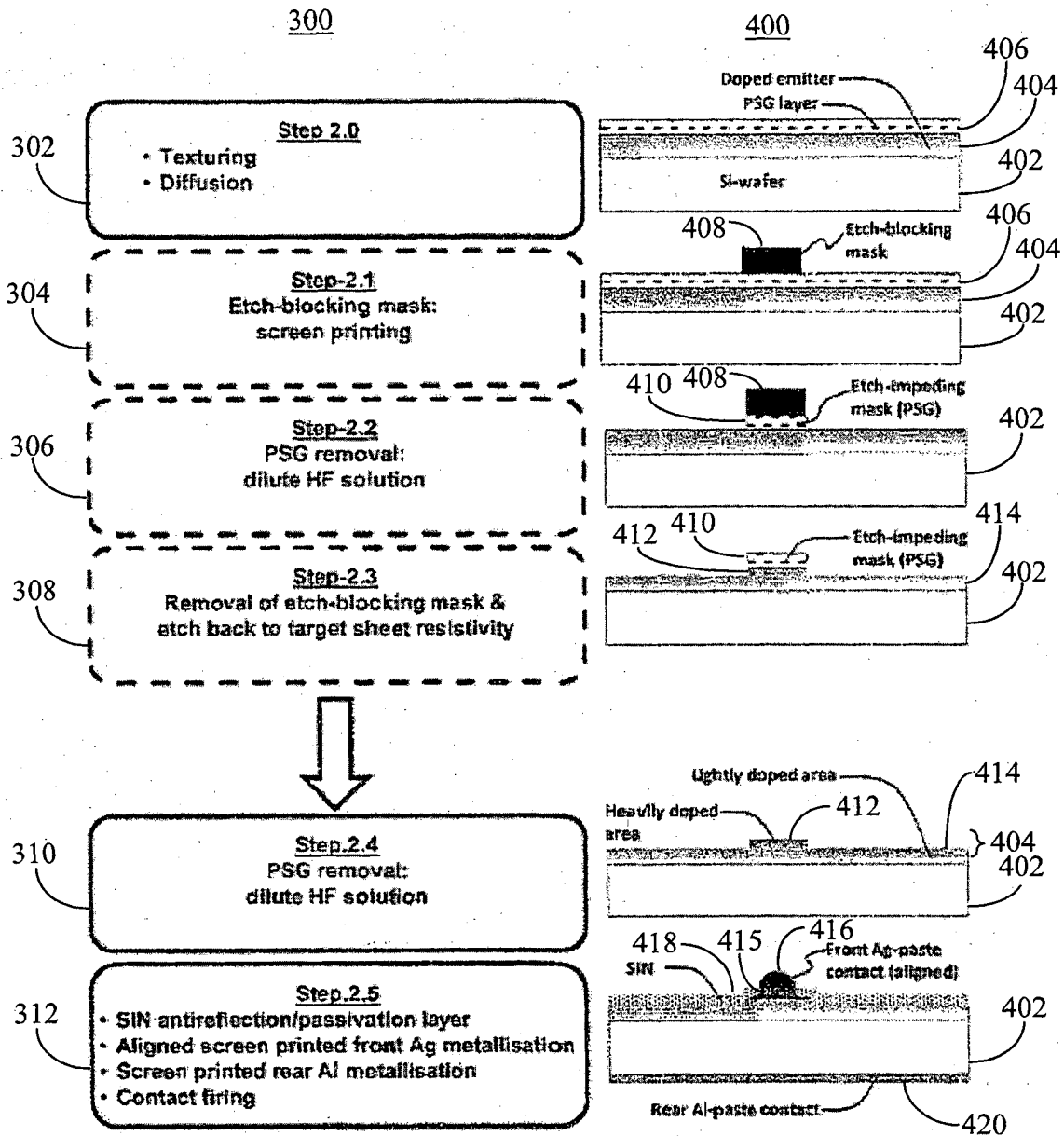
200

FIG. 2
PRIOR ART

**FIG. 3**

4/6

**FIG. 4**

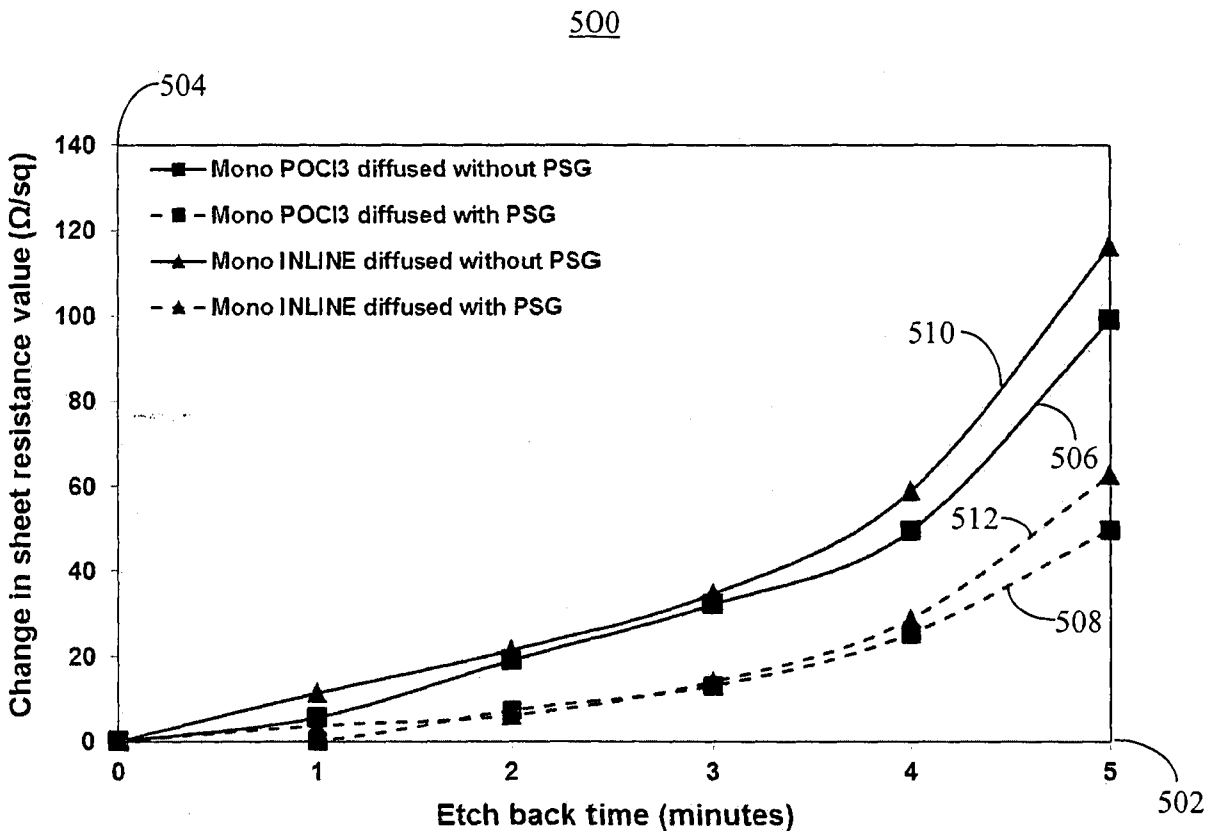
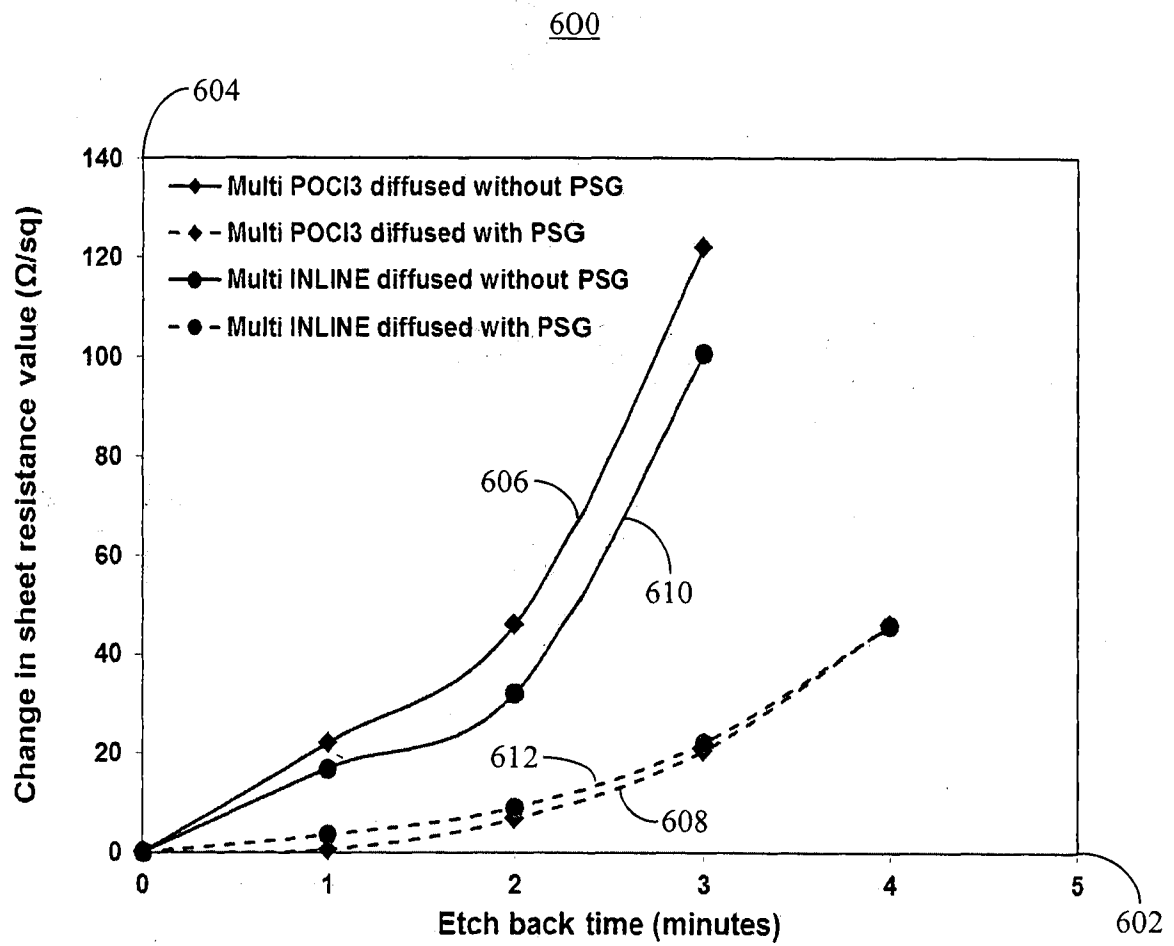


FIG. 5

6/6

**FIG. 6**

INTERNATIONAL SEARCH REPORT

 International application No.
PCT/SG2013/000299

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/3213 (2006.01) C09K 13/02 (2006.01) H01L 31/18 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

 Databases : WPI, EPODOC, TXTUS5, INSPEC & Keywords: solar-cell, photovoltaic, PV, etch, selective-emitter, patterning emitter, mask, glass, PSG, BSG, KOH, NaOCl, sodium-hypochlorite, hydroxide, oxidise, oxidize and similar terms
 Google search & keywords: emitter etch back, mask, PSG

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search 26 September 2013		Date of mailing of the international search report 26 September 2013	
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustalia.gov.au Facsimile No.: +61 2 6283 7999		Authorised officer Jayati Ray AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. 0262223654	

INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/SG2013/000299
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	RAABE B. ET AL., "The Development of Etch-Back Processes for Industrial Silicon Solar Cells", 25th European Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photovoltaic Energy Conversion, 6-10 September 2010, Valencia, Spain, pages 1174-1178. Experimental , Etch-back emitter, Fig. 3 and the associated text	1-14
Y	BOOK F. ET AL., "THE ETCHBACK SELECTIVE EMITTER TECHNOLOGY AND ITS APPLICATION TO MULTICRYSTALLINE SILICON", 35th IEEE Photovoltaic Specialists Conference (PVSC), Honolulu, HI, 20-25 June 2010, pages 001309 - 001314 Fig. 1 and the associated text	1-14
Y	US 2013/0220420 A1 (LACHOWICZ ET AL.) 29 August 2013 & WO 2012/028727 A2 paragraphs 0019-0029, 0045, 0048, Examples 1-6	1-14

INTERNATIONAL SEARCH REPORT Information on patent family members		International application No. PCT/SG2013/000299	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
US 2013/0220420 A1	29 Aug 2013	CN 103314449 A	18 Sep 2013
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		DE 102011050136 A1	08 Mar 2012
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		EP 2612362 A2	10 Jul 2013
		EP 2612364 A2	10 Jul 2013
		EP 2612365 A2	10 Jul 2013
		US 2013220420 A1	29 Aug 2013
		US 2013228220 A1	05 Sep 2013
		WO 2012028723 A2	08 Mar 2012
		WO 2012028727 A2	08 Mar 2012
		WO 2012028728 A2	08 Mar 2012
End of Annex			
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001. Form PCT/ISA/210 (Family Annex)(July 2009)			