March 23, 1965 F. R. FLUHR ETAL 3,175,195

LONG TIME DELAY LINE

Filed Oct. 31, 1961

FIG. 3

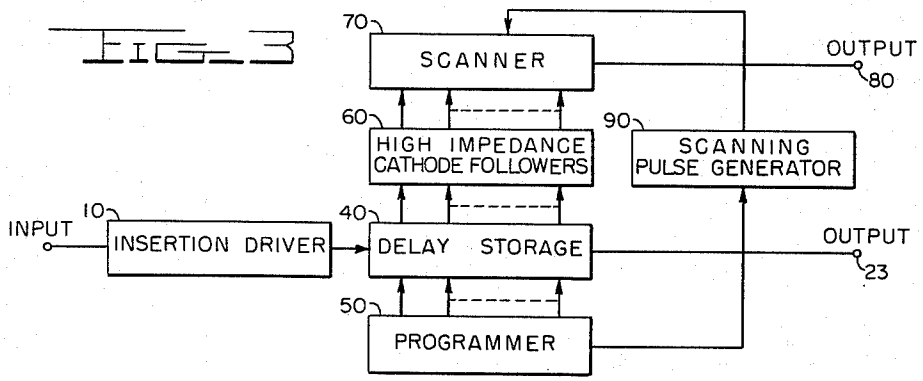


FIG. 1

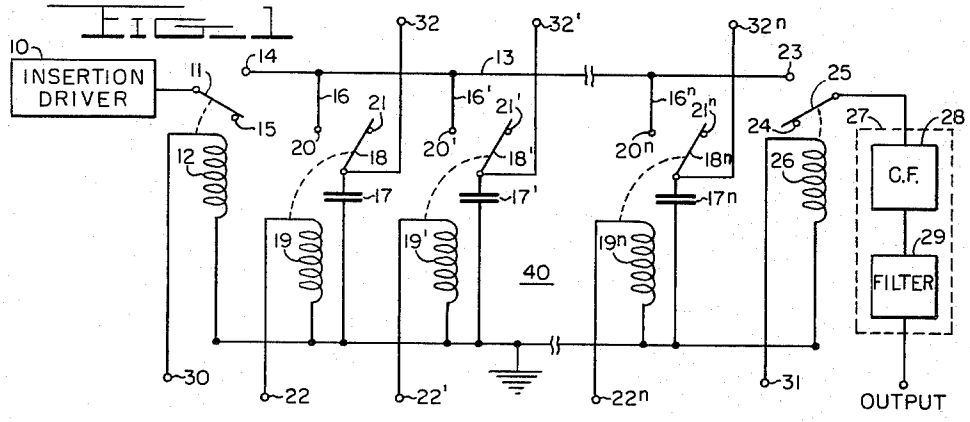
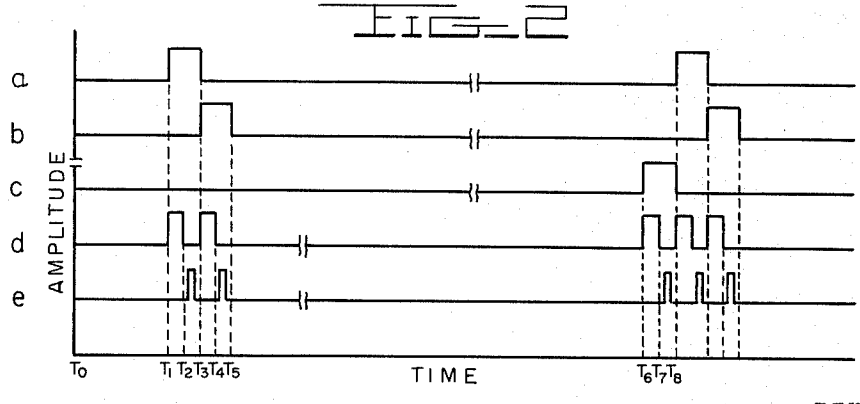


FIG. 2



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LONG TIME DELAY LINE

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The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalities thereon or therefor.

This invention relates to improvements in time delay circuits for data processing systems and more particularly to an improved circuit and method for obtaining relatively long, controlled time delays.

A delay line is a device which will accept a time-varying electrical signal at its input, and within certain limits of amplitude, time rate of change, and accuracy, deliver this signal to its output terminal following some predictable delay. Numerous techniques to accomplish this effect, such as lumped or distributed constant lines, ultrasonic waves in solids or liquids and electromechanical or electromagnetic recording having been developed in the prior art, but the field is limited by lack of a simple, reliable delay line which will provide time delays up to several seconds in length and still be capable of a fast acting continuous but variable readout.

Delay lines employing lumped or distributed electrical constants exhibit a fixed delay for a given configuration, and experience a progressive deterioration of the signal amplitude with increasing delay time. Either type of line is limited in that precautions must be taken to avoid upsetting impedances, the signals change at every point along the line from input to output at a constant rate and the delays range from millimicroseconds to milliseconds.

Prior delay lines have also converted signals to a sound wave or employed the signal to modulate an ultrasonic carrier which is transmitted acoustically through a solid, liquid or gas having the desired transit time delay. Transducers are usually employed to sample or tap the signal energy at variable positions along the carrier but then the system is limited by certain minimum distances that are necessitated due to the physical size of the carrier and transducers. Delay media which have been employed in systems previously reduced to practice have included air, water, mercury, metal wires or rods (usually of magnetostrictive material) and quartz plates. Delay times, however, must remain fixed for a given configuration and practical time delays range from a few microseconds to several milliseconds in devices of reasonable size.

Electromechanical and electromagetic recording techniques have also been employed as a delay line but to avoid endless consumption of recording media, a closed loop system providing for erasure and re-use of the media must be employed. While time delays are theoretically without limit for extended operations, the media itself is subject to wear and needs replacement. Further limiting their application is the need for driving mechanisms necessary to produce relative mechanical movements.

The most closely related previously existing delay line, is described in the British periodical "Nature," January 26, 1952, pages 148 to 149 by J. M. Janssen wherein an amplifier is used to isolate the respective capacitors. The delay line, however, is limited in that the transfer operation must be carried out at twice the transfer cycle rate, amplifier distortion or noise may introduce undesirable discrepancies in the transfer process and the equipment requirements are large since two amplifiers, capacitors and relay contacts are required for each element of time resolution in the stored signal.

Accordingly, it is an object of our invention to provide an improved method and device for storing electrical information for relatively long periods of time without undue complexity.

It is another object of our invention to provide an improved storage device for retaining data over long periods of time and to provide means for rapid, continuous and variable readout.

It is a further object of this invention to provide a signal processing circuit capable of causing a time delay of several seconds and capable of passing frequencies limited only by the sampling rate used to cause the time delay.

It is still a further object of our invention to provide a storage device useful as a signal detector wherein each stored element of an input signal is made available simultaneously and with a minimum of operations for rapid sampling operations.

Yet another object of this invention is to provide a long time delay line capable of being employed as a storage device for pattern recognition of a signal by repetitively scanning each element of time resolution.

Still another object of our invention is to provide a storage device whereby the delay line permits a wide continuous but variable range of substantially instantaneous control over the total delay.

According to the invention, a data signal is supplied to a delay line requiring only one capacitor and one relay contact for each stored element of time resolution in the stored signal. The circuit requires only one read-in amplifier and one readout amplifier while performing only one readin-readout operation for each time element, or n operations between a signal element entering the line and the time it is delivered to the output, where n is the number of capacitors in the delay line. Each signal element is also made simultaneously available by n cathode followers whereby rapid sampling operations may be performed and unlimited scanning readout of each stored element is provided.

The exact nature of this invention together with other objects, novel features and advantages thereof, will be readily apparent from consideration of the following description relating to the annexed drawing wherein similar reference numerals refer to similar parts and wherein:

FIGURE 1 shows a schematic diagram, partially in block form, of the delay line in accordance with the principles of our invention;

FIGURE 2 is an illustration of the waveforms encountered for proper operation of the delay line shown in FIGURE 1; and

FIGURE 3 is a block diagram showing a signal scanning system employing the delay line of our invention.

Referring now to the drawings and in particular to FIG. 1, the delay line of this invention is shown as comprising an insertion driver **10** for impressing data in the form of a pulsed input signal on the line and a readin relay arm **11** actuated by a readin relay coil **12**. Arm

11 is also arranged so as to be able to connect a common line 13 through input contact point 14 which with contact 15, forms a three terminal readin relay switch. Also connected along common line 13 are n number of leads 16, 16' . . . 16^n, the number depending upon, the signal bandwidth and delay desired. The stored input signal is divided into separate elements of time resolution representative of data information, with each element stored by a separate capacitor 17, 17' . . . 17^n. Each capacitor is connected to common line 13 by means of a storage relay arm 18, 18' . . . 18^n which is actuated by a storage relay coil 19, 19' . . . 19^n and with contacts 20, 20' . . . 20^n and 21, 21' . . . 21^n forms a two way relay switch. The respective storage relays are controlled from input terminals 22, 22' . . . 22^n wherever a programmed signal is applied. Common line 13 is also provided with a readout contact point 23 which with contact 24, relay arm 25 and relay coil 26 form a two way readout relay switch whereby the common line 13 can be connected to output circuit 27.

Circuit 27 comprises a series connected high impedance cathode follower 28 and filter 29. The readin switch relay is actuated by a control signal being applied to terminal 30 while the readout switch relay is actuated by applying a control signal to terminal 31.

Each capacitor is also provided with an output contact, 32, 32' . . . 32^n so as to make each stored signal element simultaneously available for further processing such as shown in FIG. 3.

The operation of the circuit is best seen by considering the pulse waveforms shown in FIG. 2. Neglecting switching time delays and assuming that the relays operate from positive signals, the waveforms shown in FIG. 2 will cause proper operation of the delay line shown in FIG. 1. As shown in FIG. 1, at time zero (T_0) all the switches are in their rest (or open) position. Starting at time T_1, storage relay coil 19 is energized by a signal (FIG. 2a) impressed on program input terminal 22 causing capacitor 17 to be connected to the common line 13. Simultaneously at time T_1, readout relay coil 26 is energized (FIG. 2d) for approximately one-half (½) the time that coil 19 is energized. This causes the voltage or signal element stored in capacitor 17 to be connected to the output circuit, allowing the voltage or signal element on capacitor 17 to be read out through a sample and hold cathode follower 28.. At T_2, approximately half (½) way through the time cycle that storage coil 19 is energized, readout coil 26 is de-energized and a pulse applied to program terminal 30 (FIG. 2e) energizing readin relay coil 12. This allows capacitor 17 to be connected to signal source 10 and causes capacitor 17 to be charged to the signal voltage at that instant representative of the signal from the driver 10. Readin coil 12 is then de-energized followed by the storage relay switch coil 19. Storage relay coil 19' is then energized (FIG. 2b) at time T_3 and again simultaneously, readout relay coil is energized by applying a control pulse to program terminal 31, capacitor 17' being connected to the output sample and hold cathode follower 28. At time T_4, approximately half way through the pulse cycle applied to terminal 22', readout coil 26 is de-energized and momentarily at T_5, readin coil 12 is again energized allowing capacitor 17' to be charged to the voltage value present at input contact point 14. This operation is repeated for n capacitors and relays (time T_6 to T_8) and when the program has passed through n steps, the signal returns to terminal 22 and begins to repeat the operation. Thus the output signal is n switching periods behind the input signal and is designated in FIG. 2 as the time delay between T_1 and T_8.

It should be appreciated that the present invention is not to be limited to any particular set of values for the circuit components or means for accomplishing the switching operation and the programming signals may

be developed by any type of counting device which will provide the proper time and waveforms.

It should also be appreciated that our invention only requires one capacitor and one relay contact for each stored element of time resolution in the stored signal. It should also become apparent that this circuit will perform only one readin-readout operation for each time element and that n operations will be performed between a signal element entering the line and the time it is delivered to an output circuit causing the delay, where n is the number of signal elements stored.

By connecting a high impedance cathode follower to each of the capacitors at terminals 32, 32' . . . 32^n a unique signal scanning system becomes possible. Considering in particular FIG. 3, n number of cathode follower circuits 60 are coupled to n number of storage elements in a delay storage 40 which is the delay line shown in FIG. 1. This allows for means for providing simultaneously for readout, each element of time resolution of the stored input signal. If each of the outputs of the cathode followers are then scanned at a high rate such as by scanner 70 an output signal representative of a function of the respective cathode followers is provided at output terminal 80. The scanner is synchronized with the programmer 50 through pulse generator 90 thereby providing a further unique signal detecting and processing system.

By varying the scan pattern and/or the programming, a wide continuous range of instantaneous control over the elements of time resolution stored in delay unit 40 becomes possible.

A unique feature of our invention is that the delay of the input signal from driver 10 is only limited by the sampling rate from programmer 50.

This invention has been utilized in providing up to 100 steps in the delay line with a signal decay of less than 1% of the input value of each stored element while making every element of a stored signal simultaneously available for rapid sampling operations with a minimum of operations.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood, that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

What is claimed is:

1. In a storage device for retaining data over long periods of time, the combination of, a common transmission line, a readin switch, means for connecting and disconnecting said switch to said line, a data signal source coupled to said readin switch, a readout switch, means for connecting and disconnecting said readout switch to said line, n number of terminals between said readin switch and said readout switch connected to said common line, n number of means for storing n elements of said data signal, switch means for connecting and disconnecting the terminals of said common line to n number of storing means and programming means for sequentially controlling the operation of all of said switches and switch means and for varying the rate at which all of said switches and switch means operate.

2. In the storage device as set forth in claim 1, wherein means are also provided for repetitively scanning the n number of storing means.

3. In a long time delay circuit, the combination of, a data signal source comprising n number of bits, a common transmitting line, readin switch means for connecting and disconnecting said data signal source to said line, first output utilizing means, readout switch means for connecting and disconnecting said first output utilizing means to said line, n number of terminals distributed between said readin switch and said readout switch on said transmitting line, n number of storage means, n storage switch means for connecting and disconnecting said n number of storage means to said n number of terminals, means for in-

dividually and in ordered sequence actuating each of said storage switch means to connect respective storage means and line terminals for a predetermined time period, means for actuating said readout switch means for one-half the time period each of said storage switch means are actuated, means for actuating said readin switch means for a portion of the remaining time period each of said storage means are connected to said line terminals and after said readout switch means are disconnected from said line, second output utilizing means for making *n* number of storage means instantaneously available and sampling means for scanning said second output utilizing means.

4. In the long time delay circuit as set forth in claim 3

wherein said second output utilizing means comprises *n* number of sample and hold high impedance cathode follower circuits which are repetitively scanned by said sampling means.

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