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(54) **Title:** APPARATUS AND METHOD FOR OPTICAL DECOUPLING

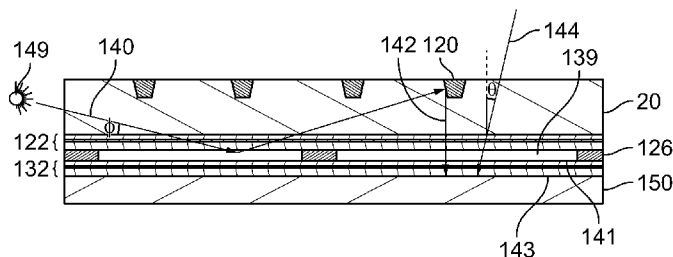


Figure 11

(57) **Abstract:** This disclosure provides apparatus, systems and methods for optical decoupling. In one implementation, an optical system includes a substrate transmissive to visible light, a first antireflective structure disposed on a surface of the substrate, a second antireflective structure. The first and second antireflective structures define at least one cavity containing air in between. The optical system further includes a plurality of support posts configured to space the first antireflective structure from the second antireflective structure to define the height of the at least one cavity. A reflective display is disposed on a surface of the second antireflective structure opposite the at least one cavity.



APPARATUS AND METHOD FOR OPTICAL DECOUPLING

TECHNICAL FIELD

[0001] This disclosure relates to electromechanical systems.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0002] Electromechanical systems include devices having electrical and mechanical elements, actuators, transducers, sensors, optical components (e.g., mirrors) and electronics. Electromechanical systems can be manufactured at a variety of scales including, but not limited to, microscales and nanoscales. For example, microelectromechanical systems (MEMS) devices can include structures having sizes ranging from about a micron to hundreds of microns or more. Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than a micron including, for example, sizes smaller than several hundred nanometers. Electromechanical elements may be created using deposition, etching, lithography, and/or other micromachining processes that etch away parts of substrates and/or deposited material layers, or that add layers to form electrical and electromechanical devices.

[0003] One type of electromechanical systems device is called an interferometric modulator (IMOD). As used herein, the term interferometric modulator or interferometric light modulator refers to a device that selectively absorbs and/or reflects light using the principles of optical interference. In some implementations, an interferometric modulator may include a pair of conductive plates, one or both of which may be transparent and/or reflective, wholly or in part, and capable of relative motion upon application of an appropriate electrical signal. In some implementations, one plate may include a stationary layer deposited on a substrate and the other plate may include a reflective membrane separated from the stationary layer by an air gap. The position of one plate in relation to another can change the optical interference of light incident on the interferometric modulator. Interferometric modulator devices have a wide range of applications, and are anticipated to

be used in improving existing products and creating new products, especially those with display capabilities.

[0004] A reflective display, such as an interferometric modulator, can be illuminated by a light source and a light guide (also referred to as a light piping slab) positioned in front of the display. Light generated by the light source can propagate through the light guide, and can be redirected toward the display using one or more light turning features in the light piping slab. However, a portion of the light may reach the display without being properly directed by the turning features and be incident on the display at an undesirable angle. This may cause the display to reflect such light at an angle that is unsuitable for viewing, which can result in image degradation. At least for this reason it can be beneficial to better control the propagation of light from a light source to a display.

SUMMARY

[0005] The systems, methods and devices of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0006] One innovative aspect of the subject matter described in this disclosure can be implemented in an optical system including a substrate transmissive to visible light and having a first surface exposed to receive ambient light and a second surface. The optical system further includes a first antireflective structure disposed on the second surface of the substrate and a second antireflective structure having a first surface and a second surface opposite the first surface. The first surface of the second antireflective structure is disposed facing the first antireflective structure. The first and second antireflective structures define at least one cavity in between, which can contain air. The optical system further includes a plurality of support posts disposed between the first antireflective structure and the second antireflective structure. The plurality of support posts separate the first antireflective structure and the second antireflective structure at a distance that defines the height of the at least one cavity. The optical system further includes a reflective display disposed on a second surface of the second antireflective structure.

[0007] In some implementations, the substrate includes at least one light turning feature configured to direct light propagating in the substrate and incident on the light turning feature toward the reflective display.

[0008] In some implementations, the first antireflective structure includes a plurality of antireflective layers. In some implementations, the first antireflective structure includes at least one of silicon dioxide (SiO_2) and zinc sulfide (ZnS).

[0009] Another innovative aspect of the subject matter described in this disclosure can be implemented in a method of making an optical system. In some implementations, the method includes forming an antireflective structure on a first surface of a transparent substrate, depositing a sacrificial layer over the first antireflective structure, forming a plurality of openings in the sacrificial layer, forming a plurality of support posts in the plurality of openings, and depositing a second antireflective structure over the plurality of support posts. The second antireflective structure includes a first surface and a second surface, and the first surface is disposed facing the first antireflective structure. The method further includes forming a reflective display on the second surface of the second antireflective structure and removing the sacrificial layer to form at least one cavity between the first antireflective structure and the second antireflective structure. The plurality of support posts support the second antireflective structure and separate the first antireflective structure and the second antireflective structure at a distance that defines the height of the at least one cavity.

[0010] In some implementations, the method further includes positioning a light source relative to the substrate such that light provided by the light source can propagate into the substrate through an edge surface of the substrate.

[0011] In some implementations, forming a reflective display on the surface of the second antireflective structure includes depositing an optical stack over the second antireflective structure, depositing a second sacrificial layer over the optical stack, forming a support structure over the optical stack, depositing a movable reflective layer over the support structure, and removing the second sacrificial layer to form an interferometric cavity.

[0012] Another innovative aspect of the subject matter described in this disclosure can be implemented in an optical system including a transparent substrate having a first surface and a second surface, the first surface exposed to receive ambient light. The

optical system further includes a first means for preventing reflections disposed on the second surface of the transparent substrate, a second means for preventing reflections, and a means for decoupling disposed between the first and second reflection preventing means. The optical system further includes a reflective display formed on a surface of the second reflection preventing means such that the second reflection preventing means is between the reflective display and the decoupling means.

[0013] In some implementations, the supporting means includes a plurality of transparent support posts.

[0014] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims. Note that the relative dimensions of the following figures may not be drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device.

[0016] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display.

[0017] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1.

[0018] Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied.

[0019] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2.

[0020] Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A.

[0021] Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1.

[0022] Figures 6B–6E show examples of cross-sections of varying implementations of interferometric modulators.

[0023] Figure 7 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0024] Figures 8A–8E show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

[0025] Figure 9 shows an example of a flow diagram illustrating a manufacturing process for an optical system.

[0026] Figures 10A–10K show examples of cross-sectional schematic illustrations of various stages in manufacturing an interferometric modulator.

[0027] Figure 11 shows an example of a cross-section of one implementation of an optical system.

[0028] Figure 12 shows an example of a cross-section of one implementation of an antireflective structure having microfeatures.

[0029] Figures 13A and 13B show examples of system block diagrams illustrating a display device that includes a plurality of interferometric modulators.

DETAILED DESCRIPTION

[0030] The following detailed description is directed to certain implementations for the purposes of describing the innovative aspects. However, the teachings herein can be applied in a multitude of different ways. The described implementations may be implemented in any device that is configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual, graphical or pictorial. More particularly, it is contemplated that the implementations may be implemented in or associated with a variety of electronic devices such as, but not limited to, mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices, smartphones, Bluetooth devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held or portable computers, netbooks, notebooks, smartbooks, printers, copiers, scanners, facsimile devices, GPS receivers/navigators, cameras, MP3 players, camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (e.g., e-readers), computer monitors, auto displays (e.g., odometer display, etc.), cockpit controls and/or displays, camera view displays (e.g., display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs,

projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (e.g., MEMS and non-MEMS), aesthetic structures (e.g., display of images on a piece of jewelry) and a variety of electromechanical systems devices. The teachings herein also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes, electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

[0031] Optical systems having a transparent substrate, an optical decoupling structure, and a reflective display are disclosed. The optical decoupling structure can be formed on the transparent substrate, and the reflective display can be formed on a surface of the optical decoupling structure opposite the transparent substrate. The optical decoupling structure can include an air gap, which may reduce light that propagates in the transparent substrate reaching the reflective display, thereby improving display performance. Including an optical decoupling structure can permit the transparent substrate to function as a light guide for a light source of the reflective display, thereby better controlling the incident angle of the light that is provided to the display. The optical decoupling structure can include a first antireflective structure and a second antireflective structure positioned on opposite sides of the air gap. The first and second antireflective structures can reduce Fresnel reflections of light propagating to and from the reflective display, thereby improving display performance. The optical decoupling structure and the reflective display can be formed over the transparent substrate using a thin-film process, thereby avoiding a need for a lamination step and/or the need for separately manufacturing a light guide, an optical decoupling structure and a reflective display in some implementations.

[0032] Particular implementations of the subject matter described in this disclosure can be implemented to realize one or more of the following potential advantages. In some implementations, a display is provided having increased brightness and/or reduced

Fresnel reflections. Additionally, some implementations include an optical decoupling layer that is formed using a fabrication process for a reflective display, thereby permitting manufacture of a transparent substrate, an optical decoupling structure and a reflective display using an integrated process. Furthermore, inclusion of an integrated optical decoupling layer can permit a transparent substrate on which a reflective display is built to be used efficiently as a light guide for a light source of the display.

[0033] An example of a suitable MEMS device, to which the described implementations may apply, is a reflective display device. Reflective display devices can incorporate interferometric modulators (IMODs) to selectively absorb and/or reflect light incident thereon using principles of optical interference. IMODs can include an absorber, a reflector that is movable with respect to the absorber, and an optical resonant cavity defined between the absorber and the reflector. The reflector can be moved to two or more different positions, which can change the size of the optical resonant cavity and thereby affect the reflectance of the interferometric modulator. The reflectance spectrums of IMODs can create fairly broad spectral bands which can be shifted across the visible wavelengths to generate different colors. The position of the spectral band can be adjusted by changing the thickness of the optical resonant cavity, i.e., by changing the position of the reflector.

[0034] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device. The IMOD display device includes one or more interferometric MEMS display elements. In these devices, the pixels of the MEMS display elements can be in either a bright or dark state. In the bright (“relaxed,” “open” or “on”) state, the display element reflects a large portion of incident visible light, e.g., to a user. Conversely, in the dark (“actuated,” “closed” or “off”) state, the display element reflects little incident visible light. In some implementations, the light reflectance properties of the on and off states may be reversed. MEMS pixels can be configured to reflect predominantly at particular wavelengths allowing for a color display in addition to black and white.

[0035] The IMOD display device can include a row/column array of IMODs. Each IMOD can include a pair of reflective layers, i.e., a movable reflective layer and a fixed partially reflective layer, positioned at a variable and controllable distance from each other to form an air gap (also referred to as an optical gap or cavity). The movable reflective layer

may be moved between at least two positions. In a first position, i.e., a relaxed position, the movable reflective layer can be positioned at a relatively large distance from the fixed partially reflective layer. In a second position, i.e., an actuated position, the movable reflective layer can be positioned more closely to the partially reflective layer. Incident light that reflects from the two layers can interfere constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel. In some implementations, the IMOD may be in a reflective state when unactuated, reflecting light within the visible spectrum, and may be in a dark state when unactuated, reflecting light outside of the visible range (e.g., infrared light). In some other implementations, however, an IMOD may be in a dark state when unactuated, and in a reflective state when actuated. In some implementations, the introduction of an applied voltage can drive the pixels to change states. In some other implementations, an applied charge can drive the pixels to change states.

[0036] The depicted portion of the pixel array in Figure 1 includes two adjacent interferometric modulators 12. In the IMOD 12 on the left (as illustrated), a movable reflective layer 14 is illustrated in a relaxed position at a predetermined distance from an optical stack 16, which includes a partially reflective layer. The voltage V_0 applied across the IMOD 12 on the left is insufficient to cause actuation of the movable reflective layer 14. In the IMOD 12 on the right, the movable reflective layer 14 is illustrated in an actuated position near or adjacent the optical stack 16. The voltage V_{bias} applied across the IMOD 12 on the right is sufficient to maintain the movable reflective layer 14 in the actuated position.

[0037] In Figure 1, the reflective properties of pixels 12 are generally illustrated with arrows 13 indicating light incident upon the pixels 12, and light 15 reflecting from the pixel 12 on the left. Although not illustrated in detail, it will be understood by a person having ordinary skill in the art that most of the light 13 incident upon the pixels 12 will be transmitted through the transparent substrate 20, toward the optical stack 16. A portion of the light incident upon the optical stack 16 will be transmitted through the partially reflective layer of the optical stack 16, and a portion will be reflected back through the transparent substrate 20. The portion of light 13 that is transmitted through the optical stack 16 will be reflected at the movable reflective layer 14, back toward (and through) the transparent substrate 20. Interference (constructive or destructive) between the light reflected from the

partially reflective layer of the optical stack 16 and the light reflected from the movable reflective layer 14 will determine the wavelength(s) of light 15 reflected from the pixel 12.

[0038] The optical stack 16 can include a single layer or several layers. The layer(s) can include one or more of an electrode layer, a partially reflective and partially transmissive layer and a transparent dielectric layer. In some implementations, the optical stack 16 is electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or more of the above layers onto a transparent substrate 20. The electrode layer can be formed from a variety of materials, such as various metals, for example indium tin oxide (ITO). The partially reflective layer can be formed from a variety of materials that are partially reflective, such as various metals, e.g., chromium (Cr), semiconductors, and dielectrics. The partially reflective layer can be formed of one or more layers of materials, and each of the layers can be formed of a single material or a combination of materials. In some implementations, the optical stack 16 can include a single semi-transparent thickness of metal or semiconductor which serves as both an optical absorber and conductor, while different, more conductive layers or portions (e.g., of the optical stack 16 or of other structures of the IMOD) can serve to bus signals between IMOD pixels. The optical stack 16 also can include one or more insulating or dielectric layers covering one or more conductive layers or a conductive/absorptive layer.

[0039] In some implementations, the layer(s) of the optical stack 16 can be patterned into parallel strips, and may form row electrodes in a display device as described further below. As will be understood by one having skill in the art, the term “patterned” is used herein to refer to masking as well as etching processes. In some implementations, a highly conductive and reflective material, such as aluminum (Al), may be used for the movable reflective layer 14, and these strips may form column electrodes in a display device. The movable reflective layer 14 may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of the optical stack 16) to form columns deposited on top of posts 18 and an intervening sacrificial material deposited between the posts 18. When the sacrificial material is etched away, a defined gap 19, or optical cavity, can be formed between the movable reflective layer 14 and the optical stack 16. In some implementations, the spacing between posts 18 may be on the order of 1–1000 μm , while the gap 19 may be on the order of $< 10,000$ Angstroms ($\text{\AA}$).

[0040] In some implementations, each pixel of the IMOD, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers. When no voltage is applied, the movable reflective layer 14 remains in a mechanically relaxed state, as illustrated by the pixel 12 on the left in Figure 1, with the gap 19 between the movable reflective layer 14 and optical stack 16. However, when a potential difference, e.g., voltage, is applied to at least one of a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the applied voltage exceeds a threshold, the movable reflective layer 14 can deform and move near or against the optical stack 16. A dielectric layer (not shown) within the optical stack 16 may prevent shorting and control the separation distance between the layers 14 and 16, as illustrated by the actuated pixel 12 on the right in Figure 1. The behavior is the same regardless of the polarity of the applied potential difference. Though a series of pixels in an array may be referred to in some instances as “rows” or “columns,” a person having ordinary skill in the art will readily understand that referring to one direction as a “row” and another as a “column” is arbitrary. Restated, in some orientations, the rows can be considered columns, and the columns considered to be rows. Furthermore, the display elements may be evenly arranged in orthogonal rows and columns (an “array”), or arranged in non-linear configurations, for example, having certain positional offsets with respect to one another (a “mosaic”). The terms “array” and “mosaic” may refer to either configuration. Thus, although the display is referred to as including an “array” or “mosaic,” the elements themselves need not be arranged orthogonally to one another, or disposed in an even distribution, in any instance, but may include arrangements having asymmetric shapes and unevenly distributed elements.

[0041] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display. The electronic device includes a processor 21 that may be configured to execute one or more software modules. In addition to executing an operating system, the processor 21 may be configured to execute one or more software applications, including a web browser, a telephone application, an email program, or any other software application.

[0042] The processor 21 can be configured to communicate with an array driver 22. The array driver 22 can include a row driver circuit 24 and a column driver circuit 26

that provide signals to, e.g., a display array or panel 30. The cross section of the IMOD display device illustrated in Figure 1 is shown by the lines 1–1 in Figure 2. Although Figure 2 illustrates a 3x3 array of IMODs for the sake of clarity, the display array 30 may contain a very large number of IMODs, and may have a different number of IMODs in rows than in columns, and vice versa.

[0043] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1. For MEMS interferometric modulators, the row/column (i.e., common/segment) write procedure may take advantage of a hysteresis property of these devices as illustrated in Figure 3. An interferometric modulator may require, for example, about a 10-volt potential difference to cause the movable reflective layer, or mirror, to change from the relaxed state to the actuated state. When the voltage is reduced from that value, the movable reflective layer maintains its state as the voltage drops back below, e.g., 10-volts, however, the movable reflective layer does not relax completely until the voltage drops below 2-volts. Thus, a range of voltage, approximately 3 to 7-volts, as shown in Figure 3, exists where there is a window of applied voltage within which the device is stable in either the relaxed or actuated state. This is referred to herein as the “hysteresis window” or “stability window.” For a display array 30 having the hysteresis characteristics of Figure 3, the row/column write procedure can be designed to address one or more rows at a time, such that during the addressing of a given row, pixels in the addressed row that are to be actuated are exposed to a voltage difference of about 10-volts, and pixels that are to be relaxed are exposed to a voltage difference of near zero volts. After addressing, the pixels are exposed to a steady state or bias voltage difference of approximately 5-volts such that they remain in the previous strobing state. In this example, after being addressed, each pixel sees a potential difference within the “stability window” of about 3–7-volts. This hysteresis property feature enables the pixel design, e.g., illustrated in Figure 1, to remain stable in either an actuated or relaxed pre-existing state under the same applied voltage conditions. Since each IMOD pixel, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers, this stable state can be held at a steady voltage within the hysteresis window without substantially consuming or losing power. Moreover, essentially little or no current flows into the IMOD pixel if the applied voltage potential remains substantially fixed.

[0044] In some implementations, a frame of an image may be created by applying data signals in the form of “segment” voltages along the set of column electrodes, in accordance with the desired change (if any) to the state of the pixels in a given row. Each row of the array can be addressed in turn, such that the frame is written one row at a time. To write the desired data to the pixels in a first row, segment voltages corresponding to the desired state of the pixels in the first row can be applied on the column electrodes, and a first row pulse in the form of a specific “common” voltage or signal can be applied to the first row electrode. The set of segment voltages can then be changed to correspond to the desired change (if any) to the state of the pixels in the second row, and a second common voltage can be applied to the second row electrode. In some implementations, the pixels in the first row are unaffected by the change in the segment voltages applied along the column electrodes, and remain in the state they were set to during the first common voltage row pulse. This process may be repeated for the entire series of rows, or alternatively, columns, in a sequential fashion to produce the image frame. The frames can be refreshed and/or updated with new image data by continually repeating this process at some desired number of frames per second.

[0045] The combination of segment and common signals applied across each pixel (that is, the potential difference across each pixel) determines the resulting state of each pixel. Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied. As will be readily understood by one having ordinary skill in the art, the “segment” voltages can be applied to either the column electrodes or the row electrodes, and the “common” voltages can be applied to the other of the column electrodes or the row electrodes.

[0046] As illustrated in Figure 4 (as well as in the timing diagram shown in Figure 5B), when a release voltage $V_{C_{REL}}$ is applied along a common line, all interferometric modulator elements along the common line will be placed in a relaxed state, alternatively referred to as a released or unactuated state, regardless of the voltage applied along the segment lines, i.e., high segment voltage V_{S_H} and low segment voltage V_{S_L} . In particular, when the release voltage $V_{C_{REL}}$ is applied along a common line, the potential voltage across the modulator (alternatively referred to as a pixel voltage) is within the relaxation window (see Figure 3, also referred to as a release window) both when the high segment voltage V_{S_H}

and the low segment voltage VS_L are applied along the corresponding segment line for that pixel.

[0047] When a hold voltage is applied on a common line, such as a high hold voltage VC_{HOLD_H} or a low hold voltage VC_{HOLD_L} , the state of the interferometric modulator will remain constant. For example, a relaxed IMOD will remain in a relaxed position, and an actuated IMOD will remain in an actuated position. The hold voltages can be selected such that the pixel voltage will remain within a stability window both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line. Thus, the segment voltage swing, i.e., the difference between the high VS_H and low segment voltage VS_L , is less than the width of either the positive or the negative stability window.

[0048] When an addressing, or actuation, voltage is applied on a common line, such as a high addressing voltage VC_{ADD_H} or a low addressing voltage VC_{ADD_L} , data can be selectively written to the modulators along that line by application of segment voltages along the respective segment lines. The segment voltages may be selected such that actuation is dependent upon the segment voltage applied. When an addressing voltage is applied along a common line, application of one segment voltage will result in a pixel voltage within a stability window, causing the pixel to remain unactuated. In contrast, application of the other segment voltage will result in a pixel voltage beyond the stability window, resulting in actuation of the pixel. The particular segment voltage which causes actuation can vary depending upon which addressing voltage is used. In some implementations, when the high addressing voltage VC_{ADD_H} is applied along the common line, application of the high segment voltage VS_H can cause a modulator to remain in its current position, while application of the low segment voltage VS_L can cause actuation of the modulator. As a corollary, the effect of the segment voltages can be the opposite when a low addressing voltage VC_{ADD_L} is applied, with high segment voltage VS_H causing actuation of the modulator, and low segment voltage VS_L having no effect (i.e., remaining stable) on the state of the modulator.

[0049] In some implementations, hold voltages, address voltages, and segment voltages may be used which always produce the same polarity potential difference across the modulators. In some other implementations, signals can be used which alternate the polarity

of the potential difference of the modulators. Alternation of the polarity across the modulators (that is, alternation of the polarity of write procedures) may reduce or inhibit charge accumulation which could occur after repeated write operations of a single polarity.

[0050] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2. Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A. The signals can be applied to the, e.g., 3x3 array of Figure 2, which will ultimately result in the line time 60e display arrangement illustrated in Figure 5A. The actuated modulators in Figure 5A are in a dark-state, i.e., where a substantial portion of the reflected light is outside of the visible spectrum so as to result in a dark appearance to, e.g., a viewer. Prior to writing the frame illustrated in Figure 5A, the pixels can be in any state, but the write procedure illustrated in the timing diagram of Figure 5B presumes that each modulator has been released and resides in an unactuated state before the first line time 60a.

[0051] During the first line time 60a: a release voltage 70 is applied on common line 1; the voltage applied on common line 2 begins at a high hold voltage 72 and moves to a release voltage 70; and a low hold voltage 76 is applied along common line 3. Thus, the modulators (common 1, segment 1), (1,2) and (1,3) along common line 1 remain in a relaxed, or unactuated, state for the duration of the first line time 60a, the modulators (2,1), (2,2) and (2,3) along common line 2 will move to a relaxed state, and the modulators (3,1), (3,2) and (3,3) along common line 3 will remain in their previous state. With reference to Figure 4, the segment voltages applied along segment lines 1, 2 and 3 will have no effect on the state of the interferometric modulators, as none of common lines 1, 2 or 3 are being exposed to voltage levels causing actuation during line time 60a (i.e., $V_{C_{REL}}$ – relax and $V_{C_{HOLD_L}}$ – stable).

[0052] During the second line time 60b, the voltage on common line 1 moves to a high hold voltage 72, and all modulators along common line 1 remain in a relaxed state regardless of the segment voltage applied because no addressing, or actuation, voltage was applied on the common line 1. The modulators along common line 2 remain in a relaxed state due to the application of the release voltage 70, and the modulators (3,1), (3,2) and (3,3)

along common line 3 will relax when the voltage along common line 3 moves to a release voltage 70.

[0053] During the third line time 60c, common line 1 is addressed by applying a high address voltage 74 on common line 1. Because a low segment voltage 64 is applied along segment lines 1 and 2 during the application of this address voltage, the pixel voltage across modulators (1,1) and (1,2) is greater than the high end of the positive stability window (i.e., the voltage differential exceeded a predefined threshold) of the modulators, and the modulators (1,1) and (1,2) are actuated. Conversely, because a high segment voltage 62 is applied along segment line 3, the pixel voltage across modulator (1,3) is less than that of modulators (1,1) and (1,2), and remains within the positive stability window of the modulator; modulator (1,3) thus remains relaxed. Also during line time 60c, the voltage along common line 2 decreases to a low hold voltage 76, and the voltage along common line 3 remains at a release voltage 70, leaving the modulators along common lines 2 and 3 in a relaxed position.

[0054] During the fourth line time 60d, the voltage on common line 1 returns to a high hold voltage 72, leaving the modulators along common line 1 in their respective addressed states. The voltage on common line 2 is decreased to a low address voltage 78. Because a high segment voltage 62 is applied along segment line 2, the pixel voltage across modulator (2,2) is below the lower end of the negative stability window of the modulator, causing the modulator (2,2) to actuate. Conversely, because a low segment voltage 64 is applied along segment lines 1 and 3, the modulators (2,1) and (2,3) remain in a relaxed position. The voltage on common line 3 increases to a high hold voltage 72, leaving the modulators along common line 3 in a relaxed state.

[0055] Finally, during the fifth line time 60e, the voltage on common line 1 remains at high hold voltage 72, and the voltage on common line 2 remains at a low hold voltage 76, leaving the modulators along common lines 1 and 2 in their respective addressed states. The voltage on common line 3 increases to a high address voltage 74 to address the modulators along common line 3. As a low segment voltage 64 is applied on segment lines 2 and 3, the modulators (3,2) and (3,3) actuate, while the high segment voltage 62 applied along segment line 1 causes modulator (3,1) to remain in a relaxed position. Thus, at the end of the fifth line time 60e, the 3x3 pixel array is in the state shown in Figure 5A, and will

remain in that state as long as the hold voltages are applied along the common lines, regardless of variations in the segment voltage which may occur when modulators along other common lines (not shown) are being addressed.

[0056] In the timing diagram of Figure 5B, a given write procedure (i.e., line times 60a–60e) can include the use of either high hold and address voltages, or low hold and address voltages. Once the write procedure has been completed for a given common line (and the common voltage is set to the hold voltage having the same polarity as the actuation voltage), the pixel voltage remains within a given stability window, and does not pass through the relaxation window until a release voltage is applied on that common line. Furthermore, as each modulator is released as part of the write procedure prior to addressing the modulator, the actuation time of a modulator, rather than the release time, may determine the necessary line time. Specifically, in implementations in which the release time of a modulator is greater than the actuation time, the release voltage may be applied for longer than a single line time, as depicted in Figure 5B. In some other implementations, voltages applied along common lines or segment lines may vary to account for variations in the actuation and release voltages of different modulators, such as modulators of different colors.

[0057] The details of the structure of interferometric modulators that operate in accordance with the principles set forth above may vary widely. For example, Figures 6A–6E show examples of cross-sections of varying implementations of interferometric modulators, including the movable reflective layer 14 and its supporting structures. Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1, where a strip of metal material, i.e., the movable reflective layer 14 is deposited on supports 18 extending orthogonally from the substrate 20. In Figure 6B, the movable reflective layer 14 of each IMOD is generally square or rectangular in shape and attached to supports at or near the corners, on tethers 32. In Figure 6C, the movable reflective layer 14 is generally square or rectangular in shape and suspended from a deformable layer 34, which may include a flexible metal. The deformable layer 34 can connect, directly or indirectly, to the substrate 20 around the perimeter of the movable reflective layer 14. These connections are herein referred to as support posts. The implementation shown in Figure 6C has additional benefits deriving from the decoupling of the optical functions of the movable reflective layer 14 from its mechanical functions, which are carried out by the deformable

layer 34. This decoupling allows the structural design and materials used for the reflective layer 14 and those used for the deformable layer 34 to be optimized independently of one another.

[0058] Figure 6D shows another example of an IMOD, where the movable reflective layer 14 includes a reflective sub-layer 14a. The movable reflective layer 14 rests on a support structure, such as support posts 18. The support posts 18 provide separation of the movable reflective layer 14 from the lower stationary electrode (i.e., part of the optical stack 16 in the illustrated IMOD) so that a gap 19 is formed between the movable reflective layer 14 and the optical stack 16, for example when the movable reflective layer 14 is in a relaxed position. The movable reflective layer 14 also can include a conductive layer 14c, which may be configured to serve as an electrode, and a support layer 14b. In this example, the conductive layer 14c is disposed on one side of the support layer 14b, distal from the substrate 20, and the reflective sub-layer 14a is disposed on the other side of the support layer 14b, proximal to the substrate 20. In some implementations, the reflective sub-layer 14a can be conductive and can be disposed between the support layer 14b and the optical stack 16. The support layer 14b can include one or more layers of a dielectric material, for example, silicon oxynitride (SiON) or silicon dioxide (SiO₂). In some implementations, the support layer 14b can be a stack of layers, such as, for example, a SiO₂/SiON/SiO₂ tri-layer stack. Either or both of the reflective sub-layer 14a and the conductive layer 14c can include, e.g., an aluminum (Al) alloy with about 0.5% copper (Cu), or another reflective metallic material. Employing conductive layers 14a, 14c above and below the dielectric support layer 14b can balance stresses and provide enhanced conduction. In some implementations, the reflective sub-layer 14a and the conductive layer 14c can be formed of different materials for a variety of design purposes, such as achieving specific stress profiles within the movable reflective layer 14.

[0059] As illustrated in Figure 6D, some implementations also can include a black mask structure 23. The black mask structure 23 can be formed in optically inactive regions (e.g., between pixels or under posts 18) to absorb ambient or stray light. The black mask structure 23 also can improve the optical properties of a display device by inhibiting light from being reflected from or transmitted through inactive portions of the display, thereby increasing the contrast ratio. Additionally, the black mask structure 23 can be

conductive and be configured to function as an electrical bussing layer. In some implementations, the row electrodes can be connected to the black mask structure 23 to reduce the resistance of the connected row electrode. The black mask structure 23 can be formed using a variety of methods, including deposition and patterning techniques. The black mask structure 23 can include one or more layers. For example, in some implementations, the black mask structure 23 includes a molybdenum-chromium (MoCr) layer that serves as an optical absorber, a layer, and an aluminum alloy that serves as a reflector and a bussing layer, with a thickness in the range of about 30–80 Å, 500–1000 Å, and 500–6000 Å, respectively. The one or more layers can be patterned using a variety of techniques, including photolithography and dry etching, including, for example, carbon tetrafluoride (CF₄) and/or oxygen (O₂) for the MoCr and SiO₂ layers and chlorine (Cl₂) and/or boron trichloride (BCl₃) for the aluminum alloy layer. In some implementations, the black mask 23 can be an etalon or interferometric stack structure. In such interferometric stack black mask structures 23, the conductive absorbers can be used to transmit or bus signals between lower, stationary electrodes in the optical stack 16 of each row or column. In some implementations, a spacer layer 35 can serve to generally electrically isolate the absorber layer 16a from the conductive layers in the black mask 23.

[0060] Figure 6E shows another example of an IMOD, where the movable reflective layer 14 is self supporting. In contrast with Figure 6D, the implementation of Figure 6E does not include support posts 18. Instead, the movable reflective layer 14 contacts the underlying optical stack 16 at multiple locations, and the curvature of the movable reflective layer 14 provides sufficient support that the movable reflective layer 14 returns to the unactuated position of Figure 6E when the voltage across the interferometric modulator is insufficient to cause actuation. The optical stack 16, which may contain a plurality of several different layers, is shown here for clarity including an optical absorber 16a, and a dielectric 16b. In some implementations, the optical absorber 16a may serve both as a fixed electrode and as a partially reflective layer.

[0061] In implementations such as those shown in Figures 6A–6E, the IMODs function as direct-view devices, in which images are viewed from the front side of the transparent substrate 20, i.e., the side opposite to that upon which the modulator is arranged. In these implementations, the back portions of the device (that is, any portion of the display

device behind the movable reflective layer 14, including, for example, the deformable layer 34 illustrated in Figure 6C) can be configured and operated upon without impacting or negatively affecting the image quality of the display device, because the reflective layer 14 optically shields those portions of the device. For example, in some implementations a bus structure (not illustrated) can be included behind the movable reflective layer 14 which provides the ability to separate the optical properties of the modulator from the electromechanical properties of the modulator, such as voltage addressing and the movements that result from such addressing. Additionally, the implementations of Figures 6A–6E can simplify processing, such as, e.g., patterning.

[0062] Figure 7 shows an example of a flow diagram illustrating a manufacturing process 80 for an interferometric modulator, and Figures 8A–8E show examples of cross-sectional schematic illustrations of corresponding stages of such a manufacturing process 80. In some implementations, the manufacturing process 80 can be implemented to manufacture, e.g., interferometric modulators of the general type illustrated in Figures 1 and 6, in addition to other blocks not shown in Figure 7. With reference to Figures 1, 6 and 7, the process 80 begins at block 82 with the formation of the optical stack 16 over the substrate 20. Figure 8A illustrates such an optical stack 16 formed over the substrate 20. The substrate 20 may be a transparent substrate such as glass or plastic, it may be flexible or relatively stiff and unbending, and may have been subjected to prior preparation processes, e.g., cleaning, to facilitate efficient formation of the optical stack 16. As discussed above, the optical stack 16 can be electrically conductive, partially transparent and partially reflective and may be fabricated, for example, by depositing one or more layers having the desired properties onto the transparent substrate 20. In Figure 8A, the optical stack 16 includes a multilayer structure having sub-layers 16a and 16b, although more or fewer sub-layers may be included in some other implementations. In some implementations, one of the sub-layers 16a, 16b can be configured with both optically absorptive and conductive properties, such as the combined conductor/absorber sub-layer 16a. Additionally, one or more of the sub-layers 16a, 16b can be patterned into parallel strips, and may form row electrodes in a display device. Such patterning can be performed by a masking and etching process or another suitable process known in the art. In some implementations, one of the sub-layers 16a, 16b can be an insulating or dielectric layer, such as sub-layer 16b that is deposited over one or more metal

layers (e.g., one or more reflective and/or conductive layers). In addition, the optical stack 16 can be patterned into individual and parallel strips that form the rows of the display.

[0063] The process 80 continues at block 84 with the formation of a sacrificial layer 25 over the optical stack 16. The sacrificial layer 25 is later removed (e.g., at block 90) to form the cavity 19 and thus the sacrificial layer 25 is not shown in the resulting interferometric modulators 12 illustrated in Figure 1. Figure 8B illustrates a partially fabricated device including a sacrificial layer 25 formed over the optical stack 16. The formation of the sacrificial layer 25 over the optical stack 16 may include deposition of a xenon difluoride (XeF_2)-etchable material such as molybdenum (Mo) or amorphous silicon (a-Si), in a thickness selected to provide, after subsequent removal, a gap or cavity 19 (see also Figures 1 and 8E) having a desired design size. Deposition of the sacrificial material may be carried out using deposition techniques such as physical vapor deposition (PVD, e.g., sputtering), plasma-enhanced chemical vapor deposition (PECVD), thermal chemical vapor deposition (thermal CVD), or spin-coating.

[0064] The process 80 continues at block 86 with the formation of a support structure e.g., a post 18 as illustrated in Figures 1, 6 and 8C. The formation of the post 18 may include patterning the sacrificial layer 25 to form a support structure aperture, then depositing a material (e.g., a polymer or an inorganic material, e.g., silicon oxide) into the aperture to form the post 18, using a deposition method such as PVD, PECVD, thermal CVD, or spin-coating. In some implementations, the support structure aperture formed in the sacrificial layer can extend through both the sacrificial layer 25 and the optical stack 16 to the underlying substrate 20, so that the lower end of the post 18 contacts the substrate 20 as illustrated in Figure 6A. Alternatively, as depicted in Figure 8C, the aperture formed in the sacrificial layer 25 can extend through the sacrificial layer 25, but not through the optical stack 16. For example, Figure 8E illustrates the lower ends of the support posts 18 in contact with an upper surface of the optical stack 16. The post 18, or other support structures, may be formed by depositing a layer of support structure material over the sacrificial layer 25 and patterning portions of the support structure material located away from apertures in the sacrificial layer 25. The support structures may be located within the apertures, as illustrated in Figure 8C, but also can, at least partially, extend over a portion of the sacrificial layer 25. As noted above, the patterning of the sacrificial layer 25 and/or the support posts 18 can be

performed by a patterning and etching process, but also may be performed by alternative etching methods.

[0065] The process 80 continues at block 88 with the formation of a movable reflective layer or membrane such as the movable reflective layer 14 illustrated in Figures 1, 6 and 8D. The movable reflective layer 14 may be formed by employing one or more deposition steps, e.g., reflective layer (e.g., aluminum, aluminum alloy) deposition, along with one or more patterning, masking, and/or etching steps. The movable reflective layer 14 can be electrically conductive, and referred to as an electrically conductive layer. In some implementations, the movable reflective layer 14 may include a plurality of sub-layers 14a, 14b, 14c as shown in Figure 8D. In some implementations, one or more of the sub-layers, such as sub-layers 14a, 14c, may include highly reflective sub-layers selected for their optical properties, and another sub-layer 14b may include a mechanical sub-layer selected for its mechanical properties. Since the sacrificial layer 25 is still present in the partially fabricated interferometric modulator formed at block 88, the movable reflective layer 14 is typically not movable at this stage. A partially fabricated IMOD that contains a sacrificial layer 25 may also be referred to herein as an “unreleased” IMOD. As described above in connection with Figure 1, the movable reflective layer 14 can be patterned into individual and parallel strips that form the columns of the display.

[0066] The process 80 continues at block 90 with the formation of a cavity, e.g., cavity 19 as illustrated in Figures 1, 6 and 8E. The cavity 19 may be formed by exposing the sacrificial material 25 (deposited at block 84) to an etchant. For example, an etchable sacrificial material such as Mo or amorphous Si may be removed by dry chemical etching, e.g., by exposing the sacrificial layer 25 to a gaseous or vaporous etchant, such as vapors derived from solid XeF_2 for a period of time that is effective to remove the desired amount of material, typically selectively removed relative to the structures surrounding the cavity 19. Other etching methods, e.g. wet etching and/or plasma etching, also may be used. Since the sacrificial layer 25 is removed during block 90, the movable reflective layer 14 is typically movable after this stage. After removal of the sacrificial material 25, the resulting fully or partially fabricated IMOD may be referred to herein as a “released” IMOD.

[0067] In certain implementations described herein, optical systems are provided having a transparent substrate, an optical decoupling structure formed over the transparent

substrate, and a reflective display formed over the optical decoupling structure. The transparent substrate can include turning features that have certain characteristics (e.g., shape, dimensions, angled surfaces, surfaces disposed at certain angles) for redirecting light that is propagating in the substrate to a suitable angle for use by the reflective display. The optical decoupling structure can aid in isolating portions of light (that would reflect off of the display at an un-viewable angle) from reaching the display, and such structure can affect light to increase the amount of light that reaches the light turning features thereby increasing brightness of the display. In certain implementations, the optical decoupling structure can include a first antireflective structure, a second antireflective structure, and a gap (or cavity) disposed between the first and second antireflective structures. The gap (e.g., an air gap) creates an interface having a large index of refraction difference on either side of the interface, forming a highly reflective surface for light incident on the interface at a shallow angle, while inclusion of the first and second antireflective layers can reduce Fresnel reflections of light propagating to and from the reflective display. The optical decoupling structure and the reflective display can be formed over the transparent substrate using a thin-film process, thereby avoiding the need for certain manufacturing steps, such as a lamination step for laminating the transparent substrate, the optical decoupling structure, and the reflective display.

[0068] Figure 9 is a flow diagram illustrating one example of a manufacturing process **100** for an optical system. The process **100** starts at block **102**. In block **104**, a first antireflective structure is formed on a transparent substrate. The transparent substrate can include, for example, glass or plastic, and can have a structural rigidity sufficient to support a subsequently fabricated optical decoupling structure and reflective display. Although the process **100** is illustrated as starting at block **102**, the substrate can be subjected to prior preparation processing. For example, the substrate may be cleaned prior to block **102** to facilitate formation of the first antireflective structure. The transparent substrate can include a variety of structures and/or features. For example, in certain implementations the transparent substrate can serve as a light piping slab for a light source, and can include one or more light turning features for directing light propagating in the transparent substrate toward a reflective display.

[0069] The first antireflective structure can be, for example, a thin film stack having one or more layers. The one or more layers can be selected to reduce Fresnel reflections of light incident the boundary between the transparent substrate and a subsequently formed air gap. The first antireflective structure can include alternating layers of a material with a relatively low index of refraction, for example, silicon dioxide (SiO_2), lithium fluoride (LiF), magnesium fluoride (MgF_2), or cerium fluoride (CeF_3) with layers of a relatively high index of refraction, such as titanium dioxide (TiO_2), zinc sulfide (ZnS), aluminum oxide (Al_2O_3), indium tin oxide (ITO), or zirconium dioxide (ZrO_2). Inclusion of a multi-layer structure formed from alternating layers of materials of high and low indices of refraction can aid in enhancing antireflectivity, thereby reducing Fresnel reflections of light incident the boundary between the transparent substrate and a subsequently formed air gap. However, the first antireflective structure need not be a thin film stack. For example, in certain implementations, the first antireflective structure can include microfeatures having a dimension (e.g., length) that is smaller than a wavelength of light reflected by a reflective display, for example, features having a length smaller than about 250 nm.

[0070] With continuing reference to Figure 9, the process **100** continues at block **106**, in which a sacrificial layer is formed over the first antireflective structure. The sacrificial layer is later removed to form a cavity or air gap, as will be discussed below. The formation of the sacrificial layer over the first antireflective structure may include deposition of an etchable material, one example being a fluorine-etchable material such as molybdenum (Mo) or amorphous silicon (Si), in a thickness selected to provide, after subsequent removal, a cavity having the desired size.

[0071] The process **100** illustrated in Figure 9 continues at block **108** with the formation of support posts in the sacrificial layer. The formation of the support posts may include patterning the sacrificial layer to form one or more apertures, and depositing a material, such as magnesium fluoride (MgF_2), lithium fluoride (LiF), or a silicon oxide, such as silicon dioxide (SiO_2), into the apertures using any suitable deposition technique. The support posts can have a rigidity sufficient to support a subsequently fabricated second antireflective structure and reflective display.

[0072] In block **110**, a second antireflective structure is formed over the support posts and the sacrificial layer. The second antireflective structure can be, but need not be,

similar in structure to the first antireflective structure formed in block **104**. The second antireflective structure can be configured to structurally support, after removal of the sacrificial layer, a reflective display formed on a surface of the second antireflective structure opposite the sacrificial layer. Additional details of the second antireflective structure can be as described above with respect to the first antireflective structure.

[0073] The process **100** continues at a block **112**, in which a reflective display is formed on a surface of the second antireflective structure opposite the sacrificial layer. For example, the reflective display can be an interferometric modulator display, and can be formed using, for example, the interferometric modulator array manufacturing processes illustrated in Figures 7–8E.

[0074] In block **114**, the sacrificial layer is removed to form a cavity or an “air gap” between the first and second antireflective structures. In some implementations, one or more other gases can be disposed in the cavity. The air gap may be formed by exposing the sacrificial material deposited at the block **106** to an etchant. For example, an etchable sacrificial material such as molybdenum (Mo), tungsten (W), tantalum (Ta) or polycrystalline or amorphous silicon may be removed by dry chemical etching, for example, by exposing the sacrificial layer to a fluorine-based gaseous or vaporous etchant, such as vapors derived from solid xenon difluoride (XeF₂). The sacrificial layer can be exposed for a period of time that is effective to remove the material, typically selected relative to the structures surrounding the air gap, such as the support posts formed in block **108**. Other selective etching techniques, for example, wet etching and/or plasma etching, also can be used.

[0075] In some implementations, the air gap formed in block **114** and the first and second antireflective structures formed in blocks **104** and **110** collectively form an optical decoupling structure. The optical decoupling structure can be used to isolate light propagating in the transparent substrate from reaching the reflective display, thereby permitting the transparent substrate to function as a light piping slab for a front light of the reflective display. The optical decoupling structure includes first and second antireflective structures for reducing Fresnel reflections of light propagating to and from the reflective display, thereby improving display performance. As described above, the optical decoupling structure is formed on the transparent substrate and the reflective display is formed on the

optical decoupling structure, thereby providing an integrated optical system that can have improved optical performance and/or a more integrated manufacturing process.

[0076] The process **100** illustrated in Figure 9 ends at **116**. Additional processing may be employed before, in the middle of, or after the illustrated sequence, but are omitted for simplicity. Additionally, in certain implementations, the order in which the blocks are performed can be rearranged.

[0077] Although the process **100** is described as forming support posts and a cavity between the first and second antireflective structures, in certain implementations, other decoupling structures can be used. For example, in certain implementations the process of making the support posts formed in block **108** and the cavity formed in block **114** can be omitted, instead using other layers having an index of refraction less than that of the transparent substrate, including, for example, a silicon dioxide (SiO_2) layer, a fluorine (F) or carbon (C) doped silicon oxide layer, and/or a fluoride layer, such as magnesium fluoride (MgF_2).

[0078] Figures 10A–10K show examples of cross-sectional schematic illustrations of various stages in manufacturing an interferometric modulator. Figure 10A illustrates a substrate **20**. The substrate **20** can include any transparent polymeric material which permits images to be viewed through the substrate **20**, such as glass or plastic. The substrate **20** can have a thickness suitable for supporting an optical decoupling structure and a reflective display. In some implementations, the substrate **20** has a thickness ranging between about 200 μm to about 1,000 μm .

[0079] The substrate **20** can include one or more turning features **120**, which turn light propagating through the substrate **20**. For example, the turning features **120** can be used to direct light propagating in the transparent substrate **20** toward a reflective display. In one implementation, the turning features **120** include facets, which can be formed using any suitable manufacturing technique, including, for example, photolithography and etching.

[0080] Although Figures 10A–10K are shown as including the turning features **120**, a person having ordinary skill in the art will recognize that the methods for providing optical decoupling described herein can be equally applicable to processes lacking turning features **120**. Additionally, in certain implementations, the turning features **120** can be

formed on the substrate **20** at a different point in the manufacturing process, including, for example, after depositing one or more antireflective structures.

[0081] In Figure 10B, a first antireflective structure **122** has been formed on a first surface **121** of the substrate **20**. The first antireflective structure **122** can include one or more thin film layers configured to reduce reflection of light incident on the first surface **121** of the substrate **20**. The first antireflective structure **122** can include any suitable material, including, for example, silicon dioxide (SiO_2), or magnesium fluoride (MgF_2). The first antireflective structure can be a multi-layer stack, such as a stack including silicon dioxide, zinc sulfide (ZnS), magnesium fluoride, or titanium dioxide (TiO_2). In some implementations, the first antireflective structure **122** has a thickness ranging between about $0.1\ \mu\text{m}$ to about $5\ \mu\text{m}$.

[0082] The first antireflective structure **122** can include one or more microfeatures to aid in reducing reflections of light. For example, providing a structure having microfeatures smaller than the wavelength of visible light can aid in preventing reflections of light arriving at the boundary of the transparent substrate **20** and a subsequently formed air gap. One implementation of an antireflective structure employing microfeatures is described below with reference to Figure 12.

[0083] Figure 10C illustrates providing and patterning a sacrificial layer **125** over the first antireflective structure **122**. The sacrificial layer **125** is later removed to form an air gap for optically decoupling the transparent substrate **20** from a reflective display. The formation of the sacrificial layer **125** over the first antireflective structure **122** can include a deposition step, such as a deposition of an etchable sacrificial material, for example, molybdenum (Mo), tungsten (W), tantalum (Ta), polycrystalline or amorphous silicon, germanium (Ge), silicon dioxide (SiO_2), silicon nitride (Si_3N_4), silicon oxynitride (SiON), or organic polymer materials. The sacrificial layer **125** can be patterned in any suitable manner, including one or more masking, and/or etching steps. The sacrificial layer **125** can be patterned to form support post apertures.

[0084] Still referring to Figure 10C, the sacrificial layer **125** can be deposited to have a thickness to form an air gap of the desired size (after the sacrificial layer is removed). In some implementations, the sacrificial layer has a thickness greater than about $1\ \mu\text{m}$, for example, a thickness ranging between about $1\ \mu\text{m}$ to about $50\ \mu\text{m}$. Providing a sacrificial

layer having a thickness greater than about 1 μm can lead to a formation of an air gap or cavity having a height greater than about 1 μm , which can aid in preventing a portion of light from crossing the air gap due to a variety of reasons, such as total internal reflection. For example, light reaching the boundary between the first antireflective structure and the air gap can have an electric field with a magnitude that exponentially decays with distance into the air gap. Thus, increasing the size of an air gap can aid in improving the optical isolation provided by the air gap.

[0085] In Figure 10D, support posts **126** have been formed in the apertures of the sacrificial layer **125** formed in Figure 10C. The support posts **126** can include a variety of materials, including, for example, magnesium fluoride (MgF_2), lithium fluoride (LiF), silicon dioxide (SiO_2) or silicon nitride (Si_3N_4). The support posts **126** can be optically transparent. However, in certain implementations, such as in implementations where the support posts **126** are disposed in optically inactive regions of the reflective display, such as pixel corners or edges, the support posts need not be optically transparent. The support posts **126** can have any suitable shape when viewed from above the transparent substrate **20**, including, for example, a shape that is circular, square, rectangular, hexagonal, and/or octagonal. In some implementations, such supporting structure can be configured as support rails. The support posts **126** can have a size and/or number sufficient for supporting a subsequently fabricated second antireflective structure and reflective display. For example, a density of the support posts **126** can be selected to be in the range of about 15 support posts per μm^2 to about 1,500 support posts per μm^2 .

[0086] In Figure 10E, a second antireflective structure **132** has been formed over the sacrificial layer **125** and the support posts **126**. The second antireflective structure **132** can include one or more thin film layers configured to reduce reflection of light that is incident on the boundary of the second antireflective structure **132** and the air gap (e.g., air gap **139** in Figure 10K) formed after the removal of the sacrificial layer **125**. The second antireflective structure **132** can include one or more of a variety of layers, including, for example, layers of silicon dioxide (SiO_2), magnesium fluoride (MgF_2), and/or zinc sulfide (ZnS). The second antireflective structure **132** can have a thickness sufficient to support a reflective display, such as an interferometric modulator display. In one implementation, the second antireflective structure **132** has a thickness ranging between about 0.25 μm to about

5.0 μm . The second antireflective structure **132** can include microfeatures disposed on its surface facing the first antireflective structure **122** to increase its antireflectivity. The first antireflective structure **122**, the support posts **126**, the air gap **139** (to be formed after the removal of the sacrificial layer **125** as shown in Figure 10K) and the second antireflective structure **132** collectively form an optically decoupling layer on the substrate **20** in some implementations.

[0087] Figures 10F–10J illustrate an example method of forming an interferometric modulator over the second antireflective structure **132**. Figure 10F illustrates forming an optical stack **16** over the second antireflective structure **132**. Formation of the optical stack **16** can include a prior preparation step, such as a cleaning step for cleaning a surface of the second antireflective structure **132** used for forming the optical stack **16**. In Figure 10G, a sacrificial layer **25** is provided over the optical stack **16** and patterned to form apertures. In Figure 10H, posts **18** are formed in the apertures of the sacrificial layer **25**. Figure 10I illustrates forming a mechanical layer **14** over the posts **18** and the sacrificial layer **25**. Although the posts **18** are illustrated as being unaligned with the support posts **126**, in certain implementations, the posts **18** of the interferometric modulator and the support posts **126** of the optical decoupling layer can be aligned. In Figure 10J, the sacrificial layer **25** is removed to form a gap **19**. Additional details of Figures 10F–10K can be similar to those described above with reference to Figures 7–8E.

[0088] In Figure 10K, the sacrificial layer **125** of Figure 10J is removed to form an air gap **139**. The sacrificial layer **125** may be removed by dry chemical etching, for example, by exposing the sacrificial layer **125** to a fluorine-based gaseous or vaporous etchant for a period of time that is effective to remove the material. The etch chemistry used to remove the sacrificial layer **125** is typically selectively non-destructive (or not significantly destructive) to the support posts **126**. Other etching methods, for example, wet etching and/or plasma etching, also can be used.

[0089] In certain implementations, the sacrificial layer **125** can be removed before the interferometric modulator is completely formed. For example, the sacrificial layers **25**, **125** can be removed together, or the sacrificial layer **125** can be removed before forming the optical stack **16**.

[0090] Figure 11 shows an example of a cross-section of one implementation of an optical system. The optical system includes the transparent substrate **20**, turning features **120** disposed in the substrate **20**, and a first antireflective structure **122** positioned along the substrate **20**. The optical system includes a second antireflective structure **132** having a first surface **141** disposed facing the first antireflective surface **122**, and a second surface **143** disposed opposite the first surface. The optical system further includes support posts **126** disposed between and separating the first antireflective structure **122** and the second antireflective structure **132**. The optical system further includes a gap **139** (e.g., an air gap) between the first antireflective structure **122** and the second antireflective structure **132**. The optical system further includes a reflective display **150**, and a light source **149**. The illustrated first antireflective structure **122** is disposed on a first surface of the transparent substrate **20**, and includes a plurality of layers. The transparent substrate **20** further includes a second surface that can be configured to receive ambient light, and which can be used for viewing the reflective display **150**. The support posts **126** are positioned between the first antireflective structure **122** and the second antireflective structure **132**, and the support posts **126** can define a size (e.g., height) of the air gap **139**. The illustrated second antireflective structure **132** is formed from a plurality of layers, and includes a first surface facing the air gap **139** and a second surface opposite the first surface. The reflective display **150** has been formed on the second surface of the second antireflective structure **132**. The reflective display **150** can be any suitable reflective display, including, for example, an interferometric modulator.

[0091] Only a portion of light that propagates through the substrate **20** may be useful for the reflective display **150**. For example, light propagating through the transparent substrate **20** can have an angle θ with respect to the boundary between the transparent substrate **20** and the first antireflective structure **122**, and a portion of light suitable for use by the display **150** can have, for example, an angle θ ranging between about $+45^\circ$ to about -45° . The light turning features **120** of the transparent substrate **20** can aid in redirecting light traveling at an unsuitable angle to an angle suitable for use by the reflective display **150**.

[0092] A portion of light **144** can travel through the transparent substrate **20** and can reach the reflective display **150**. The first and second antireflective structures **122**, **132** can aid in reducing Fresnel reflections associated with light incident the air gap **139**. For

example, the first antireflective structure **122** can aid in reducing Fresnel reflections of the light **144** when the light **144** reaches the boundary between the transparent substrate **20** and the air gap **139**. Similarly, the second antireflective structure **132** can aid in reducing Fresnel reflections of the light **144** when the light **144** arrives at the boundary between the air gap **139** and the reflective display **150**. The illustrated first and second antireflective structures **122**, **132** each include three layers. In one implementation, the first and second antireflective structures **122**, **132** each are a silicon dioxide (SiO₂)/titanium dioxide (TiO₂)/SiO₂ tri-layer stack. In another implementation, the first and second antireflective structures **122**, **132** each are a tri-layer stack, for example, a TiO₂/SiO₂/TiO₂ tri-layer stack. However, the first and second antireflective structures **122**, **132** can be formed from more or fewer layers, including, for example, a five layer stack employing alternating layers of SiO₂ and TiO₂.

[0093] To aid in illuminating the reflective display **150**, the light source **149** can be provided. For example, the light source **149** can be included in the optical system and selectively activated in low-light conditions. The light source **149** can include a variety of light sources, including, for example, an incandescent bulb, an edge bar, a light emitting diode (“LED”), a fluorescent lamp, an LED light bar, an array of LEDs, and/or any other suitable light source.

[0094] Light **140** from the light source **149** can be injected into transparent substrate **20**, and a portion of the light **140** can propagate through the transparent substrate **20** at a relatively shallow angle ϕ with respect to the surface of the transparent substrate **20**, such that the light is reflected within the transparent substrate **20** by total internal reflection. As illustrated in Figure 11, the air gap **139** can aid in isolating the portion of light **140** from reaching the reflective display **150** by providing a boundary for total internal reflection of the light **140**. Since the air gap **139** has a low index of refraction, the air gap **139** can be used to provide improved optical isolation. By retaining the portion of light **140** within the substrate **20** by total internal reflection, the portion of light **140** can be redirected by the turning features **120** to become a portion of light **142** that is directed towards the display **150**. Thus, inclusion of the air gap **139** can aid in preventing light from escaping the transparent substrate **20** before reaching the turning features **120**, thereby improving brightness of the reflective display **150**.

[0095] Although Figure 11 is illustrated as including support posts **126** and gaps **139** between the first and second antireflective structures **122**, **132**, in certain implementations, other structures for decoupling can be used. For example, in certain implementations, one or more other layers having an index of refraction less than the transparent substrate **20** can be disposed between the first and second antireflective structures **122**, **132** to form a decoupling structure. The decoupling structure may include, for example, one or more layers of silicon dioxide (SiO_2), fluorine (F) or carbon (C) doped silicon oxide, and/or fluoride, such as magnesium fluoride (MgF_2).

[0096] Figure 12 shows an example of a cross-section of one implementation of an antireflective structure **152** having microfeatures **153**. The microfeatures **153** can have a length d , which can be selected to be less than a wavelength of visible light. For example, in one implementation, the length d is selected to be less than a wavelength of at least one of red, green and blue light. As persons having ordinary skill in the art will appreciate, the microfeatures **153** can aid in reducing light reflections. Thus, the microfeatures **153** can be used as the first and/or second antireflective structure **122**, **132**. Additionally, although a moth eye configuration of the microfeatures **153** is illustrated, the antireflective structure **152** can include any other suitable configuration of microfeatures for serving as an antireflective structure, including, for example, periodic or non-periodic structures, and/or implementations having shapes different than that illustrated in Figure 12.

[0097] Figures 13A and 13B show examples of system block diagrams illustrating a display device **40** that includes a plurality of interferometric modulators. The display device **40** can be, for example, a cellular or mobile telephone. However, the same components of the display device **40** or slight variations thereof are also illustrative of various types of display devices such as televisions, e-readers and portable media players.

[0098] The display device **40** includes a housing **41**, a display **30**, an antenna **43**, a speaker **45**, an input device **48**, and a microphone **46**. The housing **41** can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum forming. In addition, the housing **41** may be made from any of a variety of materials, including, but not limited to: plastic, metal, glass, rubber, and ceramic, or a combination thereof. The housing **41** can include removable portions (not shown) that may be

interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0099] The display **30** may be any of a variety of displays, including a bi-stable or analog display, as described herein. The display **30** also can be configured to include a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD, or a non-flat-panel display, such as a CRT or other tube device. In addition, the display **30** can include an interferometric modulator display, as described herein.

[0100] The components of the display device **40** are schematically illustrated in Figure 13B. The display device **40** includes a housing **41** and can include additional components at least partially enclosed therein. For example, the display device **40** includes a network interface **27** that includes an antenna **43** which is coupled to a transceiver **47**. The transceiver **47** is connected to a processor **21**, which is connected to conditioning hardware **52**. The conditioning hardware **52** may be configured to condition a signal (e.g., filter a signal). The conditioning hardware **52** is connected to a speaker **45** and a microphone **46**. The processor **21** is also connected to an input device **48** and a driver controller **29**. The driver controller **29** is coupled to a frame buffer **28**, and to an array driver **22**, which in turn is coupled to a display array **30**. A power supply **50** can provide power to all components as required by the particular display device **40** design.

[0101] The network interface **27** includes the antenna **43** and the transceiver **47** so that the display device **40** can communicate with one or more devices over a network. The network interface **27** also may have some processing capabilities to relieve, e.g., data processing requirements of the processor **21**. The antenna **43** can transmit and receive signals. In some implementations, the antenna **43** transmits and receives RF signals according to the IEEE 16.11 standard, including IEEE 16.11(a), (b), or (g), or the IEEE 802.11 standard, including IEEE 802.11a, b, g or n. In some other implementations, the antenna **43** transmits and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna **43** is designed to receive code division multiple access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM), GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized (EV-DO), 1xEV-DO,

EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within a wireless network, such as a system utilizing 3G or 4G technology. The transceiver **47** can pre-process the signals received from the antenna **43** so that they may be received by and further manipulated by the processor **21**. The transceiver **47** also can process signals received from the processor **21** so that they may be transmitted from the display device **40** via the antenna **43**.

[0102] In some implementations, the transceiver **47** can be replaced by a receiver. In addition, the network interface **27** can be replaced by an image source, which can store or generate image data to be sent to the processor **21**. The processor **21** can control the overall operation of the display device **40**. The processor **21** receives data, such as compressed image data from the network interface **27** or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor **21** can send the processed data to the driver controller **29** or to the frame buffer **28** for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation, and gray-scale level.

[0103] The processor **21** can include a microcontroller, CPU, or logic unit to control operation of the display device **40**. The conditioning hardware **52** may include amplifiers and filters for transmitting signals to the speaker **45**, and for receiving signals from the microphone **46**. The conditioning hardware **52** may be discrete components within the display device **40**, or may be incorporated within the processor **21** or other components.

[0104] The driver controller **29** can take the raw image data generated by the processor **21** either directly from the processor **21** or from the frame buffer **28** and can re-format the raw image data appropriately for high speed transmission to the array driver **22**. In some implementations, the driver controller **29** can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array **30**. Then the driver controller **29** sends the formatted information to the array driver **22**. Although a driver controller **29**, such as an LCD controller, is often associated with the system processor **21** as a stand-alone Integrated Circuit (IC), such

controllers may be implemented in many ways. For example, controllers may be embedded in the processor **21** as hardware, embedded in the processor **21** as software, or fully integrated in hardware with the array driver **22**.

[0105] The array driver **22** can receive the formatted information from the driver controller **29** and can re-format the video data into a parallel set of waveforms that are applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of pixels.

[0106] In some implementations, the driver controller **29**, the array driver **22**, and the display array **30** are appropriate for any of the types of displays described herein. For example, the driver controller **29** can be a conventional display controller or a bi-stable display controller (e.g., an IMOD controller). Additionally, the array driver **22** can be a conventional driver or a bi-stable display driver (e.g., an IMOD display driver). Moreover, the display array **30** can be a conventional display array or a bi-stable display array (e.g., a display including an array of IMODs). In some implementations, the driver controller **29** can be integrated with the array driver **22**. Such an implementation is common in highly integrated systems such as cellular phones, watches and other small-area displays.

[0107] In some implementations, the input device **48** can be configured to allow, e.g., a user to control the operation of the display device **40**. The input device **48** can include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, or a pressure- or heat-sensitive membrane. The microphone **46** can be configured as an input device for the display device **40**. In some implementations, voice commands through the microphone **46** can be used for controlling operations of the display device **40**.

[0108] The power supply **50** can include a variety of energy storage devices as are well known in the art. For example, the power supply **50** can be a rechargeable battery, such as a nickel-cadmium battery or a lithium-ion battery. The power supply **50** also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or solar-cell paint. The power supply **50** also can be configured to receive power from a wall outlet.

[0109] In some implementations, control programmability resides in the driver controller **29** which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver **22**. The above-

described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0110] The various illustrative logics, logical blocks, modules, circuits and algorithm steps described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and steps described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0111] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular steps and methods may be performed by circuitry that is specific to a given function.

[0112] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by, or to control the operation of, data processing apparatus.

[0113] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the disclosure is not intended to be limited to the implementations shown herein, but is to be accorded the widest scope consistent with the claims, the principles and the novel features disclosed herein. The word “exemplary” is used exclusively herein to mean “serving as an example, instance, or illustration.” Any implementation described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other implementations. Additionally, a person having ordinary skill in the art will readily appreciate, the terms “upper” and “lower” are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of the IMOD as implemented.

[0114] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0115] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring

such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

CLAIMS

What is claimed is:

1. An optical system comprising:
 - a substrate transmissive to visible light, the substrate having a first surface exposed to receive ambient light and a second surface;
 - a first antireflective structure disposed on the second surface of the substrate;
 - a second antireflective structure having a first surface and a second surface opposite the first surface of the second antireflective structure, the first surface of the second antireflective structure disposed facing the first antireflective structure, wherein the first antireflective structure and the second antireflective structure define at least one cavity in between;
 - a plurality of support posts disposed between the first antireflective structure and the second antireflective structure, the plurality of support posts separating the first antireflective structure and the second antireflective structure at a distance that defines a height of the at least one cavity; and
 - a reflective display disposed on the second surface of the second antireflective structure.
2. The optical system of claim 1, wherein the substrate includes at least one light turning feature configured to direct light propagating in the substrate and incident on the light turning feature toward the reflective display.
3. The optical system of claim 1, wherein the first antireflective structure comprises a plurality of antireflective layers.
4. The optical system of claim 1, wherein the first antireflective structure includes at least one of silicon dioxide (SiO₂) and zinc sulfide (ZnS).
5. The optical system of claim 4, wherein the first antireflective structure is between about 0.1 μm to about 5 μm thick.

6. The optical system of claim 1, wherein the substrate is between about 200 μm to about 1,000 μm thick.
7. The optical system of claim 1, wherein the at least one cavity contains air and has a height of between about 1 μm to about 50 μm .
8. The optical system of claim 1, wherein the support posts comprise at least one of magnesium fluoride (MgF_2), lithium fluoride (LiF), and a silicon oxide.
9. The optical system of claim 1, wherein the plurality of support posts are transparent to visible light.
10. The optical system of claim 1, wherein the plurality of support posts are disposed to have a spatial density of between about 15 support posts per μm^2 and about 1,500 support posts per μm^2 .
11. The optical system of claim 1, wherein the first antireflective structure, the second antireflective structure, and the at least one cavity have indices of refraction selected to substantially allow light having an angle of incidence ranging between about -45 degrees to about 45 degrees with respect to a normal of the first surface of the substrate to pass.
12. The optical system of claim 1, wherein the reflective display includes an interferometric modulator display.
13. The optical system of claim 12, wherein the interferometric modulator display includes an optical stack, a stationary electrode disposed on the optical stack, and a support structure for supporting a movable reflective layer over the optical stack.

14. The optical system of claim 13, further comprising a bias circuit configured to apply a voltage across the movable reflective layer and the electrode that is sufficient to actuate the reflective layer.

15. The optical system of claim 1, further comprising:
a processor that is configured to communicate with said reflective display, said processor being configured to process image data; and
a memory device that is configured to communicate with said processor.

16. The optical system of claim 15, further comprising a driver circuit configured to send at least one signal to said reflective display.

17. The optical system of claim 16, further comprising a controller configured to send at least a portion of said image data to said driver circuit.

18. The optical system of claim 17, further comprising an image source module configured to send said image data to said processor.

19. A method of making an optical system, the method comprising:
forming an antireflective structure on a first surface of a transparent substrate;
depositing a sacrificial layer over the first antireflective structure;
forming a plurality of openings in the sacrificial layer;
forming a plurality of support posts in the plurality of openings;
depositing a second antireflective structure over the plurality of support posts, the second antireflective structure having a first surface and a second surface, the first surface being disposed facing the first antireflective structure;
forming a reflective display on the second surface of the second antireflective structure; and
removing the sacrificial layer to form at least one cavity between the first antireflective structure and the second antireflective structure, wherein the plurality of support posts support the second antireflective structure and separate the first

antireflective structure and the second antireflective structure at a distance that defines a height of the at least one cavity.

20. The method of claim 19, further comprising forming turning features on a second surface of the transparent substrate, the second surface opposite the first surface.

21. The method of claim 19, further comprising positioning a light source relative to the substrate such that light provided by the light source can propagate into the substrate through an edge surface of the substrate.

22. The method of claim 19, wherein forming a reflective display on the second surface of the second antireflective structure comprises:

- depositing an optical stack on the second surface of the second antireflective structure;

- depositing a second sacrificial layer over the optical stack;

- forming a support structure over the optical stack;

- depositing a movable reflective layer over the support structure; and

- removing the second sacrificial layer to form a second cavity.

23. The method of claim 22 further comprising coupling the movable reflective layer and the optical stack to a bias circuit configured to apply a bias voltage to the optical stack and the movable reflective layer.

24. An optical system comprising:

- a transparent substrate having a first surface and a second surface, the first surface exposed to receive ambient light;

- a first means for preventing reflections disposed on the second surface of the transparent substrate;

- a second means for preventing reflections;

- a means for decoupling disposed between the first and second reflection preventing means; and

a reflective display formed on a surface of the second reflection preventing means such that the second reflection preventing means is between the reflective display and the decoupling means.

25. The optical system of claim 24, wherein the decoupling means includes a means for supporting the second reflection preventing means and separating the second reflection preventing means from the first reflection preventing means, wherein the first reflection preventing means and the second reflection preventing means define at least one cavity therebetween.

26. The optical system of claim 24, wherein the decoupling means includes at least one of a silicon dioxide (SiO_2) layer, a fluorine doped silicon oxide layer, a carbon doped silicon oxide layer, and a fluoride layer.

27. The optical system of claim 24, wherein the first reflection preventing means includes a first antireflective structure including a plurality of antireflective layers.

28. The optical system of claim 24, wherein the second reflection preventing means includes a second antireflective structure including a plurality of antireflective layers.

29. The optical system of claim 24, wherein the supporting means includes a plurality of transparent support posts.

30. The optical system of claim 24, wherein the reflective display includes an array of interferometric modulators.

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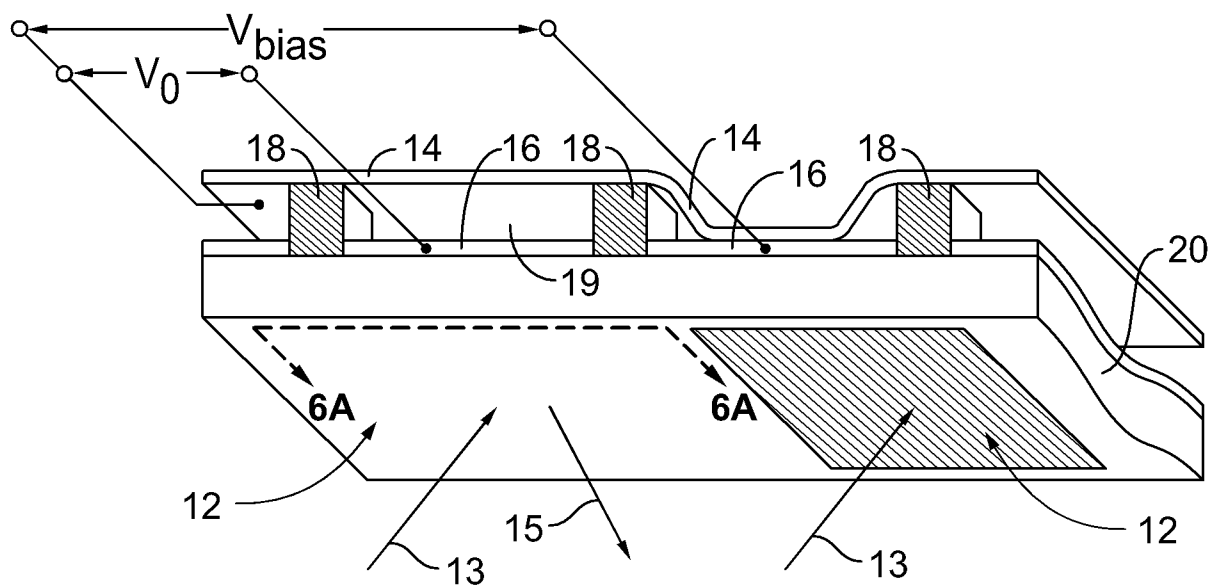


Figure 1

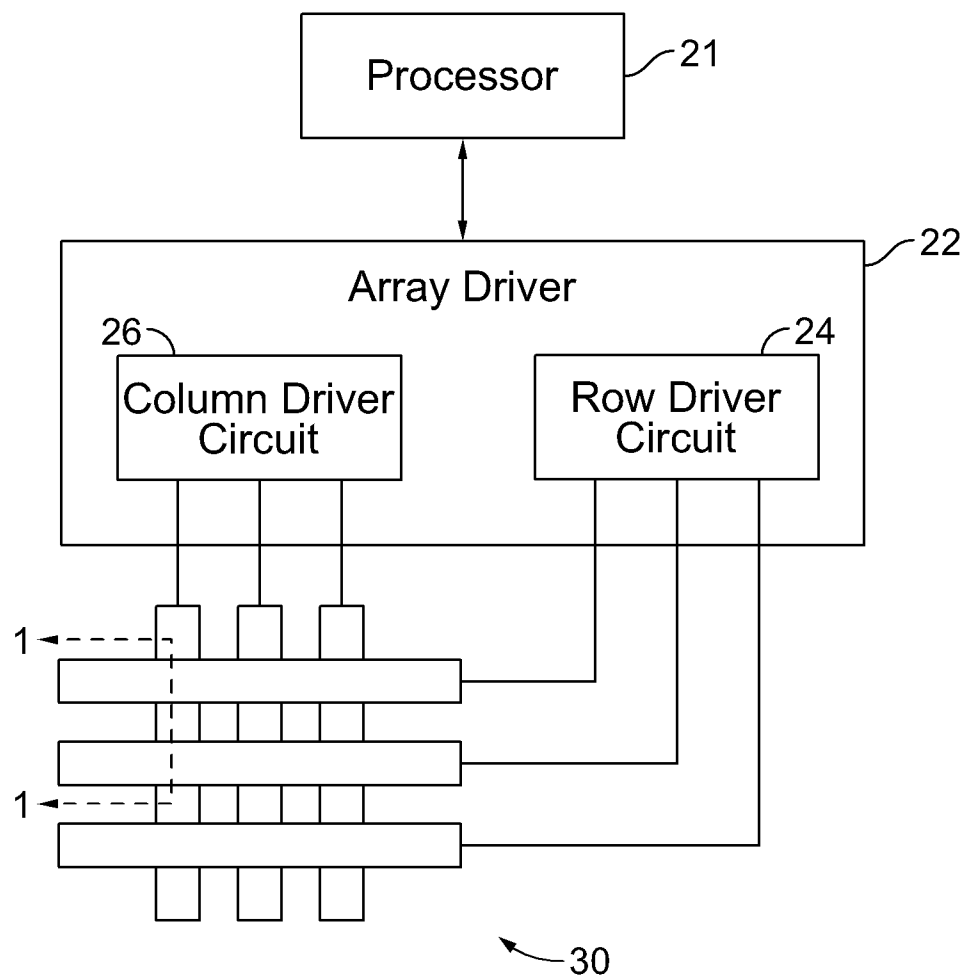


Figure 2

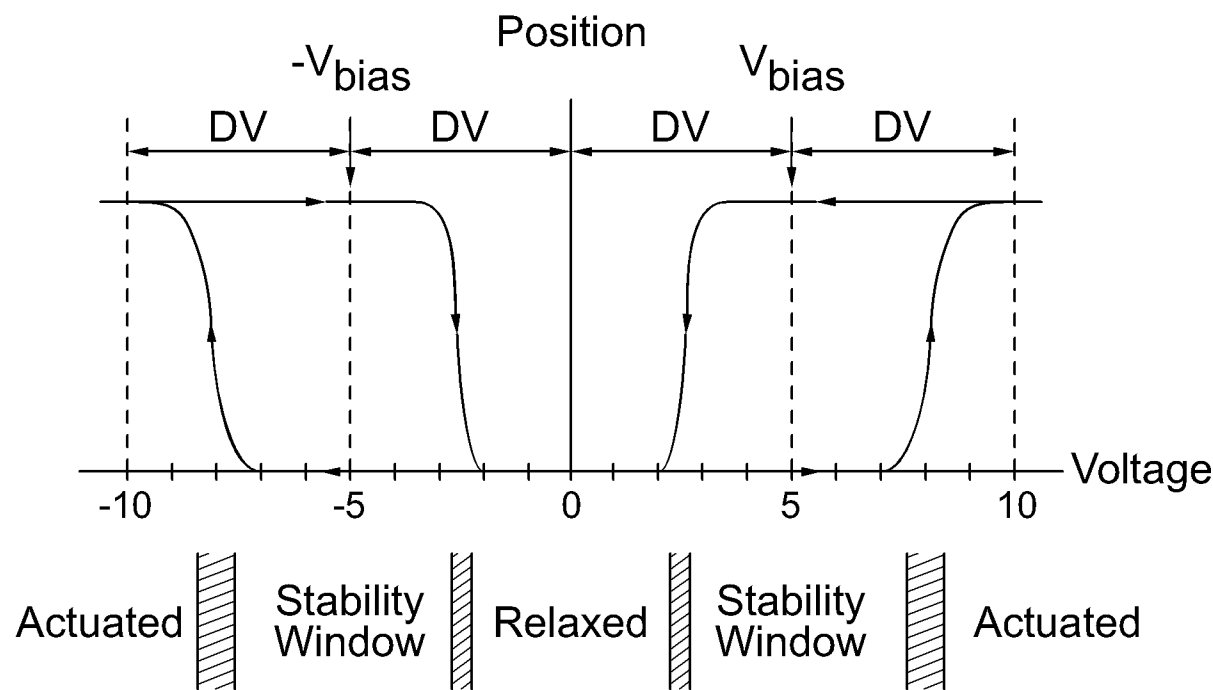


Figure 3

Common Voltages						
Segment Voltages		V _{CADD_H}	V _{CHOLD_H}	V _{CREL}	V _{CHOLD_L}	V _{CADD_L}
	V _{SH}	Stable	Stable	Relax	Stable	Actuate
	V _{SL}	Actuate	Stable	Relax	Stable	Stable

Figure 4

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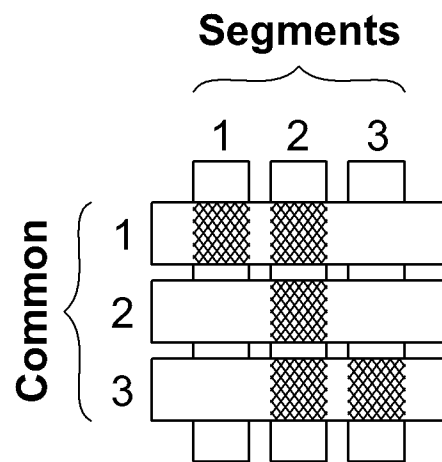


Figure 5A

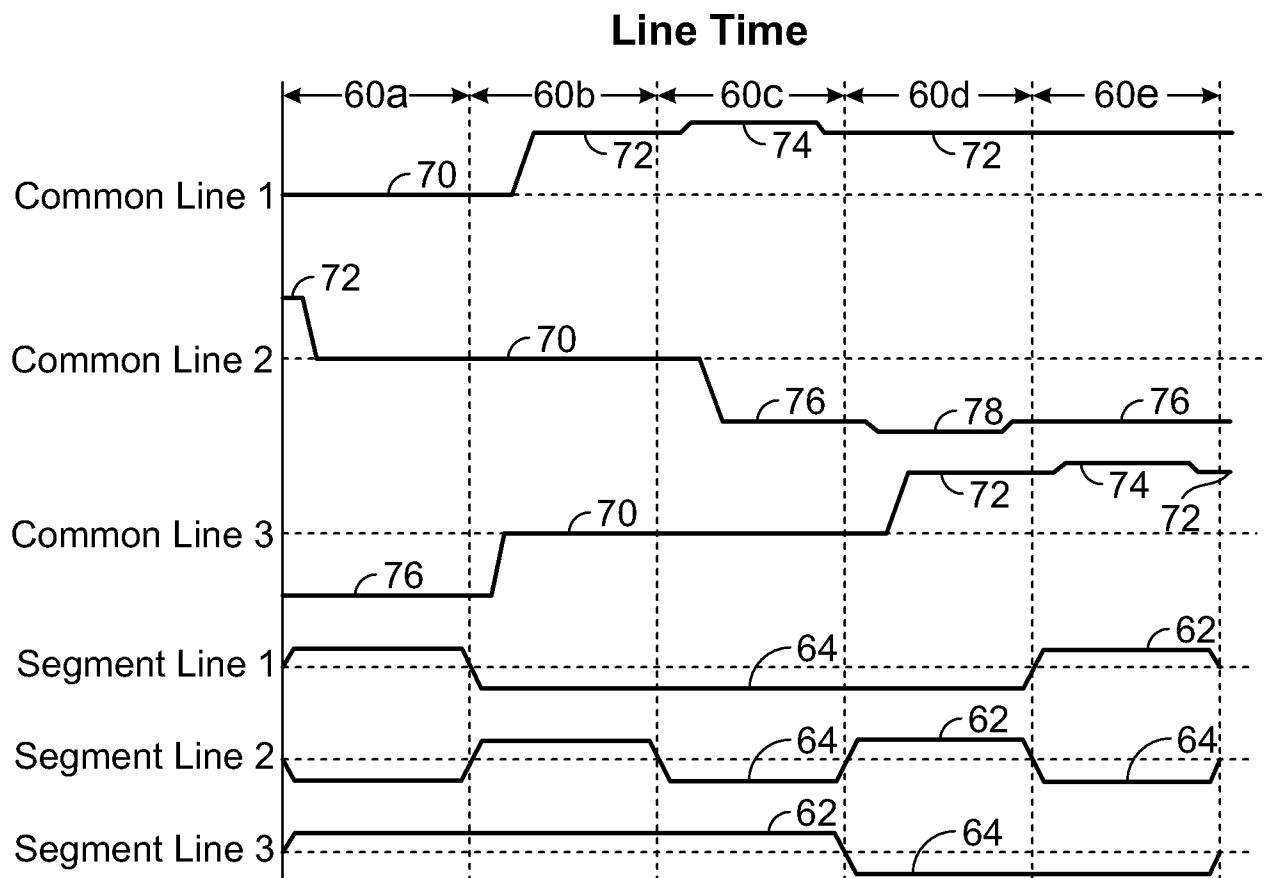


Figure 5B

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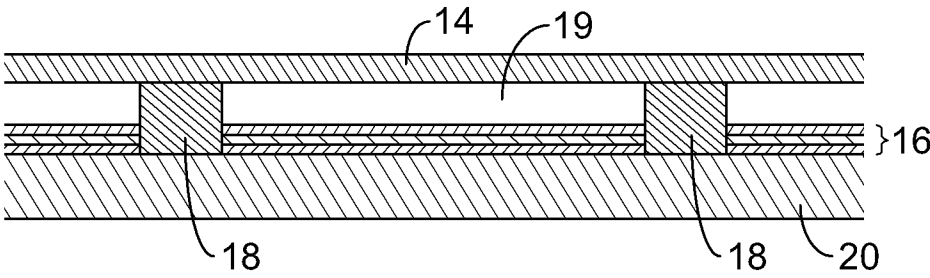


Figure 6A

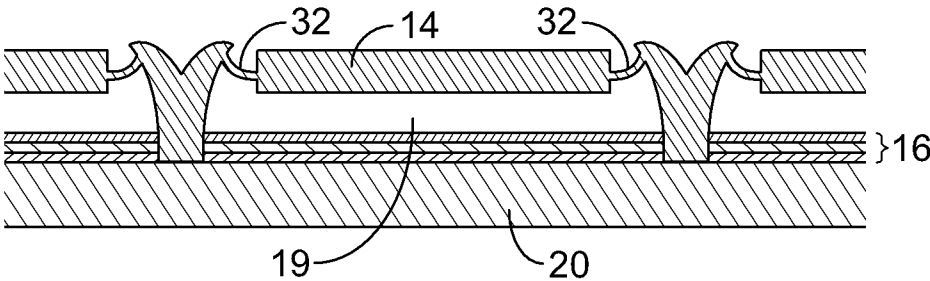


Figure 6B

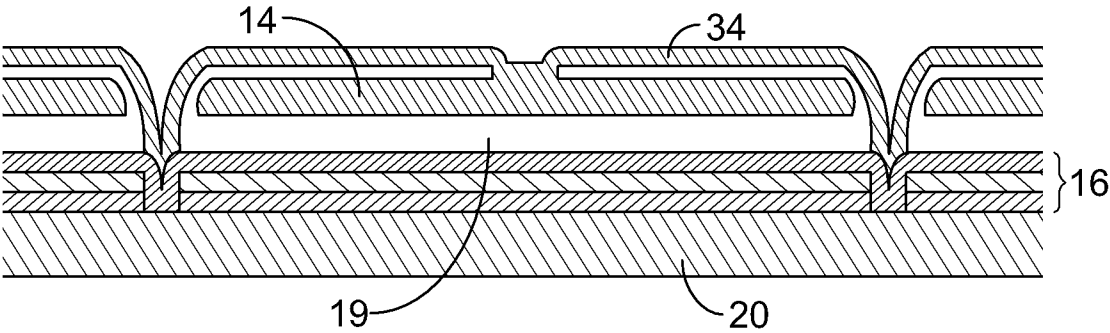


Figure 6C

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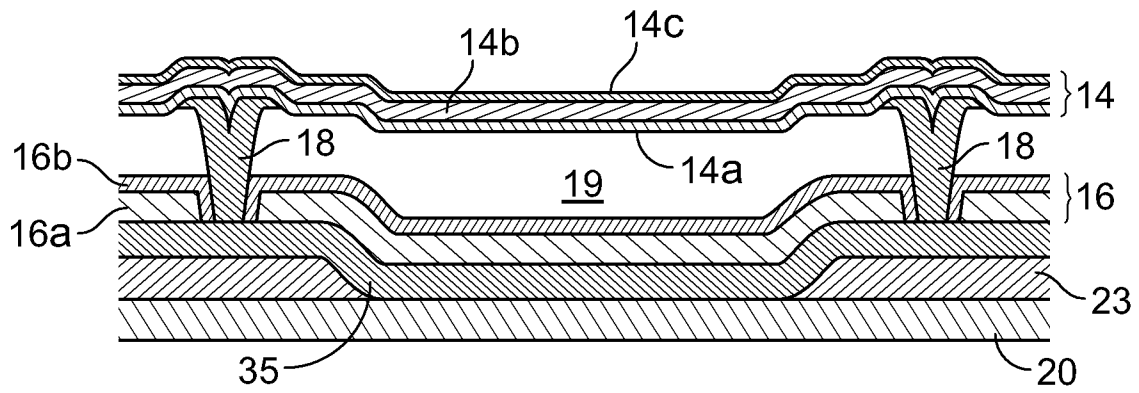


Figure 6D

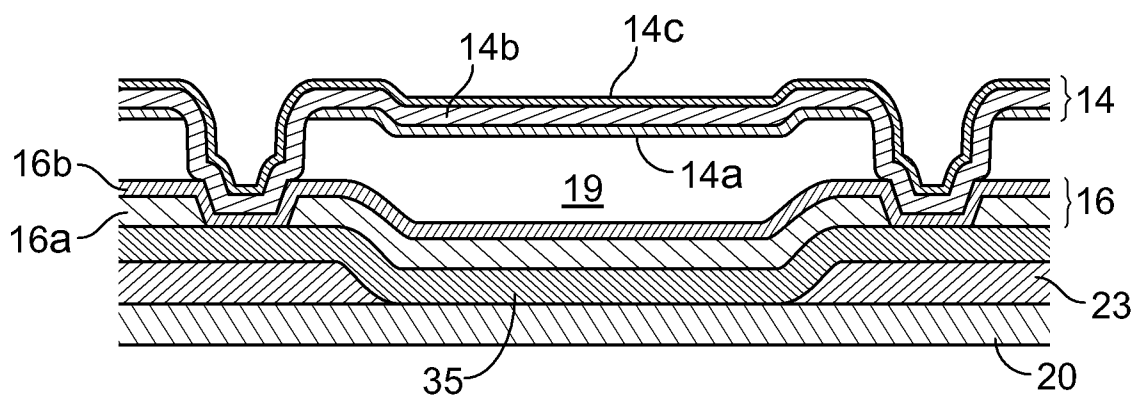


Figure 6E

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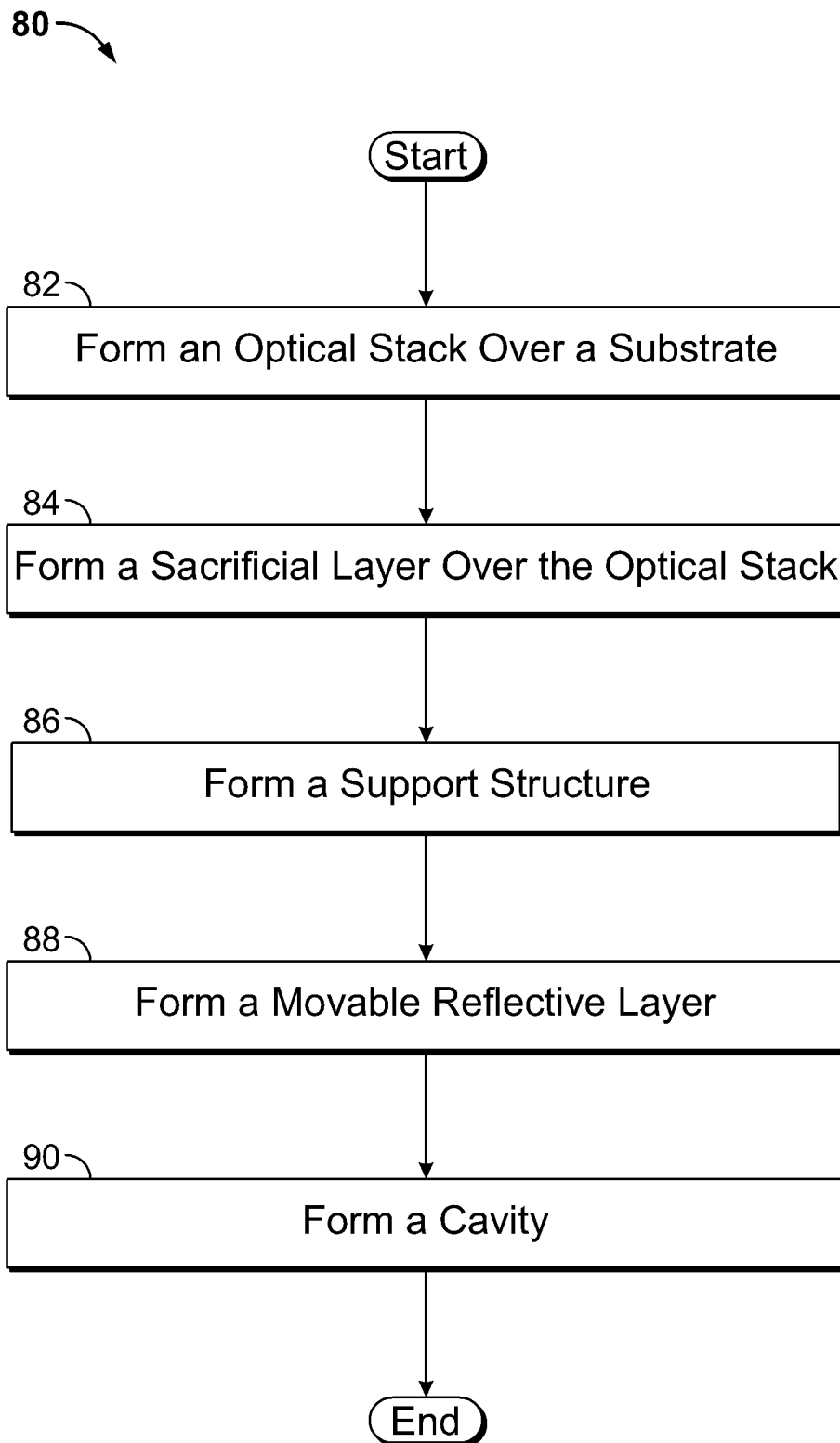


Figure 7

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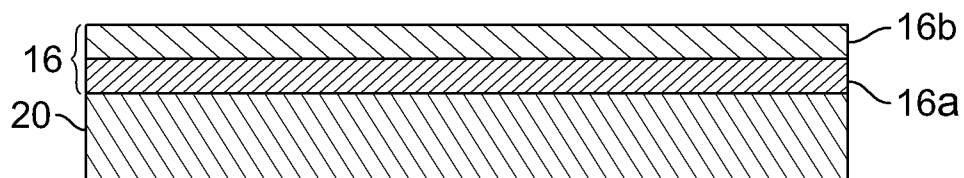


Figure 8A

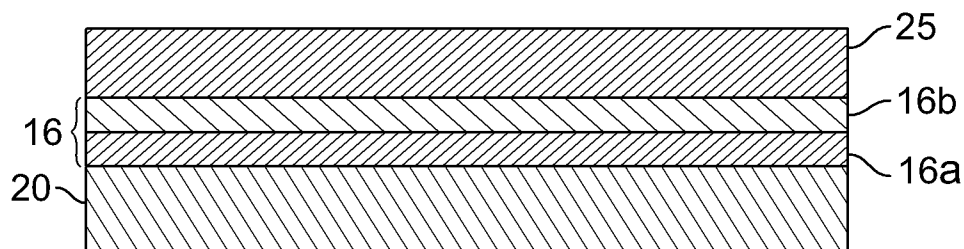


Figure 8B

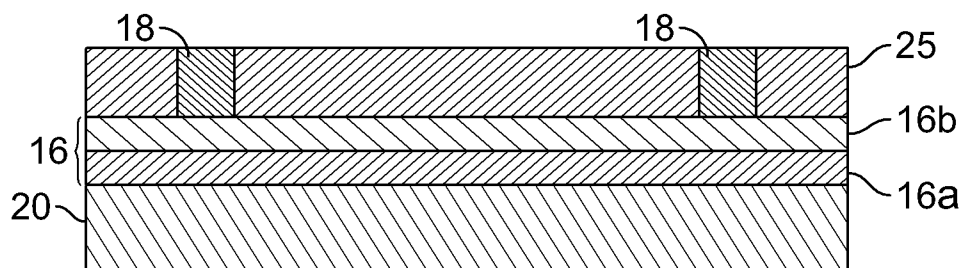


Figure 8C

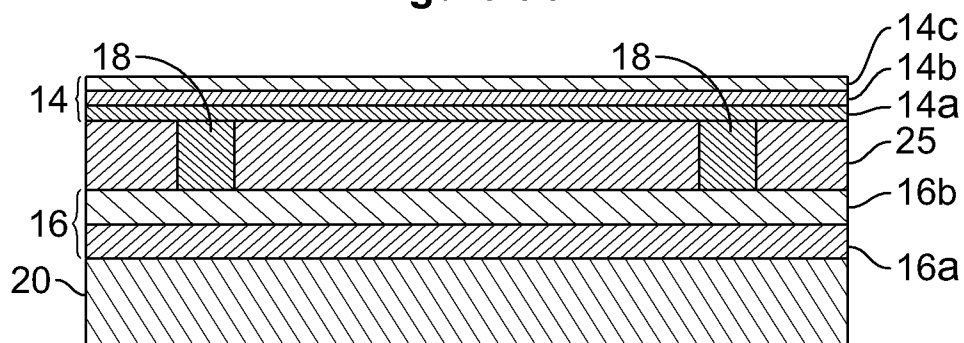


Figure 8D

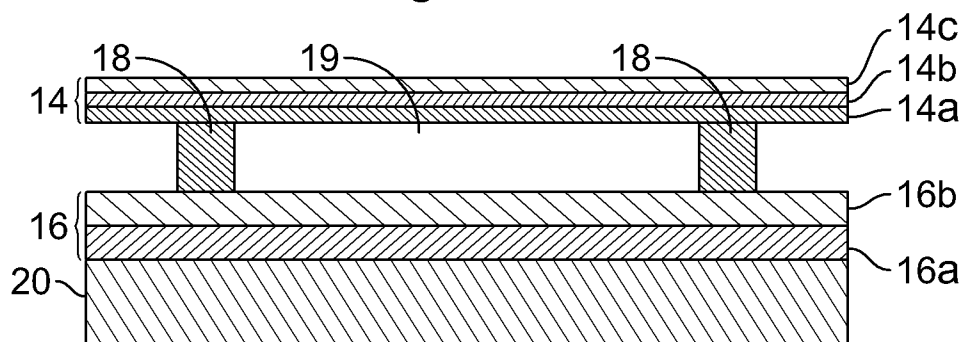


Figure 8E

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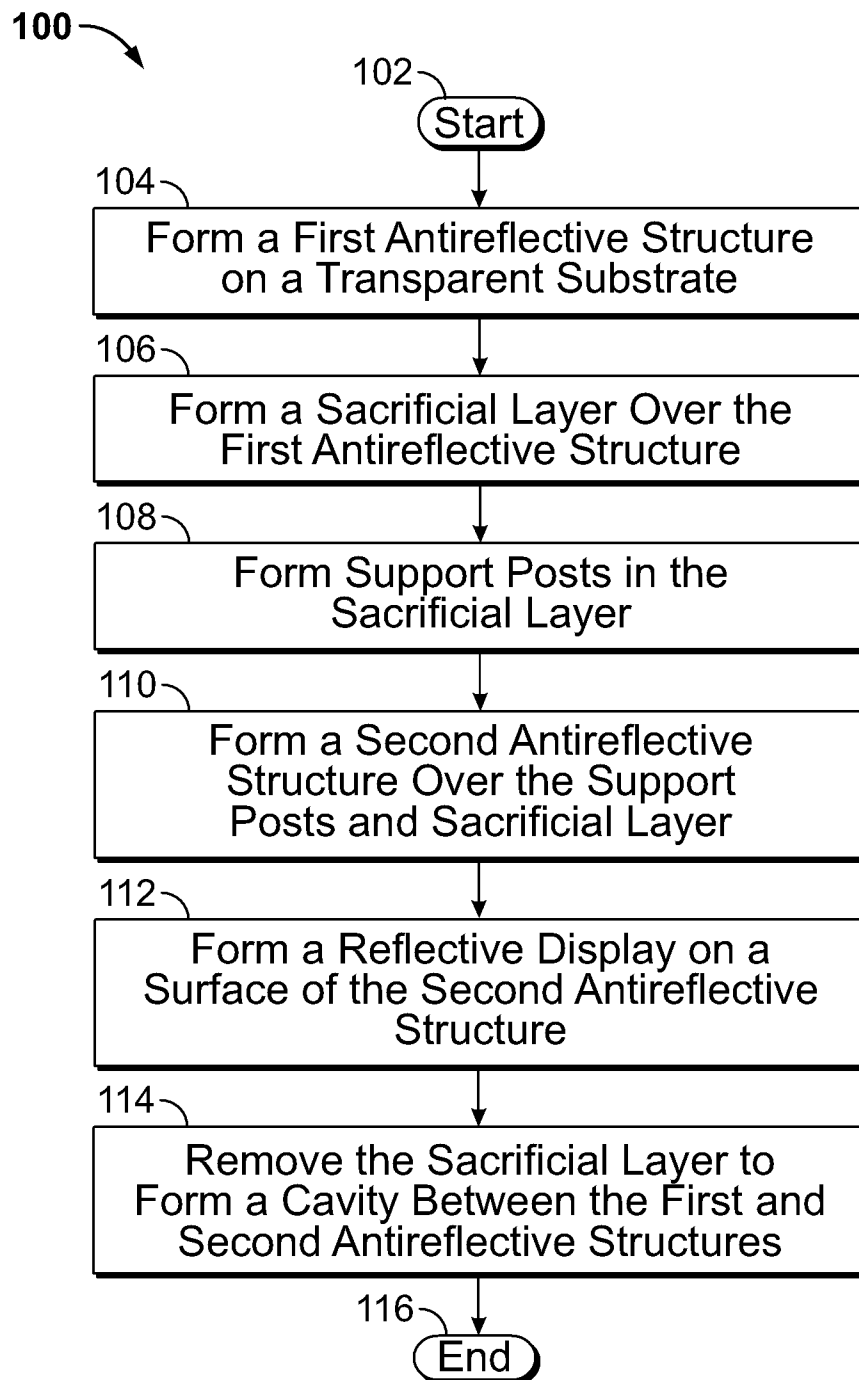
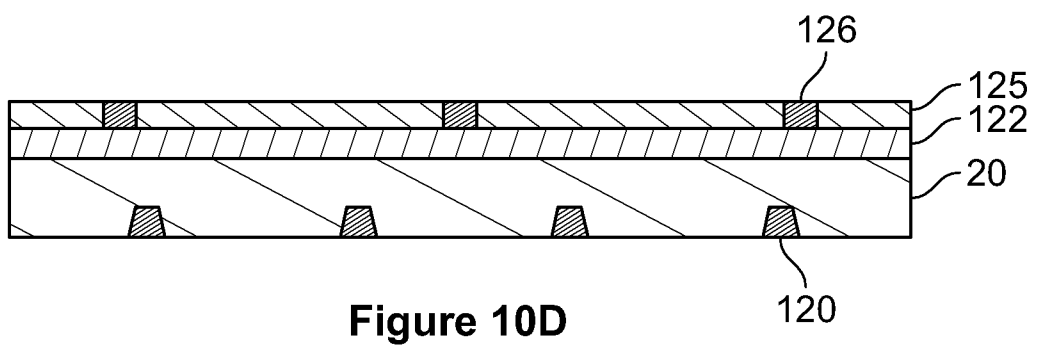
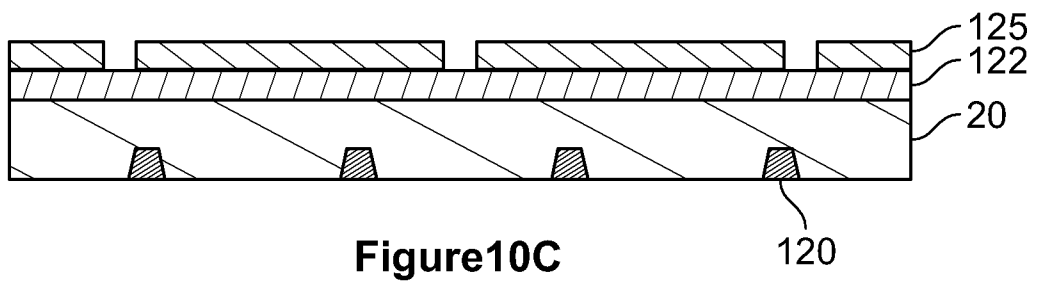
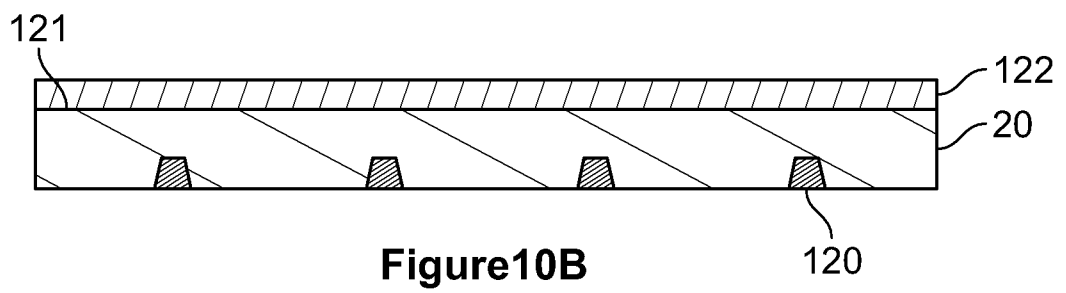
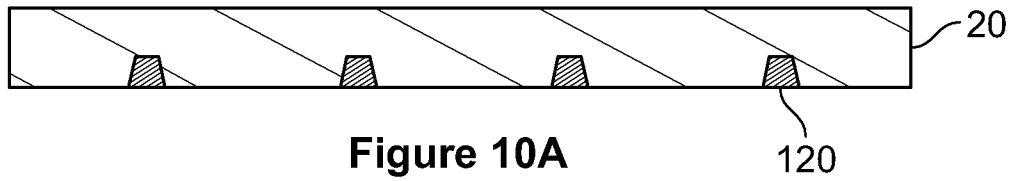


Figure 9

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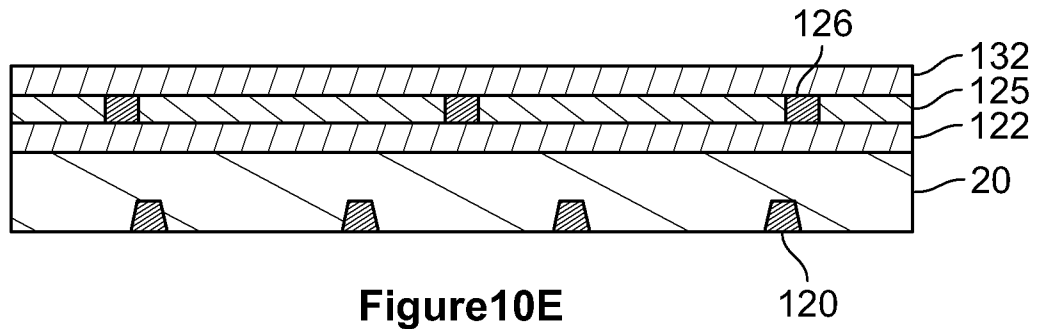


Figure 10E

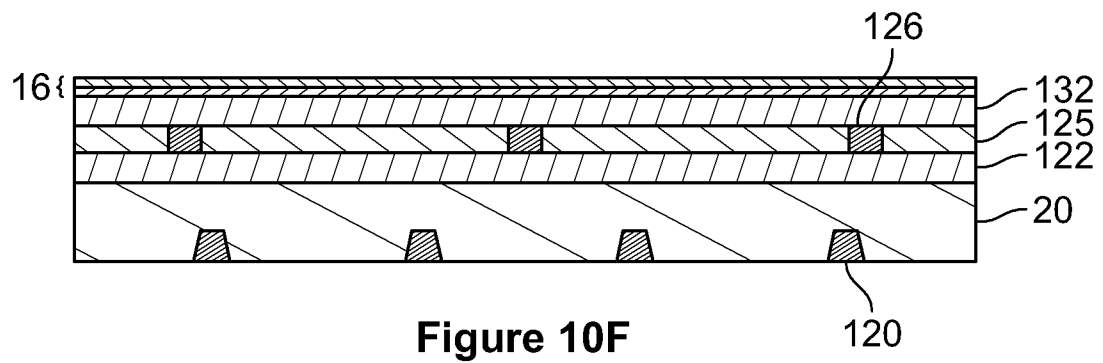


Figure 10F

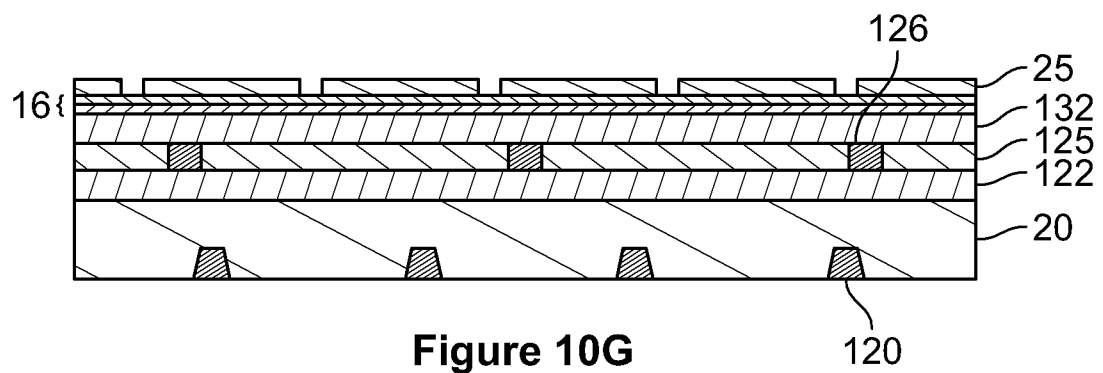


Figure 10G

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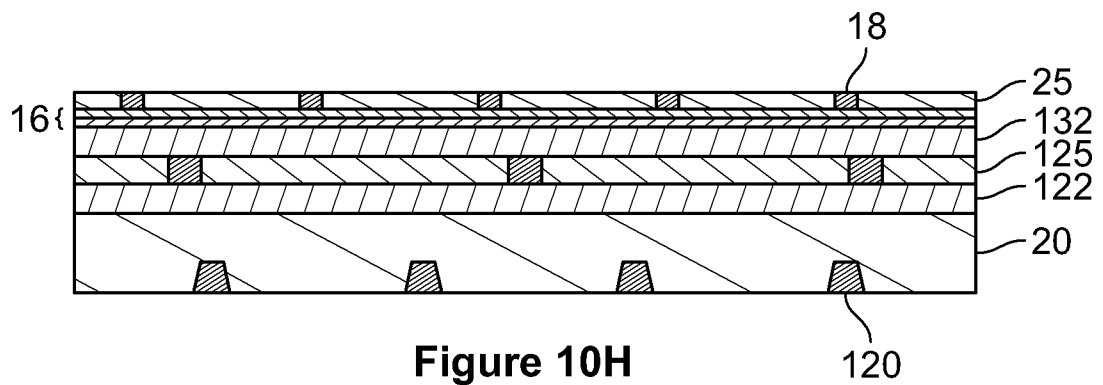


Figure 10H

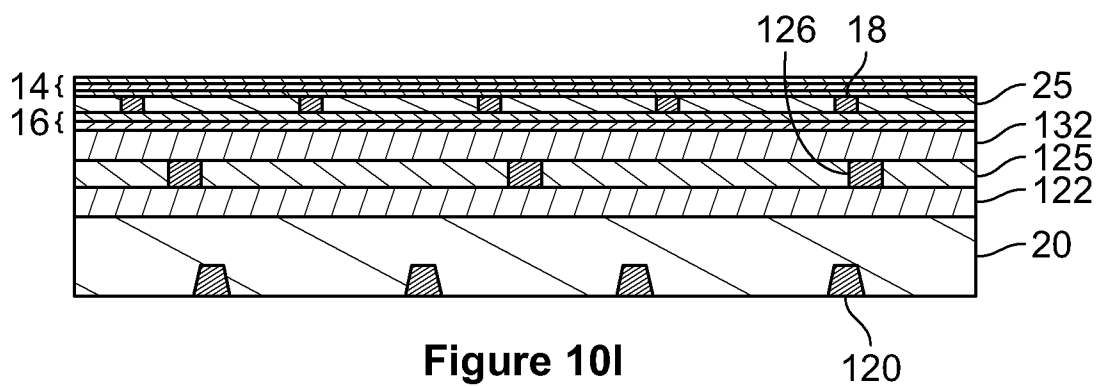


Figure 10I

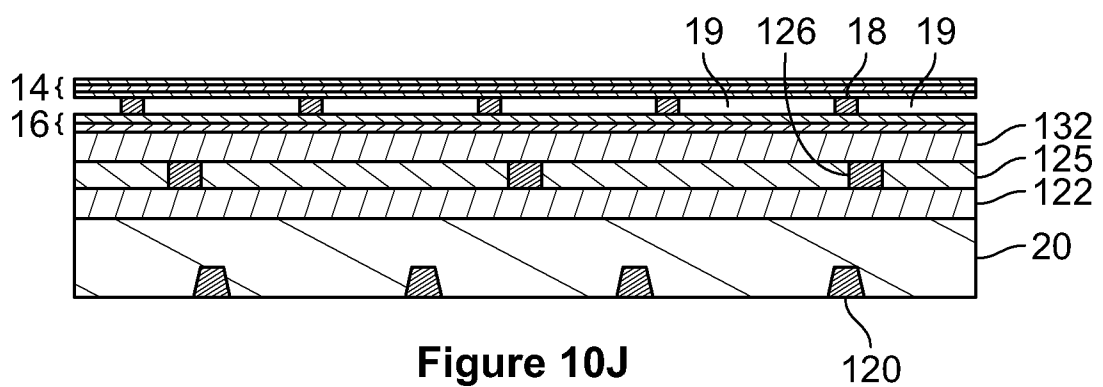


Figure 10J

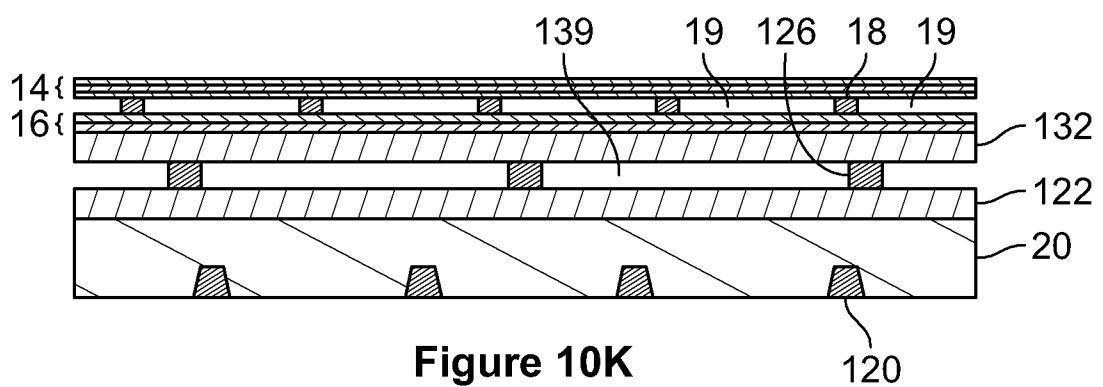


Figure 10K

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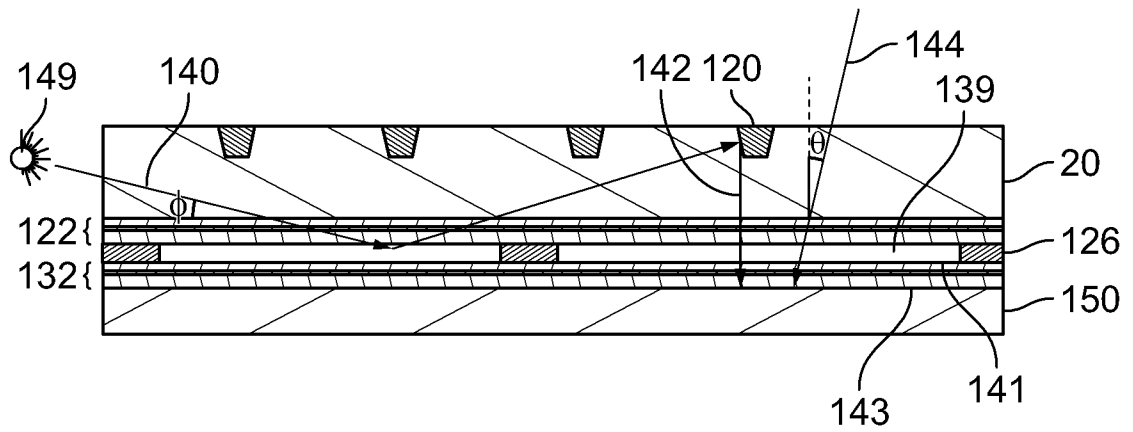


Figure 11

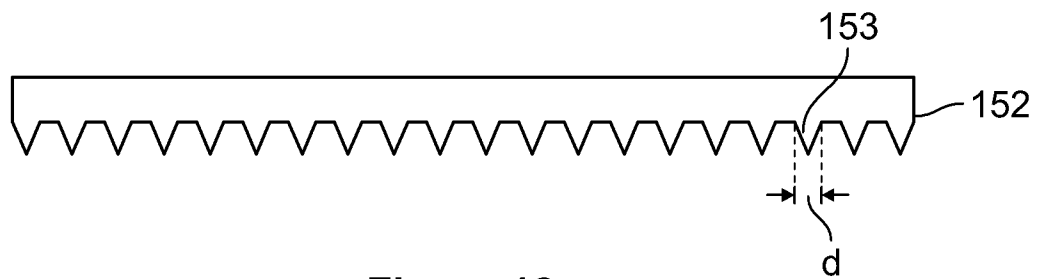


Figure 12

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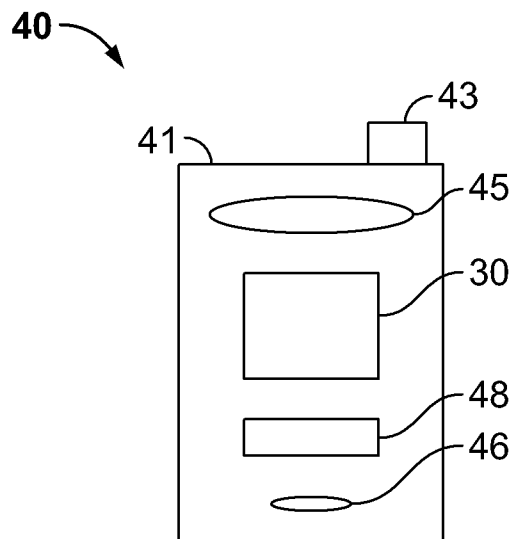


Figure 13A

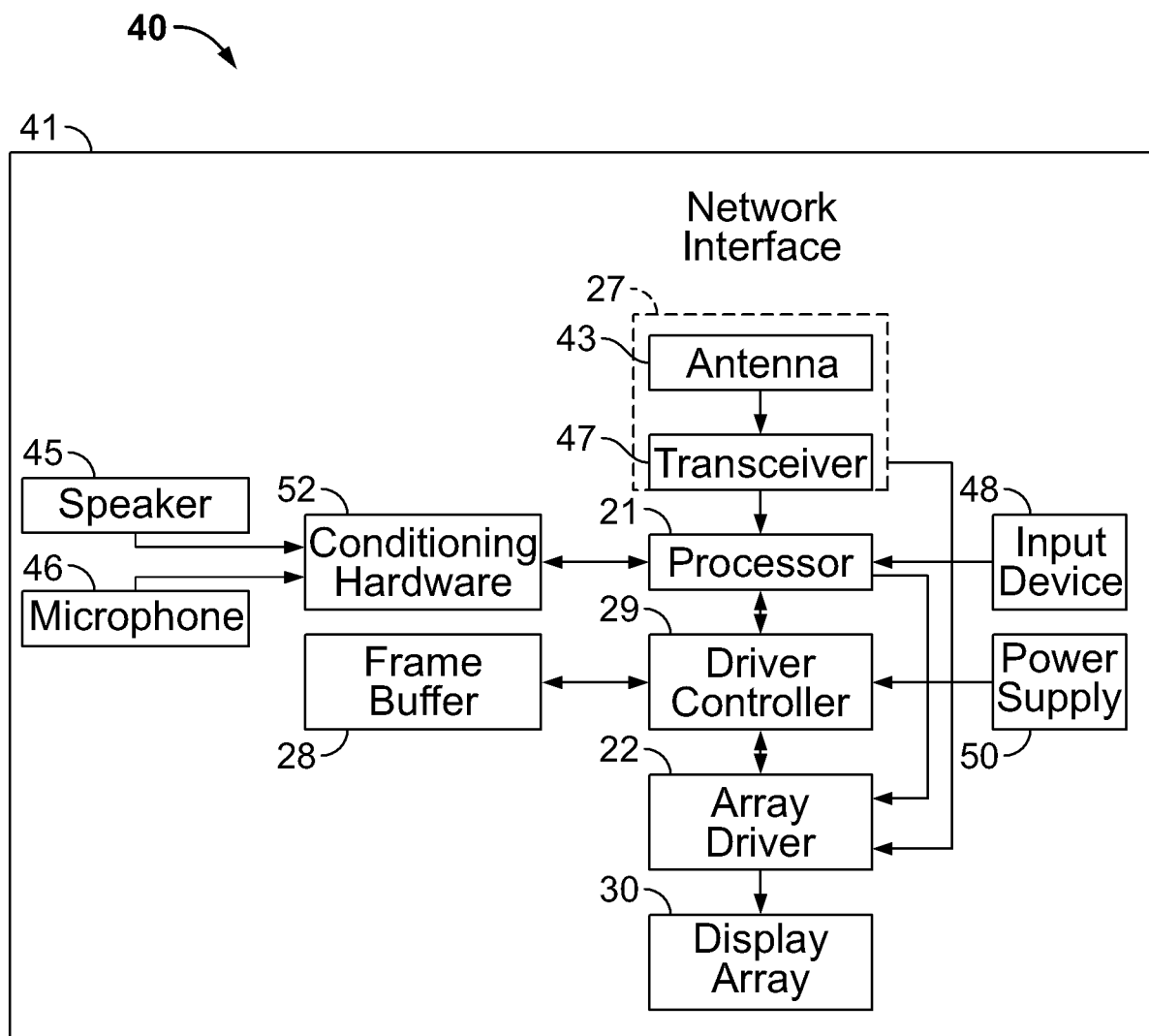


Figure 13B

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2012/043164

A. CLASSIFICATION OF SUBJECT MATTER
 INV. G02F1/1335
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 02/081965 A1 (3M INNOVATIVE PROPERTIES CO [US]) 17 October 2002 (2002-10-17) page 10, line 1 - page 11, column 18; figures 1-12	1-23
X	US 2001/055076 A1 (OCHI KEIZOU [JP] ET AL) 27 December 2001 (2001-12-27) paragraph [0046]; figures 1-5	1
X	JP 2002 229023 A (ROHM CO LTD) 14 August 2002 (2002-08-14) abstract; figure 1	1-23
A	JP 2006 286263 A (CASIO COMPUTER CO LTD) 19 October 2006 (2006-10-19) abstract; figure 11	1-23



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 September 2012

Date of mailing of the international search report

30/11/2012

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
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 Fax: (+31-70) 340-3016

Authorized officer

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/043164

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-23

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-23

Provision of support posts, thus defining a cavity.

2. claims: 24-30

Provision of a decoupling means.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2012/043164

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 02081965	A1	17-10-2002	CN 1545603 A 10-11-2004
			EP 1407185 A1 14-04-2004
			JP 4156931 B2 24-09-2008
			JP 2004528689 A 16-09-2004
			US 2002149925 A1 17-10-2002
			WO 02081965 A1 17-10-2002
US 2001055076	A1	27-12-2001	NONE
JP 2002229023	A	14-08-2002	NONE
JP 2006286263	A	19-10-2006	NONE