(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 September 2001 (27.09.2001)

PCT

(10) International Publication Number
WO 01/70454 A1

(51) International Patent Classification[7]: **B24B 1/00**, 7/00, 9/00, H01L 21/302, 21/461

(21) International Application Number: PCT/US01/08506

(22) International Filing Date: 16 March 2001 (16.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/190,278	17 March 2000 (17.03.2000)	US
60/190,221	17 March 2000 (17.03.2000)	US
60/202,495	5 May 2000 (05.05.2000)	US
09/808,790	15 March 2001 (15.03.2001)	US
09/808,749	15 March 2001 (15.03.2001)	US
09/808,748	15 March 2001 (15.03.2001)	US

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

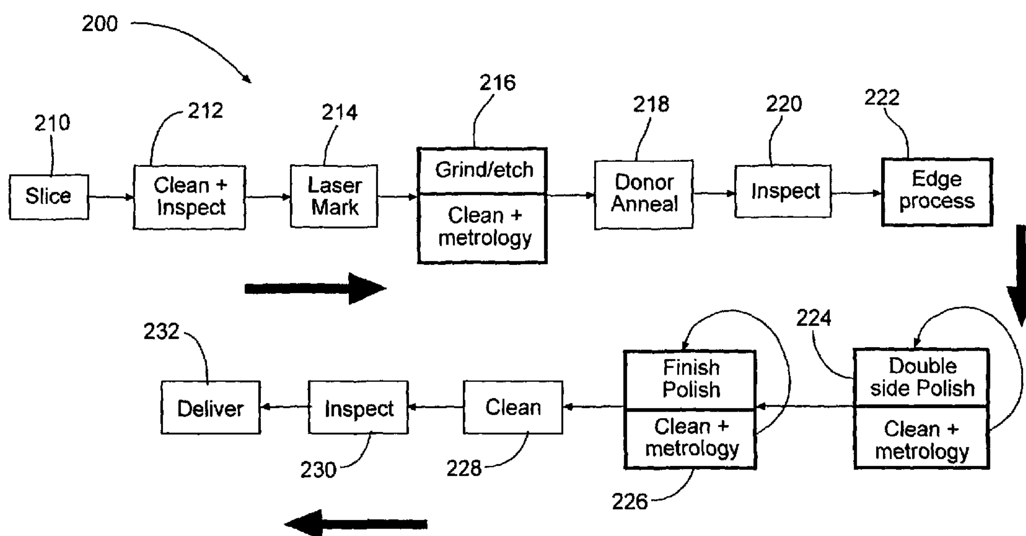
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 01/70454 A1

(54) Title: CLUSTER TOOL SYSTEMS AND METHODS FOR PROCESSING WAFERS



(57) Abstract: The present invention provides exemplary cluster tool systems and methods for processing wafers, such as semiconductor wafers. One method includes providing a wafer having initial thickness variations between two wafer surfaces. Thw wafer is processed (Step 216) through a first module (300), with the first module having apparatus for performing a grinding process, a clean process and a metrology process, all preferably within a clean room environment (310). Wafer processing through the ifrst module includes performing the grinding process, clean process and metrology process. The method further includes defining an edge profile on the wafer and processing (Step 222) the wafer through a second module (400).

CLUSTER TOOL SYSTEMS AND METHODS FOR PROCESSING WAFERS

CROSS-REFERENCES TO RELATED APPLICATIONS

5 This application claims the benefit of the following U.S. Patent Applications, the complete disclosures of which are incorporated herein by reference:

U.S. Provisional Application No. 60/190,278 (Attorney Docket No. 20468-000100), filed on March 17, 2000;

U.S. Patent Application No. _________, entitled "Cluster Tool Systems and
10 Methods for Processing Wafers," (Attorney Docket No. 20468-000110), filed on March 15, 2001;

U.S. Provisional Application No. 60/190,221 (Attorney Docket No. 20468-000300), filed on March 17, 2000;

U.S. Patent Application No. _________, entitled "Cluster Tool Systems and
15 Methods for In Fab Wafer Processing," (Attorney Docket No. 20468-000310), filed on March 15, 2001;

U.S. Provisional Application No. 60/202,495 (Attorney Docket No. 20468-001000) filed on May 5, 2000; and

U.S. Patent Application No. _________, entitled "Cluster Tool Systems and
20 Methods to Eliminate Wafer Waviness During Grinding," (Attorney Docket No. 20468-001010), filed on March 15, 2001.

BACKGROUND OF THE INVENTION

25 The present invention is directed to the processing of wafers, substrates or disks, such as silicon wafers, and more specifically to cluster tool systems and methods for processing wafers prior to device formation.

Wafers or substrates with exemplary characteristics must first be formed prior to the formation of circuit devices. In determining the quality of the semiconductor wafer,
30 the flatness of the wafer is a critical parameter to customers since wafer flatness has a direct impact on the subsequent use and quality of semiconductor chips diced from the wafer. Hence, it is desirable to produce wafers having as near a planar surface as possible.

In a current practice, cylindrical boules of single-crystal silicon are formed, such as by Czochralski (CZ) growth process. The boules typically range from 100 to 300 millimeters in diameter. These boules are cut with an internal diameter (ID) saw or a wire saw into disc-shaped wafers approximately one millimeter (mm) thick. The wire saw reduces the kerf loss and permits many wafers to be cut simultaneously. However, the use of these saws results in undesirable waviness of the surfaces of the wafer. For example, the topography of the front surface of a wafer may vary by as much as 1-2 microns (μ) as a result of the natural distortions or warpage of the wafer as well as the variations in the thickness of the wafer across its surface. It is not unusual for the amplitude of the waves in each surface of a wafer to exceed fifteen (15) micrometers. The surfaces need to be made more planar (planarized) before they can be polished, coated or subjected to other processes.

Fig. 1 depicts a typical prior art method 10 for processing a silicon wafer prior to device formation. Method 10 includes a slice step 12 as previously described to remove a disc-shaped portion of wafer from the silicon boule. Once the wafer has been sliced, the wafer is cleaned and inspected (Step 14). Thereafter, an edge profile process (Step 16) is performed. Once the edge profile has been performed, the wafer is again cleaned and inspected (Step 18), and is laser marked (Step 20).

Next, a lapping process (Step 22) is performed to control thickness and remove bow and warp of the silicon wafer. The wafer is simultaneously lapped on both sides with an abrasive slurry in a lapping machine. The lapping process may involve one or more lapping steps with increasingly finer polishing grit. The wafer is then cleaned (Step 24) and etched (Step 26) to remove damage caused by the lapping process. The etching process may involve placing the wafer in an acid bath to remove the outer surface layer of the wafer. Typically, the etchant is a material requiring special handling and disposal. Thereafter, an additional cleaning of the wafer (Step 28) is performed.

The prior art method continues with a donor anneal (Step 30) followed by wafer inspection (Step 32). Thereafter, the wafer edge is polished (Step 24) and the wafer is again cleaned (Step 36). Typical wafer processing involves the parallel processing of a multitude of wafers. Hence at this juncture wafers may be sorted, such as by thickness (Step 38), after which a double side polish process is performed (Step 40).

The wafers then are cleaned (Step 42) and a final polish (Step 44) is performed. The wafers are again cleaned (Step 46), inspected (Step 48) and potentially cleaned and inspected again (Steps 50 and 52). For epitaxial substrates, a poly or oxide layer

is overlaid to seal in the dopants after inspection Step 52. At this point, the wafer is packed (Step 54), shipped (Step 56) and delivered to the end user (Step 58). Hence, as seen in Fig. 1 and as described above, typical wafer processing involves a lengthy, time consuming process with a large number of processing steps.

5 A number of deficiencies exist with the prior art method. As can be seen from even a precursory review of Fig. 1, the prior art method requires a large number of steps to transform a wafer slice into a substrate suitable for creating circuit devices. The large number of process steps involved negatively effects production throughput, requires a large production area, and results in high fabrication costs. Additionally, each of the steps in Fig. 1
10 are typically performed at individual process stations. The stations are not grouped or clustered together, and manual delivery of the wafers between stations is often used.

Additionally, the large production area required results in the need for a separate facility for the wafer processing described in Fig. 1 than for device formation on the wafer. To produce integrated circuits and other devices from the wafers, the wafers are
15 packed, shipped and delivered to the appropriate fabrication facility. Upon receipt by the fabrication facility, the wafers must be received, unpacked, inspected and delivered to a wafer processing chamber for subsequent process steps necessary for device formation. These additional processing and delivering steps add to the complexity and cost of wafer processing prior to device fabrication. Unfortunately, to date, separate facilities are required due at least
20 in part to the large area needed for Fig. 1 processing. As a result, small volume manufacturing of wafers is difficult.

In addition to the large number of process steps, at least some of the prior art steps themselves are slow or produce unacceptable results. For example, compared to a grinding process, the lapping process is slow and must be followed by careful cleaning and
25 etching steps to relieve stresses before the wafer is polished. These additional steps cause the conventional method to be more expensive and time-consuming than methods of the present invention. Also, the etching process employed after the lapping step is undesirable from an environmental standpoint, because the large amount of strong acids used must be disposed of in an acceptable way.

30 In another prior art method, a grinding process replaces the lapping procedure in Fig. 1. A first surface of the wafer is drawn or pushed against a hard flat holder while the second surface of the wafer is ground flat. The forces used to hold the wafer elastically deform the wafer during grinding of the second surface. When the wafer is released, elastic restoring forces in the wafer cause it to resume its original shape, and it can be seen that the

waves in the first surface have been transferred to the surface that has been ground. Thus while this technique produces a wafer of more uniform thickness, it does not eliminate the residual saw waves.

One technique used to try to solve the residual wave problem is to apply a thick coating of grease or wax to the wafer holder and then bring one side of the wafer into contact with the exposed surface of the grease. The wafer is then partially supported by the grease, and because the weight of the wafer is distributed uniformly across the wafer, the wafer is not deformed from its original shape. At this point, the temperature could be lowered so that the grease would become thicker so as to better oppose any localized stresses that might be imposed on the wafer by the grinding process. In place of grease, a wax or pitch could be used.

This technique is undesirable, however, because the grease clogs the pores in the vacuum plate holding the wafer. Another disadvantage is the need to remove the grease or other material from the wafer after the grinding has been completed. This can be difficult due to the stickiness or tackiness of the wax, grease or other materials. The wafer, vacuum plate and/or the cleaning device often has residual material sticking to it. For these and other reasons, the above technique is undesirable.

Additional deficiencies in the current art, and improvements in the present invention, are described below and will be recognized by those skilled in the art.

SUMMARY OF THE INVENTION

The present invention provides exemplary cluster tool systems and methods for processing wafers, such as semiconductor wafers, including exemplary grinding methods and apparatus. One method of the present invention includes providing a wafer having initial thickness variations between two wafer surfaces. The wafer is processed through a first module, with the first module having apparatus for performing a grinding process, a clean process and a metrology process. Wafer processing through the first module includes performing the grinding process, clean process and metrology process. The method further includes defining an edge profile on the wafer and processing the wafer through a second module. The wafer edge profile preferably is performed after first module processing, though need not be.

The second module includes apparatus for performing a double side polish (DSP) process, a clean process and a metrology process. Again, processing the wafer

through the second module includes the above noted processes. In this manner, the wafer processing is compartmentalized in an efficient manner which results in the reduction of process steps compared to the prior art. Further, in one embodiment, the wafer edge profile is defined subsequent to the grinding process. In this manner, the edge profiling helps remove
5 damage to the wafer edge caused by the grinding process.

In one aspect, the first and second modules each comprise a cluster tool defining a clean room or other micro environment.

In one embodiment of the present invention, the first module processing further includes an etch process which reduces the wafer thickness by less than about ten (10)
10 microns. One advantage of the present invention is the use of the grinding process to provide a generally flat wafer surface, In such a process, a reduced amount of etching is required to produce a flat surface and remove grinding damage from the wafer.

In an aspect of the present invention, the first module metrology process occurs simultaneously with the grinding process. In a further aspect, the first module
15 metrology process produces a metrology profile for the wafer. Processing the wafer through the first module further includes modifying the grinding process in response to the wafer metrology profile. Alternatively, the first module metrology process occurs after the wafer grinding process.

In one aspect, the wafer edge is polished after the wafer edge profile has been
20 defined. In another aspect, the method includes processing the wafer through a third module. The third module includes apparatus for performing, and the method includes performing, a finish polish process, a clean process and a metrology process.

The compact nature of the cluster tools according to the present invention facilitate their use within a fabrication facility. In one aspect of the invention, after
25 completion of processing through the third module, the processed wafer is directly provided to a process chamber for fabrication of a semiconductor device. In this manner, packing, shipping and delivery steps as shown in Fig. 1 are avoided. Alternatively, methods of the present invention may be performed offsite from the fabrication facility, with wafers intended to be processed therethrough first being packaged, shipped and delivered to the fabrication
30 facility.

In one aspect of the invention, the wafer has a total thickness variation (TTV) between two surfaces of less than about 0.3 microns after processing through the second module. In another aspect, the wafer has a side flatness quotient reading (SFQR) of less than 0.12 microns after processing through the second module. In still another aspect, the TTV

between the two wafers surfaces is less than about 0.5 microns, is less than about 0.3 microns, or is less than about 0.2 microns after processing through a finish polishing module.

In alternative aspects, the methods of processing a wafer further include laser marking the wafer prior to defining the edge profile, and/or performing a donor anneal
5 process prior to defining the edge profile. In one aspect of the present invention, the wafer is processed through a third module comprising apparatus for performing an edge profile process and an edge polishing process.

The method further includes exemplary wafer processing systems according to the present invention. In one aspect of the present invention, the wafer processing system
10 includes means for grinding the wafer, means for cleaning the wafer, and means for testing the wafer metrology, wherein the means for grinding, cleaning and testing are contained within a single clean room environment. In one embodiment, the system includes a first clean room environment containing a grinder for grinding first and second wafer surfaces, an etcher for etching the wafer, a cleaner for cleaning the wafer, and a metrology tester for
15 testing wafer metrology. In one aspect, the etcher and cleaner comprise the same device.

In one aspect, the system further includes a transfer mechanism, such as a robot, adapted to transfer the wafer between the grinder and the etcher within the first clean room environment. In another aspect, the system includes a second clean room environment comprising an edge grinder for defining an edge profile of the wafer and an edge polisher for
20 polishing the wafer edge. In alternative aspects, the system includes a third clean room containing a polisher, a cleaner and a metrology tester, and/or a fourth clean room comprising a finish polisher, a cleaner and a metrology tester.

One method of the present invention includes providing a wafer having initial thickness variations between two wafer surfaces. The wafer is processed through a first
25 module, with the first module having apparatus for performing a grinding process, and where processing through the first module includes performing the grinding process. The wafer is processed through a second module having apparatus for performing a double side polish (DSP) process. Processing the wafer through the second module includes performing a DSP process. The wafer is processed through a third module having an apparatus for performing a
30 finish polish process, with processing therethrough including the finish polish process.

The method further includes cleaning the wafer after processing through the third module, and thereafter transferring the wafer to a wafer processing chamber within a same facility as that containing the first, second and third modules. In this manner, initial wafer processing occurs in the same facility as circuit device formation. Circuit device

formation includes a myriad of processes know to those skilled in the art, including the deposition or formation of dielectric layers or conductive layers, etching processes, thermal oxidation and the like. Exemplary processing chambers include the Centura platform and the Endura platform, available from Applied Materials, Inc. in Santa Clara, California.

5 In one embodiment, the first and/or second modules each comprise a cluster tool defining a clean room environment. In one aspect, the method further includes testing wafer metrology and transferring the wafer to the wafer processing chamber only if the wafer has a desired flatness profile. In this manner, only wafers suitable for device formation are transferred to the wafer processing chamber. In another aspect, the wafer has a total 10 thickness variation (TTV) between the two surfaces of less than about 0.3 microns, and/or a SFQR of less than about 0.12 microns, prior to transferring to the wafer processing chamber. In one embodiment, the method further includes performing a circuit device fabrication process, such as the deposition of a dielectric or conductive layer, on the wafer within the processing chamber.

15 In one aspect, the first module has a footprint between about ninty (90) square feet (sqft) and about one hundred and fifty (150) sqft, and has a capacity of processing between about twenty-nine (29) and about thirty-three (33) 300mm wafers therethrough per hour. In another aspect, the second module has a footprint between about one hundred (100) square feet (sqft) and about one hundred and eighty (180) sqft, and has a capacity of 20 processing between about twenty nine (29) and about thirty-three (33) 300mm wafers therethrough per hour. In still another aspect, the third module has a footprint between about one hundred (100) square feet (sqft) and about one hundred and eighty (180) sqft, and has a capacity of processing between about twenty nine (29) and about thirty-three (33) 300mm wafers therethrough per hour. In this manner, the process modules are sufficiently compact 25 in size, with appropriate throughput, to be co-located in a circuit device fabrication facility with circuit device processing chambers and other equipment.

In another embodiment of the present invention, a method of processing a wafer prior to device formation thereon includes providing a wafer having first and second surfaces with thickness variations therebetween. The method includes grinding the first and 30 second wafer surfaces, polishing the first and second wafer surfaces, cleaning the wafer, and thereafter transferring the wafer to a wafer processing chamber.

In one aspect, the wafer polishing, cleaning and transferring all occur in a single wafer fabrication facility. In another aspect, the wafer is transferred to the wafer processing chamber with a robot. In alternative embodiments, the method further includes

depositing a dielectric layer and/or a conductive layer on the wafer within the processing chamber. In this manner, wafer fabrication and device fabrication take place in a single fabrication facility.

In still another aspect, the wafer is cleaned and then transferred, with the cleaning and transferring adapted to provide the wafer to the processing chamber in a wafer condition sufficient for forming an integrated circuit device thereon. In another aspect, the method further includes defining a wafer edge profile after wafer grinding.

The compact nature of the cluster tools according to the present invention facilitate their use within a fabrication facility, such as a circuit device fabrication facility. In this manner, packing, shipping and delivery steps as shown in Fig. 1 are avoided. Additionally, unpacking, inspecting and cleaning steps may be avoided at the device fabrication facility since the wafer can be delivered directly to the processing chamber.

One method of the present invention includes providing a cut wafer having initial thickness variations between first and second wafer surfaces. A polymer is applied to the first surface to form a substantially smooth outer surface. The wafer is positioned on a grinding tool, and the method includes grinding the second surface to form a substantially planar second surface. In this manner, applying the polymer helps form a substantially smooth, flat surface on which the wafer can rest while grinding operations are performed. As a result, waves or undulations in the wafer first surface are not transferred to the wafer second surface during or after grinding.

In one aspect, a liquid polymer is applied, after which the liquid polymer is cured to form the substantially smooth outer surface. Curing is performed, in alternative embodiments, using electromagnetic energy, using heat, using ultraviolet light, and the like. In one aspect, the polymer is a spin-on polymer, which in one embodiment is applied while simultaneously rotating the wafer. In another aspect, applying the polymer forms a polymer film having a thickness between about five (5) microns and about thirty (30) microns.

In one aspect of the method, positioning the wafer on a grinding tool includes placing the polymer covered wafer surface on a grinding tool platen. In another aspect, the method includes grinding the polymer and first surface. In another embodiment, the second surface is cleaned before grinding of the polymer and first surface.

In one aspect, wafer grinding according to the present invention substantially removes the wafer thickness variations. This may be accomplished by grinding to remove substantially all of the polymer, and a portion of the wafer first and second surfaces.

The present invention further includes methods for preparing a substrate for grinding operations. In one embodiment, the method includes providing a substrate having first and second surfaces, applying a curable liquid to the first surface, curing the curable liquid to form a substantially smooth outer surface, and positioning the outer surface on a grinding tool platen to expose the second surface to a grinder.

The present invention still further includes exemplary wafer grinding apparatus. In one embodiment, grinding apparatus include an applicator for applying a curable liquid to a wafer surface, a curer for curing the curable liquid, a platen for holding the wafer, and a grinder for grinding the wafer surface. In one aspect, the apparatus includes a rotation device coupled to the platen for rotating the wafer. In another aspect, the applicator includes a spin on applicator and the curable liquid comprises a liquid polymer.

Other objects, features and advantages of the present invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 depicts a prior art method for processing a silicon wafer;

Fig. 2 is a simplified flow diagram of a wafer processing method according to the present invention;

Figs. 3A-C depict grind damage cluster tools according to the present invention;

Fig. 4 depicts an edge profile/polish cluster tool according to the present invention;

Figs. 5A and 5B depict double side polish cluster tools according to the present invention;

Fig. 6 depicts a finish polish cluster tool according to the present invention;

Fig. 7A is a simplified schematic showing wafer preparation and grinding apparatus according to the present invention;

Fig. 7B is a simplified flow diagram showing wafer preparation and grinding methods of the present invention; and

Fig. 8 is a simplified flow diagram of methods of the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Fig. 2 depicts an exemplary method 200 of the present invention. Method 200 includes a slice process 210, using a wire saw, inner diameter saw or the like, to create a generally disc-shaped wafer or substrate. In one embodiment, the wafer is a silicon wafer. Alternatively, the wafer may comprise polysilicon, germanium, glass, quartz, or other materials. Further, the wafer may have an initial diameter of about 200mm, about 300mm, or other sizes, including diameters larger than 300mm.

The wafer is cleaned and inspected (Step 212) and then may, or may not, be laser-marked (Step 214). Laser marking involves creating an alphanumeric identification mark on the wafer. The ID mark may identify the wafer manufacturer, flatness, conductivity type, wafer number and the like. The laser marking preferably is performed to a sufficient depth so that the ID mark remains even after portions of the wafer have been removed by subsequent process steps such as grinding, etching, polishing, and the like.

Thereafter, the wafer is processed through a first module (Step 216), with details of embodiments of the first module described below in conjunction with Figs. 3A-3C. First module processing (Step 216) includes a grinding process, an etching process, a cleaning process and metrology testing of the wafer. In this module, the use of a grinding process in lieu of lapping helps to remove wafer bow and warpage. The grinding process of the present invention also is beneficial in removing wafer surface waves caused by the wafer slicing in Step 210. Benefits of grinding in lieu of lapping include reduced kerf loss, better thickness tolerance, improved wafer shape for polishing and better laser mark dot depth tolerance, and reduced damage, among others.

The etching process within the first module is a more benign process than the prior art etch step described in conjunction with Fig. 1. For example, typical prior art etching (Step 26 in Fig. 1) may involve the bulk removal of forty (40) or more microns of wafer thickness. In contrast, the etch process of the present invention preferably removes ten (10) microns or less from the wafer thickness. In one embodiment, the first module etch process removes between about two (2) microns to about five (5) microns of wafer material per side, or a total of about four (4) to about ten (10) microns. In another embodiment, the first module etch process removes between about three (3) microns and about four (4) microns of wafer material per side for a total of about six (6) to about (8) microns.

After first module processing, the wafer is subjected to a donor anneal (Step 218) and thereafter inspected (Step 220). The donor anneal removes unstable oxygen impurities within the wafer. As a result, the original wafer resistivity may be fixed. In an alternative embodiment, donor anneal is not performed.

5 The wafer then is processed through a second module (Step 222) in which an edge process is performed. The edge process includes both an edge profile and an edge polish procedure. Edge profiling may include removing chips from the wafer edge, controlling the diameter of the wafer and/or the creation of a beveled edge. Edge profiling also may involve notching the wafer to create primary and secondary flat edges. The flats 10 facilitate wafer alignment in subsequent processing steps and/or provide desired wafer information (e.g., conductivity type). In one embodiment, one or both flats are formed near the ID mark previously created in the wafer surface. One advantage of the present invention involves performing the edge profiling after wafer grinding. In this manner, chips or other defects to the wafer edge, which may arise during grinding or lapping, are more likely to be 15 removed. Prior art edge profiling occurs before lapping, and edge polishing subsequent to the lapping step may not sufficiently remove edge defects.

The wafer is then processed through a third module (Step 224). A third module process includes a double side polish, a cleaning process and wafer metrology. Wafer polishing is designed to remove stress within the wafer and smooth any remaining 20 roughness. The polishing also helps eliminate haze and light point defects (LPD) within the wafer, and produces a flatter, smoother finish wafer. As shown by the arrow in Fig. 2, wafer metrology may be used to adjust the double side polishing process within the third module. In other words, wafer metrology may be feed back to the double side polisher and used to adjust the DSP device in the event the processed wafer needs to have different or improved 25 characteristics, such as flatness, or to further polish out scratches.

Thereafter, the wafer is subjected to a finish polish, a cleaning process and metrology testing, all within a fourth process module (226). The wafer is cleaned (Step 228), inspected (Step 230) and delivered (Step 232).

The reduced number of clean and inspection steps, particularly near the end of 30 the process flow, are due in part to the exemplary metrology processing of the wafer during prior process steps. Wafer metrology testing may test a number of wafer characteristics, including wafer flatness, haze, LPD, scratches and the like. Wafer flatness may be determined by a number of measuring methods known to those skilled in the art. For example, "taper" is a measurement of the lack of parallelism between the unpolished back

surface and a selected focal plane of the wafer. Site Total Indicated Reading (STIR) is the difference between the highest point above the selected focal plane and the lowest point below the focal plane for a selected portion (e.g., 1 square cm) of the wafer, and is always a positive number. Site Focal Plane Deviation (SFPD) is the highest point above, or the lowest point below, the chosen focal plane for a selected portion (e.g., 1 square cm) of the wafer and may be a positive or negative number. Total thickness variation (TTV) is the difference between the highest and lowest elevation of the polished front surface of the wafer.

Further, metrology information, in one embodiment, is fed back and used to modify process parameters. For example, in one embodiment metrology testing in the first module occurs after wafer grinding and may be used to modify the grinding process for subsequent wafers. In one embodiment, wafers are processed through the first module in series. More specifically, each station within the first module processes a single wafer at a time. In this manner, metrology information may be fed back to improve the grinding or other process after only about one (1) to five (5) wafers have been processed. As a result, a potential problem can be corrected before a larger number of wafers have been processed through the problem area, thus lowering costs.

Further, the present invention produces standard process times for each wafer. More specifically, each wafer is subjected to approximately the same duration of grinding, cleaning, etching, etc. The delay between each process also is the same or nearly the same for each wafer. As a result, it is easy to troubleshoot within the present invention methods and systems.

In contrast, prior art methods typically uses a batch process mode for a number of process steps. For example, a batch containing a large number of wafers (say, twenty (20)) may be lapped one to a few at a time (say, one (1) to four (4) at a time). After all twenty have been lapped, the batch of twenty wafers then are cleaned together as a group (Step 24), and etched together as a group (Step 26). As a result, the wafers that were lapped first sit around for a longer period of time prior to cleaning than do the wafers lapped last. This varying delay effects wafer quality, due in part to the formation of a greater amount of haze, light point defects, and other time-dependent wafer defects. One negative outcome of irregular process times is the resultant difficulty in locating potential problems within the process system.

As with the first module, metrology information may be fed back within the second, third and fourth modules. For example, metrology information may be fed back to the double side polisher or finish polisher to adjust those processes to produce improved

results. Additionally, in one embodiment, metrology information is fed back within the third and/or fourth module in real time. As a result, process steps such as the double side polishing can be modified during processing of the same wafer on which metrology testing has occurred.

5 With reference to Figs. 3-6, additional details on process modules according to the present invention will be provided. It will be appreciated by those skilled in the art that the process modules described in Figs. 3-6 are embodiments of the present invention, from which a large number of variations for each module exist within the scope of the present invention. Further, additional process steps may be removed or added, and process steps may 10 be rearranged within the scope of the present invention.

Fig. 3A depicts a grind damage cluster module described as first module 216 in conjunction with Fig. 2. First module 300 defines a clean room environment 310 in which a series of process steps are carried out. Wafers that have been processed through Step 214 (Fig. 2) are received in first module 300 via a portal, such as a front opening unified pod 15 (FOUP) 312. First module 300 is shown with two FOUPs 312, although a larger or smaller number of FOUPs/portals may be used. FOUPs 312 are adapted to hold a number of wafers so that the frequency of ingress into the clean room environment 310 may be minimized. A transfer device 314, schematically depicted as a robot, operates to remove a wafer from FOUPs 312 and place the wafer on a grinder 318. If needed, transfer device 314 travels 20 down a track 316 to properly align itself, and hence the wafer, in front of grinder 318. Grinder 318 operates to grind a first side of the wafer.

The wafer may be held down on grinder 318 by way of a vacuum chuck, and other methods. Once grinder 318 has ground the first side of the wafer, the wafer is cleaned in cleaner 322 and the transfer device 314 transfers the wafer back to grinder 318 for grinding 25 the converse side of the wafer. In one embodiment, wafer grinding of both wafer sides removes about forty (40) microns to about seventy (70) microns of wafer thickness. After the second wafer side is ground, the wafer is again cleaned in cleaner 322. In one embodiment, cleaning steps occur on grinder 318 subsequent to grinding thereon. In one embodiment, cleaning and drying are accomplished by spraying a cleaning solution on the wafer held by or 30 near the edges and spun.

In another embodiment, at least one side of the wafer is subjected to two sequential grinding steps on grinder 318. The two grinding processes preferably include a coarse grind followed by a fine grind. Grinder 318 may include, for example, two different grinding platens or pads with different grit patterns or surface roughness. In one

embodiment, the wafer is cleaned on grinder 318 between the two grinding steps to the same wafer side. Alternatively, cleaning may occur after both grinding steps to the same wafer side.

In some embodiments, transfer device 314 transfers the wafer from cleaner 322 to a backside polisher 326. For example, this process flow may occur for 200 mm wafers. In this embodiment, the back side is polished and not ground, or both ground and polished.

As shown in Fig. 3A, a second grinder 320 and a second cleaner 324 are provided within module 300. In this manner, two wafers may be simultaneously processed therethrough. Since both grinders 318, 320 have a corresponding cleaner 322, 324, wafer processing times are consistent even if two wafers are being ground simultaneously on grinders 318, 320. In one embodiment, grinders 318 and 320 are used to grind opposite sides of the same wafer. In this case, one side of the wafer is ground on grinder 318 and the other side of the same wafer is ground on grinder 320. As with grinder 318, wafers may be ground on grinder 320 and then cleaned on grinder 320 before removal, or cleaned in cleaner 324.

Once the wafers have been ground, a second transfer device 336, again a robot in one embodiment, operates to transfer the wafer to an etcher 330. Etcher 330 operates to remove material from the wafer, preferably a portion on both primary sides of the wafer. The etching process is designed to remove stresses within the silicon crystal caused by the grinding process. Such an operation, in one embodiment, removes ten (10) microns or less of total wafer thickness. In this manner, etcher 330 operates to remove less wafer material than in prior art etch processes. Further, the present invention requires less etchant solution, and hence poses fewer environmental problems related to disposal of the acids or other etchants.

Wafer metrology is then tested at a metrology station 328. In one embodiment wafer metrology is tested subsequent to grinding on grinder 318, and prior to the etching within etcher 330. Alternatively, wafer metrology is tested subsequent to etching in etcher 330. In still another embodiment, wafer metrology is tested both prior to and subsequent to the etching process. Evaluation of wafer metrology involves the testing of wafer flatness and other wafer characteristics to ensure the wafer conforms to the desired specifications. If the wafer does not meet specifications, the wafer is placed in a recycle area 342, which in one embodiment comprises a FOUP 342 (not shown in Fig. 3A). Wafers with acceptable specifications are placed in an out portal or FOUP 340 for removal from first module 300.

As shown and described in conjunction with Fig. 3A, first module 300 provides an enclosed clean room environment in which a series of process steps are

performed. Wafers are processed in series through first module 300. Hence, each wafer has generally uniform or uniform process time through the module as well as generally uniform or uniform delay times between process steps. Further, by immediately cleaning and etching the wafer after grinding, the formation of haze and light point defects (LPD) within the wafer
5 are reduced. Such a module configuration is an improvement over the prior art in which wafers are typically processed during the lapping step in batch mode. As a result, some wafers will wait longer before the cleaning or etching steps than others within the same batch. As a result, haze and other wafer defects vary from wafer to wafer, even between wafers within the same batch. Such a shortcoming of the prior art can make it difficult if not
10 impossible to isolate problems within the wafer process flow in the event defective wafers are discovered.

An additional benefit of first module 300 is its compact size. In one embodiment, module 300 has a width 342 that is about 9 feet 3 inches and a length 344 that is about 12 feet 6 inches. In another embodiment, first module 300 has a footprint between
15 about ninety (90) square feet (sqft) and about one hundred and fifty (150) square feet. It will be appreciated by those skilled in the art that the width and length, and hence the footprint of first module 300, may vary within the scope of the present invention. For example, additional grinders 318, 320 may be added within first module 300 to increase the footprint of module 300. In one embodiment, first module 300 is adapted to process about thirty (30)
20 wafers per hour. In another embodiment, first module 300 is adapted to process between about twenty-nine (29) and about thirty-three (33) 300mm wafers per hour.

Fig. 3B depicts an alternative embodiment of a grind damage cluster module according to the present invention. Again, the grind damage cluster module 350 may correspond to first module 216 described in conjunction with Fig. 2. Module 350 includes
25 many of the same components as the embodiment depicted in Fig 3A, and like reference numerals are used to identify like components. Module 350 receives wafers or substrates to be processed at portal 312, identified as a send FOUP 312 in Fig. 3B. Wafers are transferred by transfer device 314, shown as wet robot 314, to a preprocessing station 354. In one embodiment, transfer device 314 travels on a track, groove, raised member or other
30 mechanism which allows transfer device 314 to reach several process stations within module 350.

At preprocessing station 354, a coating is applied to one side of the wafer. In one embodiment, a polymer coating is spun on the wafer to provide exemplary coverage. This coating then is cured using ultraviolet (UV) light to provide a low shrink, rapid cured

coating on one side of the wafer. In addition to UV curing, curing of the coating may be accomplished by heating and the like. In a particular embodiment, the coating is applied to a thickness between about five (5) microns and about thirty (30) microns.

Once cured, the coating provides a completely or substantially tack free, stress free surface on one side of the wafer. In one embodiment of the present invention, transfer device 314 transfers the wafer to grinder 318, placing the polymer-coated side down on the grinder 318 platen. In one embodiment, the platen is a porous ceramic chuck which uses a vacuum to hold the wafer in place during grinding. The waves created during wafer slicing are absorbed by the coating and not reflected to the front side of the wafer when held down during the grinding process. After the first wafer side is ground on grinder 318, the wafer is flipped over and the second side is ground. As described in conjunction with Fig. 3A, an in situ clean of the wafer may occur before turning the wafer, or the wafer may be cleaned subsequent to grinding of both sides. Again, the second side grinding may occur on grinder 318 or grinder 320. Grinding of the second side removes the cured polymer, and a portion of the second wafer surface resulting in a generally smooth wafer on both sides, with little to no residual surface waves. Additional details on exemplary grinding apparatus and methods of the present invention are discussed in conjunction with Figs. 7A and 7B.

After grinding on grinder 318 and/or 320, the wafer is transferred to a combined etch/clean station 352 for wafer etch. Again, wafer etching in station 352 removes a smaller amount of wafer material, and hence requires a smaller amount of etchant solutions, than is typically required by prior art processes.

Processing continues through module 350 ostensibly as described in Fig. 3A. The wafer metrology is tested at metrology station 328. Wafers having desired characteristics are transferred by transfer device 336, shown as a dry robot, to out portals 340, identified as receive FOUPS 340 in Fig. 3B. Wafers having some shortcoming or undesirable parameter are placed in a recycle area 342, shown as a buffer FOUP 342, for appropriate disposal.

In one embodiment, module 350 has a width 342 at its widest point of about one hundred and fourteen (114) inches, and a length at its longest point of about one hundred and forty-five inches (145), with a total footprint of about one hundred and fourteen square feet (114 sqft). As will be appreciated by those skilled in the art, the dimensions and footprint of module 350 may vary within the scope of the present invention.

Still another embodiment of a grind damage cluster module according to the present invention is shown in Fig. 3C. Fig 3C depicts a first module 360 having similar

stations and components as module 350 described in Fig. 3B. However, module 350 is a flow through module, with wafers being received at one end or side of module 350 and exiting an opposite end or side of module 350. Module 360 has FOUPS 312, 342 and 340 grouped together. Such a configuration provides a single entry point into module 360, and hence into clean room environment 310. Transfer devices 314 and 336 again facilitate the movement of wafers from station to station within module 360. As shown in Figs. 3B and 3C, transfer device 314 travels on mechanism 316, as discussed in conjunction with Fig. 3B. Transfer device 336 operates from a generally fixed position with arms or platens extending therefrom to translate the wafer to the desired processing station. Module 360 further includes station 354 for application of a wafer coating, such as the UV cured polymer coating described above.

Turning now to Fig. 4, an exemplary second module comprising an edge profile and edge polishing module will be described. Second module 400 again includes a clean room environment 410 to facilitate clean operations. Second module 400 has a portal 412 for receiving wafers to be processed. Again, in one embodiment, portal 412 is one or more FOUPs. A robot or other transfer device 414 operates to take a wafer from portal 412 and transfer the wafer to an edge profiler/polisher 418. Edge profiler/polisher 418 may comprise one device, or two separate devices with the first device for profiling and the second device for polishing. Transfer device 414 may travel down a track 416 to permit proper placement of the wafer in the edge profiler/polisher 418.

The edge of the wafer is profiled and polished as described in conjunction with Fig. 2. In one embodiment, edge profiling removes about ten (10) microns to about fifty (50) microns of material from the diameter of the wafer, with a resultant diameter tolerance of about +/- 0.5μ. After edge profiling and polishing, a transfer device 420 operates to transfer the wafer to a cleaner 430. Again, transfer device 420 may travel on a track 422 to place the wafer in cleaner 430. Cleaner 430 may comprise a mixture of dilute ammonia, peroxide, and water, or an ammonia peroxide solution and soap, followed by an aqueous clean, and the like.

Subsequent to cleaning in cleaner 430, the wafer is transferred to a metrology station 432 at which wafer metrology is examined. An out-portal 434 is positioned to receive wafers having successfully completed processing through second module 400. In one embodiment, portal 434 is a FOUP which collects wafers meeting desired specifications. Again, rejected wafers are set aside in a separate area or FOUP.

Second module 400 has a compact configuration similar to first module. In one embodiment, second module 400 has a width 450 of about 7 feet 6 inches and a length 460 of about 22 feet 11 inches. In another embodiment, second module 400 has a footprint between about ninety (90) square feet (sqft) and about one hundred and fifty (150) square
5 feet. The module 400 shown in Fig. 4 may be used to carry out process step 222 depicted in Fig. 2. In one embodiment, second module 400 processes about thirty (30) wafers per hour. In another embodiment, second module 400 is adapted to process between about twenty-nine (29) and about thirty-three (33) 300mm wafers per hour. In still another embodiment, second module 400 processing occurs prior to first module 300 processing. In this manner, edge
10 profile and/or edge polish procedures occur before wafer grinding.

Fig. 5A depicts a third module 500 comprising a double side polisher for use in process step 224 shown in Fig. 2. Module 500 again includes an in-portal 512 which may be one or more FOUPs in one embodiment. Wafers are received in portal 512 and transferred within a clean room environment 510 by a transfer device 514. Transfer device 514, which in
15 one embodiment is a robot, may travel along a track 516 to deliver the wafer to one or more double side polishers (DSP) 518.

As shown in Fig. 5A, double side polisher 518 accommodates three wafers 520 within each polisher. It will be appreciated by those skilled in the art that a greater or fewer number of wafers may be simultaneously polished within DSP 518. Prior art double
20 side polishing (DSP) typically polishes a batch of ten or more wafers at a time in a double side polisher. The polisher initially only contacts the two or three thickest wafers due to their increased height within the DSP machine. Only after the upper layers of the thickest wafers are removed by polishing, are additional wafers polished within the batch. As a result, the batch mode polishing takes longer, and uses more polishing fluids and deionized water than
25 in the present invention.

Hence in one preferred embodiment of the present invention, three wafers are polished simultaneously. Subsequent to polishing on polisher 518, the wafers are transferred via a transfer device 536, traveling on track 538 to a buffer station 522. Thereafter, the wafers are buffed, cleaned and dried. Either prior to or after processing through station 522,
30 or both, wafers are tested at a metrology station 540. For wafers meeting desired specifications, transfer device 536 transfers those wafers to an out-portal 544, again, one or more FOUPs in one embodiment. Wafers which do not meet specifications are placed in a reject FOUP 542.

As with prior modules, the third module 500 has a compact footprint. In one embodiment, module 500 has a width 546 that is about 13 feet 11 inches and a length 548 that is about 15 feet 11 inches. In another embodiment, third module 500 has a footprint between about one hundred (100) square feet (sqft) and about one hundred and eighty (180)
5 square feet. Third module 500 may have a different footprint within the scope of the present invention.

In one embodiment, DSP 518 removes about twelve (12) microns of wafer thickness from both sides combined, at a rate of about 1.25 to 2.0 microns per minute. DSP 518 operates on a twelve (12) minute cycle time per load. Hence, in one embodiment, two
10 DSPs 518 process about thirty (30) wafers per hour. In another embodiment, third module 500 is adapted to process between about twenty-nine (29) and about thirty-three (33) 300mm wafers per hour. It will be appreciated by those skilled in the art that DSP 518 process times, third module 500 throughput, and other parameters may vary within the scope of the present invention. For example, additional DSPs 518 may be added to increase module 500
15 throughput. In one embodiment, wafer metrology tested at metrology station 540 is fed back to DSPs 518 to adjust DSP 518 operation as needed to produce desired wafer metrology.

Fig. 5B depicts an alternative embodiment of a third module according to the present invention. As shown in Fig. 5B, third module 550 comprises a double side polisher for use in process step 224 shown in Fig. 2, as well as several other components shown in
20 Fig. 5A. As a result, like components are identified with like reference numerals. Module 550 includes a clean/dry station 552 for wafer cleaning and drying subsequent to wafer polishing in polisher 518. Transfer devices 514 and 536, shown as a wet robot and a dry robot, respectively, operate to transfer wafers within module 550. In one embodiment, transfer device 514 travels on a track, groove, raised feature or the like to reach several
25 processing stations and portals 512, while transfer device 536 operates from a fixed base.

While module 500 in Fig. 5A is a flow through module, with wafers received by module 500 at one side and exiting from an opposite side, module 550 in Fig. 5B groups portals 512 and 544. Again, such a grouping of in and out portals facilitates access to module 550 from a single point or side. In one embodiment, a buffer or reject FOUPS (not shown)
30 also is grouped with portals 512 and 544. Alternatively, one or more of portals 512 and 544 may operate as a reject FOUPS.

Third module 550, in one embodiment, has a compact footprint with a width 546 at the widest point of about one hundred and forty two (142) inches and a length at the longest point of about one hundred and fifty-five inches (155).

Turning now to Fig. 6, a fourth module 600, comprising a finish polish cluster, will be described. Fourth module 600 in one embodiment will be used for process step 226 shown in Fig. 2. As with the prior modules, fourth module 600 defines a clean room environment 610 which has ingress and egress through one or more portals or FOUPs. For example, an in-portal or FOUP 612 receives a plurality of wafers for finish polishing. Wafers are removed from FOUP 612 and transferred by a transfer device 614 along a track 616 to a finish polisher 618. While two finish polishers 618 are depicted in Fig. 6, a larger or smaller number of polishers 618 may be used within the scope of the present invention.

Wafers are finish polished for about five (5) to six (6) minutes within finish polisher 618 in an embodiment. Wafers that have undergone finish polishing are transferred to a single wafer cleaner 630 by a transfer device 636. Again, transfer device 636 in one embodiment comprises a robot that travels along a track 638. After wafer cleaning at cleaner station 630, wafer metrology is again tested at a metrology station 640. In one embodiment, metrology processing within fourth module 600 uses a feedback loop to provide data to finish polishers 618 as a result of wafer metrology testing. In one embodiment, the feedback loop is of sufficiently short duration to permit adjustments to the finish polisher process prior to the polishing of the next wafer after the wafer being tested. Wafers which do not meet specification are placed in a reject FOUP or portal 642 for proper disposal. Wafers meeting specifications will be placed in an out-portal or FOUP 644 for subsequent processing, packaging and shipping.

Fourth module 600, in one embodiment, has a width 650 of about 14 feet 0 inches and a length 660 of about 16 feet 0 inches. In another embodiment, fourth module 600 has a footprint between about one hundred (100) square feet (sqft) and about one hundred and eighty (180) square feet. Again, as with all prior modules, the exact size may vary within the scope of the present invention. In one embodiment, fourth module 600 processes about thirty (30) wafers per hour. In another embodiment, fourth module 600 is adapted to process between about twenty-nine (29) and about thirty-three (33) 300mm wafers per hour.

In one embodiment, the four modules 300, 400, 500 and 600, or their alternative embodiments, and ancillary equipment take up about 4,000 square feet or less of a production facility. This total footprint is much smaller than required for prior art equipment performing similar processes. As a result, apparatus, systems and methods of the present invention may be incorporated more readily in smaller facilities, or as part of a device fabrication facility in which circuit devices are formed. In this manner, the time and cost of packing and shipping, as well as unpacking and inspecting, are avoided. The costs of packing

and shipping can, for example, save on the order of about two (2) percent or more of the total wafer processing costs.

Turning now to Figs. 7A and 7B, exemplary methods and apparatus for grinding a wafer will be described. In one embodiment, a wafer or substrate 710 having
5 thickness variations between two sides is provided. An apparatus 700 has a platen 712, on which is placed substrate 710 to be planarized by grinding. An applicator or dispenser 714 applies a curable liquid to a first surface 724 of substrate 710. In this case, first surface 724 is an upper surface, although different wafer orientations are within the scope of the present invention. The curable liquid, in one embodiment, comprises a liquid polymer, a liquid resin,
10 an acrylic, an epoxy, and the like. In a particular embodiment, the curable material is an acrylic or epoxy obtained from Lens Technology LLC in La Mirada, California.

In one embodiment, the curable liquid is applied using a spin-on process. For example, platen 712, and hence substrate 710, may be rotated about an axis 718 as indicated by arrow 720. Preferably, rotation of platen 712 is in a continuous 360° fashion, and may be
15 clockwise or counterclockwise. By rotating platen 712 simultaneous with the spraying or application of a curable liquid by applicator 714, the liquid spreads out over surface 724. By controlling the curable liquid viscosity, dispense time, dispense rate, and/or the wafer 710 angular velocity, the film thickness formed by the curable liquid may be controlled.

Preferably, apparatus 700 includes a curer 716. Curer 716 is adapted to cure
20 the spun-on curable liquid in order to harden the liquid onto surface 724. In alternative embodiments, curer 716 provides an electromagnetic energy, an ultraviolet light, and the like. Additionally, curer 716 may be a heat source, such as a heat lamp, for use with curable liquids that are cured using elevated temperatures. While shown coupled to applicator 714, curer 716 may be a separate device uncoupled from applicator 714. As previously described
25 in conjunction with Fig. 3B, the curable liquid, when hardened, forms a substantially planar or smooth upper surface notwithstanding any surface irregularities, waves or undulations otherwise present in surface 724. In one embodiment, surface 724, having a coating or film of hardened curable liquid or polymer, is placed on platen 712. In one embodiment, apparatus 700 includes a grinder 722 which is positioned over substrate 710 to facilitate
30 grinding processes thereof.

Turning now to Fig. 7B, an exemplary method 740 according to the present invention will be described. The method includes providing a substrate or wafer having surface irregularities or thickness variations to be removed (Step 745). Such surface irregularities may comprise generally horizontal lines or grooves formed in surface 724

during wire saw operation to cut substrate 710 from the boule. A curable liquid, such as a curable polymer, resin and the like is applied (750) to surface 724. Thereafter the liquid is cured to a hardened state (755), and the substrate is positioned (760) on the grinding apparatus platen with the surface 724 side down. Thereafter, the non-cured side of the wafer,
5 surface 726, is ground (765) to be planar or substantially planar. An optional clean procedure (770) may be formed on wafer 710, such as on surface 726. Once wafer surface 726 has been ground, the substrate is repositioned (775) to place surface 726 on platen 712. Thereafter, grinder 722 grinds both the cured coating and a portion of wafer surface 724 (Step 780). Thereafter, an optional wafer clean may be performed (785).

10 Another particular embodiment of the present invention will now be described. Substrate 710 having surface irregularities and/or thickness variations is coupled to platen 712 and cleaned. In one embodiment, substrate 710 cleaning comprises applying RCA1, SC1, some combination of ammonia, peroxide and water, or the like, to substrate 710 for about ten (10) to about fifteen (15) seconds while platen 712 and substrate 710 are spun.
15 Substrate 710 is dried through the application of isopropyl alcohol (IPA) or the like, again while spinning, with the spinning accelerating up to about 1,200 to about 1,800 revolutions per minute (RPM).

Applicator 714 then dispenses the curable material on wafer 710 for a duration sufficient to wet all or substantially all of first surface 724. Curable material may flow over
20 the peripheral edges of substrate 710. The platen speed during dispensing ranges from about sixty (60) RPM to about one hundred and eighty (180) RPM in one embodiment. In an alternative embodiment, applicator 714 is rotated or spun during dispensing. In one embodiment, the volume of curable material used ranges from about 10 milliliters (ml) to about 25 ml, although the volume may differ from this amount depending in part on the
25 substrate 710 size and surface 724 topography. In an embodiment, apparatus 700 further includes an ultrasound device (not shown) for producing ultrasound energy to facilitate the distribution of curable material over surface 724. In one embodiment, substrate 710 then is rotated at about 800 RPM to about 2,500 RPM for about five (5) to about ten (10) seconds, or longer, after which the substrate is allowed to settle at a lower RPM. Rotating substrate 710
30 after dispensing the curable material helps the material spread over surface 724.

Curer 716 then operates to cure the curable material coating on surface 724. In one embodiment, curer 716 is a UV lamp have a spectrum range of about 250 nm to about 800 nm. In one embodiment, curer 716 is positioned about two (2) to about six (6) inches from first surface 724, and in a particular embodiment is positioned about three (3) inches

from surface 724, while curer 716 applies electromagnetic energy to surface 724. In one embodiment, substrate 710 is spun during the application of electromagnetic energy. As a result, the coating of surface 724 fills or substantially fills the undulations in surface 724. In some embodiments, the coating has a thickness ranging from about five (5) microns to about forty (40) microns, from about fifteen (15) microns to about thirty (30) microns, and from about fifteen (15) to about forty (40) microns. The coating is a hard, substantially scratch resistant material that is relatively uncompressed. As a result, no thermal gradients are formed, and little to no localized stresses are formed due to thermal mismatches that may otherwise occur when waxes or other adhesives are used. Grinding operations as described herein ensue.

Hence, as provided in methods of the present invention, the cured coating provides a substantially planer and hard surface on which to mount the substrate. By doing so, wafer surface 726 may be ground flat with little to no surface reflection resulting from irregularities in wafer surface 724. The cured coating and wafer surface 724 then are subjected to grinding processes. As a result, a substantially planar wafer having generally uniform thickness between two opposite sides is produced. Local uniformity also is improved.

The present invention is an improvement over prior art attempts to solve the residual wave problems, such as by the use of grease or wax on one side of the wafer. The present invention also improves upon the use of thin resilient pads, in lieu of grease or wax, disposed between platen 712 and wafer 710. For example, the use of resilient pads, while potentially acceptable for one or a few wafers, cannot be made to act repetitively due to material fatigue. As a result, these pads may wear, leading to processing inconsistency. Additionally, these resilient pads may pose a limitation in terms of system cleaning, as particles generated during the grinding process become embedded in the thin pad. Increased wafer defects and part breakages may occur. Alternatively, new pads must be used for each wafer processed, a cost prohibitive, undesirable alternative.

A number of benefits result from the above-described apparatus and methods of the present invention. For example, each wafer uses a fresh film of polymer, resin, or the like, thus avoiding any issues related to wear and tear of the pads, platens and the like. Also, the coating may be ground off the wafer, thereby avoiding environmental issues otherwise associated with cleansing solutions used to clean grease, wax, or the like that may otherwise be used to hold the wafer during grinding. Further, the cured coating protects the wafer backside during grinding procedures and from chemical attack that may otherwise occur.

Still further, the intimate contact of the wafer surface with the cured coating, due to interfacial Van der waals forces, insures a more homogeneous force distribution during the grinding process. The cured coating provides a stress free or substantially stress free wafer-coating interface, as well as coating removal. As a result, the wafer suffers less surface distortion and produces better wafer-to-wafer consistency.

A schematic of a method of processing wafers 800 according to the present invention is shown in Fig. 8. Method 800 includes providing a wafer (Step 810), which typically has thickness variations between its two primary surfaces. The wafer sides are ground (Step 820) and polished (Step 830). The wafer then undergoes a cleaning process (Step 840), although additional cleaning processes may be used throughout the method. The wafer, having desired specifications, is then transferred to a wafer processing chamber (Step 850). The wafer processing chamber is located in a same facility as the equipment for performing the other method steps, including grinding, polishing and cleaning. In this manner, the transferring of the wafer may occur by way of a robot or other transfer mechanism within the facility. The present invention reduces or eliminates the need for additional cleaning, packing, shipping, unpacking, cleaning and inspecting steps prior to placing the wafer in a processing chamber. As a result, a more efficient, streamlined process is realized.

Once the wafer has been positioned in the processing chamber, device formation processes are performed on the wafer (Step 860). These processes may include, but are not limited to, depositing a dielectric layer on the wafer (Step 870), depositing a conductive layer on the wafer (Step 880), performing thermal oxidation, etching, photolithography, annealing, electroplating and a number of other processes known to those skilled in the art.

The invention has now been described in detail for purposes of clarity and understanding. However, it will be appreciated that certain changes and modifications may be practiced within the scope of the appended claims. For example, the modules may have different layouts, dimensions and footprints than as described above. Additionally, transfer devices that have been described as traveling or fixed, may also be fixed or traveling, respectively.

WHAT IS CLAIMED IS:

1 1. A method of processing a wafer, comprising:.
2 providing a wafer having initial thickness variations between two
3 surfaces of said wafer;
4 processing said wafer through a first module, said first module
5 comprising apparatus for performing a grinding process, a clean process and a metrology
6 process, and said processing therethrough includes said grinding process, said clean process
7 and said metrology process;
8 defining an edge profile on said wafer; and
9 processing said wafer through a second module, said second module
10 comprising apparatus for performing a double side polish (DSP) process, a clean process and
11 a metrology process, and said processing therethrough includes said DSP process, said clean
12 process and said metrology process.

1 2. The method of claim 1 wherein said first module processing further
2 comprises an etch process, said etch process reducing said wafer thickness by less than about
3 ten (10) microns.

1 3. The method of claim 1 wherein said first module processing precedes
2 said defining said edge profile.

1 4. The method of claim 1 wherein said first and second modules each
2 comprise a cluster tool defining a clean room environment.

1 5. The method of claim 1 wherein said first module metrology process is
2 simultaneous with said grinding process.

1 6. The method of claim 5 wherein said first module metrology process
2 produces a metrology profile for said wafer, said processing through said first module further
3 comprising modifying said grinding process in response to said metrology profile.

1 7. The method of claim 1 wherein said first module metrology process is
2 after said grinding process.

1 8. The method of claim 1 further comprising polishing said edge of said
2 wafer after said defining said edge profile.

1 9. The method of claim 1 further comprising processing said wafer
2 through a third module, said third module comprising apparatus for performing a finish polish
3 process, a clean process and a metrology process, and wherein said processing through said
4 third module comprises said finish polishing process, said clean process and said metrology
5 process.

1 10. The method of claim 9 further comprising, after completion of said
2 processing through said third module, providing said wafer directly to a process chamber for
3 fabrication of a semiconductor device.

1 11. The method of claim 9 further comprising, in order after completion of
2 said processing through said third module, cleaning said wafer, inspecting said wafer,
3 packaging said wafer, and delivering said wafer to a wafer process facility for subsequent
4 fabrication of a semiconductor device.

1 12. The method of claim 1 wherein said wafer has a total thickness
2 variation (TTV) between said two surfaces of less than about 0.3 microns after said
3 processing through said second module.

1 13. The method of claim 1 wherein said wafer has a SFQR of less than
2 0.12 microns after said processing through said second module.

1 14. The method of claim 1 further comprising processing said wafer
2 through at least a portion of said first module prior to processing a second wafer through said
3 first module.

1 15. The method of claim 1 further comprising laser marking said wafer
2 prior to said defining said edge profile.

1 16. The method of claim 1 further comprising performing a donor anneal
2 process prior to said defining said edge profile.

1 17. The method of claim 1, further comprising processing said wafer
2 through a third module, said third module comprising apparatus for performing said defining
3 said edge profile, and an edge polishing process, said processing through said third module
4 comprising said defining said edge profile and said polishing said wafer edge.

1 18. A method of processing a wafer prior to device formation thereon, said
2 method comprising, in order:
3 providing a wafer having first and second surfaces and a peripheral
4 edge;
5 grinding said first and second wafer surfaces;
6 defining an edge profile of said wafer, and polishing said peripheral
7 edge; and
8 polishing said first and second wafer surfaces.

1 19. A wafer processing system, comprising:
2 a grinder for grinding first and second wafer surfaces;
3 an etcher for etching said wafer;
4 a cleaner for cleaning said wafer; and
5 a metrology tester for testing a metrology of said wafer;
6 wherein said grinder, etcher, cleaner and metrology tester are
7 contained within a first clean room environment.

1 20. The wafer processing system as in claim 19 further comprising a
2 transfer mechanism adapted to transfer said wafer from said grinder to said etcher within said
3 first clean room environment.

1 21. The wafer processing system as in claim 20 wherein said transfer
2 mechanism comprises a robot.

1 22. The wafer processing system as in claim 19 further comprising a
2 second clean room environment, said second clean room environment comprising:
3 an edge grinder for defining an edge profile of said wafer; and
4 an edge polisher for polishing said wafer edge.

1 23. The wafer processing system as in claim 19 further comprising a third
2 clean room environment, said third clean room environment comprising:
3 a polisher for polishing said wafer;
4 a cleaner for cleaning said wafer; and
5 a metrology tester for testing said wafer metrology.

1 24. The wafer processing system as in claim 19 further comprising a fourth
2 clean room environment, said fourth clean room environment comprising:
3 a finish polisher for polishing said wafer;
4 a cleaner for cleaning said wafer; and
5 a metrology tester for testing said wafer metrology.

1 25. A wafer processing system, comprising:
2 means for grinding said wafer;
3 means for cleaning said wafer;
4 means for testing a wafer metrology;
5 wherein said means for grinding, cleaning and testing are contained
6 within a single clean room environment; and
7 means for transferring said wafer between said means for grinding and
8 said means for cleaning, within said clean room environment.

1 26. A method of processing a wafer, comprising:
2 providing a wafer having initial thickness variations between two
3 surfaces of said wafer;
4 processing said wafer through a first module, said first module
5 comprising apparatus for performing a grinding process and said processing therethrough
6 includes said grinding process;
7 processing said wafer through a second module, said second module
8 comprising apparatus for performing a double side polish (DSP) process, and said processing
9 therethrough includes said DSP process;
10 processing said wafer through a third module, said third module
11 comprising an apparatus for performing a finish polish process, and said processing
12 therethrough includes said finish polish process;
13 cleaning said wafer after said processing through said third module;
14 and
15 thereafter transferring said wafer to a wafer processing chamber within
16 a same facility as that containing said first, second and third modules.

1 27. The method of claim 26 wherein said first module comprises a cluster
2 tool defining a clean room environment.

1 28. The method of claim 26 wherein said second module comprises a
2 cluster tool defining a clean room environment.

1 29. The method of claim 26 further comprising testing said wafer
2 metrology and wherein said transferring said wafer comprises transferring said wafer only if
3 said wafer has a desired flatness profile.

1 30. The method of claim 26 wherein said providing, said processing
2 through said first module, said defining, said processing through said second module, said
3 processing through said third module, said cleaning and said transferring occur in the order
4 listed in claim 1.

1 31. The method of claim 26 wherein said wafer has a total thickness
2 variation (TTV) between said two surfaces of less than about 0.3 microns prior to said
3 transferring.

1 32. The method of claim 26 wherein said wafer has a SFQR of less than
2 0.12 microns prior to said transferring.

1 33. The method of claim 26 further comprising performing a circuit device
2 fabrication process on said wafer within said processing chamber.

1 34. The method of claim 33 wherein said circuit device fabrication process
2 is selected from a conductive layer deposition process and a dielectric layer formation
3 process.

1 35. The method of claim 26 wherein said first module has a footprint
2 between about ninety (90) square feet (sqft) and about one hundred and fifty (150) sqft, and
3 has a capacity of processing between about twenty-nine (29) wafers and about thirty-three
4 (33) wafers therethrough per hour.

1 36. The method of claim 26 wherein said second module has a footprint
2 between about one hundred (100) square feet (sqft) and about one hundred and eighty (180)
3 sqft, and has a capacity of processing between about twenty-nine (29) wafers and about
4 thirty-three (33) wafers therethrough per hour.

1 37. The method of claim 26 wherein said third module has a footprint
2 between about one hundred (100) square feet (sqft) and about one hundred and eighty (180)
3 sqft, and has a capacity of processing between about twenty-nine (29) wafers and about
4 thirty-three (33) wafers therethrough per hour.

1 38. A method of processing a wafer prior to device formation thereon, said
2 method comprising:
3 providing a wafer having first and second surfaces with thickness
4 variations therebetween;
5 grinding said first and second wafer surfaces;
6 polishing said first and second wafer surfaces;
7 cleaning said wafer; and
8 thereafter transferring said wafer to a wafer processing chamber for
9 device formation processes.

1 39. The method of claim 38 wherein said polishing, said cleaning and said
2 transferring all occur in a single wafer fabrication facility.

1 40. The method of claim 38 wherein said transferring comprises
2 transferring said wafer to said wafer processing chamber with a robot.

1 41. The method of claim 38 further comprising depositing a dielectric
2 layer on said wafer within said processing chamber.

1 42. The method of claim 38 further comprising depositing a conductive
2 layer on said wafer within said processing chamber.

1 43. The method of claim 38 wherein said transferring said wafer occurs
2 after said cleaning, and said cleaning and transferring are adapted to provide said wafer to
3 said processing chamber in a wafer condition sufficient for forming an integrated circuit
4 device thereon.

1 44. The method of claim 38 further comprising defining an edge profile of
2 said wafer after said grinding.

1 45. A method of grinding wafers, said method comprising:

2 providing a cut wafer having initial thickness variations between first
3 and second wafer surfaces;
4 applying a polymer to said first surface to form a substantially smooth
5 outer surface;
6 positioning said wafer on a grinding tool; and
7 grinding said second surface to form a substantially planar second
8 surface.

1 46. The method as in claim 45 wherein said applying said polymer
2 comprises applying a liquid polymer to said first surface.

1 47. The method as in claim 46 further comprising curing said liquid
2 polymer before grinding said second surface.

1 48. The method as in claim 47 wherein said curing comprises a heat cure.

1 49. The method as in claim 47 wherein said curing comprises an
2 ultraviolet light cure.

1 50. The method as in claim 47 wherein said curing comprises a cure with
2 electromagnetic energy.

1 51. The method as in claim 45 wherein said applying said polymer forms a
2 polymer film having a thickness between about five (5) microns and about thirty (30)
3 microns.

1 52. The method as in claim 45 wherein said positioning comprises placing
2 said outer surface on a grinding tool platen.

1 53. The method as in claim 45 further comprising grinding said polymer
2 and said first surface.

1 54. The method as in claim 53 further comprising cleaning said second
2 surface prior to said grinding said polymer and said first surface.

1 55. The method as in claim 53 wherein said grinding said second surface,
2 said polymer and said first surface substantially removes said thickness variations.

1 56. The method as in claim 53 wherein said grinding removes substantially
2 all of said polymer, and a portion of said first and second surfaces.

1 57. The method as in claim 45 further comprising:
2 cleaning said wafer after grinding said second surface;
3 repositioning said wafer on said grinding tool to expose said outer
4 surface; and
5 grinding said polymer and said first surface.

1 58. The method as in claim 45 further comprising applying said polymer
2 while simultaneously rotating said wafer.

1 59. A method of preparing a substrate for grinding operations, said method
2 comprising:
3 providing a substrate having first and second surfaces;
4 applying a curable liquid to said first surface;
5 curing said curable liquid to form a substantially smooth outer surface;
6 and
7 positioning said outer surface on a grinding tool platen to expose said
8 second surface to a grinder.

1 60. A wafer grinding apparatus, comprising:
2 an applicator for applying a curable liquid to a wafer surface;
3 a curer for curing said curable liquid;
4 a platen for holding said wafer; and
5 a grinder for grinding said wafer surface.

1 61. The apparatus as in claim 60 further comprising a rotation device
2 coupled to said platen for rotating said wafer.

1 62. The apparatus as in claim 60 wherein said applicator comprises a spin
2 on applicator and said curable liquid comprises a liquid polymer.

1 63. The apparatus as in claim 60 wherein said curer comprises an
2 ultraviolet light source.

1 64. The apparatus as in claim 60 wherein said curer comprises an
2 electromagnetic energy source.

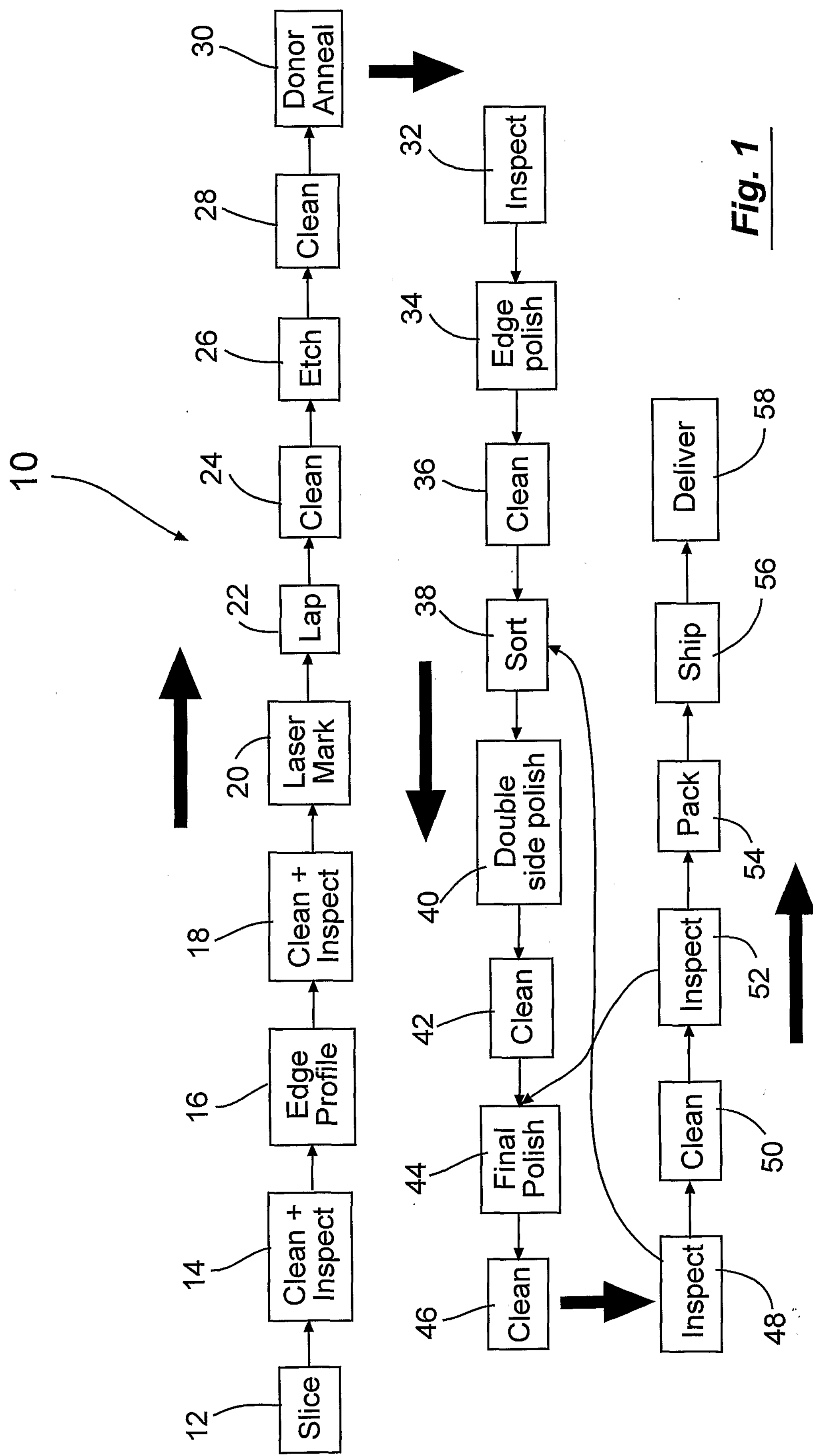


Fig. 1

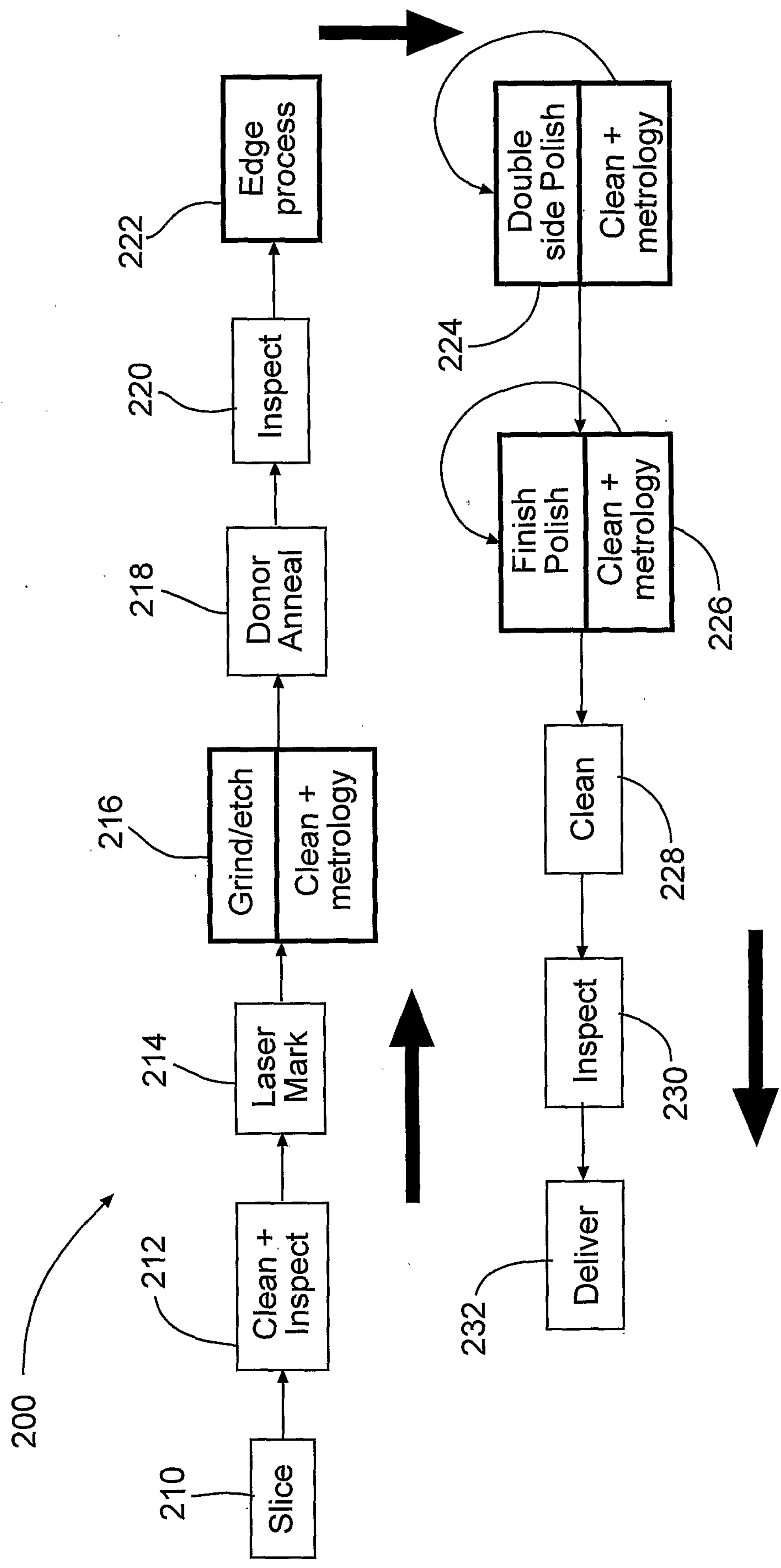


Fig. 2

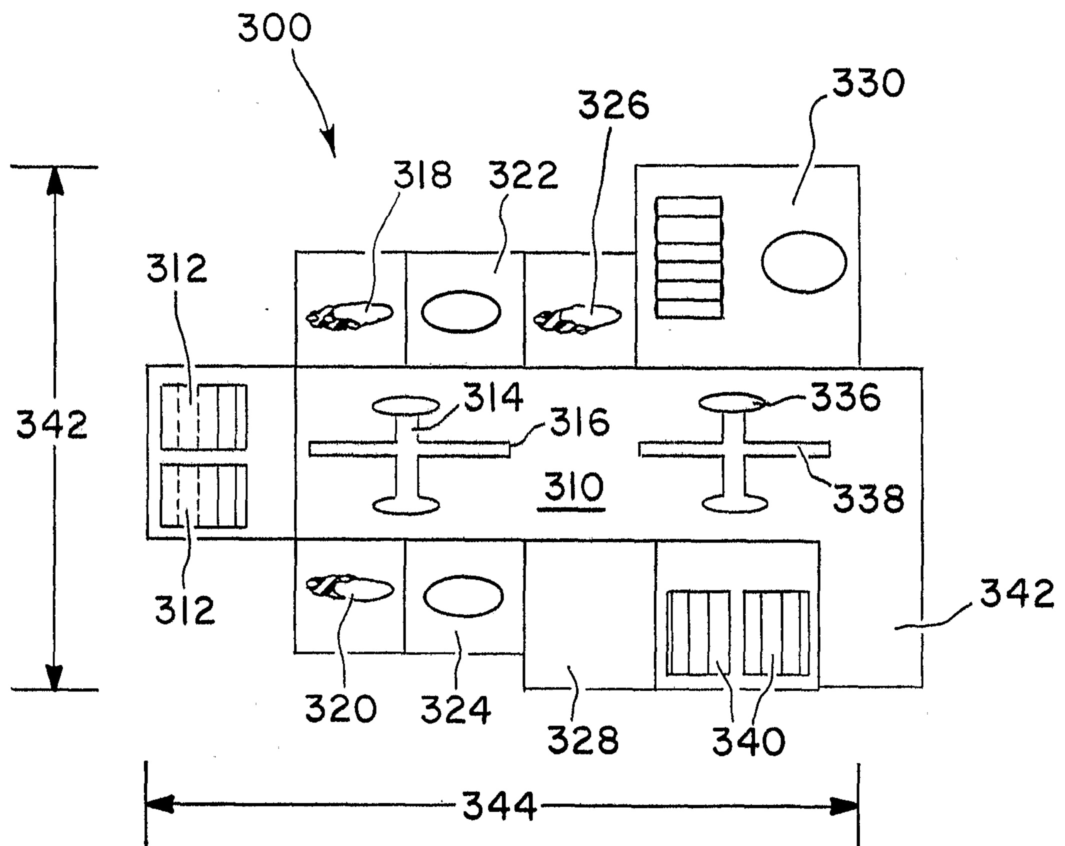


Fig. 3A

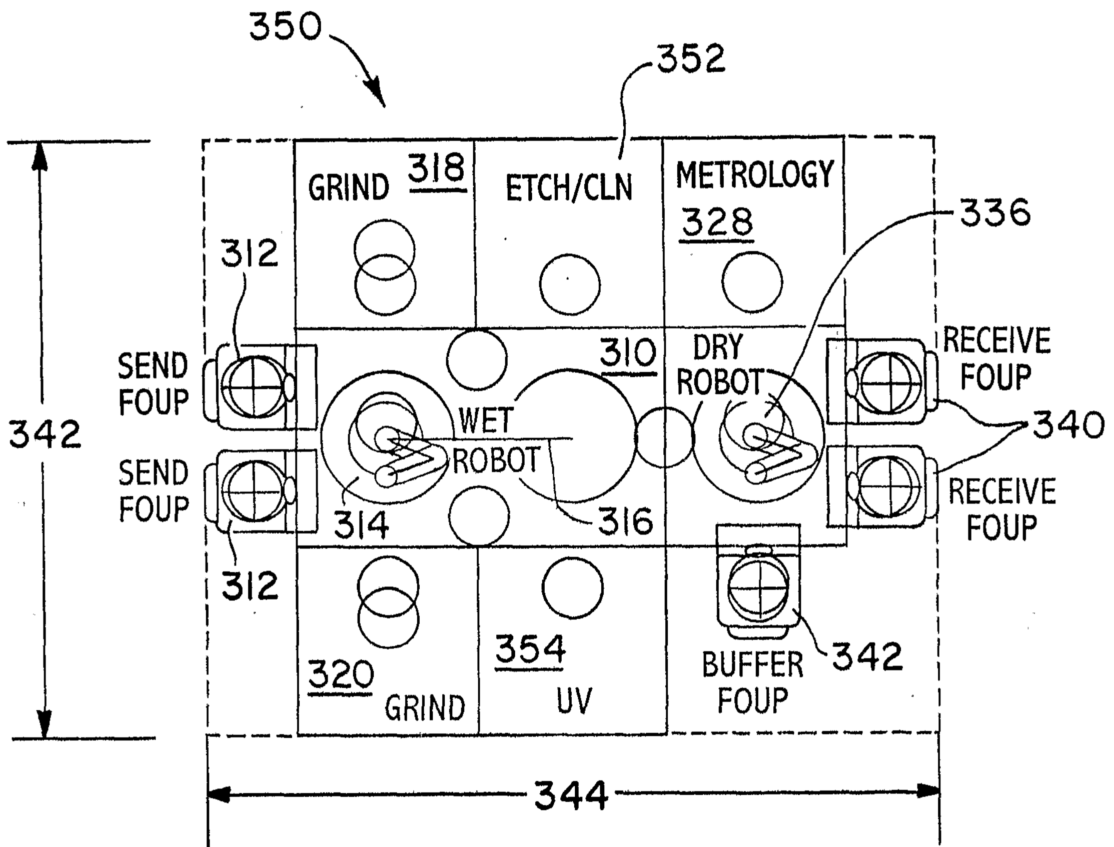


Fig. 3B

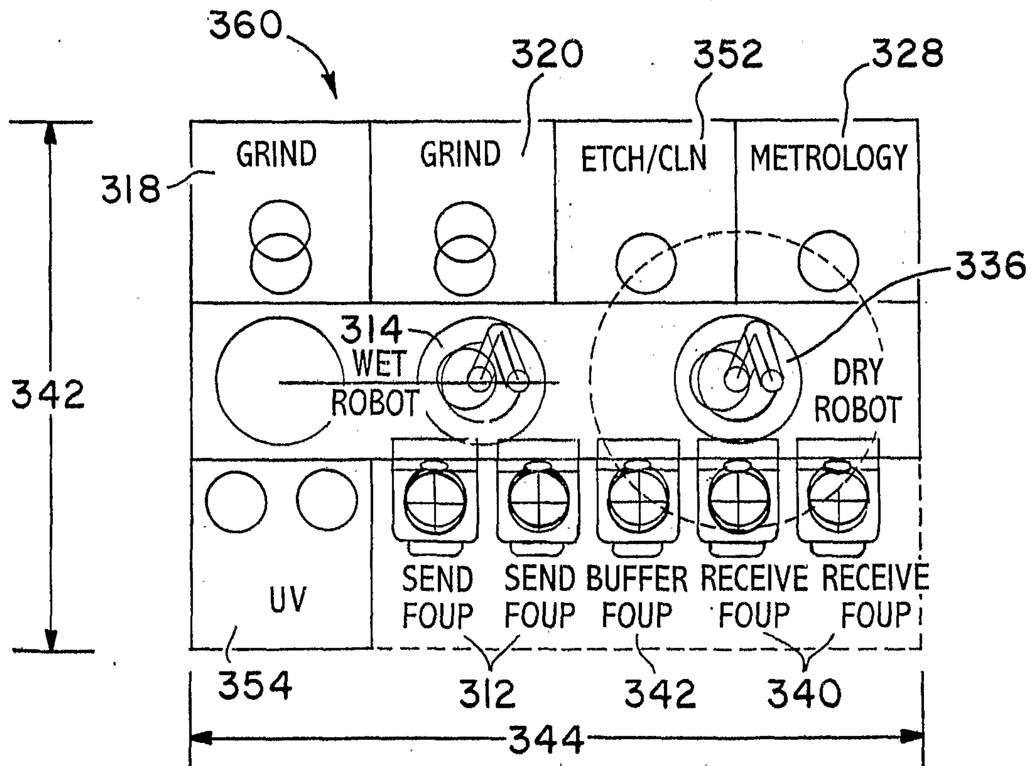


Fig. 3C

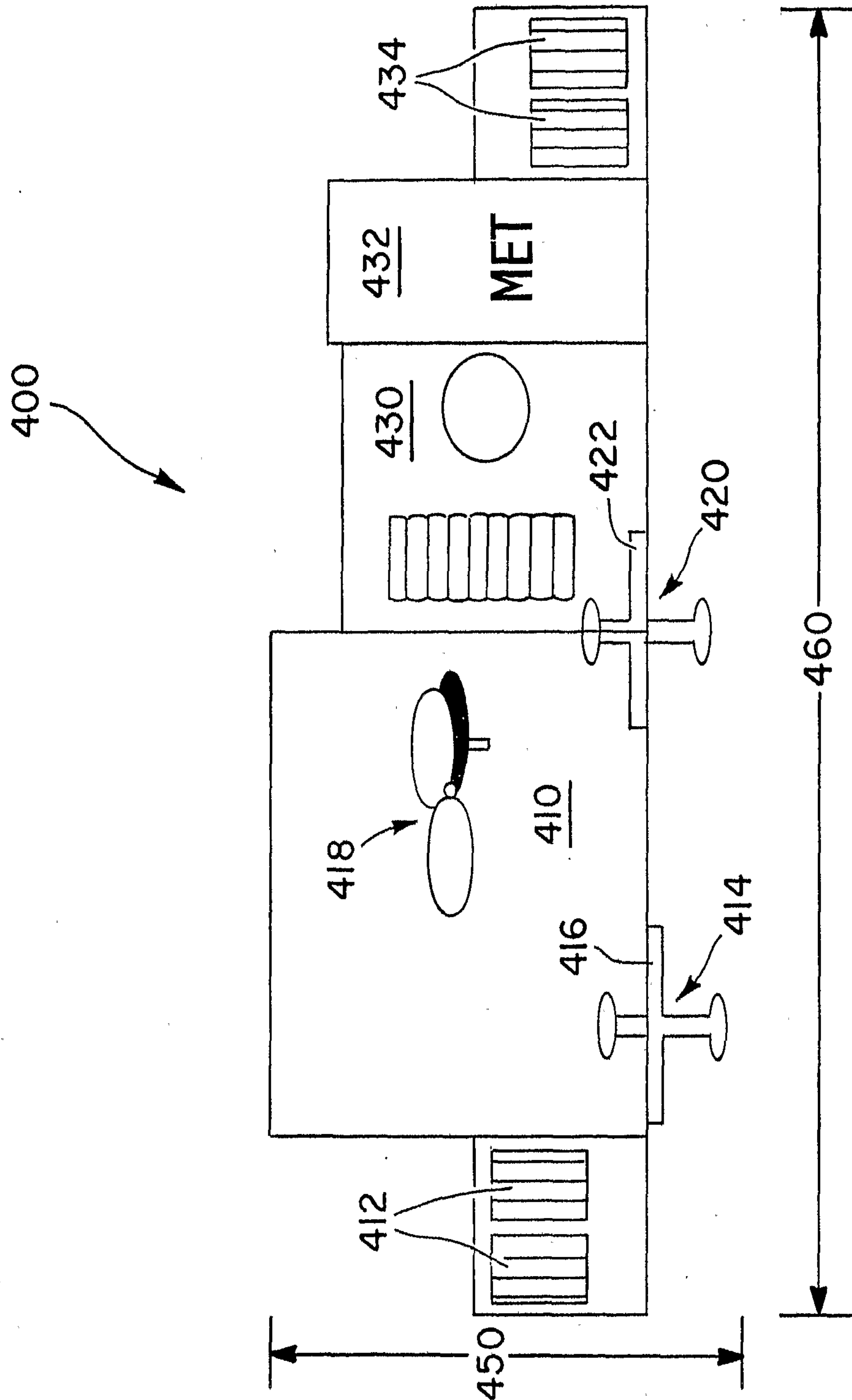

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Fig. 4

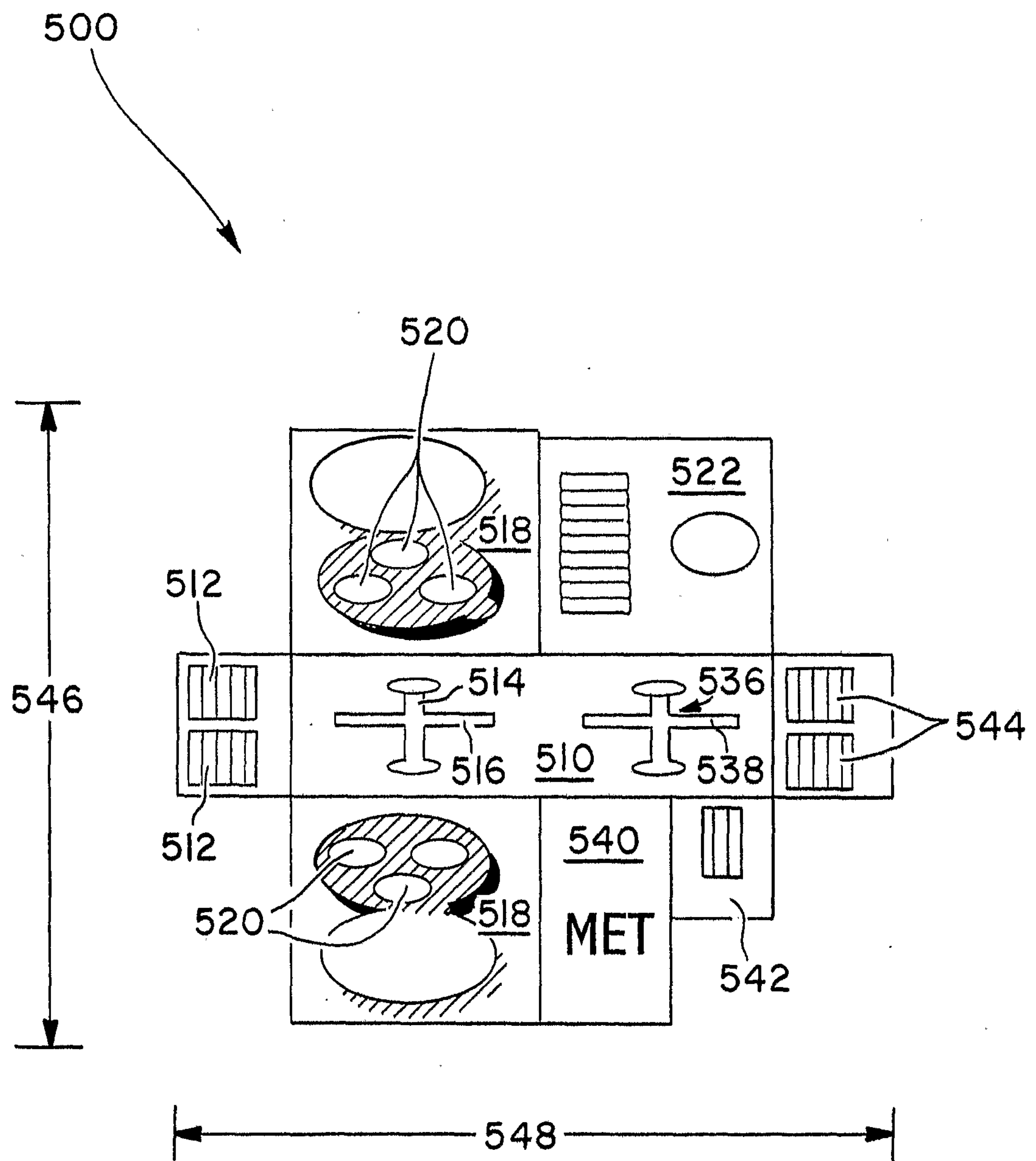

Fig. 5A

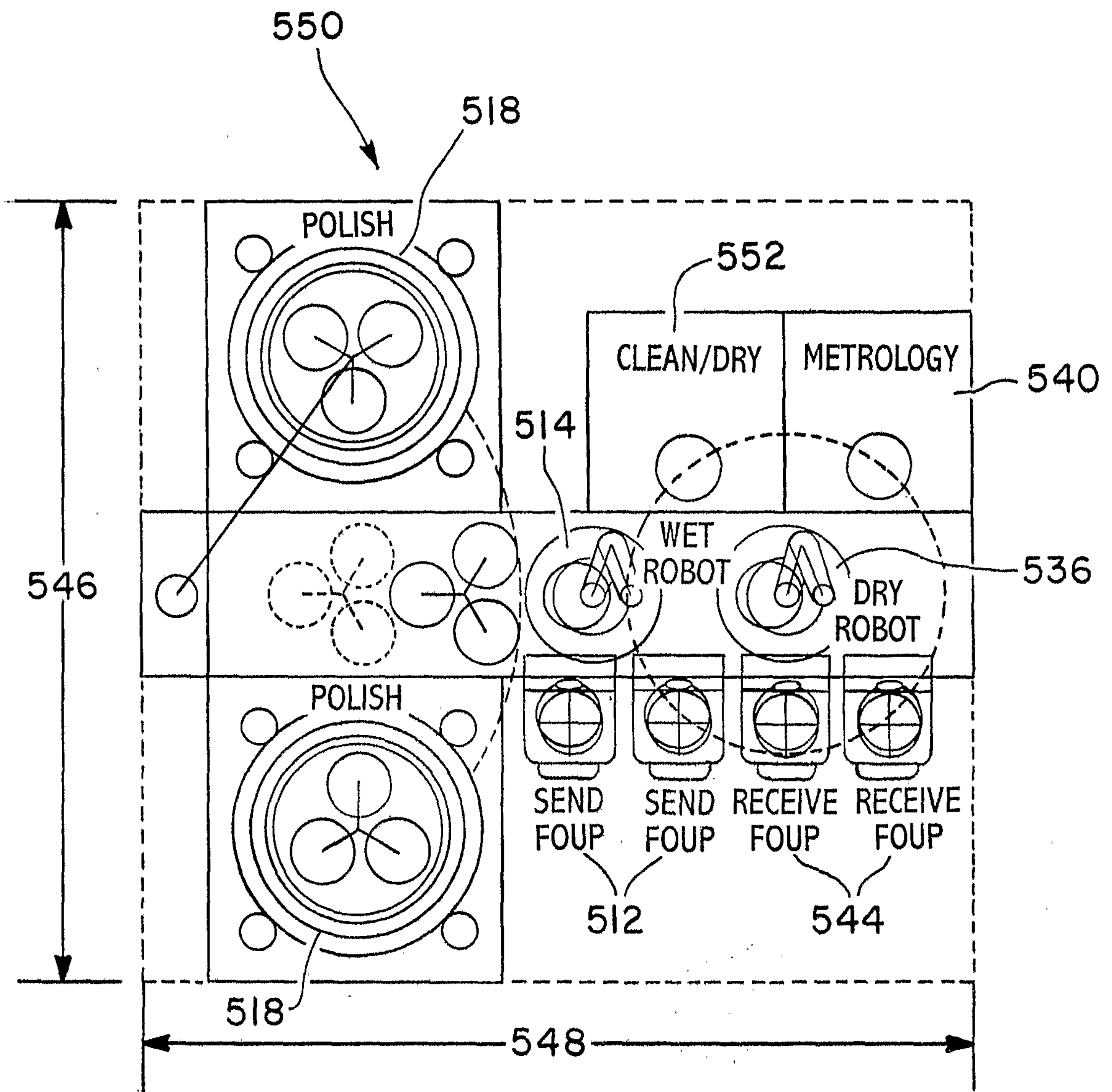

Fig. 5B

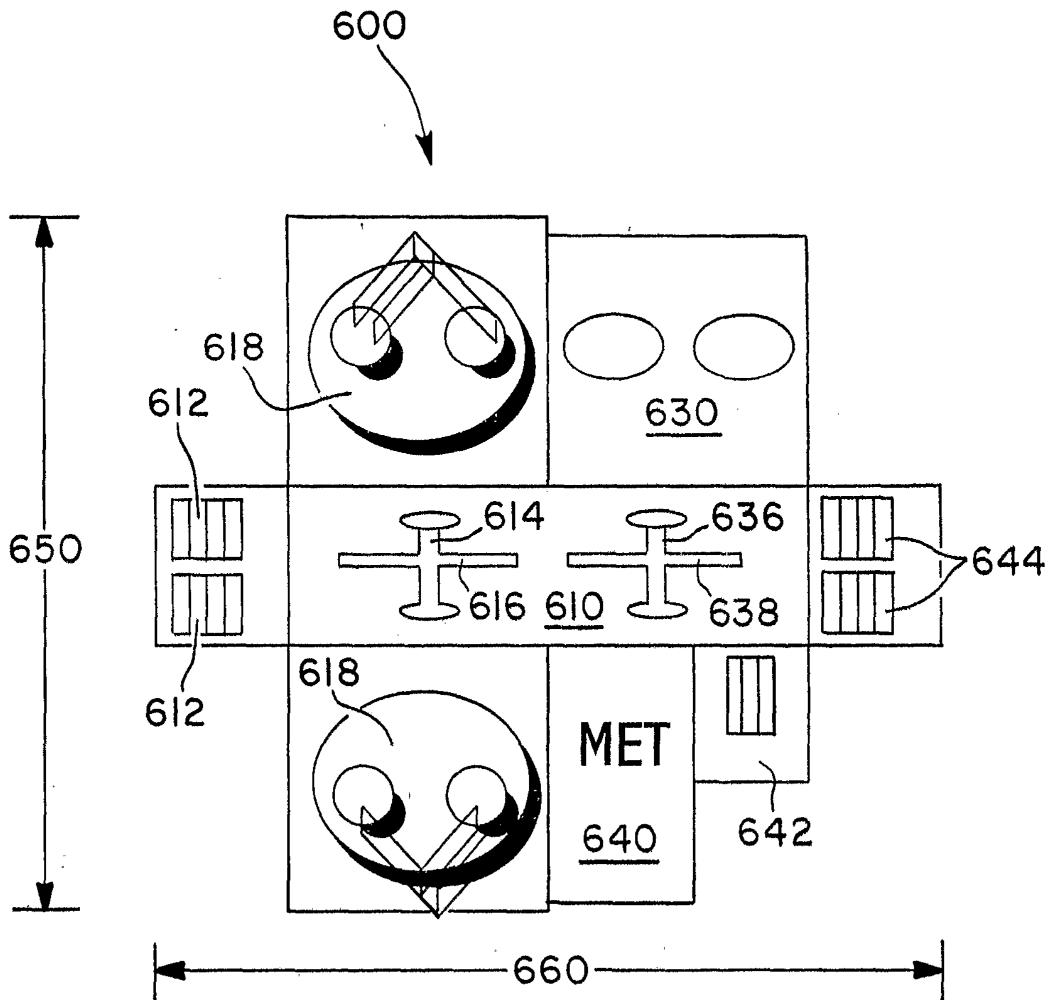

Fig. 6

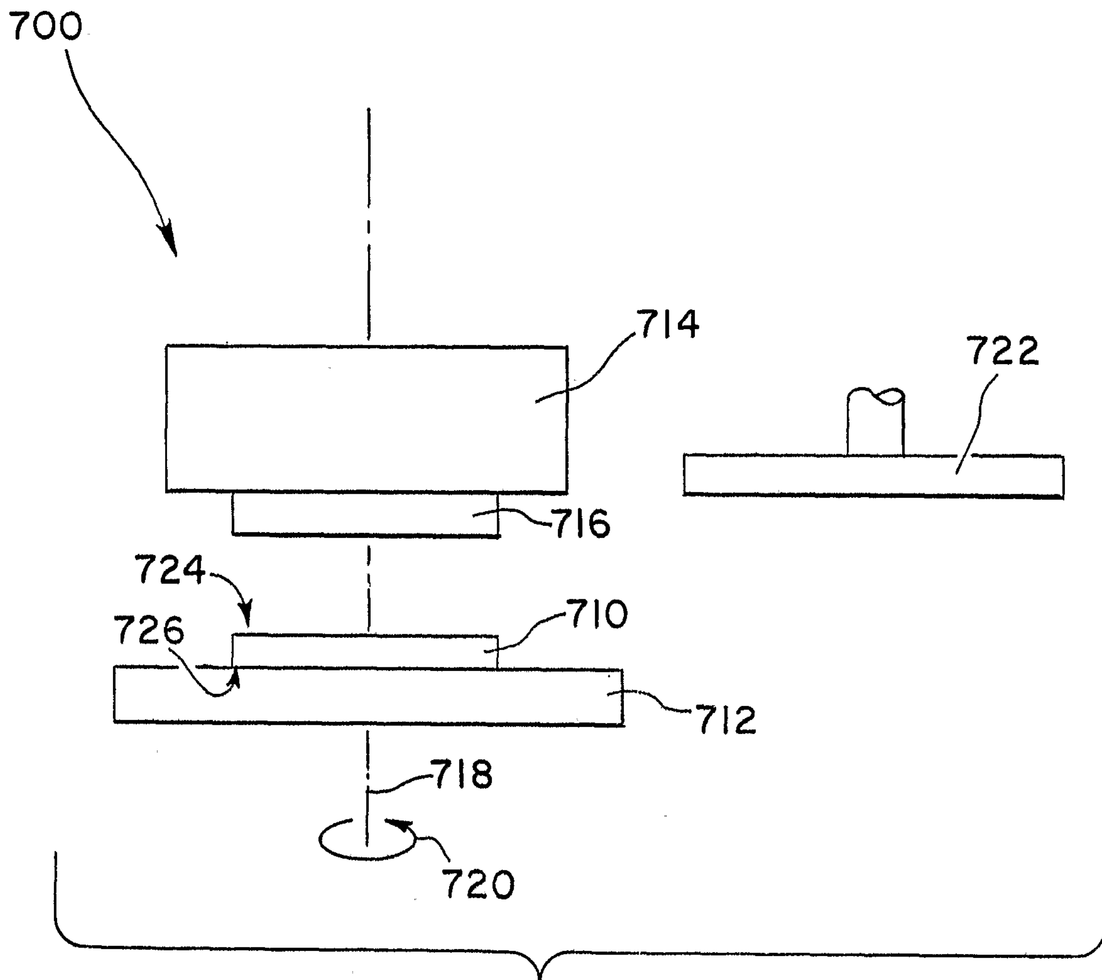

Fig. 7A

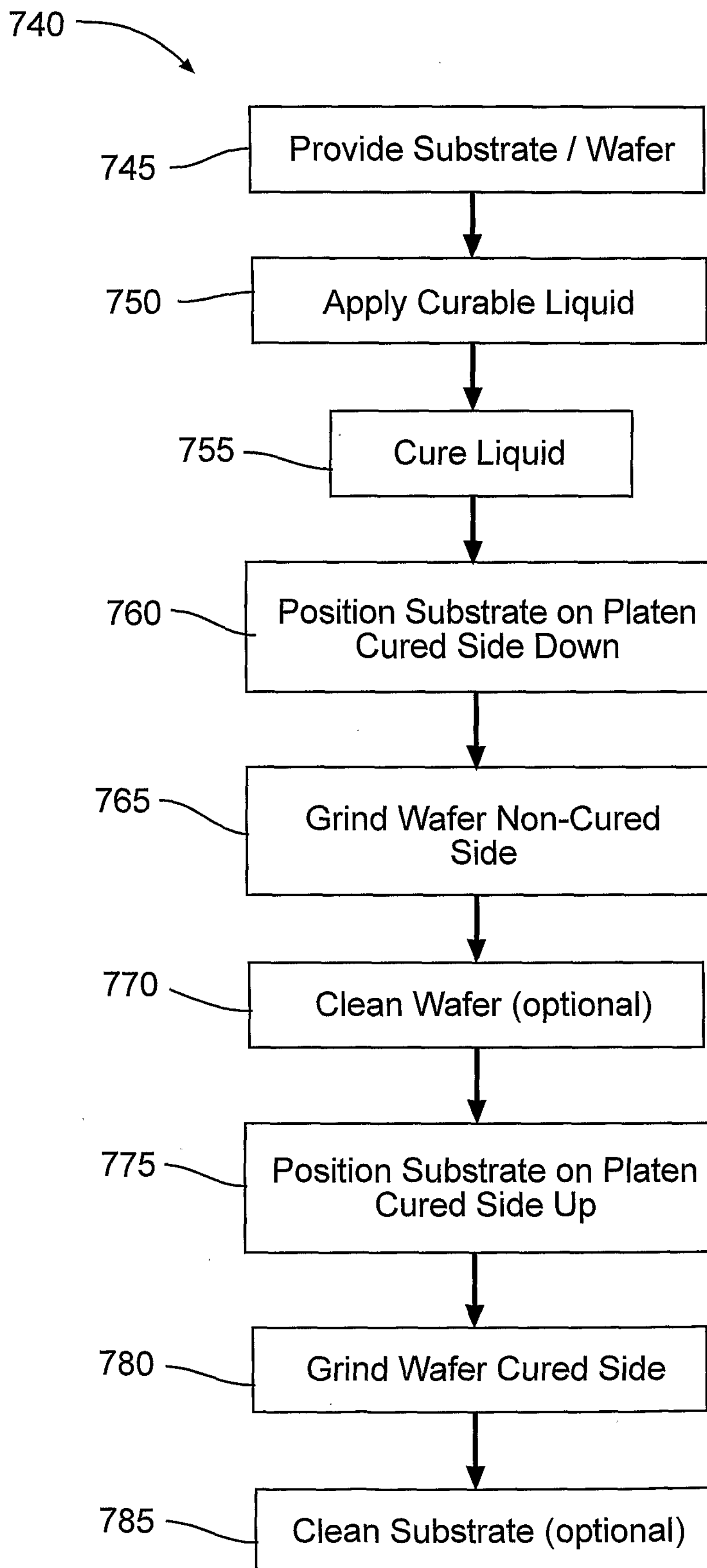

Fig. 7B

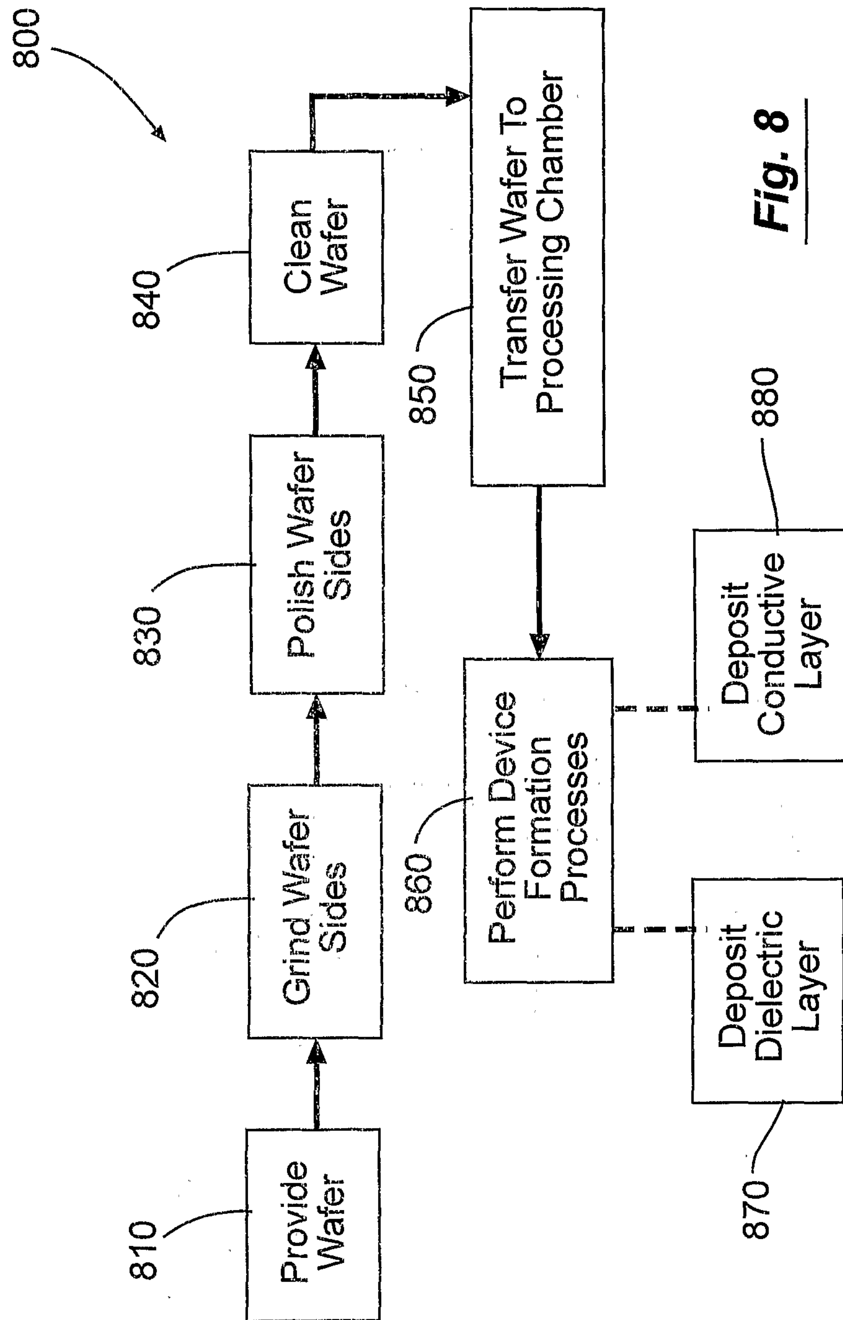

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/08506

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :B24B 1/00, 7/00, 9/00; H01L 21/302, 21/461
US CL : 451/63, 66, 67; 438/691
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WEST Text search [grind$3, polish$3, wafer$1, with selected text as indicated by search report print-outs placed in the file]

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,853,286 A (NARIMATSU et al.) 01 August 1989 (01/08/89) columns 1-4.	45-52, 59
X	US 5,851,664 A (BENNETT et al.) 22 December 1998 (22/12/98) col. 5, lines 24-40.	45-52, 59
X	US 5,880,027 A (HAJIME et al.) 09 March 1999 (09/03/99) Fig. 1	38
X --- Y	US 5,942,445 A (KATO et al.) 24 AUGUST 1999 (24/08/99) Fig. 2	18 --- 19
X	US 5,981,391 A (YAMADA) 09 November 1999 (09/11/99) Fig. 10	45-52, 59

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 JUNE 2001	15 JUN 2001

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 6,095,897 A (STOCKER et al.) 01 August 2000 (01/08/00) Abstract, col. 1-2	25
A, P	US 6,114,245 A (VANDAMME et al.) 05 September 2000 (05/09/00) entire document	1-64
A, P	US 6,149,507 A (LEE et al.) 21 November 2000 (21/11/00) entire document.	1-44
X	JP 61-152358 A (SHIN) 11 July 1986 (11/07/86) Abstract wherein resin is a polymer	45
A	JP 6-295891 A (Sumitomo Sitix Co Ltd) 21 October 1994 (21/10/94) entire document	1-44
Y	JP 10-146751 A (CANON KK) 02 June 1998 (02/06/98) Abtract indicating in situ metrology	19
A	JP 10-242088 A (TOSHIBA KK) 11 September 1998 (11/09/98) entire document.	19-24
X	JP 10-256203 A (ABE) 25 September 1998 (25/09/98) Abstract Solution	26
X	WO 99/09588 A1 (VANDAMME et al.) 25 Februrary 1999 (25/02/99) Fig. 4	18, 38
A	WO 99/31723 A1 (DAVIS et al.) 24 June 1999 (24/06/99) entire document	1-44

B. FIELDS SEARCHED
Minimum documentation searched
Classification System: U.S.

438/5, 7, 14, 16, 689, 690, 691, 692, 693, 694, 800;
451/1, 2, 3, 5, 6, 28, 63, 64, 65, 66, 67, 158;
427/154, 289, 290, 292, 307, 309, 346, 401, 424, 425;
216/2;
118/712