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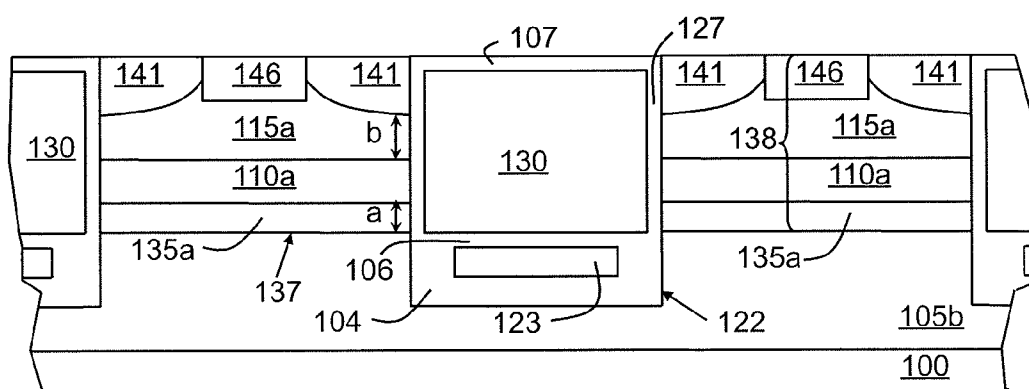


FIG. 1

(57) Abstract: A trench-gate field effect transistor includes trenches extending into a silicon region of a first conductivity type, and a gate electrodes in each trench. Body regions of second conductivity type extend over the silicon region between adjacent trenches. Each body region forms a first PN junction with the silicon region, and each body region includes a silicon-germanium layer of the second conductivity type laterally extending between adjacent trenches. Source regions of the first conductivity flank the trenches, and each source region forms a second PN junction with one of the body regions. Channel regions extend in the body regions along sidewalls of the trenches between the source regions and a bottom surface of the body regions. The silicon-germanium layers extend into corresponding channel regions to thereby reduce the channel resistance.

STRUCTURE AND METHOD FOR FORMING FIELD EFFECT TRANSISTOR WITH LOW RESISTANCE CHANNEL REGION

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims the benefit of US Provisional Application No. 61/013,411, filed December 13, 2007, which is incorporated herein by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

[0002] The present invention relates in general to semiconductor structures and methods for forming the same, and more particularly to semiconductor power field effect transistors (FETs) with low resistance channel regions.

[0003] Some conventional vertically conducting trench-gate power MOSFETs include an n-type substrate over which an n-type epitaxial layer extends. The substrate embodies the drain of MOSFET. A p-type body region extends into the epitaxial layer. Trenches extend through the body region and into the portion of the epitaxial layer bounded by the body region and the substrate (commonly referred to as the drift region). A dielectric layer lines the sidewalls and bottom of each trench. Gate electrodes (e.g., from polysilicon) are formed in the trenches and embody the gate of the MOSFET. Source regions extend into the body regions and flank the trenches. Heavy body regions are formed in the body regions between the source regions. When the MOSFET is in the on state, a current flows vertically through the channel region formed in the body region between the source regions and the drift region along the trench sidewalls.

[0004] To obtain high current capability, the transistor on-resistance needs to be reduced. One contributing factor to the on-resistance is the channel resistance. Also, minimizing the resistance of the body region helps improve the UIS (unclamped inductive switching) capability of the transistor. Various techniques for reducing the channel resistance and/or the resistance of the body region have been proposed but with limited success. Thus, there is a need for techniques which enable significant reduction in the channel resistance and the resistance of the body region for n-channel and p-channel power transistors.

BRIEF SUMMARY OF THE INVENTION

[0005] In accordance with one embodiment of the invention, a trench-gate field effect transistor includes trenches extending into a silicon region of a first conductivity type, and a gate electrodes in each trench. Body regions of second conductivity type extend over the silicon region between adjacent trenches. Each body region forms a first PN junction with the silicon region, and each body region includes a silicon-germanium layer of the second conductivity type laterally extending between adjacent trenches. Source regions of the first conductivity flank the trenches, and each source region forms a second PN junction with one of the body regions. Channel regions extend in the body regions along sidewalls of the trenches between the source regions and a bottom surface of the body regions. The silicon-germanium layers extend into corresponding channel regions to thereby reduce the channel resistance.

[0006] In one embodiment, the silicon-germanium layer is spaced a predetermined distance from the second PN junctions.

[0007] In accordance with another embodiment of the invention, an N-channel trench-gate field effect transistor includes trenches extending into an N-type silicon region, and a gate electrode in each trench. Body regions of P-type conductivity extend over the silicon region between adjacent trenches, and each body region includes a lower silicon layer of P-type conductivity forming a first PN junction with the N-type silicon region, a silicon-germanium layer of P-type conductivity over the lower silicon layer, and an upper silicon layer of P-type conductivity over the silicon-germanium layer. Source regions of N-type conductivity type flank the trenches, and each source region forms a second PN junction with the upper silicon layer.

[0008] In one embodiment, channel regions extend in the body regions along sidewalls of the trenches between the source regions and a bottom surface of the body regions. The silicon-germanium layers extend into corresponding channel regions to thereby reduce the channel resistance.

[0009] In accordance with another embodiment of the invention, a trench-gate field effect transistor includes trenches extending into a silicon region of a first conductivity type, and a gate electrode in each trench. Body regions of a second conductivity type extend over the silicon region between adjacent trenches, and each body region forms a PN junction with the silicon region. A gate dielectric layer lines at least upper sidewalls of each trench, and the

gate dielectric layer insulates the gate electrode from the body region. Source regions of the first conductivity flank the trenches. A silicon-germanium region vertically extends through each source region and through a corresponding body region. The silicon-germanium region terminates within the corresponding body region before reaching the PN junction.

5 [0010] In one embodiment, when the transistor is in an on state, a channel region is formed in the body region along each trench sidewall between each source region and a bottom surface of a corresponding body region, and the silicon-germanium region forms at least a part of the channel region so as to reduce the channel resistance.

10 [0011] In accordance with another embodiment of the invention, a vertically-conducting planar-gate field effect transistor includes a silicon region of a first conductivity type, a silicon-germanium layer extending over the silicon region and a gate electrode laterally extending over but being insulated from the silicon-germanium layer. A body region of the second conductivity type extends in the silicon-germanium layer and the silicon region. A source region of the first conductivity type extends in the silicon-germanium layer. The gate
15 electrode laterally overlaps both the source and body regions such that a portion of the silicon germanium layer extending directly under the gate electrode between the source region and an outer boundary of the body region forms a channel region.

[0012] In one embodiment, the portion of the silicon-germanium layer through which the source region extends is of first conductivity type, and the portion of the silicon-germanium
20 layer through which the body region extends is of the second conductivity type.

[0013] In accordance with another embodiment of the invention, a method for forming a trench-gate field effect transistor includes the following steps. Trenches extending into a silicon region of a first conductivity type are formed. A gate electrode is formed in each trench. Body regions of a second conductivity are formed such that each body region
25 includes a lower silicon region forming a first PN junction with the silicon region, a silicon-germanium layer over the lower silicon layer, and an upper silicon layer over the silicon-germanium layer. Source regions of the first conductivity type flanking the trenches are formed such that each source region forms a second PN junction with the upper silicon layer.

[0014] In one embodiment, the step of forming body regions includes the following steps.
30 A silicon-germanium layer is formed over the silicon region. An epitaxial silicon layer is formed over the silicon-germanium layer, where the epitaxial silicon layer forms the upper silicon layer. Dopants of second conductivity type are implanted through the silicon-

germanium layer and the epitaxial silicon layer to thereby form an implant region in the silicon region, where the implant region forms the lower silicon layer.

[0015] In another embodiment, the step of forming body regions includes the following steps. Dopants of the second conductivity type are implanted to form an implant region of the second conductivity type in the silicon region. Dopants are implanted to form a layer of silicon-germanium layer within the implant region such that a portion of the implant region extending below the silicon-germanium layer forms the lower silicon region, and a portion of the implant region extending over the silicon-germanium layer forms the upper silicon region.

[0016] In accordance with another embodiment of the invention, a method for forming a trench-gate field effect transistor includes the following steps. Trenches extending into a silicon region of a first conductivity type are formed. Body regions of a second conductivity are formed such that each body region forms a PN junction with the silicon region, and each body region includes a vertically extending silicon-germanium layer. A gate electrode is formed in each trench. Source regions of the first conductivity flanking the trenches are formed. The silicon-germanium layers are formed so as to terminate along the vertical dimension before reaching the PN junction.

[0017] In one embodiment, the step of forming body regions includes the following steps. A dielectric layer is formed in each trench. Upper trench sidewalls are lined with a silicon-germanium layer over the dielectric layer. The dielectric layer is recessed to expose a portion of each trench sidewall directly below the silicon-germanium layer. An epitaxial silicon layer is formed inside the trench such that the epitaxial layer lines the exposed portion of each trench sidewall. Dopants of the second conductivity type are implanted into the silicon region, the silicon-germanium layer and the epitaxial silicon layer to thereby form the body region.

[0018] In accordance with another embodiment of the invention, a method of forming a vertically-conducting planar-gate field effect transistor includes the following steps. A silicon-germanium layer is formed over a silicon region of a first conductivity type. A gate electrode laterally extending over but insulated from the silicon-germanium layer is formed. A body region of a second conductivity type extending in the silicon-germanium layer and the silicon region is formed. A source region of the first conductivity type extending at least into the silicon-germanium layer is formed. The gate electrode laterally overlaps both the

source and body regions such that a portion of the silicon germanium layer extends directly under the gate electrode between the source region and an outer boundary of the body region forms a channel region.

BRIEF DESCRIPTION OF THE DRAWINGS

5 [0019] FIG. 1 is a simplified cross section view of an N-channel shielded gate FET with a silicon germanium layer embedded in the body region in accordance with an embodiment of the invention;

[0020] FIGS. 2A-2F are simplified cross-section views showing an exemplary method for forming the N-channel shielded gate FET shown in FIG. 1 in accordance with an
10 embodiment of the present invention;

[0021] FIGS. 3A-3F are simplified cross-section views showing another exemplary method for forming the N-channel shielded gate FET shown in FIG. 1, in accordance with another embodiment of the invention;

[0022] FIG. 4 is a simplified cross-section view of an exemplary N-channel trench gate
15 FET with a SiGe layer embedded in the body region in accordance with an embodiment of the present invention;

[0023] FIG. 5 is a simplified cross-section view of a P-channel shielded gate FET with a SiGe layer extending in the channel region, in accordance with an embodiment of the present invention;

20 [0024] FIGS. 6A-6J are simplified cross-section views showing an exemplary method for forming the P-channel shielded gate FET shown in FIG. 5 in accordance with an embodiment of the present invention;

[0025] FIG. 7 is a simplified cross-section view of an exemplary N-channel trench gate FET with a SiGe layer extending into the channel region in accordance with an embodiment
25 of the present invention;

[0026] FIGS. 8A-8I are simplified cross section views showing an exemplary method for forming the P-channel trench gate FET shown in FIG. 7; and

[0027] FIGS. 9A-9E are simplified cross-section views showing an exemplary method for forming a planar gate N-channel FET with a low resistance channel region in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

5 [0028] In accordance with embodiments of the present invention, structures and methods for forming power field effect transistors (such as n-channel and p-channel variations of MOSFETs and IGBTs) with a silicon-germanium layer advantageously integrated therein so as to obtain a low channel resistance are described. In some embodiments, the silicon-germanium layer is embedded in the body region in a particular manner so as to reduce both
10 the channel resistance and the overall resistance of the body region without inducing leakage current or adversely impacting the transistor breakdown voltage. The techniques in accordance with the invention may be implemented in many types of FETs, including both the N-channel and P-channel variations of trench gate, shielded gate and planar gate MOSFETs and IGBTs. Implementation of one exemplary embodiment of the invention in an
15 N-channel shielded gate FET will be described first with reference to FIGS. 1 and 2A-2F.

[0029] FIG. 1 is a simplified cross section view of an N-channel shielded gate FET with a silicon germanium layer embedded in the body region in accordance with an embodiment of the invention. The FET includes a highly doped substrate 100. Substrate 100 may be N-type in the case of an N-channel MOSFET or P-type in the case of an N-channel IGBT. Lightly
20 doped N-type drift region 105b extends over substrate 100. P-type body region 138 extends over drift region 105b. Body region 138 comprises lower silicon layer 135a, middle silicon-germanium (SiGe) layer 110a and upper silicon layer 115a. Thus, SiGe layer 110a is sandwiched between two P-type silicon layers 135a and 115a.

[0030] Trenches 122 extend through body region 138 and terminate in drift region 105b. In
25 an alternate embodiment, trenches 122 extend deeper and terminate within substrate 100. Shield dielectric 104 (e.g., comprising one or both of oxide and nitride layers) lines lower sidewalls and bottom of each trench 122. Shield electrode 123 (e.g., comprising doped or undoped polysilicon) fills a lower portion of each trench 122. Shield dielectric 104 insulates shield electrode 123 from drift region 105b. The shape of shield electrodes 123 as shown in
30 FIG. 1 is strictly illustrative. In practice, shield electrodes 123 may extend longer along the vertical dimension than along the lateral dimension.

[0031] Inter-electrode dielectric 106 (e.g., comprising one or more oxide layers) laterally extends over shield electrode 123. Gate dielectric 127 (e.g., comprising gate oxide) lines upper trench sidewalls. Gate electrode 130 (e.g., comprising doped or undoped polysilicon) fills an upper portion of each trench 122. Inter-electrode dielectric (IED) 106 insulates the gate and shield electrodes from one another. In one embodiment, IED 106 and gate dielectric 127 are of substantially the same thickness. In another embodiment, IED 106 and shield dielectric 104 are both thicker than gate dielectric 127. Dielectric cap 107 (e.g., comprising oxide and/or BPSG) extends over gate electrode 130. Highly doped N-type source regions 141 are in upper silicon layer 115a adjacent trenches 122. Highly doped P-type heavy body regions 146 are in upper silicon layer 115a between adjacent source regions 141.

[0032] A top-side interconnect layer (not shown) extends along the top-side of the structure and electrically contacts source regions 141 and heavy body regions 146. A bottom-side interconnect layer (not shown) extends along the bottom-side of the structure to electrically contact substrate 100. In one embodiment, the top-side and bottom-side interconnect layers comprise a metal. Dielectric cap 107 insulates gate electrodes 130 from the top-side interconnect layer. In an alternate embodiment, dielectric cap 107 is dome-shaped and extends out of each trench to laterally overlap source regions 141.

[0033] Because the lattice structures of silicon-germanium and silicon are different, when the SiGe layer is being formed during the manufacturing process, the SiGe layer becomes strained upon coming in contact with the underlying silicon. A strained SiGe layer can thus be formed. Such a strained SiGe layer provides a higher carrier mobility than silicon specially when carriers are transported in the vertical direction (i.e., perpendicular to the interface between SiGe 110a and lower silicon layer 135a).

[0034] When the FET is turned on a channel is formed in body region 138 along each trench sidewall between source regions 141 and drift region 105b. The channel region thus vertically extends through upper silicon layer 115a, middle SiGe layer 110a, and lower silicon layer 135a along each trench sidewall. When the FET is turned on, the electrons in the channel region are transported in the direction perpendicular to the interface between middle SiGe layer 110a and lower silicon layer 135a and thus enjoy a lower resistance when traveling through middle SiGe layer 110a. The lower channel resistance in turn reduces the transistor R_{dson} as compared to prior art structures where no SiGe layer is embedded in the body region. Further, because SiGe layer 110a forms a middle part of body region 138, the

overall resistance of body region 138 is reduced which in turn improves the transistor switching performance (e.g., UIS characteristics).

[0035] It has been found that structures where a SiGe layer extends through a PN junction exhibit leakage current and degraded breakdown voltage characteristics under particular biasing conditions. To address these problems, as shown in FIG. 1, SiGe layer 110a is disposed in body region 138 a distance "a" from PN junction 137 that is formed between lower silicon layer 135a and drift region 105b, and a distance "b" from the bottom-most portion of the PN junction formed between source regions 141 and body regions 138. In high voltage transistors where PN junction 137 is reverse biased under a high reverse voltage, spacing "a" may be set such that the depletion region resulting from the high reverse voltage does not reach SiGe layer 110a. In contrast, in low voltage devices where PN junction 137 is under a lower reverse voltage, spacing "a" may be made smaller or even eliminated altogether. Spacing "a" and spacing "b" may be the same length, or spacing "a" may be greater than spacing "b", or vice versa. In one embodiment, spacing "a" and spacing "b" are selected from the range of 500 Å to 1,000 Å.

[0036] FIGS. 2A-2F are cross-section views showing an exemplary method for forming the N-channel shielded gate FET in FIG. 1 in accordance with an embodiment of the invention. Referring to FIG. 2A, at least one epitaxial layer such as silicon epitaxial layer 105, at least one silicon-germanium ($\text{Si}_{1-x}\text{Ge}_x$) layer such as silicon-germanium epitaxial layer 110 and at least one other epitaxial layer such as silicon epitaxial layer 115 are sequentially formed over a substrate 100. Substrate 100 can be a silicon substrate, a III-V compound substrate, a silicon/germanium (SiGe) substrate, silicon carbide substrate, an epi-substrate, or a silicon-on-insulator (SOI) substrate. In the case of an N-channel MOSFET, substrate 100 is N-type, and in the case of an N-channel IGBT, substrate 100 is P-type.

[0037] Silicon epitaxial layer 105 may be formed by a conventional epitaxial process. Silicon epitaxial layer 105 has N-type dopants such as boron, gallium, aluminum and/or other group III element. The dopant concentration of silicon epitaxial layer 105 may be lower than that of substrate 100. Silicon-germanium epitaxial layer 110 may be formed by a conventional epitaxial process. Silicon-germanium epitaxial layer 110 has P-type dopants such as boron, gallium, aluminum and/or other group III element. In some embodiments, silicon-germanium epitaxial layer 110 may have a thickness between about 100 Å and about 500 Å. Silicon epitaxial layer 115 may be formed by a conventional epitaxial process.

Silicon epitaxial layer 115 has P-type dopants such as boron, gallium, aluminum and/or other group III element.

[0038] In FIG. 2B, one or more etch processes 120 may be carried out to form trenches 122 extending through epitaxial layer 115, SiGe layer 110m and epitaxial layer 105. In some
5 embodiments, a patterned mask (not shown) with openings corresponding to trenches 122 may be formed over epitaxial layer 115. Etch process(s) 120 uses the patterned mask as an etch mask to define trenches 122. The patterned mask may be, for example, a patterned photoresist layer, a patterned dielectric layer, or any patterned material layer that can be adapted to be an etch mask. After etch process(s) 120, the patterned mask layer may be
10 removed.

[0039] In FIG. 2C, shield dielectric 124 is formed along lower sidewalls and bottom of each trench 122 using known techniques. Shield electrodes 123 are formed in lower portions of trenches 122 using conventional methods. Gate insulator 127 is formed along upper
sidewalls of trenches 122 using known techniques. In one embodiment, gate insulator 127
15 also extends over shield electrodes 123 to thereby form an inter-electrode dielectric (IED) 106 over shield electrodes 123. In another embodiment, an IED layer 106 that is thicker than gate dielectric 127 is formed over shield electrodes 123 in a separate step from the step of forming gate insulator 127. Recessed gate electrodes 130 are formed over IED 106 in
trenches 122 using conventional techniques. Dielectric cap 107 (e.g., comprising oxide or
20 BPSG) is formed over each gate electrode 130 using known techniques.

[0040] Shield electrodes 123 and gate electrodes 130 comprise a conductive material such as doped or undoped polysilicon, copper, aluminum copper, aluminum, tungsten, other
conductive material or various combinations thereof. Each of shield dielectric 124, IED 106,
and gate insulator 127 may comprise, for example, an oxide layer, a nitride layer, an
25 oxynitride layer, other dielectric layer or various combinations thereof.

[0041] In FIG. 2D, using known techniques, implant process 135 is carried out to implant dopants that penetrate silicon-germanium layer 110a, thereby converting an upper portion of N-type epitaxial layer 105 into P-type region 135a. P-type dopants such as boron, aluminum
and/or other group III elements may be used in implant process 135. Upper silicon region
30 115a, middle SiGe layer 110a, and lower silicon layer 135a are all P-type and together form body region 138. Body region 138 forms a PN junction 137 with drift region 105b (i.e., the portion of epitaxial layer 105a that is bounded by body region 138 and substrate 100). As

discussed above in connection with FIG. 1, depending on various considerations, a smaller or larger spacing "a" may be desirable, and implantation process 135 may be designed accordingly. In one embodiment, spacing "a" is set to a value selected from the range of 500 Å to 1,000 Å.

5 [0042] In one embodiment, implant process 135 is performed without a patterned mask layer. In other embodiments, implant process 135 is performed with a patterned mask layer having a pattern substantially covering gate electrodes 130. Such patterned mask may be, for example, a patterned photoresist layer, or a patterned dielectric layer. After implantation process 135, the patterned mask layer may be removed. In yet some other embodiments,
10 implant process 135 may be carried out prior to forming trenches 122.

[0043] In an alternate embodiment, lower silicon layer 135a is formed epitaxially rather than by implantation of dopants. That is, in the process steps depicted in FIG. 2A, a P-type silicon epitaxial layer 135a can be formed between N-type silicon epitaxial layer 105 and SiGe layer 110. In yet another embodiment, silicon layer 135a is formed as follows. In FIG.
15 2A, after forming N-type epitaxial layer 105 and before forming SiGe layer, P-type dopants are implanted into epitaxial layer 105 to thereby convert an upper region of N-type epitaxial layer 105 into P-type layer 135a.

[0044] Referring to FIG. 2E, implant process 140 is carried out to form highly doped source regions 141 in upper silicon layer 115a adjacent trenches 122. N-type dopants such as
20 phosphorus, arsenic and/or other group V elements may be used in implant process 140. In one embodiment, a patterned mask layer (not shown) having a pattern exposing surfaces of epitaxial layer 115a through which the dopants are to be implanted may be used. The patterned mask may be, for example, a patterned photoresist layer, a patterned dielectric layer, or various combinations thereof. After implant process 140, the patterned mask layer
25 may be removed.

[0045] As stated above in connection with FIG. 1, various process parameters and layer thicknesses may be adjusted so that a distance "b" between SiGe layer 110a to the bottom-most portion of source regions 141 is set to a value which insures that silicon germanium layer 110a does not reach the PN junction formed between source regions 141 and upper
30 silicon layer 115a. In one embodiment, spacing "b" is selected from the range of about 500 Å and about 1,000 Å. In one embodiment, SiGe layer 110 is extended all the way up to source regions 141.

[0046] In FIG. 2F, a further implant process 145 is carried out to form heavy body regions 146 within upper silicon layer 115a between adjacent source regions 141. P-type dopants such as boron, aluminum and/or other group III element may be used in implant process 145. In one embodiment, implant process 145 is performed with a patterned mask layer (not shown) having a pattern exposing predefined surfaces of upper silicon layer 115a through which the dopants are to be implanted. The patterned mask may be, for example, a patterned photoresist layer or a patterned dielectric layer. After implant process 145, the patterned mask layer may be removed. As can be seen, the top surface of mesa regions (i.e., semiconductor regions between adjacent trenches) and the top surface of dielectric cap 107 are substantially coplanar. In an alternate embodiment, using known techniques, dielectric cap 107 may be formed to have a dome shape and extend out of each trench to overlap the adjacent mesa regions.

[0047] Using known techniques, a top-side interconnect layer (not shown) is formed on the top-side of the structure to electrically contact source regions 141 and heavy body regions 146. A back-side interconnect layer (not shown) is formed on the back-side of the structure to electrically contact substrate 100. The top-side and back-side interconnect layers may comprise a metal.

[0048] FIGS. 3A-3F are cross-section views showing another exemplary method for forming the shielded gate N-channel FET shown in FIG. 1, in accordance with another embodiment of the invention. In FIG. 3A, a silicon epitaxial layer 205 is formed over a substrate 200. Substrate 200 and epitaxial layer 205 may respectively be similar to substrate 100 and epitaxial layer 105 described above in conjunction with FIG. 1A. In FIG. 3B, trenches 212 are formed in epitaxial layer 205 in a similar manner to trenches 112 in FIG. 2B. In FIG. 3C, the shield dielectric, shield electrodes 215, the IED, gate insulator 217, the dielectric cap over gate electrode 220, gate electrodes 220 and other trench structures are formed similar to those described above in connection with FIG. 2C.

[0049] In FIG. 3D, an implant process 225 is carried out to implant P-type dopants into the mesa regions between adjacent trenches so as to form body regions 225a in epitaxial layer 205a. A PN junction is thus formed at interfaces 227 between body regions 225a and epitaxial layer 205b. In some embodiments, implant process 225 uses p-type dopants such as boron, aluminum and/or other group III element. In some embodiment, implant process 225 is performed without a patterned mask layer. In other embodiments, implant process 225 is

performed with a patterned mask layer having a pattern covering gates 220. The patterned mask may be, for example, a patterned photoresist layer or a patterned dielectric layer. After implant process 225, the patterned mask layer may be removed.

[0050] In FIG. 3E, an implant process 230 implants germanium dopants into body regions 225a so as to form silicon-germanium layer 230a embedded within body regions 225a. In some embodiments, implant process 230 is designed so that SiGe layer 230a is spaced a distance "c" from interface 227. The considerations in selecting a value for distance "c" would be similar to those for distance "a" in FIG. 2F. In some embodiments, SiGe layer 230a may have a thickness between about 100 Å and about 500 Å. In some embodiments, implant process 230 is performed without a patterned mask layer. In other embodiments, implant process 230 is performed with a patterned mask layer having a pattern covering gate electrodes 220. In one embodiment, the patterned mask layer is the same mask layer used in implant process 225 in FIG. 3D.

[0051] In FIG. 3F, the processes for forming source regions 235a and heavy body regions 240a are similar to those in FIGS. 2E and 2F and thus will not be described. In an alternate embodiment, implantation processes 225, 230 and those for source and heavy body regions may be performed before the formation of trenches 212.

[0052] The above-described techniques of embedding a SiGe layer in the body region in a manner that reduces the channel resistance is not limited in application to shielded gate FETs. FIG. 4 shows a cross-sectional view of an exemplary N-channel trench gate transistor with a SiGe layer embedded in the body region in accordance with an embodiment of the present invention. The trench gate FET in FIG. 4 is similar to the shielded gate FET in FIG. 1 except that the trenches do not extend as deep and the shield electrodes are absent. That is, substrate 100, drift region 105b, body region 138 and its three sub-layers 135a, 110a and 115a, source regions 141 and heavy body regions 146 are all similar to their corresponding regions in the shielded gate FET shown in FIG. 1. However, the trench structure in FIG. 4 includes only a gate electrode 150 and dielectric layers insulating gate electrode 150 from surrounding regions.

[0053] Any one of the process techniques and their variations described above in connection with FIGS. 2A-2F and 3A-3F can be used, with some modification, to form the transistor in FIG. 4. The required process changes relating to forming the trenches and their inner elements would be obvious to one skilled in the art in view of this disclosure. For

example, the trenches need not extend as deep, and the steps related to forming the shield dielectric and the shield electrode are eliminated. Although FIG. 4 shows gate dielectric layer 127 along the trench sidewalls to have the same thickness as the dielectric layer along the trench bottoms, in one variation, a thicker dielectric layer (commonly referred to as thick bottom dielectric - TBD) is formed along the bottom of the trenches below gate electrodes 150 to reduce the gate to drain capacitance.

[0054] FIG. 5 is a simplified cross-section view of a P-channel shielded gate FET with a SiGe layer that extends into the channel region, in accordance with an embodiment of the present invention. The FET includes a highly doped substrate 300. Substrate 300 may be P-type in the case of a P-channel MOSFET or N-type in the case of a P-channel IGBT. Lightly doped P-type drift region 305b extends over substrate 300. N-type body region 355a extends over drift region 305b. Trenches 312 extend through body region 335a and terminate within drift region 305b. In an alternate embodiment, trenches 312 extend deeper and terminate within substrate 300. The vertical dashed lines are included in FIG. 5 only to show the contours of trenches 312 when it is originally formed. Silicon regions 340b and 340c partially fill trenches 312 as will be described more fully further below in connection with the process flow depicted by FIGS. 6A-6J.

[0055] Shield dielectric 315a (e.g., comprising one or both of oxide and nitride layers) lines lower sidewalls and bottom of each trench 312. Shield electrode 320 (e.g., comprising doped or undoped polysilicon) fills a lower portion of each trench 312. Shield dielectric 315a insulates shield electrode 320 from drift region 305b. The shape of shield electrodes 123 as shown in FIG. 1 is strictly illustrative. In an actual device, shield electrodes 320 may extend longer along the vertical dimension than along the lateral dimension.

[0056] Inter-electrode dielectric 306s (e.g., comprising one or more oxide layers) laterally extends over shield electrode 320. Gate dielectric 347 (e.g., comprising gate oxide) lines upper trench sidewalls. Recessed gate electrode 350 (e.g., comprising doped or undoped polysilicon) fills an upper portion of each trench 312. Inter-electrode dielectric (IED) 309 insulates the gate and shield electrodes from one another. In one embodiment, IED 309 and gate dielectric 347 are of substantially the same thickness. In another embodiment, IED 309 and shield dielectric 315a are both thicker than gate dielectric 347. Dielectric cap 307 (e.g., comprising oxide and/or BPSG) extends over gate electrode 350. Highly doped P-type

source regions 360a are in body region 355a adjacent trenches 312. Highly doped N-type heavy body regions 365a are in body region 355a between adjacent source regions 360a.

[0057] SiGe strips 325a vertically extends through each source regions 360a and into body regions 355a. The portion of SiGe layer 325a that extends in body region 355a is N-type, and the portion of SiGe layer 325a that extends in source region 360a is P-type. Silicon regions 340b are N-type and extend vertically between SiGe strips 325a and the trench sidewalls and below the bottom-end of SiGe strips 325a. Silicon regions 340b together with SiGe strips 325a form the channel regions. Silicon region 340c is P-type and forms part of drift region 305b.

[0058] A top-side interconnect layer (not shown) extends along the top-side of the structure and electrically contacts source regions 360a and heavy body regions 365a. A bottom-side interconnect layer (not shown) extends along the bottom-side of the structure to electrically contact substrate 300. In one embodiment, the top-side and bottom-side interconnect layers comprise a metal. Dielectric cap 307 insulates gate electrodes 350 from the top-side interconnect layer. In an alternate embodiment, dielectric cap 307 has a dome shape and extends out of each trench to laterally overlap source regions 360a.

[0059] When the FET is turned on a channel is formed in body region 355a along each trench sidewall between source regions 360a and drift region 305b. The channel region includes SiGe strip 25a which is laterally sandwiched between two silicon regions. When the FET is turned on, holes travel through the channel region but away from the gate dielectric interface. However, SiGe strips 325a substantially reduce scattering of the holes in the channel region and thus reduce the channel resistance. The lower channel resistance in turn reduces the transistor $R_{ds(on)}$ as compared to prior art structures where no SiGe layer extends into the channel region.

[0060] Further, similar to prior embodiments, by maintaining a spacing "e" between SiGe strips 325a and the PN junction 357 between body regions 355a and drift region 305b, the leakage current and degraded breakdown voltage characteristics that would otherwise be present are eliminated. In one embodiment, spacing "e" is set so that a depletion region formed when junction 357 is under a reverse voltage does not reach SiGe strips 325a. In one embodiment, spacing "e" is selected from the range of 500-5000 Å. In another embodiment, SiGe strips 325a have a thickness in the range of 100 Å to 500 Å.

[0061] FIGS. 6A-6J are simplified cross-section views showing an exemplary method for forming the P-channel shielded gate FET shown in FIG. 5 in accordance with an embodiment of the present invention. In FIG. 6A, P-type silicon epitaxial layer 305 is formed over a heavily doped substrate 300. In the case of a P-channel MOSFET, substrate 300 is P-type, and in the case of a P-channel IGBT, substrate 300 is N-type. Silicon epitaxial layer 305 may be formed by a conventional epitaxial process, and may have a lower doping concentration than that of substrate 300.

[0062] In FIG. 6B, a silicon etch process 310 similar to that described above in connection with FIG. 3B may be carried out to form trenches 312 in epitaxial layer 305. In FIG. 6C, shield dielectric 315 and shield electrodes 320 are formed in trenches 312 in a similar manner to those described above in connection with FIG. 3C. A thick dielectric layer 306 is formed over shield electrodes 320 to a predetermined thickness. As will be seen from the subsequent process steps, the upper surface of dielectric layer 306 defines the depth within the channel regions to which the SiGe strips extends.

[0063] In Fig. 6D, SiGe layer 325 is formed over the mesa regions between adjacent trenches, along the exposed upper trench sidewalls, and over dielectric layer 306. SiGe layer 325 may be in-situ doped with N-type dopant. In some embodiments, SiGe 325 may be formed by, for example, an epitaxial process, a chemical vapor deposition (CVD) process, an ultra high vacuum chemical vapor deposition (UHVCVD) process, an atomic layer chemical vapor deposition (ALCVD) process, a metal organic chemical vapor deposition (MOCVD) process or other CVD processes. In some embodiments, SiGe layer 325 may have a thickness between about 100 Å and about 500 Å.

[0064] In FIG. 6E, an etch process 330 may be carried out to remove horizontally extending portions of SiGe layer 325, leaving SiGe strips 325a along upper trench sidewalls. In some embodiments, etch process 330 may be a dry etch process and/or a wet etch process. In FIG. 6F, an etch process 335 may be carried out to remove a portion of dielectric layers 306 thereby forming a gap between SiGe strips 325a and a remaining dielectric portion 306a. Etch process 335 may be a wet etch process and/or a dry etch process.

[0065] In FIG. 6G, silicon layer 340 is formed over the entire structure. Silicon layer 340 may be doped P-type so as to have the same conductivity type as epitaxial layer 305a. The vertical dashed lines indicate the original contour of trenches 312. Silicon layer 340 may be formed by, for example, an epitaxial process, a chemical vapor deposition (CVD) process, an

ultra high vacuum chemical vapor deposition (UHVCVD) process, an atomic layer chemical vapor deposition (ALCVD) process, a metal organic chemical vapor deposition (MOCVD) process or other CVD process.

[0066] In FIG. 6H, etch process 345 is carried out to remove horizontally extending portions of the silicon layer 340 while preserving vertically portions 340a. Etch process 345 may be a dry etch process and/or a wet etch process, and may use dielectric portion 360a as etch stop. This prevents over etching of the mesa regions between adjacent trenches.

[0067] In Fig. 6I, gate dielectric 347 (e.g., comprising oxide) lining sidewalls of silicon regions 340a are formed. Gate dielectric 347 may be formed to also extend over dielectric portion 306a to thereby form a thicker inter-electrode dielectric (IED) layer 309. Alternatively, prior to forming gate dielectric 347, a laterally-extending layer of dielectric (e.g., comprising oxide) may be formed over dielectric portion 306a to obtain an inter-electrode dielectric 309 with the desired thickness. Gate electrodes 350 are formed over IED 309 in a similar manner to those in prior embodiments.

[0068] A conventional body implant 355 may be carried out to form N-type body regions 355a in epitaxial layer 305b. Note that body implant 355 converts an upper portion 340b of silicon region 340a into N-type silicon, while a lower portion 340c remains P-type. Body implant 355 may be carried out at an earlier stage (e.g., before forming gate electrode 350 or even before forming trenches 312) if desired. As can be seen, vertically extending SiGe strips 325a are vertically sandwiched by silicon regions 340b and 355a, and are advantageously spaced from PN junction 357 by a spacing "e." In one embodiment, spacing "e" selected from the range of about 500 Å to 1,000 Å.

[0069] Referring to FIG. 6J, a conventional source implant 360 is carried out to form highly doped P-type source regions 360a flanking trenches 312. Note that source implant 360 converts an upper portion of silicon region 340b to P-type. Next, a conventional heavy body implant 365 is carried out to form highly doped N-type heavy body regions 365a between adjacent source regions 360a. The various considerations discussed above in connection with forming the source and heavy body regions of the above embodiments also apply to present embodiment. The top-side and bottom-side interconnect layers (not shown) may be formed in a similar manner to prior embodiments.

[0070] FIG. 7 shows a cross-section view of an exemplary P-channel trench gate FET with a SiGe strip extending into the channel region in accordance with an embodiment of the

present invention. The trench gate FET in FIG. 7 is similar to the shielded gate FET in FIG. 5 except that the trenches don't extend as deep and the shield electrodes are removed. That is, substrate 300, drift region 305b, body region 355a, SiGe strips 325a, silicon regions 340b and 340c, source regions 360a, and heavy body regions 365a are all similar to their
5 corresponding regions in the shielded gate FET shown in FIG. 5. However, the trench structure in FIG. 7 includes only a gate electrode 350 and dielectric layers insulating gate electrode 350 from the surrounding regions. Note that a thick bottom dielectric 319 is optionally disposed along the bottom of each trench to reduce the gate to drain capacitance.

[0071] FIGS. 8A-8I are simplified cross section views at various stages of an exemplary
10 process for forming the P-channel trench gate FET shown in FIG. 7. In FIG. 8A, trenches 313 are formed in P-type epitaxial layer 305b in a similar manner to trenches 312 in FIG. 6B except that trenches 313 do not extend as deep as trenches 312. In FIG. 8B, a thick dielectric layer 317 (e.g., comprising oxide) filling a bottom portion of trenches 313 is formed using known techniques. As will be seen in subsequent steps, the upper surface of dielectric layer
15 317 defines the depth within the channel regions to which the SiGe strips extends. The steps depicted in FIGS. 8C and 8D for forming SiGe strips 325a are similar to those depicted in FIGS. 6D-6E, and thus will not be described. In FIG. 8E, dielectric layer 317 in each trench 313 is recessed to a predetermined depth using known techniques. Dielectric portion 317a thus remains. The steps depicted in FIGS. 8F and 8G for forming N-type silicon regions
20 340a are similar to those depicted in FIGS. 6G-6H, and thus will not be described.

[0072] In FIG. 8H, gate dielectric 347 (e.g., comprising oxide) lining sidewalls of silicon regions 340a are formed. Gate dielectric 347 may be formed to also extend over dielectric portion 317a to thereby form a thicker bottom dielectric 319. Alternatively, prior to forming gate dielectric 347, a layer of dielectric (e.g., comprising oxide) may be formed over
25 dielectric portion 317a to obtain a bottom dielectric 319 with the desired thickness. Gate electrode 350 is formed over thick bottom dielectric 319 in a similar manner to prior embodiments and may have similar properties to the gate electrodes of prior embodiments. Thick bottom dielectric 319 helps reduce the gate to drain capacitance and thus improves the switching performance of the FET. The steps depicted in FIG. 8I for forming source regions
30 360a and heavy body regions 365a are similar to those in FIG. 6J and thus will not be described.

[0073] FIGS. 9A-9E are cross-section views showing an exemplary method for forming a planar gate N-channel field effect transistor with a low resistance channel region in accordance with an embodiment of the present invention. In FIG. 9A, N-type silicon epitaxial layer 405 is formed over highly doped substrate 400. In the case where the FET is an N-channel MOSFET, substrate 400 is N-type, and in the case where the FET is an N-channel IGBT, substrate 400 is P-type. In some embodiments, the materials and methods for forming silicon epitaxial layer 405 and substrate 400 are similar to those of silicon epitaxial layer 105 and substrate 100, respectively, described above in connection to FIG. 1A.

[0074] SiGe layer 410 is formed over silicon epitaxial layer 405. In some embodiments, SiGe layer 410 is a SiGe epitaxial layer. The materials and methods for forming silicon-germanium layer 410 may be similar to SiGe layer 110 described above in connection with FIG. 1A. In other embodiments, SiGe layer 410 may be formed by an implant process. The implant process may be similar to implant process 230 for forming SiGe layer 230a described above in connection with FIG. 3E.

[0075] In FIG. 9B, stacks of gate dielectric 417 and gate electrode 420 are formed over SiGe layer 410 using conventional masking techniques. Gate dielectric 417 may comprise, for example, oxide, nitride, oxynitride, high-k dielectric material or various combinations thereof. Gate electrodes 420 may comprise, for example, doped or undoped polysilicon, amorphous silicon, copper, aluminum, tungsten, silicide or various combinations thereof. Gates electrodes 420 are insulated from SiGe layer 410 by gate dielectric 417.

[0076] In FIG. 9C, a body implant 415 and drive-in are carried out to form P-type body regions 415 that extend through SiGe layer 410 and terminate in silicon epitaxial layer 405. Gate electrodes 420 can be used as a mask during body implant 415 so that body regions 415 become self-aligned with gate electrodes 420. In some embodiments, dopants such as boron, gallium, aluminum, other group III dopants or various combinations thereof may be used in body implant 415. Body implant 415 converts those portions of SiGe layer 410 that extend through body regions 415 to P-type. Accordingly, silicon germanium layer 410 includes P-type regions 410a and N-type regions 410b.

[0077] In FIG. 9D, dielectric spacers 427 (e.g., comprising oxide and/or nitride) are formed along sidewalls of gate electrodes 420 using known techniques. Source implant 425 is then carried out to form highly doped N-type source regions 425 in body regions 415. Dielectric spacers 427 can be used as a mask during source implant 425 so that source regions 425

become self-aligned with dielectric spacers 427. The extend to which gate electrodes 420 overlap source regions 425 can be controlled by adjusting the thickness of dielectric spacers 427. Note that portions 410c of SiGe layer 410 which receive source implant 425 are converted to N-type.

5 **[0078]** In FIG. 9E, highly dope P-type heavy body regions 419 extending through source regions 425 and into body regions 425 are formed using a conventional heavy body implant. A mask may be used to define the areas that are to receive the heavy body implant. The line delineating SiGe layer 410 is shown as a dashed line in FIG. 9E in order to make the diagram less cluttered. Next, conventional techniques are used to form a dielectric layer (not shown),
10 e.g., comprising boron-phosphorus-silicate-glass (BPSG), covering gate electrodes 420 while leaving surface areas of source regions 425 and heavy body regions 419 exposed. A top-side interconnect layer (not shown) electrically contacting source regions 425 and heavy body regions 419 is then formed using known techniques. A bottom-side interconnect layer contacting substrate 400 is formed on the backside using conventional techniques. The top-
15 side and bottom-side interconnect layers may comprise a metal.

[0079] During operation, when an appropriate source voltage V_s , gate voltage V_g and drain voltage V_d are applied to turn on the transistor, a current flows through the channel region formed in portions 410a of SiGe layer 410. As with the FIG. 1 embodiment, the higher mobility associated with the strained SiGe layer 410 reduces the channel resistance, thus
20 lowering the transistor $R_{ds(on)}$.

[0080] While the various embodiments of the invention have been described in the context of particular types of transistor, the invention is not limited as such. For example, while one or more of the device structures and /or process sequences described above relate to N-channel and P-channel variations of MOSFETs and IGBTs, the techniques in accordance
25 with embodiments of the invention may also be applied other types of devices such as trench gate synchFETs (where Schottky diode is monolithically integrated with trench gate or shielded gate MOSFET) or suprajunction variations of the devices described herein (i.e., devices with columns of alternating conductivity type silicon). Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the
30 appended claims.

WHAT IS CLAIMED IS:

1 1. A trench-gate field effect transistor comprising:
2 trenches extending into a silicon region of a first conductivity type;
3 a gate electrode in each trench;
4 body regions of second conductivity type extending over the silicon region
5 between adjacent trenches, each body region forming a first PN junction with the silicon
6 region, and each body region including a silicon-germanium layer of the second conductivity
7 type laterally extending between adjacent trenches;
8 a gate dielectric layer lining at least upper sidewalls of each trench, the gate
9 dielectric layer insulating the gate electrode from the body region;
10 source regions of the first conductivity flanking the trenches, each source
11 region forming a second PN junction with one of the body regions; and
12 channel regions extending in the body regions along sidewalls of the trenches
13 between the source regions and a bottom surface of the body regions, wherein the silicon-
14 germanium layers extend into corresponding channel regions to thereby reduce the channel
15 resistance.

1 2. The transistor of claim 1 wherein the silicon-germanium layer is
2 spaced a predetermined distance from the second PN junctions.

1 3. The transistor of claim 1 wherein the silicon-germanium layer is
2 spaced a predetermined distance from the first and second PN junctions.

1 4. The transistor of claim 1 wherein the silicon-germanium layer
2 separates an upper portion of the body region from a lower portion of the body region.

1 5. The transistor of claim 1 wherein each silicon-germanium layer abuts
2 sidewalls of two adjacent trenches.

1 6. The transistor of claim 1 wherein each silicon-germanium layer is
2 vertically spaced from a corresponding first PN junction by a distance in the range of 500 Å
3 to 1,000 Å, and from a corresponding second PN junction by a distance in the range of 500 Å
4 to 1,000 Å.

1 7. The transistor of claim 1 wherein each trench further includes:
2 a shield dielectric layer thicker than the gate dielectric lining lower sidewalls
3 of the trench;
4 a shield electrode in a lower portion of the trench under the gate electrode; and
5 an inter-electrode dielectric layer insulating the gate and shield electrodes
6 from one another.

1 8. The transistor of claim 1 wherein each trench includes a thick bottom
2 dielectric along the trench bottom below the gate electrode.

1 9. An N-channel trench-gate field effect transistor comprising:
2 trenches extending into an N-type silicon region;
3 a gate electrode in each trench;
4 body regions of P-type conductivity extending over the silicon region between
5 adjacent trenches, each body region including a lower silicon layer of P-type conductivity
6 forming a first PN junction with the N-type silicon region, a silicon-germanium layer of P-
7 type conductivity over the lower silicon layer, and an upper silicon layer of P-type
8 conductivity over the silicon-germanium layer; and
9 source regions of N-type conductivity type flanking the trenches, each source
10 region forming a second PN junction with the upper silicon layer.

1 10. The transistor of claim 9 wherein each silicon-germanium layer abuts
2 sidewalls of two adjacent trenches.

1 11. The transistor of claim 9 wherein each silicon-germanium layer is
2 vertically spaced from corresponding first and second PN junctions.

1 12. The transistor of claim 9 wherein each trench further includes:
2 a shield dielectric layer thicker than the gate dielectric lining lower sidewalls
3 of the trench;
4 a shield electrode in a lower portion of the trench under the gate electrode; and
5 an inter-electrode dielectric layer insulating the gate and shield electrodes
6 from one another.

1 13. The transistor of claim 9 wherein each trench includes a thick bottom
2 dielectric along the trench bottom below the gate electrode.

1 14. The transistor of claim 9 further comprising channel regions extending
2 in the body regions along sidewalls of the trenches between the source regions and a bottom
3 surface of the body regions, wherein the silicon-germanium layers extend into corresponding
4 channel regions to thereby reduce the channel resistance.

1 15. A trench-gate field effect transistor comprising:
2 trenches extending into a silicon region of a first conductivity type;
3 a gate electrode in each trench;
4 body regions of a second conductivity type extending over the silicon region
5 between adjacent trenches, each body region forming a PN junction with the silicon region;
6 a gate dielectric layer lining at least upper sidewalls of each trench, the gate
7 dielectric layer insulating the gate electrode from the body region;
8 source regions of the first conductivity flanking the trenches; and
9 a silicon-germanium region vertically extending through each source region
10 and through a corresponding body region, the silicon-germanium region terminating within
11 the corresponding body region before reaching the PN junction.

1 16. The transistor of claim 15 wherein each silicon-germanium region is
2 spaced from the corresponding PN junction a distance in the range of 500 Å to 1,000 Å.

1 17. The transistor of claim 15 wherein each silicon-germanium region is
2 bounded along its vertical boundaries by silicon regions.

1 18. The transistor of claim 15 wherein when the transistor is in an on state,
2 a channel region is formed in the body region along each trench sidewall between each
3 source region and a bottom surface of a corresponding body region, and the silicon-
4 germanium region forms at least a part of the channel region so as to reduce the channel
5 resistance.

1 19. The transistor of claim 15 wherein each trench includes silicon
2 material insulated from the gate electrode therein.

1 20. The transistor of claim 15 wherein the silicon-germanium regions are
2 disposed inside the trenches.

1 21. The transistor of claim 15 wherein the transistor is an P-channel
2 transistor with the first conductivity type being P-type and the second conductivity type being
3 N-type.

1 22. The transistor of claim 15 wherein each trench further includes:
2 a shield dielectric layer thicker than the gate dielectric lining lower sidewalls
3 of the trench;
4 a shield electrode in a lower portion of the trench under the gate electrode; and
5 an inter-electrode dielectric layer insulating the gate and shield electrodes
6 from one another.

1 23. The method of claim 15 wherein each trench includes a thick bottom
2 dielectric along the trench bottom below the gate electrode.

1 24. A vertically-conducting planar-gate field effect transistor comprising:
2 a silicon region of a first conductivity type;
3 a silicon-germanium layer extending over the silicon region;
4 gate electrode laterally extending over but being insulated from the silicon-
5 germanium layer;
6 a body region of the second conductivity type extending in the silicon-
7 germanium layer and the silicon region;
8 source region of the first conductivity type extending in the silicon-germanium
9 layer, the gate electrode laterally overlapping both the source and body regions such that a
10 portion of the silicon germanium layer extending directly under the gate electrode between
11 the source region and an outer boundary of the body region forms a channel region.

1 25. The transistor of claim 24 wherein the portion of the silicon-
2 germanium layer through which the source region extends is of first conductivity type, and
3 the portion of the silicon-germanium layer through which the body region extends is of the
4 second conductivity type.

1 26. A method of forming a trench-gate field effect transistor, comprising:
2 forming trenches extending into a silicon region of a first conductivity type;
3 forming a gate electrode in each trench;
4 forming body regions of a second conductivity such that each body region
5 includes a lower silicon region forming a first PN junction with the silicon region, a silicon-
6 germanium layer over the lower silicon layer, and an upper silicon layer over the silicon-
7 germanium layer; and
8 forming source regions of the first conductivity type flanking the trenches,
9 each source region forming a second PN junction with the upper silicon layer.

1 27. The method of claim 26 wherein each silicon-germanium layer abuts
2 sidewalls of two adjacent trenches.

1 28. The method of claim 26 wherein each silicon-germanium layer is
2 vertically spaced from corresponding first and second PN junctions.

1 29. The method of claim 26 further comprising:
2 before forming the gate electrode:
3 forming a shield dielectric layer lining lower sidewalls of each trench;
4 forming a shield electrode in a lower portion of each trench; and
5 forming an inter-electrode dielectric layer over the shield electrode in
6 each trench.

1 30. The method of claim 26 further comprising:
2 before forming the gate electrode, forming a thick bottom dielectric along a
3 bottom of each trench.

1 31. The method of claim 26 wherein when the transistor is in an on state, a
2 channel is formed in the body region along each trench sidewall between each source region
3 and a bottom surface of a corresponding body region, the silicon-germanium laterally
4 extending into at least a portion of the channel so as to reduce the channel resistance.

1 32. The method of claim 26 wherein the step of forming body regions
2 includes:
3 forming a silicon-germanium layer over the silicon region;
4 forming an epitaxial silicon layer over the silicon-germanium layer, the
5 epitaxial silicon layer forming the upper silicon layer;
6 implanting dopants of second conductivity type through the silicon-
7 germanium layer and the epitaxial silicon layer to thereby form an implant region in the
8 silicon region, the implant region forming the lower silicon layer.

1 33. The method of claim 26 wherein the step of forming body regions
2 includes:
3 implanting dopants of the second conductivity type to form an implant region
4 of the second conductivity type in the silicon region; and
5 implanting dopants to form a layer of silicon-germanium layer within the
6 implant region such that a portion of the implant region extending below the silicon-
7 germanium layer forms the lower silicon region, and a portion of the implant region
8 extending over the silicon-germanium layer forms the upper silicon region.

1 34. A method of forming a trench-gate field effect transistor, comprising:
2 forming trenches extending into a silicon region of a first conductivity type;
3 forming body regions of a second conductivity such that each body region
4 forms a PN junction with the silicon region, and each body region includes a vertically
5 extending silicon-germanium layer;
6 forming a gate electrode in each trench; and
7 forming source regions of the first conductivity flanking the trenches,
8 wherein the silicon-germanium layers terminate along the vertical dimension
9 before reaching the PN junction.

1 35. The method of claim 15 wherein each silicon-germanium layer is
2 spaced from the corresponding PN junction a distance in the range of 500 Å to 1,000 Å.

1 36. The method of claim 15 wherein each silicon-germanium layer is
2 bounded along its vertical boundaries by silicon regions.

1 37. The method of claim 15 wherein when the transistor is in an on state, a
2 channel region is formed in the body region along each trench sidewall between each source
3 region and a bottom surface of a corresponding body region, and the silicon-germanium layer
4 forms at least a part of the channel region so as to reduce the channel resistance.

1 38. The method of claim 15 wherein the step of forming body regions
2 includes:
3 forming a dielectric layer in each trench;
4 lining upper trench sidewalls with a silicon-germanium layer over the
5 dielectric layer;
6 recessing the dielectric layer to expose a portion of each trench sidewall
7 directly below the silicon-germanium layer;
8 forming an epitaxial silicon layer inside the trench such that the epitaxial layer
9 lines the exposed portion of each trench sidewall; and
10 implanting dopants of the second conductivity type into the silicon region, the
11 silicon-germanium layer and the epitaxial silicon layer to thereby form the body region.

1 39. The method of claim 15 wherein the silicon-germanium regions are
2 formed inside the trenches.

1 40. The method of claim 15 wherein the transistor is an P-channel
2 transistor with the first conductivity type being P-type and the second conductivity type being
3 N-type.

1 41. The method of claim 26 further comprising:
2 before forming the gate electrode:
3 forming a shield dielectric layer lining lower sidewalls of each trench;
4 forming a shield electrode in a lower portion of each trench; and
5 forming an inter-electrode dielectric layer over the shield electrode in
6 each trench.

1 42. The method of claim 26 further comprising:
2 before forming the gate electrode, forming a thick bottom dielectric along a
3 bottom of each trench.

1 43. A method of forming a vertically-conducting planar-gate field effect
2 transistor comprising:
3 forming a silicon-germanium layer over a silicon region of a first conductivity
4 type;
5 forming a gate electrode laterally extending over but insulated from the
6 silicon-germanium layer;
7 forming a body region of a second conductivity type extending in the silicon-
8 germanium layer and the silicon region; and
9 forming a source region of the first conductivity type extending at least into
10 the silicon-germanium layer, the gate electrode laterally overlapping both the source and
11 body regions such that a portion of the silicon germanium layer extending directly under the
12 gate electrode between the source region and an outer boundary of the body region forms a
13 channel region.

1 44. The method of claim 43 further comprising:
2 prior to forming source regions, forming dielectric spacers along sidewalls of
3 the gate electrode.

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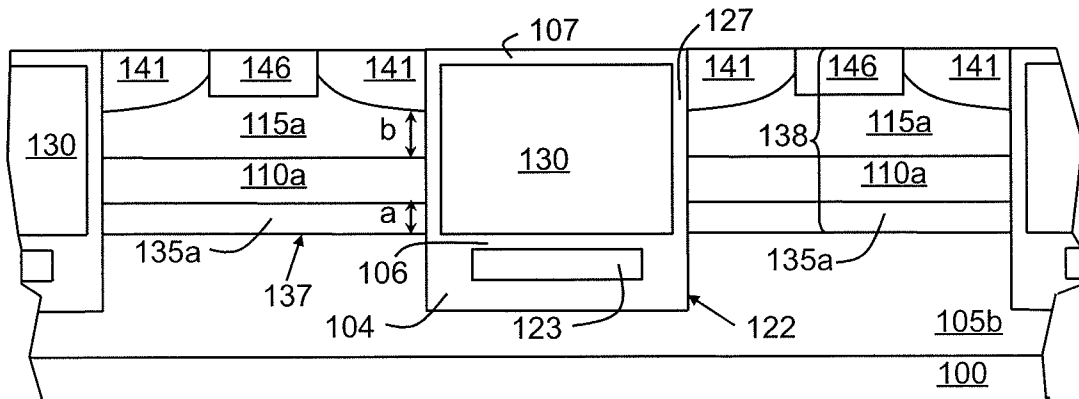


FIG. 1

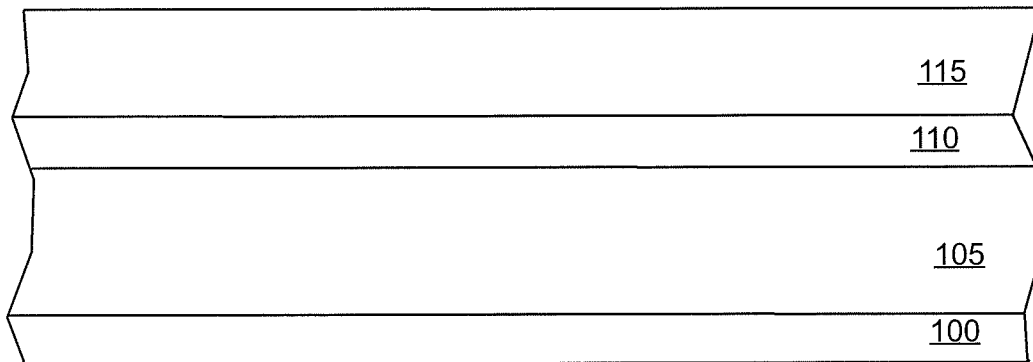


FIG. 2A

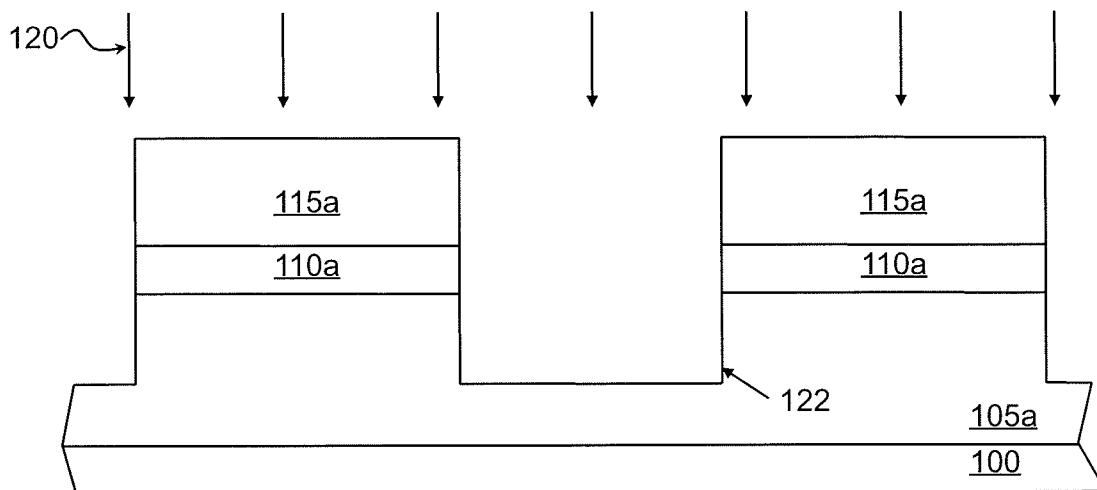


FIG. 2B

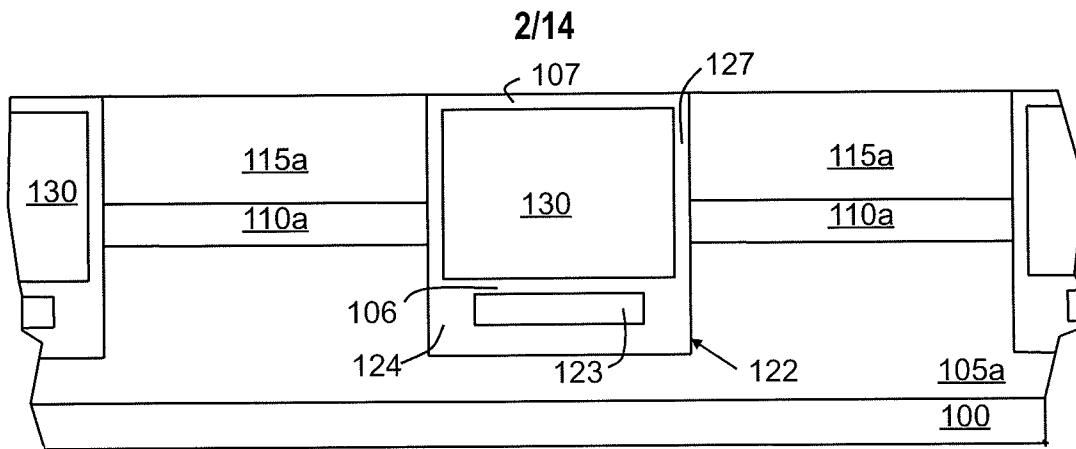


FIG. 2C

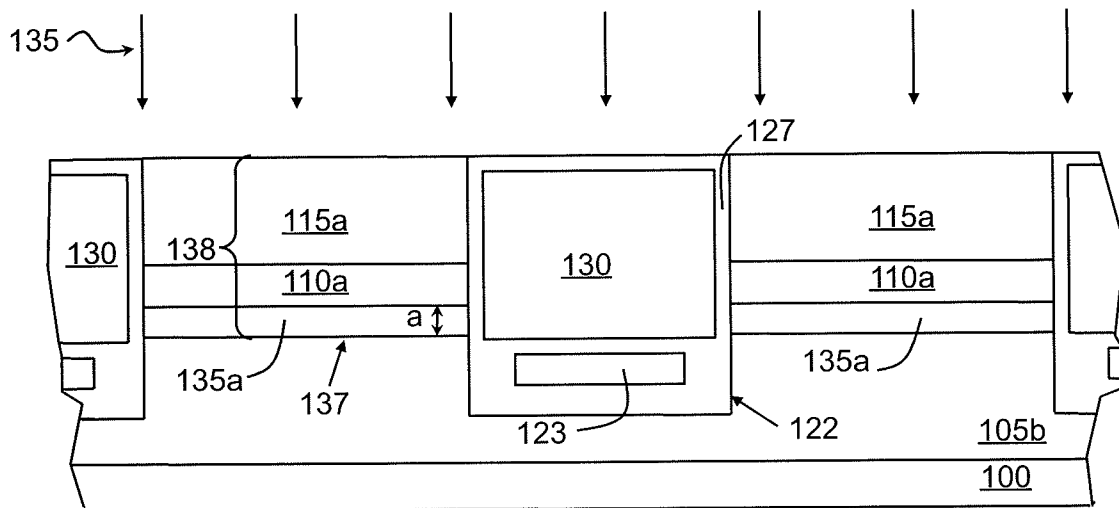


FIG. 2D

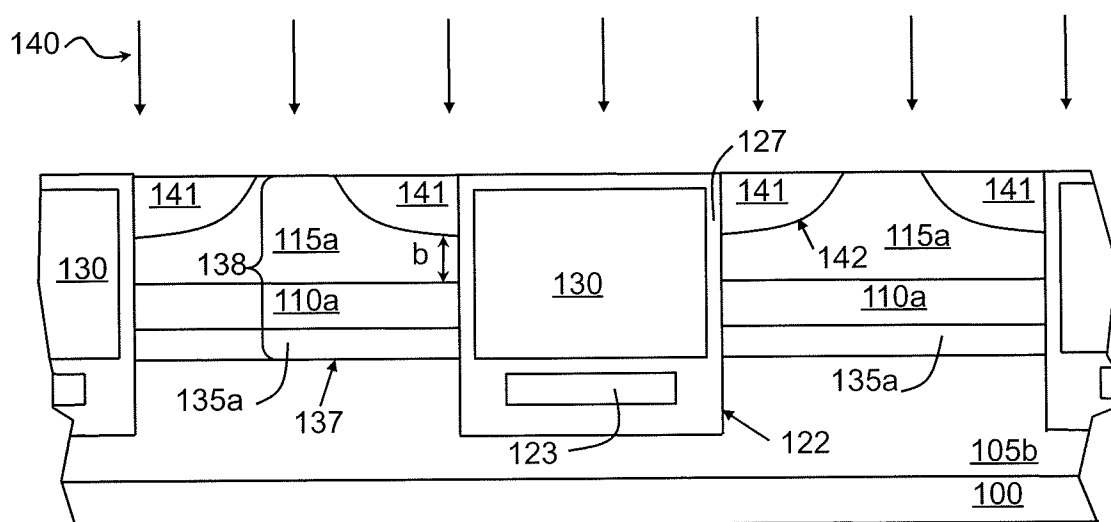


FIG. 2E

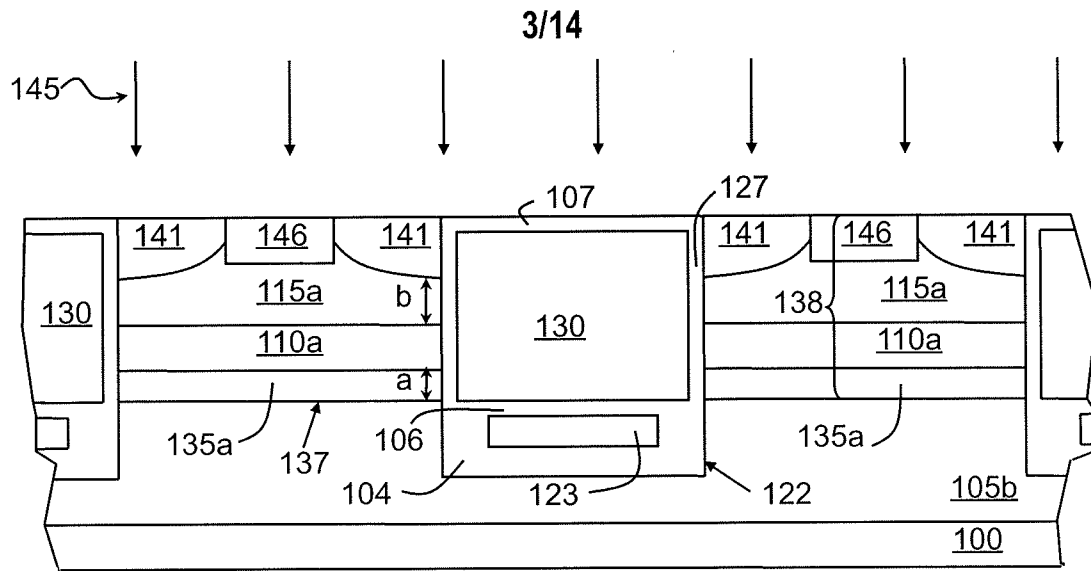


FIG. 2F

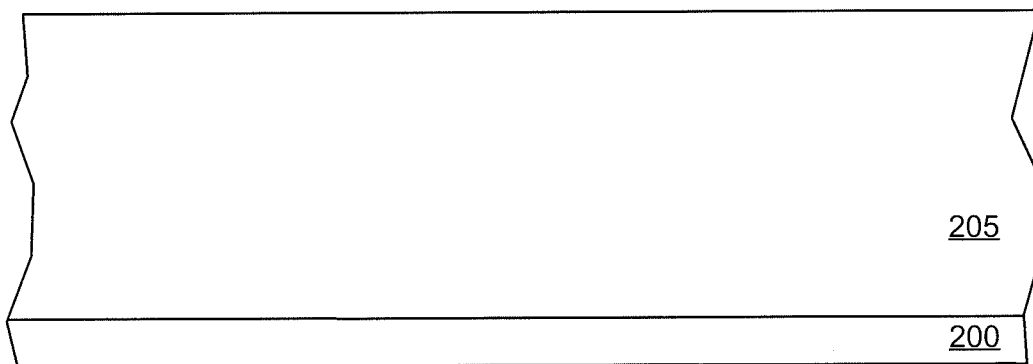


FIG. 3A

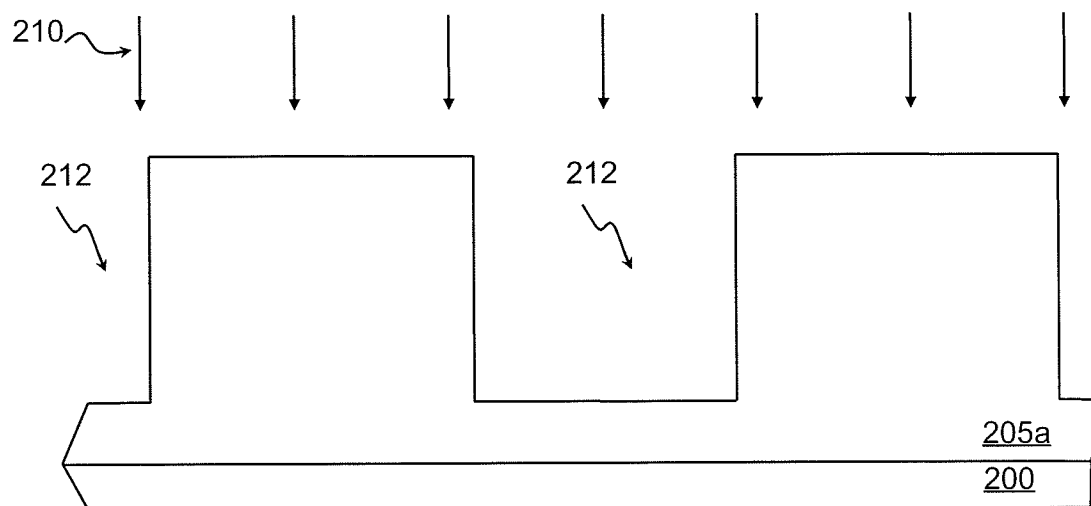


FIG. 3B

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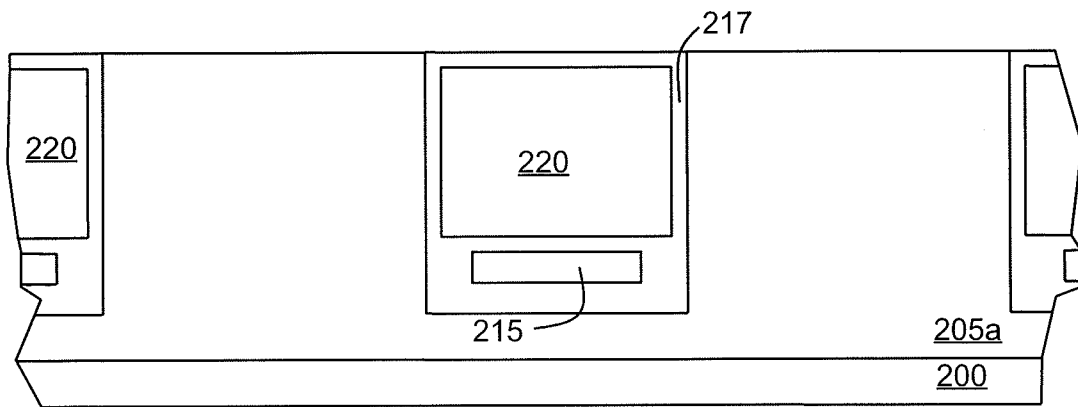


FIG. 3C

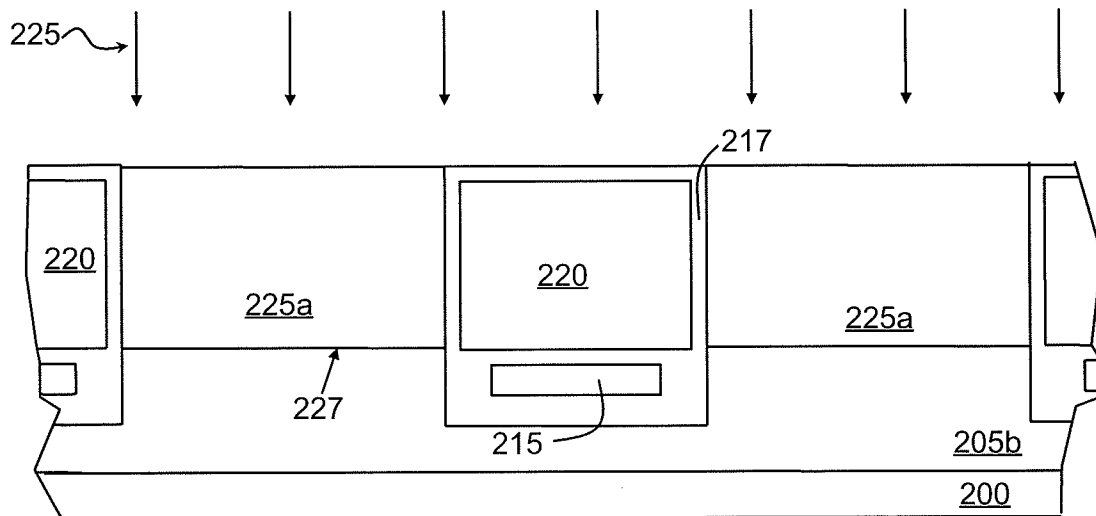


FIG. 3D

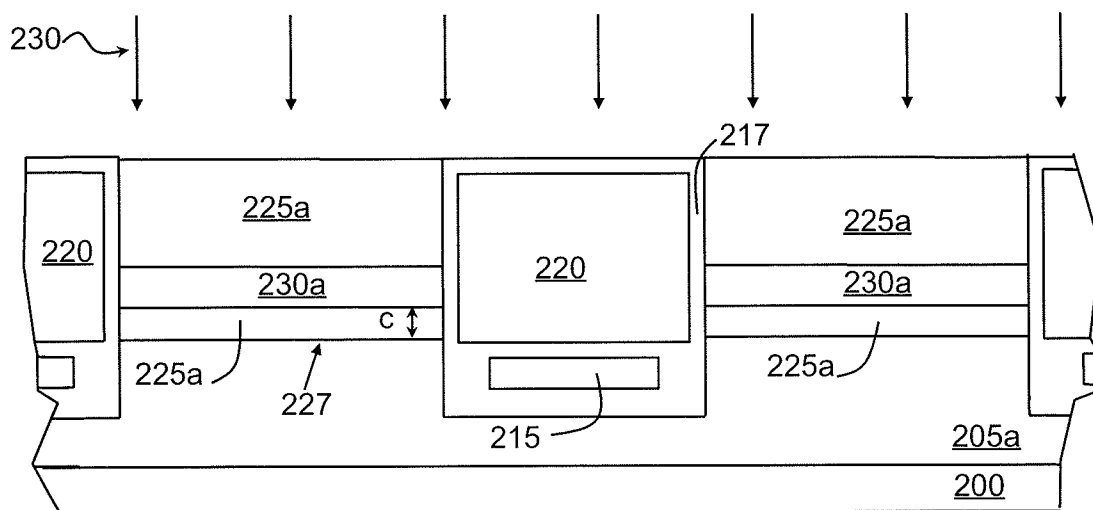


FIG. 3E

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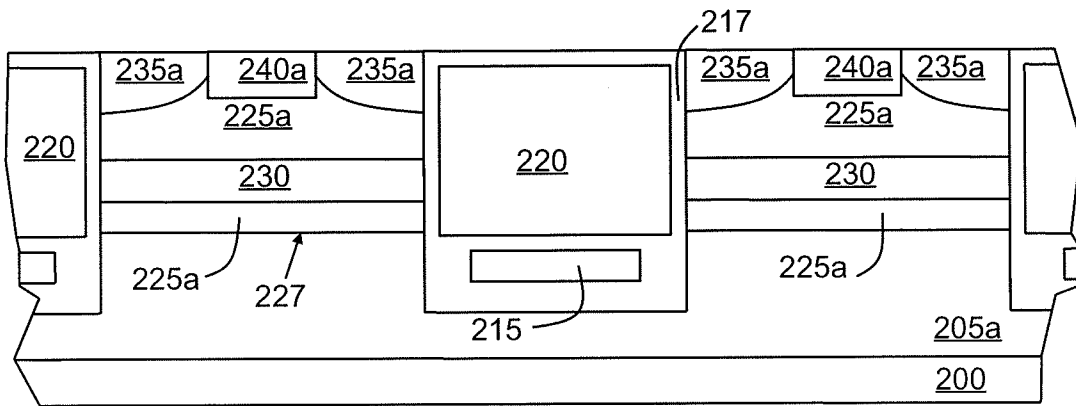


FIG. 3F

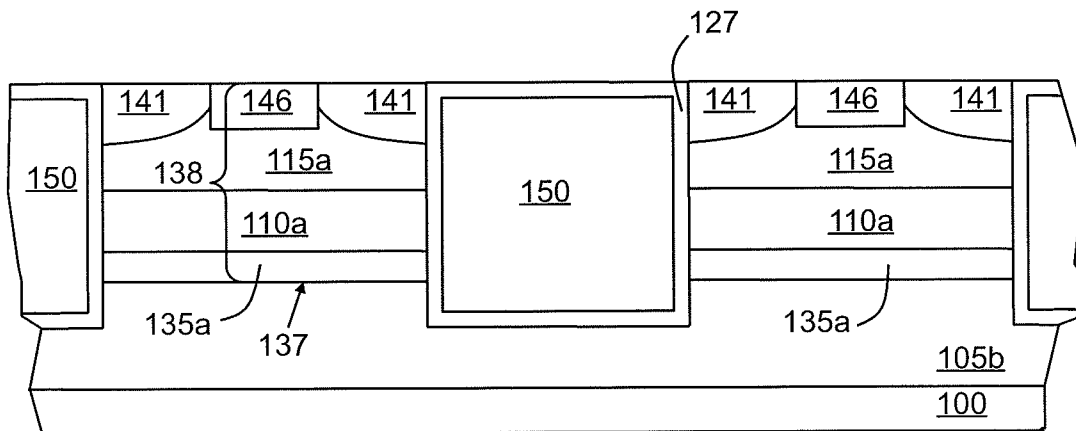


FIG. 4

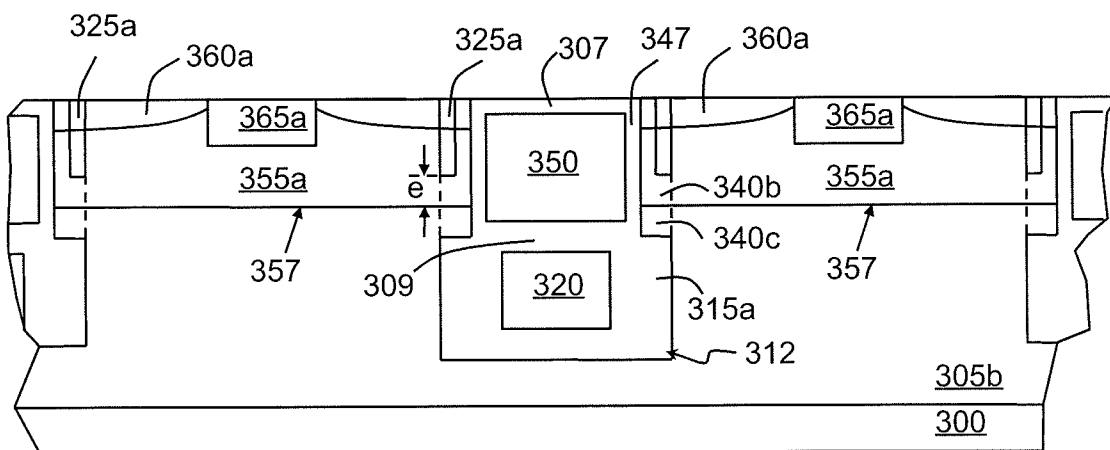


FIG. 5

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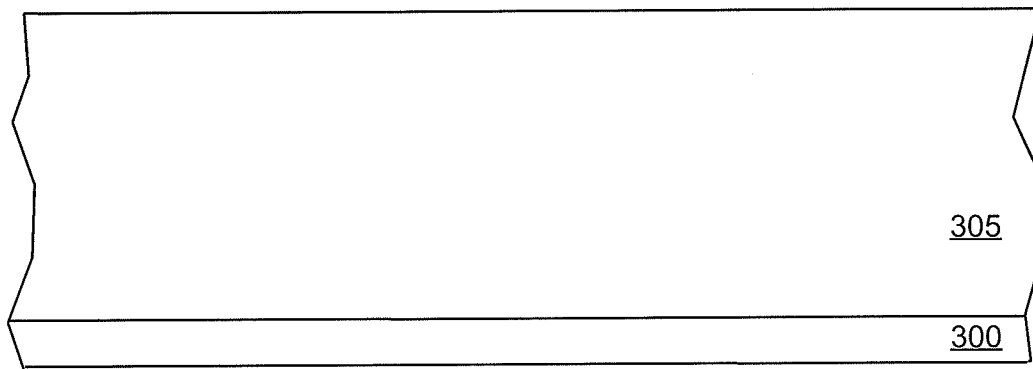


FIG. 6A

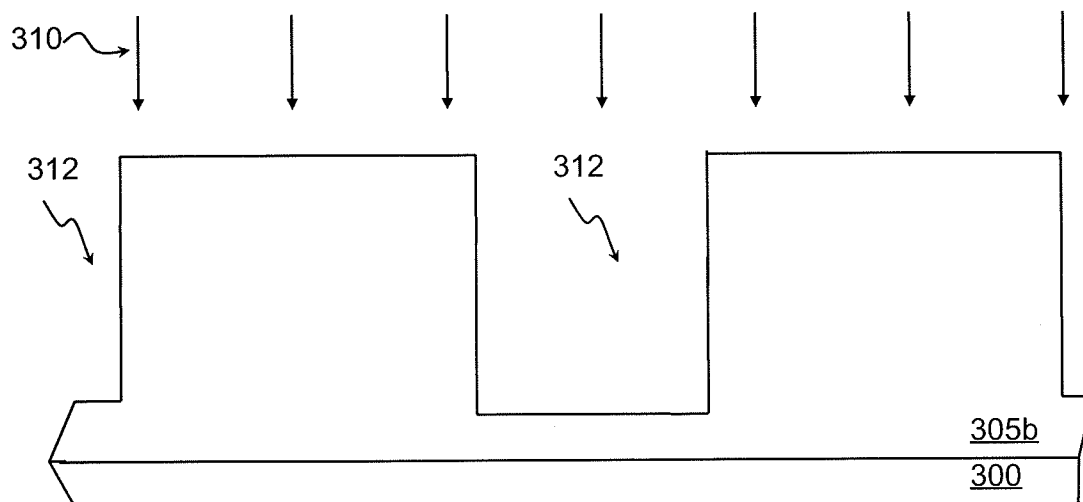


FIG. 6B

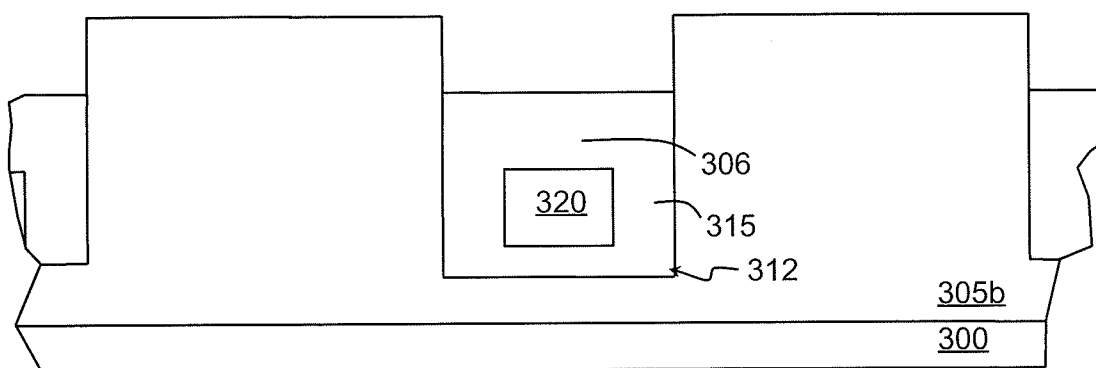


FIG. 6C

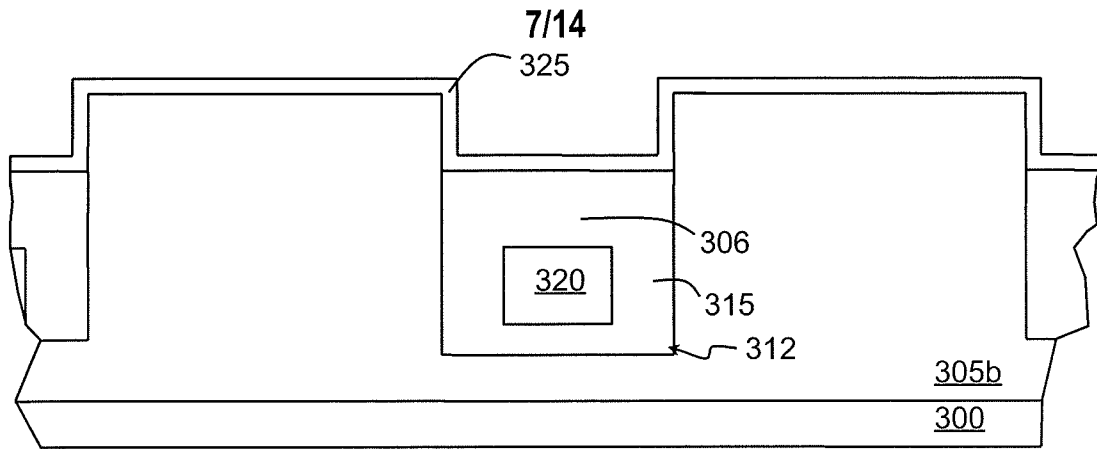


FIG. 6D

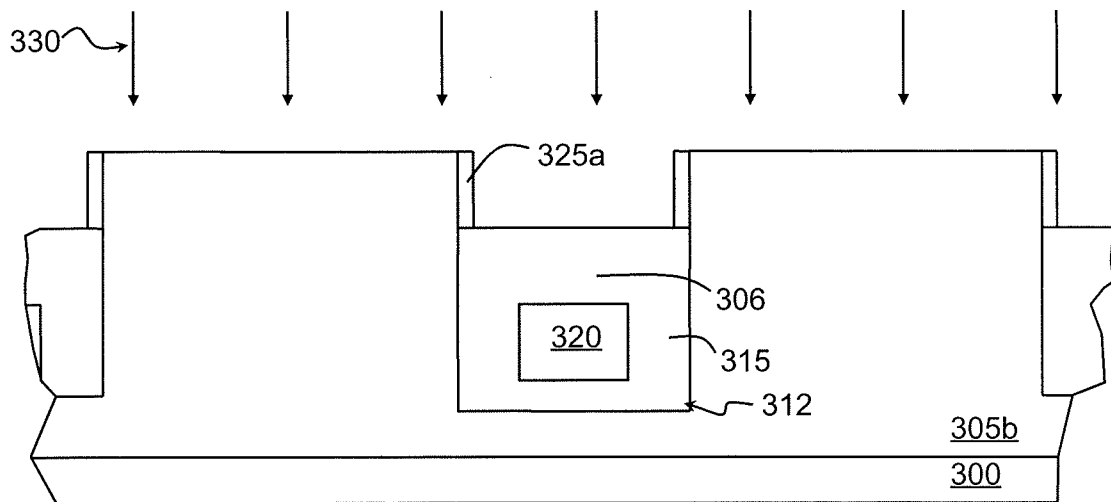


FIG. 6E

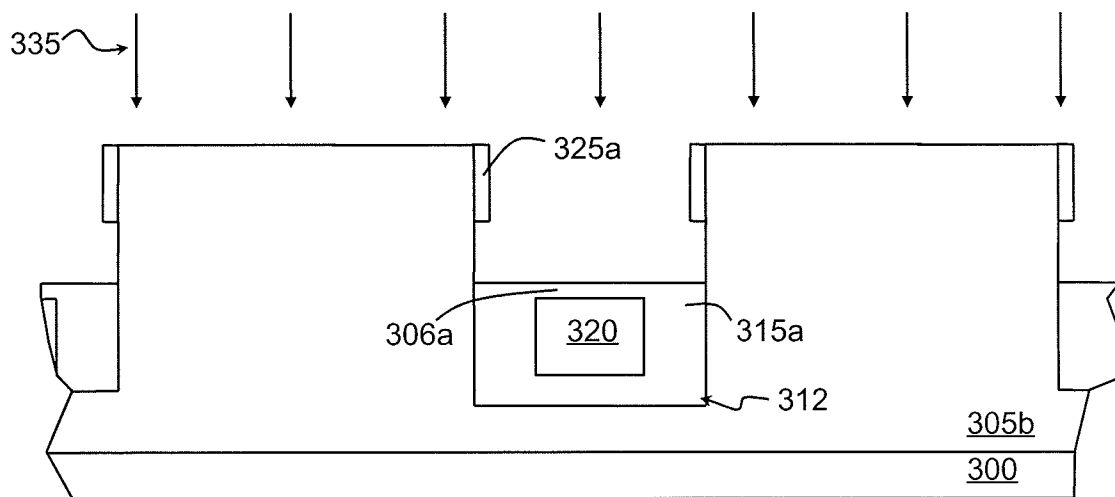


FIG. 6F

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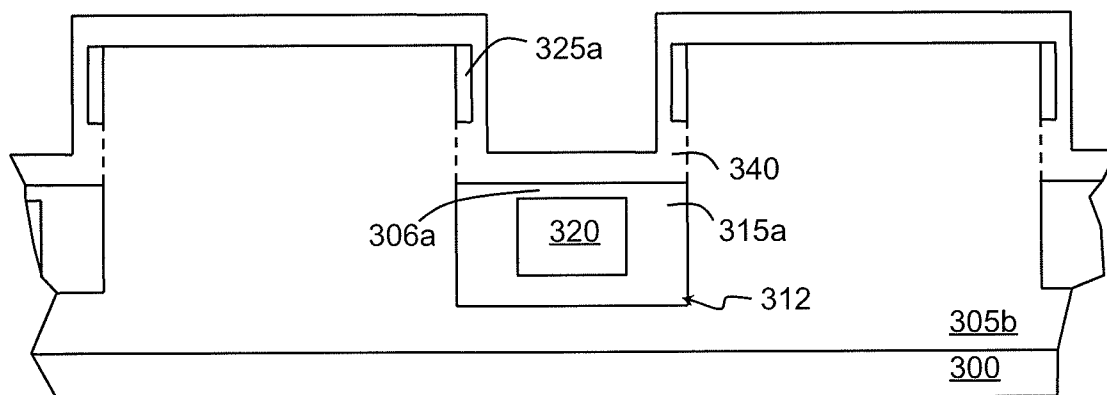


FIG. 6G

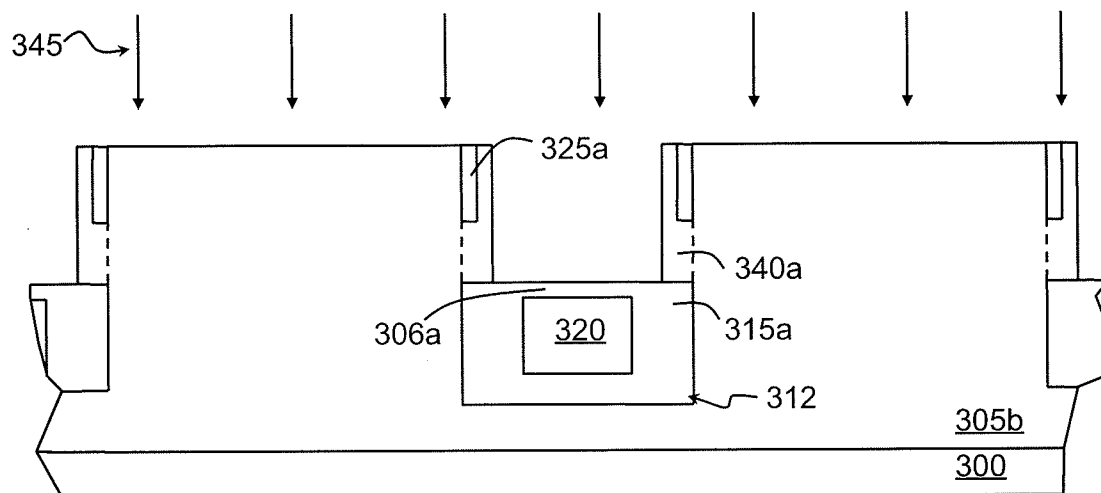


FIG. 6H

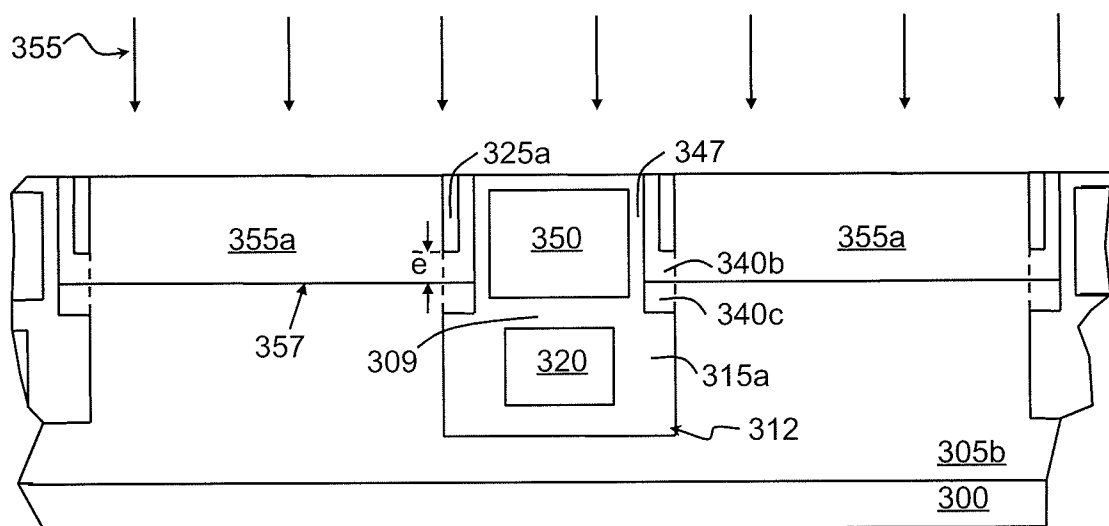


FIG. 6I

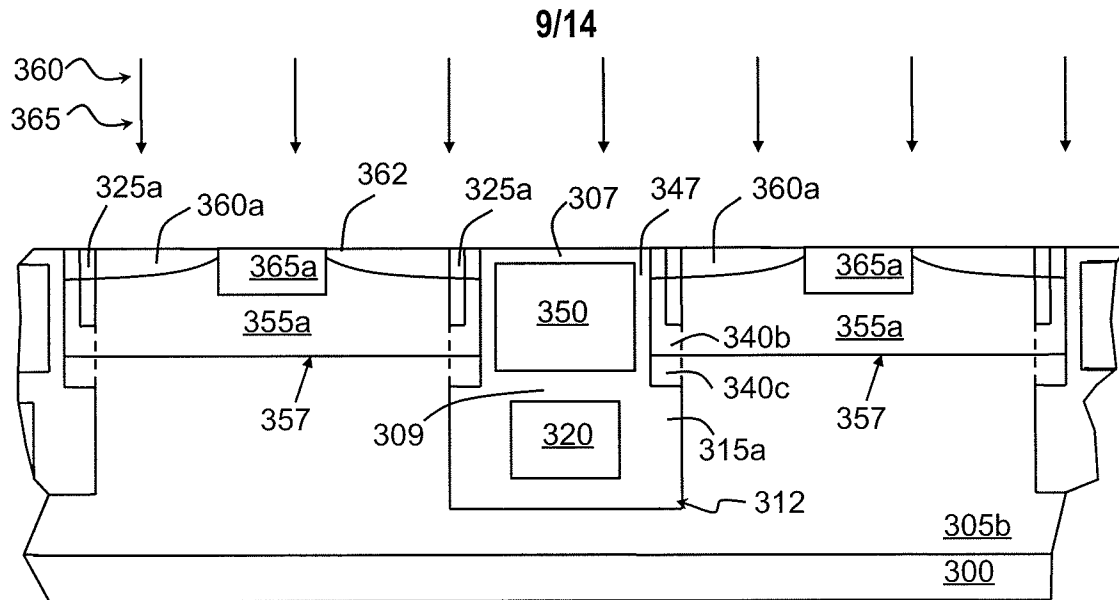


FIG. 6J

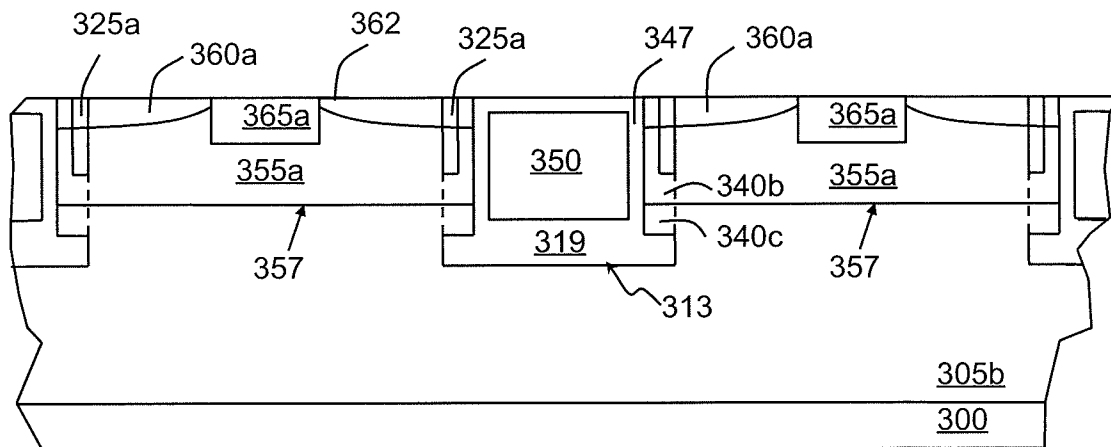


FIG. 7

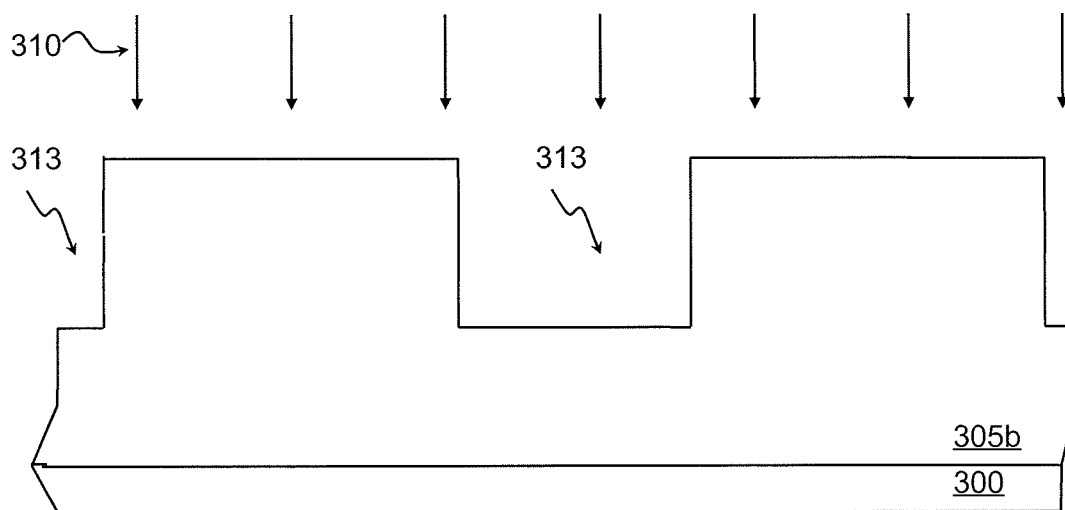


FIG. 8A

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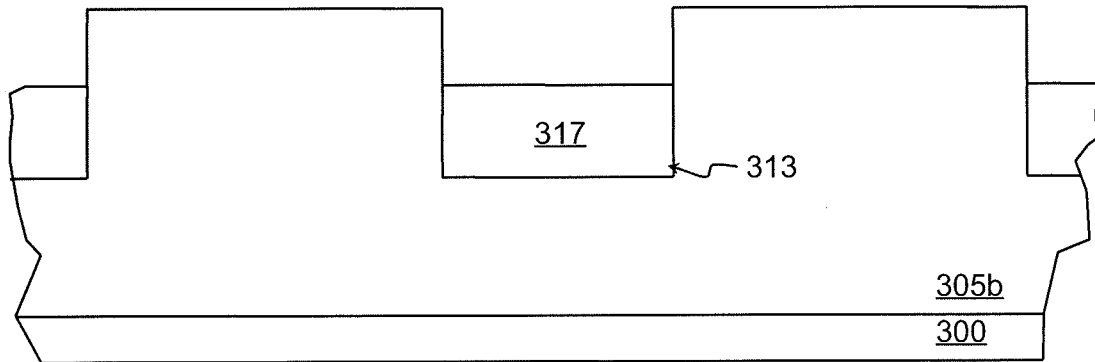


FIG. 8B

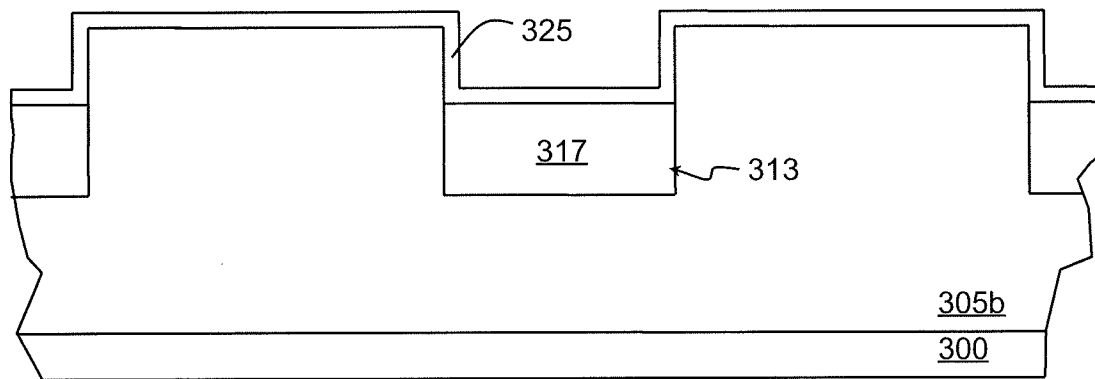


FIG. 8C

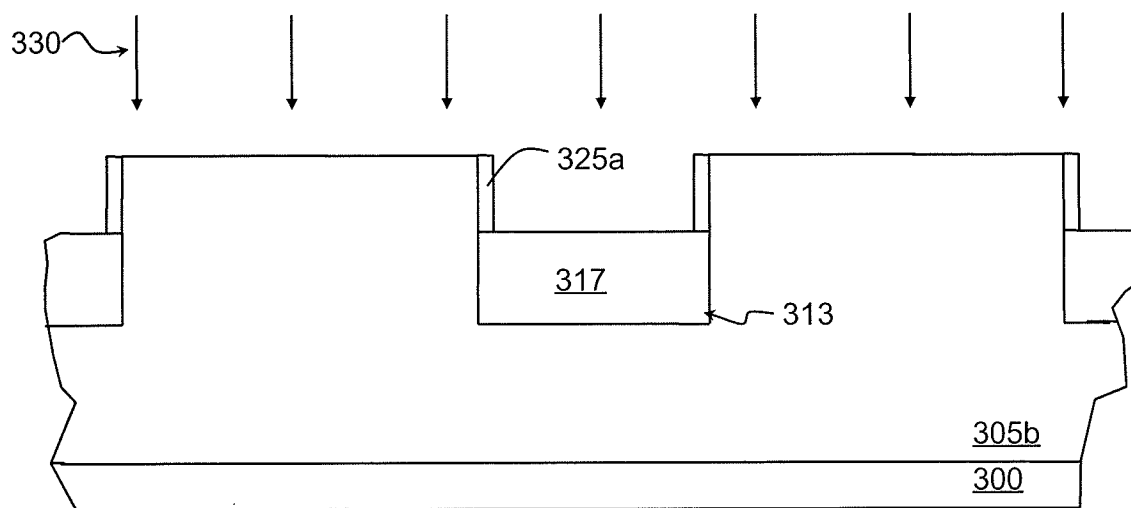


FIG. 8D

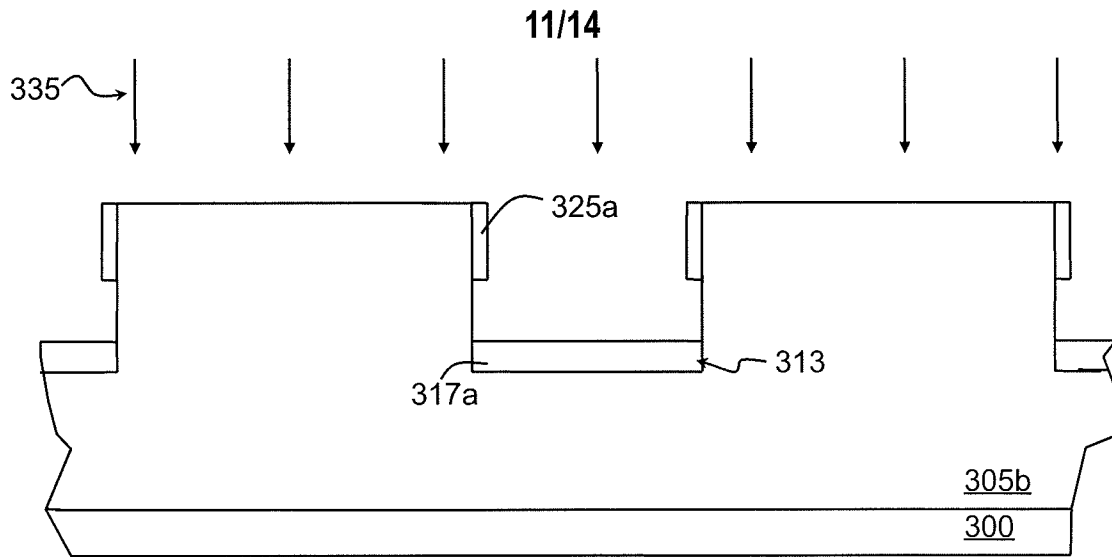


FIG. 8E

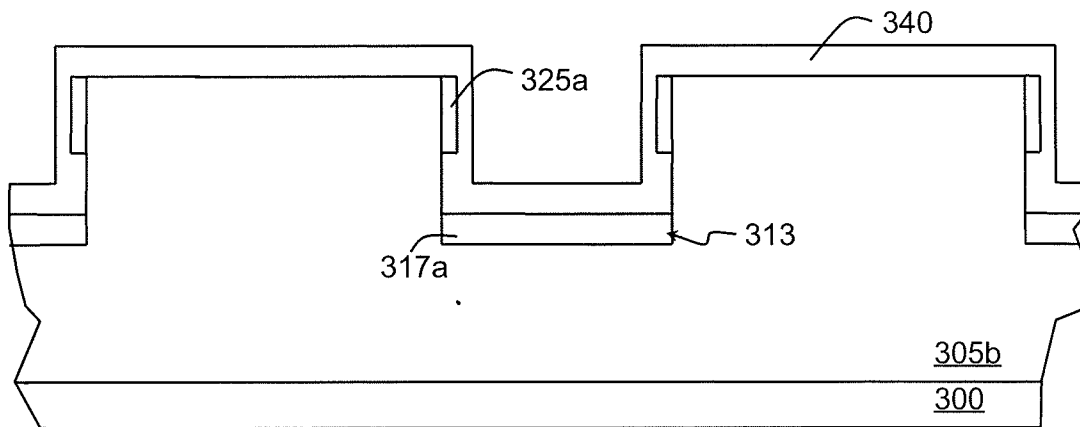


FIG. 8F

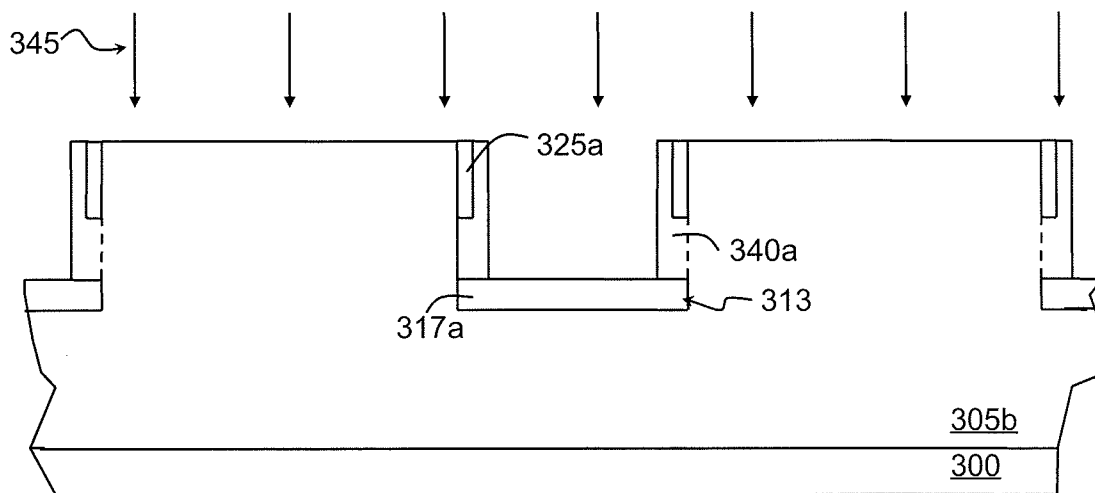


FIG. 8G

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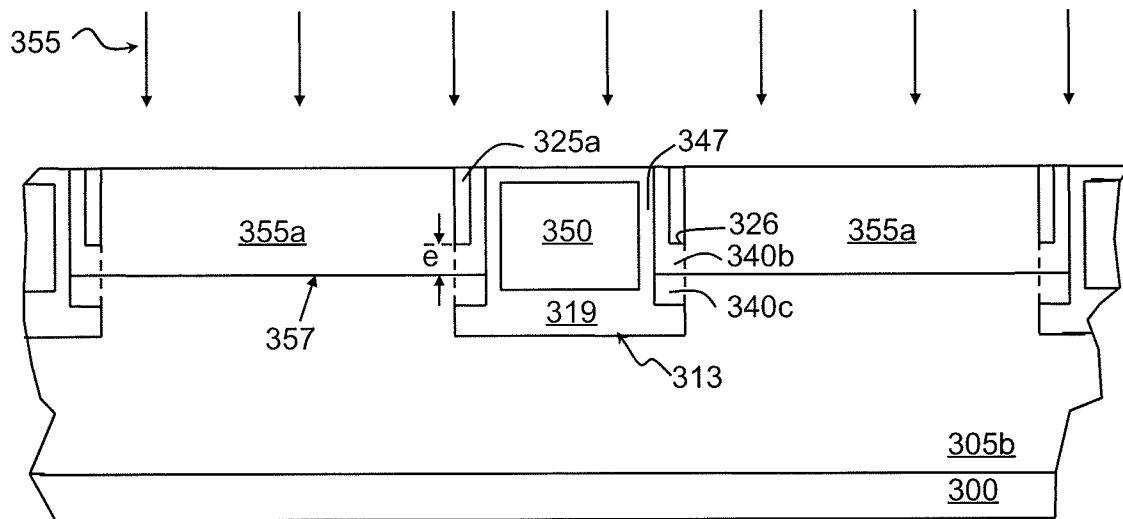


FIG. 8H

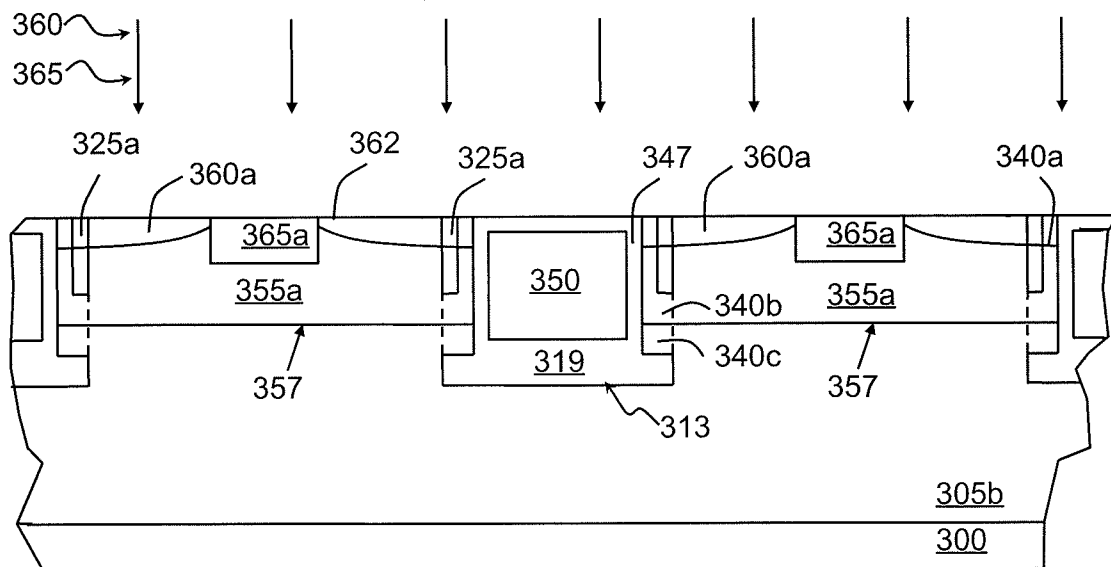


FIG. 81

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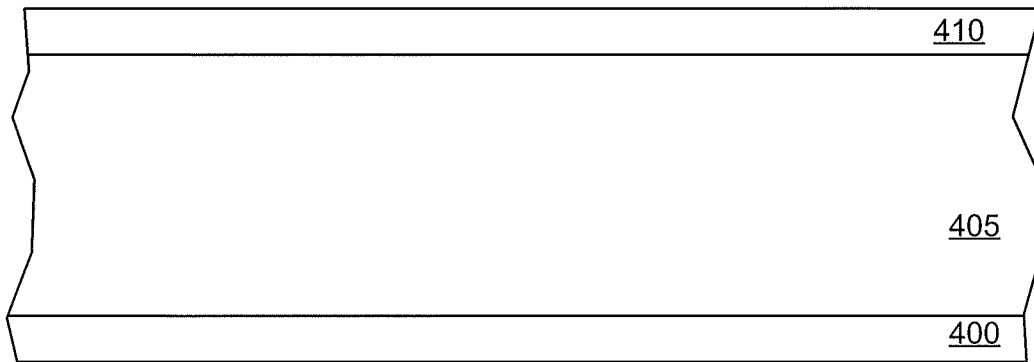


FIG. 9A

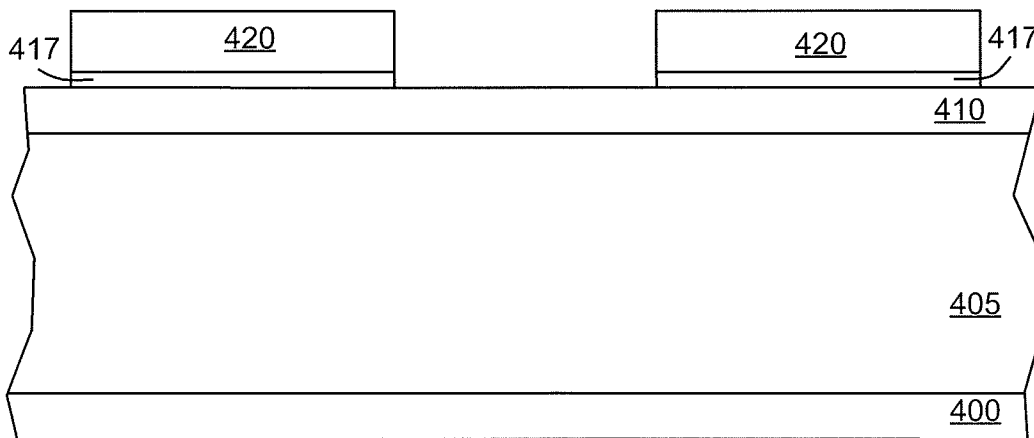


FIG. 9B

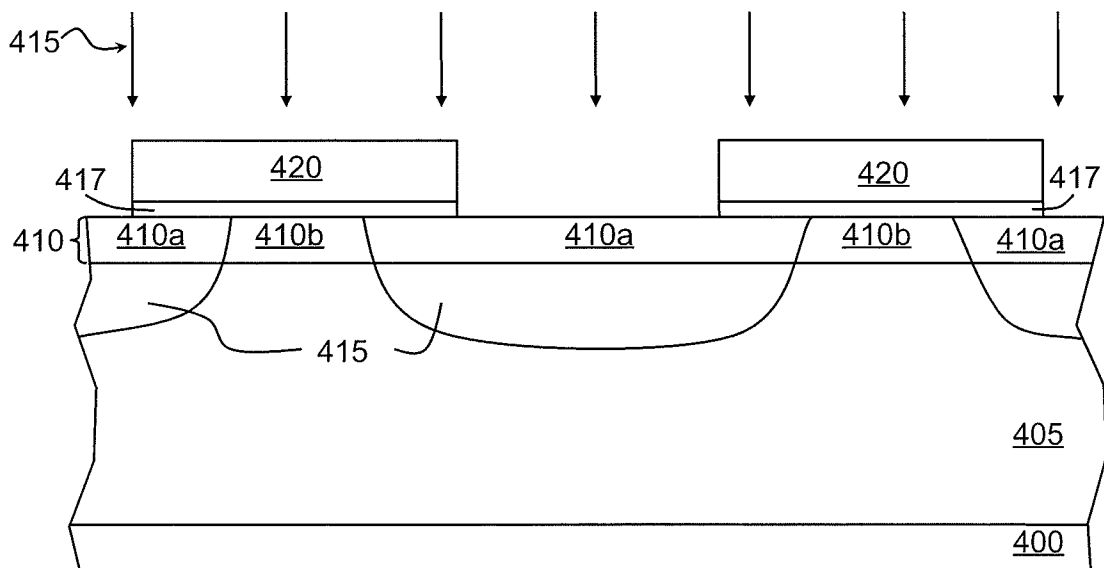


FIG. 9C

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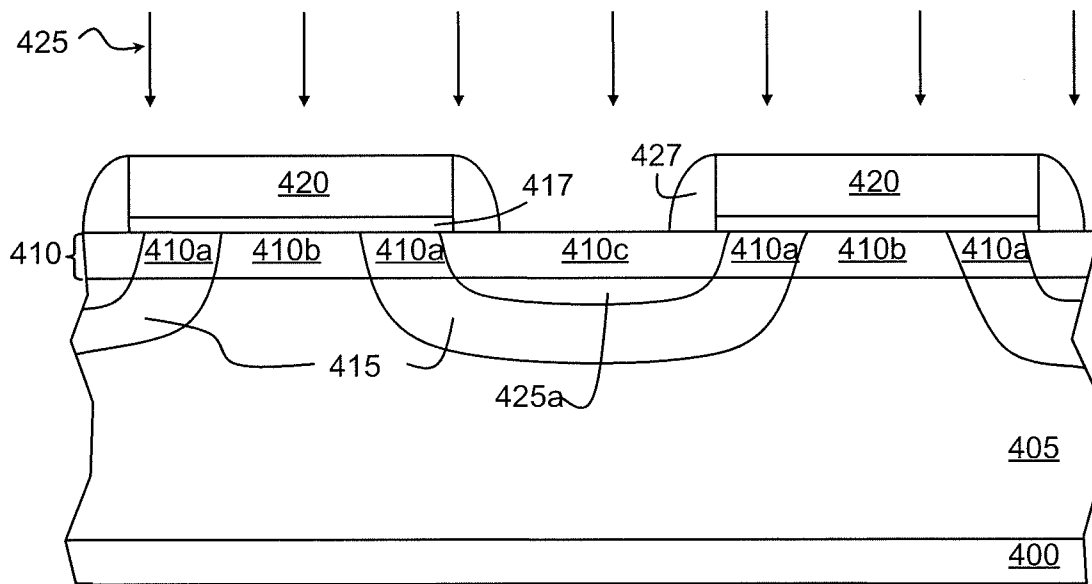


FIG. 9D

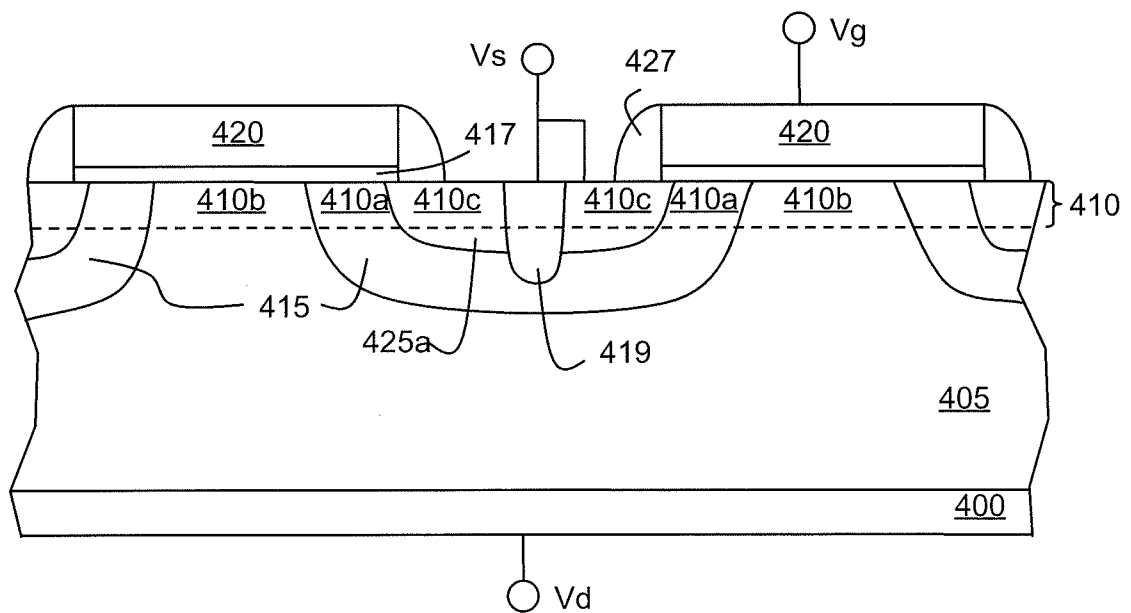


FIG. 9E

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2008/086081

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 29/76 (2009.01)

USPC - 257/328

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - H01L 29/76 (2009.01)

USPC - 257/328

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatBase, Google Patent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,239,463 B1 (WILLIAMS et al) 29 May 2001 (29.05.2001) entire document	1-44
Y	US 6,191,432 B1 (SUGIYAMA et al) 20 February 2001 (20.02.2001) entire document	1-14, 18, 24-34, 37, 41-44
Y	US 7,078,283 B1 (WANG) 18 July 2006 (18.07.2006) entire document	15-23, 35-40
Y	US 2006/0273386 A1 (YILMAZ et al) 07 December 2006 (07.12.2006) entire document	7, 12, 22, 29, 41
Y	US 2006/0226455 A1 (LEE et al) 12 October 2006 (12.10.2006) entire document	19, 20, 38, 39
Y	US 2006/0157806 A1 (RHODES) 20 July 2006 (20.07.2006) entire document	33

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Date of the actual completion of the international search

27 January 2009

Date of mailing of the international search report

19 FEB 2009

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