

[54] MULTI-CHANNEL AC CONFLICT
MONITOR

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[22] Filed: Oct. 7, 1974

[21] Appl. No.: 512,874

[52] U.S. Cl. 340/41 R; 340/248 A

[51] Int. Cl.² G08G 1/08

[58] Field of Search 340/41 R, 37

[56] References Cited

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3,828,307 8/1974 Hungerford 340/41 R

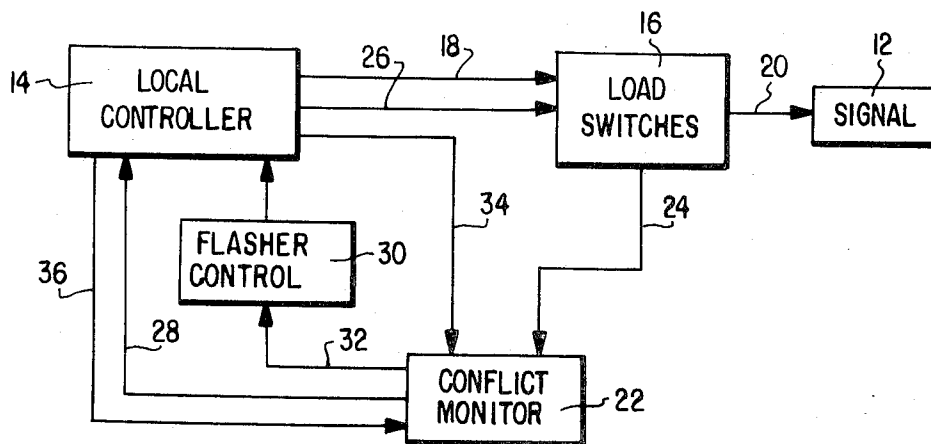
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[57]

ABSTRACT

A circuit is provided for monitoring the signals displayed by a traffic signal system to detect the displaying of conflicting signals to two or more traffic paths. The circuit includes sensors responsive to the energization of the traffic signal lights and logic elements for determining when conflicting signals are displayed. The signal controller can override the monitor circuit to permit certain normally conflicting signal combinations. Additional logic elements in the circuit determine whether overlaps are permissible with the normal signal displays. When the circuit detects a conflict or an improper overlap, it transfers signal light operation from the normal sequencing mode to a flashing mode.

15 Claims, 11 Drawing Figures



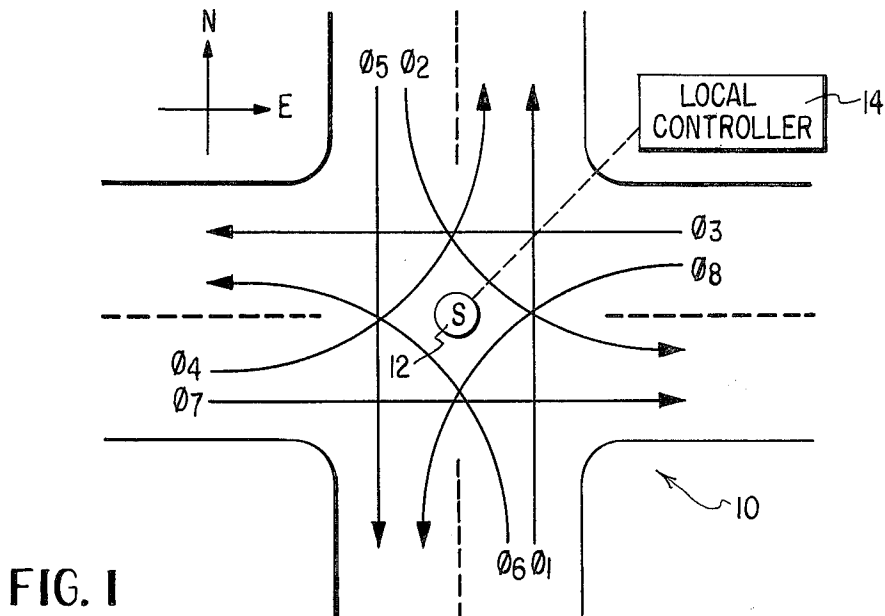


FIG. 1

PHASE	CONFLICTS WITH INPUTS TO PHASES	COMPATABLE WITH INPUTS TO PHASES
1	2, 3, 4, 7, 8	5, 6
2	1, 3, 4, 7, 8	5, 6
3	1, 2, 4, 5, 6	7, 8
4	1, 2, 3, 5, 6	7, 8
5	3, 4, 6, 7, 8	1, 2
6	3, 4, 5, 7, 8	1, 2
7	1, 2, 5, 6, 8	3, 4
8	1, 2, 5, 6, 7	3, 4

FIG. 2

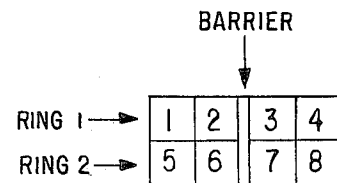


FIG. 3

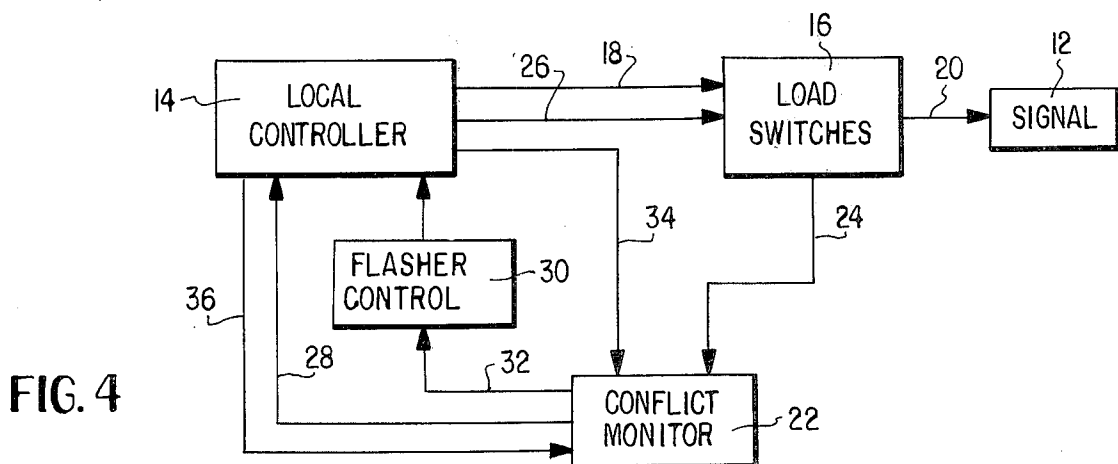


FIG. 4

FIG. 5A

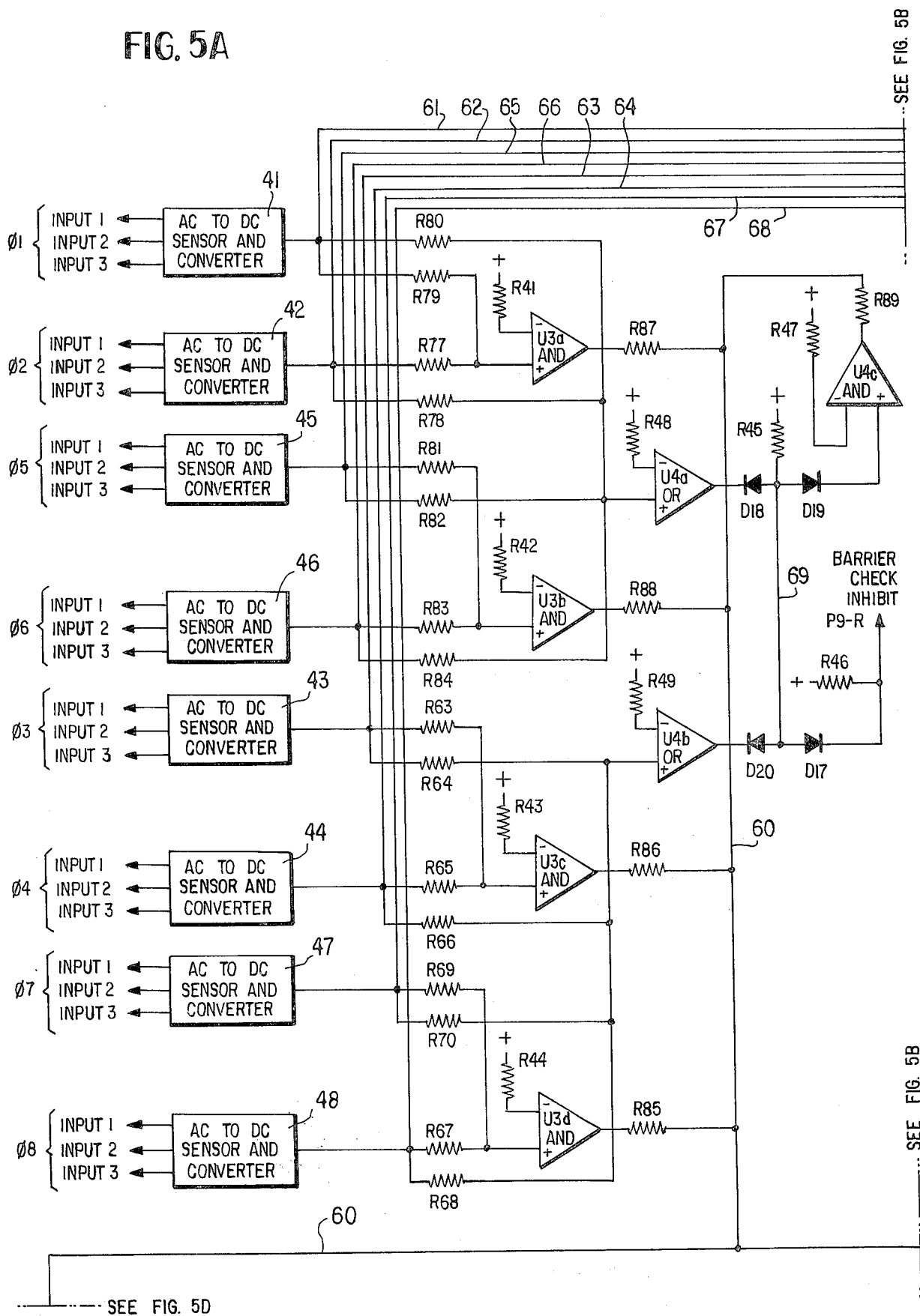


FIG. 5B

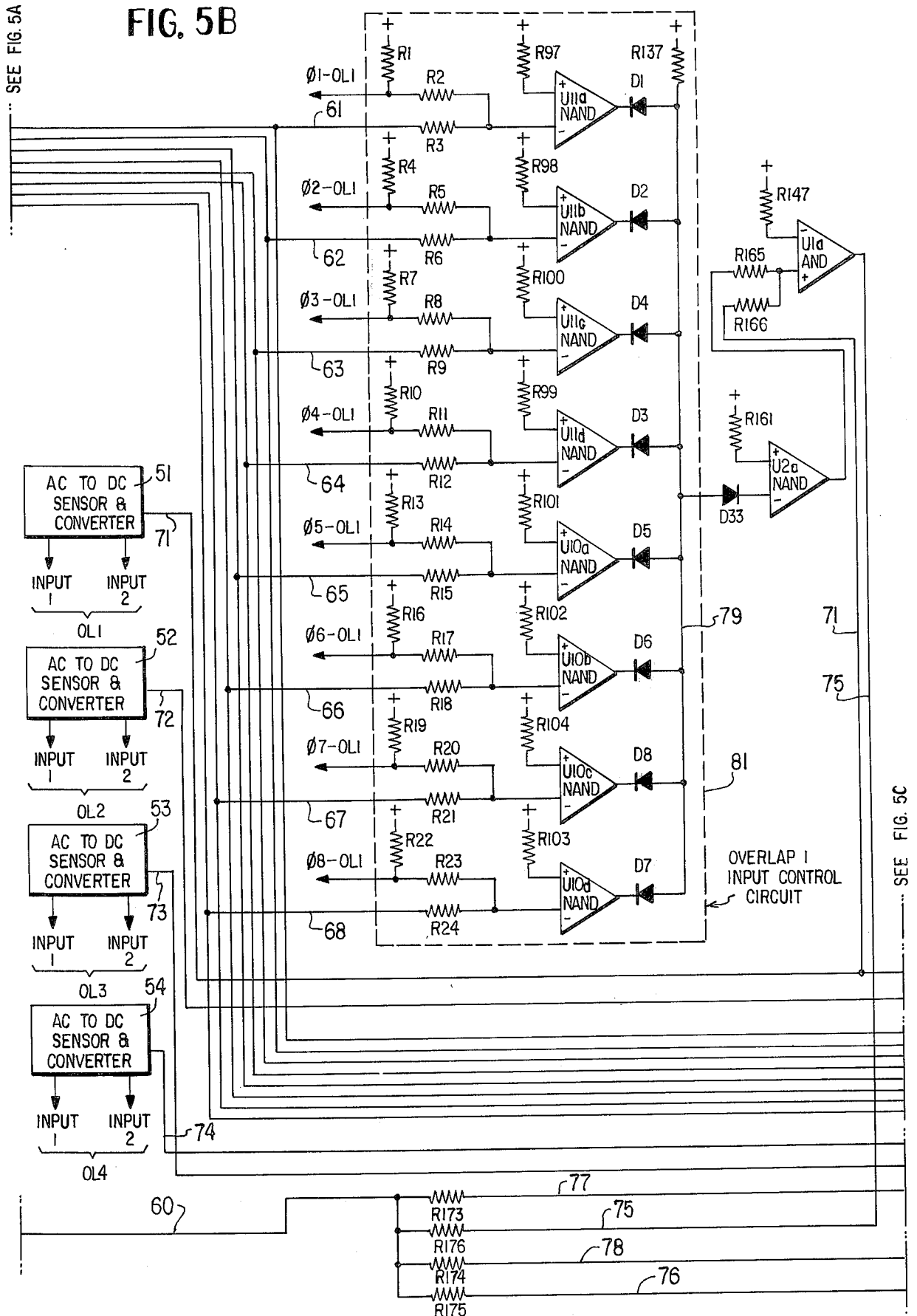
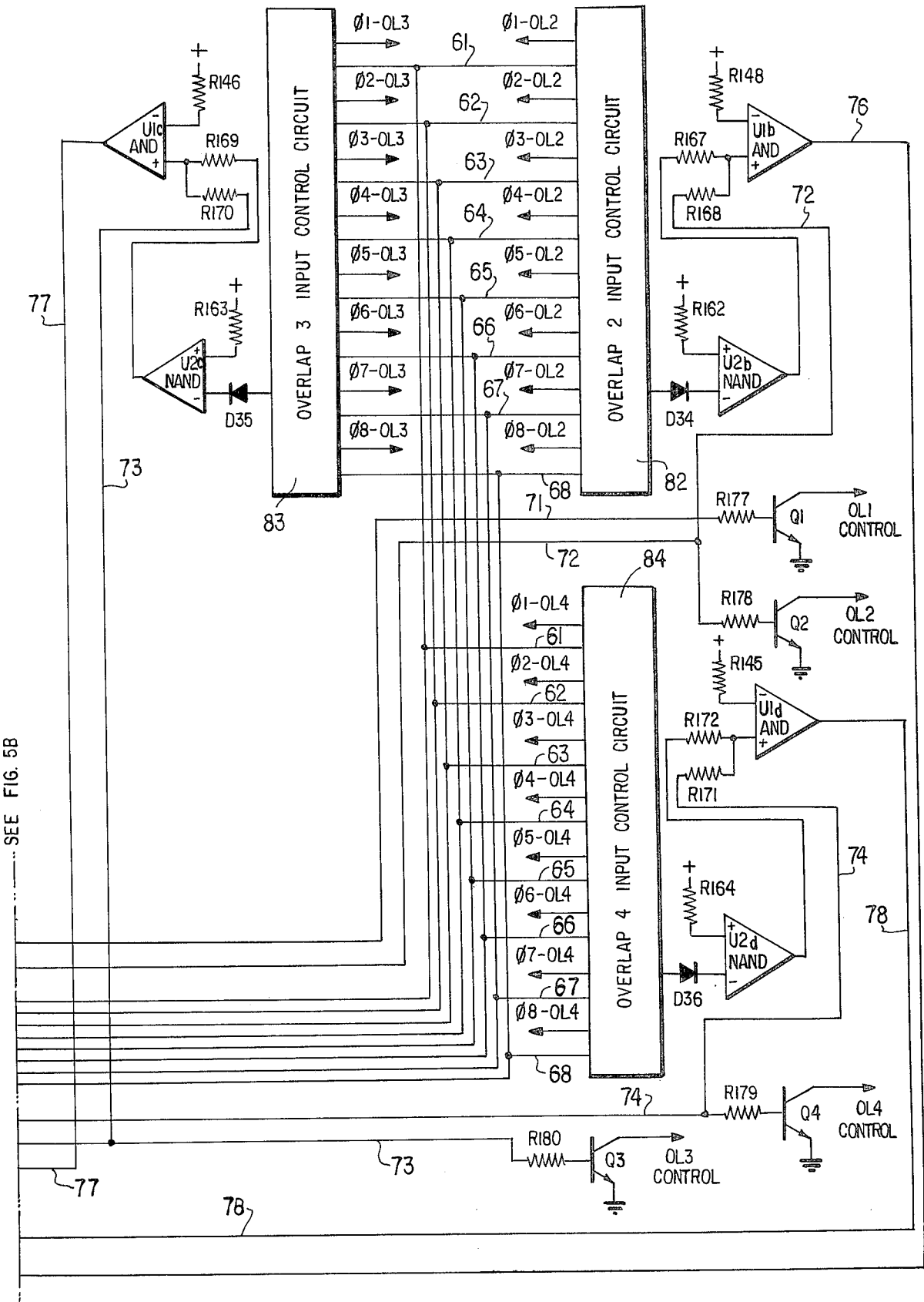


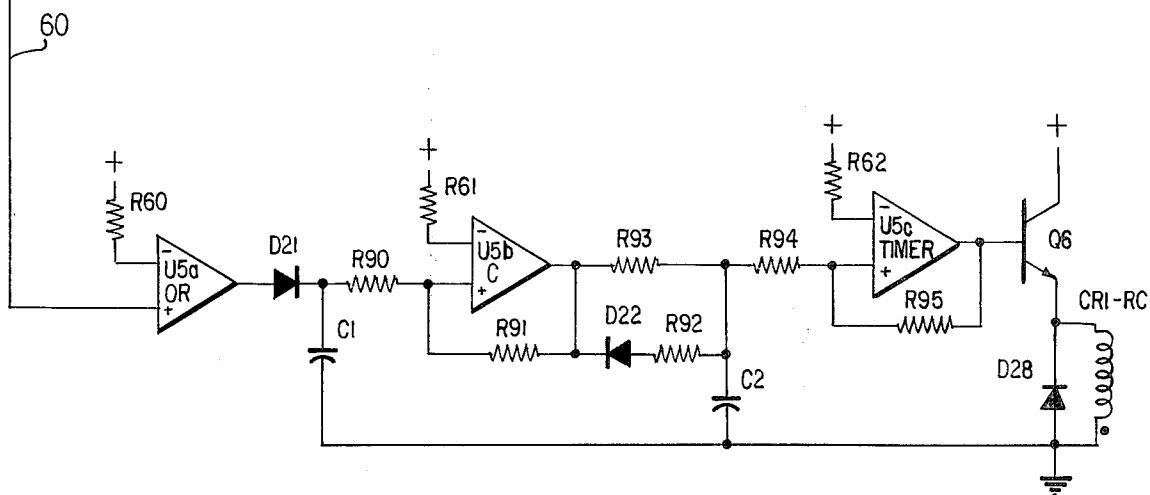
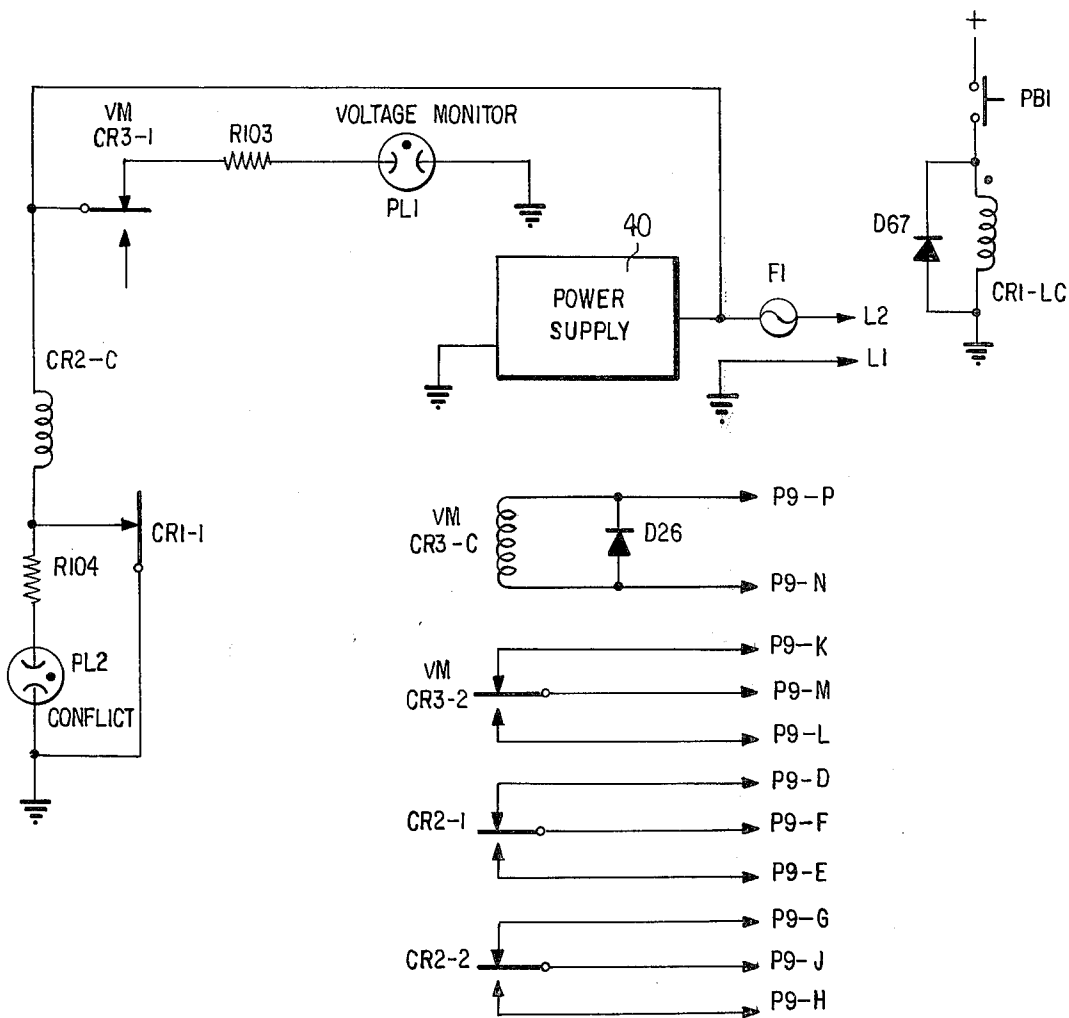
FIG. 5C



SEE FIG. 5B

SEE FIG. 5A

FIG. 5D



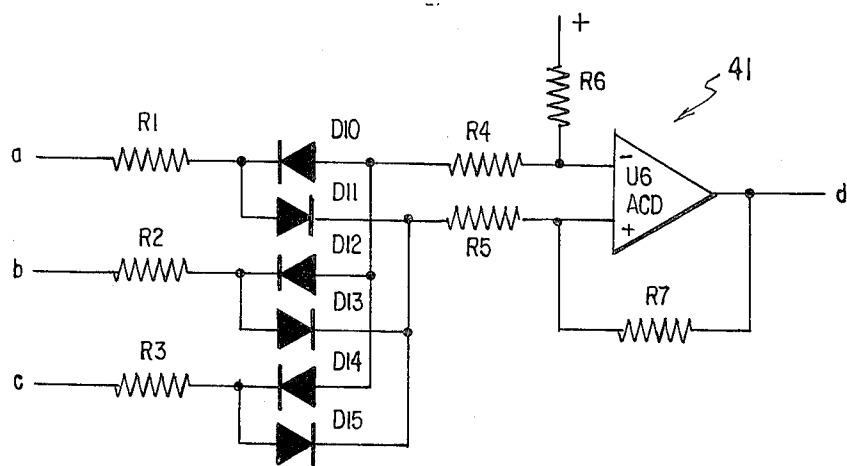


FIG. 6

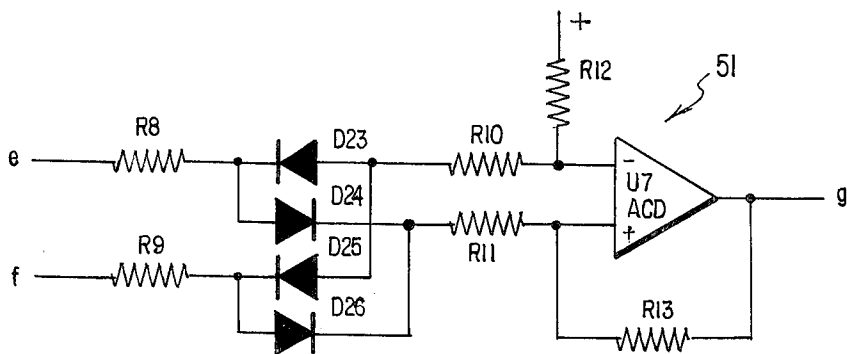


FIG. 7

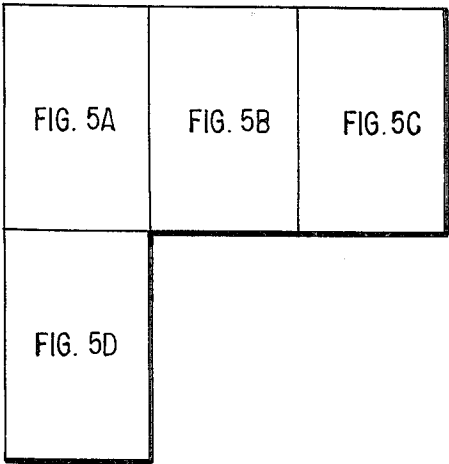


FIG. 8

MULTI-CHANNEL AC CONFLICT MONITOR

BACKGROUND OF THE INVENTION

The present invention pertains to traffic light controllers and, more particularly, to systems for monitoring the operation of traffic light controllers to prevent the displaying of conflicting traffic controlling signals.

The control of vehicular and pedestrian traffic at intersections is commonly accomplished by the use of traffic light systems providing command signals to the motorists and pedestrians to regulate the orderly flow of traffic. These signal systems normally operate under the control of a local controller which sequentially actuates the individual signal lights to provide proceed (green or WALK), caution (yellow) or stop (red or DON'T WALK) signals. Under normal operating conditions, the controller sequence is such that proceed or caution signals will be given only to those traffic flow patterns which are not in conflict with one another. In the event of a malfunction of the system, however, permissive indications such as proceed or caution signals may be given to conflicting traffic flow routes. Such malfunctioning presents a hazardous situation as motorists frequently tend to rely on the traffic signal commands. Also, even when the motorists are aware of the malfunctioning, the smooth flow of traffic may be impeded as motorists are often hesitant to proceed through the intersection in such a situation.

Experience has shown that when a traffic light controller malfunctions, the least disruption of traffic flow results if the sequencing of the signal lights by the controller is interrupted and the lights caused to flash a caution indication. A number of arrangements have been designed to monitor signal operation and to effect transfer of the signal light from a sequencing mode to a flashing mode in the event of a malfunction. Clark et al U.S. Pat. No. 3,629,802, assigned to the assignee of the present application, discloses an error detection system having a logic network receiving inputs corresponding to each possible permissive signal indication and operable to produce an error signal if two or more conflicting permissive signal indications are displayed at the same time. The error detection system of this patent does not provide, however, for variations in the traffic signal operating sequence. In Jarko et al U.S. Pat. No. 3,778,762, a traffic signal control monitoring device is disclosed which is operative to produce an error signal in the event conflicting permissive signal indications are displayed and which includes a programming capability permitting the monitoring circuit to be adapted to different signal control sequences. While the Jarko et al system provides a degree of flexibility over the Clark et al system, the modification of the monitor is accomplished by the use of a wiring matrix or the like and, thus, requires manual changes to adapt the unit to different signal sequencing patterns. In other words, while the Jarko et al monitor may be readily adapted for use with a variety of sequencing patterns, it is not capable of automatically accommodating variations in a sequencing pattern.

A primary object of the present invention is the provision of a system for monitoring the operation of a traffic control signal to detect malfunctions of the signal and to transfer the signal operation from a sequencing mode to a flashing mode in the event conflicting traffic control signals are given.

Another object of the present invention is the provision of a traffic signal conflict monitor which may be employed with a variety of different control sequences without the necessity of rewiring or other modification of the conflict monitor.

A further object of the present invention is the provision of a traffic signal conflict monitor which may be controlled to permit normally conflicting signal indications to be displayed when special traffic movement patterns are required.

Yet another object of the present invention is the provision of a traffic signal conflict monitor which employs solid state logic circuitry furnishing a high level of reliability.

BRIEF DESCRIPTION OF THE INVENTION

The above and other objects of the present invention which will become apparent in the following detailed description of the preferred embodiment are achieved by the provision of a conflict monitor having an input circuit associated with each traffic movement phase, receiving an AC signal from each line switch associated with the respective phase and producing a DC signal during the time interval in which any of the respective line switches are energized; a first solid state logic network comprised of a plurality of AND gates each of which receives the output signals of two of the input circuits associated with conflicting phases and producing an output signal whenever the two phases are in conflict; a second solid state logic network having a pair of OR gates receiving, respectively, the output signals of first and second groups of input circuits with the groups being arranged so that any one phase of either group is in conflict with any phase of the other group, and an AND gate responsive to the outputs of the OR gates to produce an output signal in the event a conflict occurs between any phase of one group and any phase of the other group; means under the control of the signal controller for disabling the second logic network in the event a normally conflicting signal indication is to be intentionally displayed; a relay operable to switch the signal operation from a sequencing mode to a flashing mode; a timing circuit responsive to the output of each of the AND gates and operable to actuate the relay; an additional input circuit associated with each overlap function and producing a DC signal whenever the overlap indication is being displayed; and an overlap monitoring circuit for each overlap function including a solid state logic network programmable for determining which overlap signals are permissible with the phase indications, each overlap monitoring circuit including an AND gate producing an output signal in the event the phase and overlap displays are conflicting, the output signal of each of these AND gates also providing an actuating input to the timing circuit. The conflict monitor may also include means for monitoring the signal controller operating voltage and operable to transfer signal operation from a sequencing mode to a flashing mode in the event the operating voltage deviates from its normal level.

For a more complete understanding of the invention and the objects and advantages thereof, reference should be had to the following detailed description and the accompanying drawings wherein there is shown a preferred embodiment of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a diagrammatic plan view of a typical street intersection with traffic movements or phases indicated by arrows;

FIG. 2 is a chart giving the conflicting and compatible phases of traffic movement through the intersection of FIG. 1;

FIG. 3 is a chart illustrating a relationship between the phases of traffic movement through the intersection of FIG. 1;

FIG. 4 is a block diagram of a traffic signal control system incorporating the conflict monitor of the present invention;

FIG. 5a-e is a schematic showing of the conflict monitor of the present invention;

FIG. 6 is a schematic showing of the normal function input circuit of the conflict monitor;

FIG. 7 is a schematic showing of the overlap function input circuit of the conflict monitor; and

FIG. 8 is a block diagram showing the manner in which the sections of FIG. 5 are arranged.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

a typical intersection 10 is shown in FIG. 1. The intersection, formed by the crossing of a north-south street and an east-west street, is provided with a traffic signal 12 operated by a controller 14. The traffic signal 12 has a plurality of lights for providing traffic control signals to motorists. In the illustrated arrangement, the signal 12 provides proceed (green), caution (yellow) and stop (red) indications for each of the four through movements, designated $\phi 1$, $\phi 3$, $\phi 5$ and $\phi 7$, as well as each left turn movement, designated $\phi 2$, $\phi 4$, $\phi 6$, $\phi 8$. Pedestrian signals may also be included. It should be understood that the intersection and traffic movement patterns of FIG. 1 were chosen for purposes of illustration and that the control and conflict monitor of the present invention is not limited to this arrangement.

As will be seen from FIG. 1, certain traffic movements through the intersection 10 are compatible with one another while other movements represent conflicting patterns. Thus, northbound traffic, phase one movement ($\phi 1$), and southbound traffic, phase five movement ($\phi 5$) may proceed simultaneously. Likewise, northbound traffic, phase one movement ($\phi 1$), and north-to westbound turning traffic, phase six movement ($\phi 6$), are compatible. However, northbound and westbound traffic flow, phase one and phase three movements ($\phi 1$ and $\phi 3$), respectively, represent conflicting movements which cannot occur at the same time. The chart of FIG. 2 details the conflicting and compatible traffic movements for the intersection 10. This relationship of the compatible and conflicting phases of traffic movement is also illustrated in the chart of FIG. 3 where any phase on one side of the barrier is in conflict with each of the phases on the opposite side thereof while any phase of either ring is compatible with each of the phases in the other ring and on the same side of the barrier.

Under certain circumstances, it may be desirable to display normally conflicting signals to two or more phases of traffic movement. For example, where an intersection includes a railroad grade crossing, it may be desirable to display green indications to the phase one,

phase three, phase five and phase seven movements following actuation of the crossing signals and prior to the passing of the train through the intersection to permit any vehicles within the intersection to move clear thereof. As will be apparent in the description below, the conflict monitor of the present invention has the capability of permitting such a signal display without sensing such a display as an error or malfunction.

Referring now to FIG. 4, the overall control and monitoring system for operating the traffic signal 12 is illustrated. The controller 14 includes switching means, either mechanical or solid state, which are sequentially operated to provide actuating signals over conductors 18 to load switches 16 which serve to connect the lights of signal 12 to an AC power source by way of conductors 20. The conflict monitor 22 receives an AC input signal from each of the load switches 16 over the conductors 24. As will be described in greater detail below, the conflict monitor 22 includes a logic network which determines whether the energized signal lights represent a compatible or a conflicting combination of phases. A compatible combination of phases results in no output being produced by the conflict monitor 22. A conflicting combination of phases, however, causes the conflict monitor 22 to override the local controller 14 by way of line 28 and to actuate a flasher control circuit 30 over line 32, placing the signal 12 in flashing operation.

The switching means of the controller 14 also provides command signals for overlap functions, signals being furnished over conductors 26 to energize the load switches 16.

The conflict monitor 22 may also include means for monitoring the operating voltage levels of the local controller 14 over the line 36 and will transfer signal operation for the normal sequencing mode to the flashing mode of operation in the event the controller operating voltages depart from specified values.

The conflict monitor 14, illustrated schematically in FIG. 5, is comprised of a normal function sensing and monitoring section (FIG. 5A), an overlap function sensing and monitoring section (FIGS. 5B and 5C) and a relay control and switching section (FIG. 5D). A power supply circuit 40 is connected to an AC power source over the lines L1 and L2 and provides a regulated DC voltage for the logic circuitry of the conflict monitor.

The normal function sensing and monitoring section includes an AC to DC sensor and converter 41-48 for each of the eight traffic movement phases. Each of the sensors has a plurality of input lines which are connected to the line switches associated with the respective phases to receive AC signals when the respective line switches are energized. Each sensor 41-48 produces a DC output signal whenever an AC signal is present at any one of the inputs to the sensor. The sensor 41 associated with $\phi 1$ is illustrated in greater detail in FIG. 6. Input signals present at the terminals a, b and c are connected across resistors R1, R2 and R3, respectively, to diode pairs D10, D11; D12, D13; and D14, D15. The diodes of each pair are of opposite polarity to one another. The signals through the first diode of each pair D10, D12, D14 are supplied across resistor R4 to the negative input of AC-DC converter U6 while the signals across the second diode of each pair D11, D13, D15 are supplied across resistor R5 to the positive input of the converter U6. The circuit is arranged so

that a DC output signal is present at the terminal d whenever a full wave AC signal or a half-wave AC signal of either polarity is present at any of the input terminals a, b and c.

The DC output signals of the AC to DC sensor and converter circuits 41-48 are supplied to conductors 61-68, respectively. These conductors are connected in pair-wise fashion to AND gates U3a, U3b, U3c and U3d. The AND gate U3a receives the outputs of the sensor and converter circuits 41 and 42 across resistors R79 and R77, respectively. The $\phi 5$ and $\phi 6$ signals are connected across the resistors R81 and R83, respectively, to the AND gate U3b; the $\phi 3$ and $\phi 4$ signals, across resistors R63 and R65, respectively to AND gate U3c; and the $\phi 7$ and $\phi 8$ signals across resistors R69 and R67, respectively, to the AND gate U3d. Each of the AND gates U3a-U3d is also connected to the regulated DC output of the power supply 40 over the resistors R41-R44, respectively.

In the illustrated embodiment of the conflict monitor circuit, the logic elements, including the AND gates U3a-U3d, are comprised of current type operational amplifiers. It should be understood, however, that the invention is not limited to the use of logic elements of this type. In the following description of the monitor circuit and its operation, reference is made to logic ZERO and logic ONE signals. These terms are used in their conventional senses in logic circuit terminology and, in the case of circuits employing current type operational amplifiers, denote the absence or presence of current signals.

As will be noted from the charts of FIGS. 2 and 3, the pair of inputs to each of the AND gates U3a-U3d represent a pair of conflicting phases on the same side of the barrier. Each of the AND gates U3a-U3d operates to produce an output, logic ONE, signal in the event input signals are supplied by both of the sensor and converter circuits connected thereto. Thus, for example, if the line switches for both the $\phi 1$ and $\phi 2$ signal indications are energized, the DC currents from the sensor and converter circuits 41 and 42 will be supplied across resistors R79 and R77, respectively, triggering the AND gate U3a to produce a DC output signal from this gate. As a result, a DC current is impressed across resistor R87 on the conductor 60. The AND gates U3b, U3c and U3d are also connected to conductor 60 across the resistors R88, R86 and R85, respectively, so that the occurrence of $\phi 5$ and $\phi 6$ signals together, $\phi 3$ and $\phi 4$ signals together, or $\phi 7$ and $\phi 8$ signals together will result in a logic ONE signal in the conductor 60.

The conductor 60 provides the control input to an OR gate U5a. The OR GATE U5a is also connected to the power supply 40 over the resistor R60. The OR gate U5a produces an output signal whenever a logic ONE signal is present on the conductor 60 and this output signal is supplied across diode D21, resistor R90, operational amplifier U5b, resistors 93 and 94 to timer U5c. If the input signal on conductor 60 to OR gate U5a remains present for the time interval determined by the timer U5c, the timer U5c then switches on the transistor Q6. Typically, the time interval imposed by timer U5c is $300\text{MS} \pm 100\text{MS}$. The switching on of transistor Q6 energizes release coil CR1-RC. When coil CR1-RC is energized contact CR1 opens removing operating current from relay CR2-C. Deenergization of relay CR2-C causes the contacts CR2-1 and CR2-2 of this relay to switch from their normal to re-

verse positions thus switching conductor P9-F from the conductor P9-D to the conductor P9-E and switching conductor P9-J from conductor P9-G to conductor P9-H. These conductors are connected to the controller and flash control circuits and, when switched to their reverse positions, cause control of the traffic signal 12 to switch from the normal or sequencing mode to a flashing mode of operation.

Opening of relay contact CR1-1 also causes the potential across neon lamp PL2 to increase to the level at which this lamp conducts providing a visual indication that a conflict has occurred.

Relay CR1 is returned to its normal state by the closing of push button PB1 which energizes the latching coil CR1-LC.

The output signals of the sensor and converter circuits 41, 42, 45 and 46 are also connected across resistors R80, R78, R82 and R84, respectively, to an input of OR gate U4a. As will be seen from FIG. 3, these four signals represent the four phases on the left side of the barrier. The OR gate U4a is also connected to the power supply 40 across the resistor R48 and this gate is operable to produce a logic ONE output signal upon the occurrence of a logic ONE signal from any one of the four sensor and converter circuits connected thereto. The four sensor and converter circuits corresponding to the $\phi 3$, $\phi 4$, $\phi 7$ and $\phi 8$ sensor and converter circuits are also connected to an OR gate U4b. These signals represent the four phases on the right side of the barrier of FIG. 3. Diodes D18 and D20 connect the outputs of the OR gates U4a and U4b, respectively, to a conductor 69 which is also connected across resistor R45 to power supply 40 and across diodes D17 and resistor R46 to the power supply 40. The conductor 69 is further connected through a diode D19 to one input of AND gate U4c, the other input of which is connected to the power supply 40 across resistor R47. AND gate U4c operates to produce a logic ONE signal in the event logic ONE output signals are supplied from both OR gates U4a and U4b. The output signal of AND gate U4c is supplied across resistor R89 to the conductor 60. Thus, AND gate U4c will produce a logic ONE output signal whenever any one phase on one side of the barrier and any one phase on the opposite side of the barrier are attempted to be displayed at the same time. Since each phase on either side of the barrier is normally in conflict with each phase on the opposite side of the barrier, this portion of the circuit provides for the monitoring of cross-barrier conflicts. The operation of this portion of the circuit may be overridden by the controller 14 when it is desired to display cross-barrier conflicting signals. This is accomplished through the terminal P9-R which provides a connection to the controller 14. When a cross-barrier conflicting signal display is desired, the terminal P9-R is grounded thus grounding the resistor R46 and, through the diode D17, the conductor 69 so that the outputs of the OR gates U4a and U4b are grounded and AND gate U4c is not energized.

An AC to DC sensor and converter circuit is provided for each of the four overlap functions. Each of these circuits 51-54 is of the type shown in FIG. 7 and, as will be seen from a comparison of FIGS. 6 and 7, differs from the AC to DC sensor and converter circuits associated with the normal functions only in that the overlap function AC to DC sensor and converter circuits 51-54 are provided with only two input terminals.

The circuit operates in the same manner as does the circuit of FIG. 6, providing a DC current at the terminal *g* whenever full or half wave AC signals are present at either of the input terminals *e* or *f*. The DC output signals of the circuits 51–54 are supplied to conductors 71–74, respectively.

An overlap input control circuit is provided for each of the four overlap functions. The circuit 81 associated with overlap one (OL1) is shown in detail in FIG. 5B while the circuits 82–84 associated with overlaps two–four (OL2–OL4), respectively, are shown in block diagrams in FIG. 5C, each of these latter three circuits being identical to the circuit 81. The overlap input control circuit 81 includes NAND gates U11a–d, U10a–d, each of which is connected to the regulated DC output of power supply 40 across resistors R97, R98, R100, R99, R101, R102, R104, R103, respectively. The control input terminal of NAND gate U11a is connected to the conductor 61 across resistor R3 and to the power supply 40 across resistors R1 and R2. The junction of resistors R1 and R2 is also connected to a terminal $\phi 1$ -OL1. Similar connections are provided for the second terminal of each of the remaining NAND gates of the circuit 81. The output of each NAND gate is connected through a diode D1–D8, respectively, to a bus 79 which is also connected across resistor R137 to the regulated DC output of power supply circuit 40. The bus 79 is also connected across diode D33 to the input of an additional NAND gate U2a. NAND gate U2a is connected to the regulated DC output of power supply circuit 40 across resistor R161. The output of NAND gate U2a provides one control input, across resistor R165, to AND gate U1a. A second control input to AND gate U1a is derived from the overlap one AC to DC sensor and converter circuit 51 over conductor 71 and resistor R166. The AND gate U1a is connected to the regulated DC power supply across resistor R147. The overlap input control circuits associated with overlaps two, three and four provide control inputs to NAND gates U2b, U2c and U2d, respectively, and the output of each of these NAND gates is directed to an AND gate U1b, U1c, U1d, respectively, with each of these AND gates receiving a second control input from the corresponding AC to DC sensor and converter circuits 52, 53, 54, respectively. The outputs of the AND gates U1a–U1d are connected respectively to conductors 75–78 which, in turn, are connected through resistors R173–R176 to the conductor 60 which provides the control input to the timer circuit OR gate U5a.

A switching transistor Q1 has its base connected to the output of the overlap one AC to DC sensor and converter circuit 51 through resistor R177 and conductor 71. The emitter of transistor Q1 is grounded while the collector is connected to terminal OL1 Control. Transistor Q1 is non-conducting except when a signal is supplied from the sensor and converter circuit 51. Each of the control inputs $\phi 1$ -OL1 – $\phi 8$ -OL1 of the overlap one input control circuit 81 which corresponds to a permissible phase during the overlap one interval is connected to the OL1 Control terminal. For example, if phases one and five are a permissible combination during the overlap one interval, connections will be provided between terminals $\phi 1$ -OL1 and $\phi 5$ -OL1 to the OL1 Control terminal. In order to provide flexibility in programming permissive overlap combinations, the inputs $\phi 1$ -OL1 – $\phi 8$ -OL1 and OL1 Control are connected to a terminal strip and jumper wires are em-

ployed to effect the desired interconnections. Transistors Q2, Q3 and Q4 are similarly controlled by the sensor and converter circuits 52, 53 and 54, respectively, and provide input control signals to the overlap input control circuits 82, 83 and 84, respectively.

During the overlap one interval, the controller 14 energizes the ones of the load switches 16 which correspond to the signal lights of the indications being displayed. The sensor and converter circuit 51 detects the signals from these load switches and produces an output signal on conductor 71. Transistor Q1 is turned on and completes a connection to ground for each of the control inputs of the overlap one input and control circuit 81 which is connected to the OL1 Control terminal. If, as assumed above, phases one and five are permitted during the overlap one interval, the input terminals $\phi 1$ -OL1 and $\phi 5$ -OL1 will be grounded while the remaining terminals $\phi 2$ -OL1 – $\phi 4$ -OL1 and $\phi 6$ -OL1 – $\phi 8$ -OL1 will not be grounded. A logic ONE input is thus provided to NAND gate U11b across resistors R4 and R5 and, in a similar manner the NAND gates U11c, U11d, U10b–U10d will all receive logic ONE inputs across the corresponding resistors. Assuming that the phase one and five displays are the only displays occurring during the overlap one interval, the phase one AC to DC sensor and converter 41 will, during the phase one interval, supply a signal to conductor 61 which is sensed by the NAND gate U11a across resistor R3 as a logic ONE input while the phase five AC to DC sensor and converter 45 will supply a signal to conductor 65 which is sensed by the NAND gate U10a across resistor R15 as a logic ONE input. Since the $\phi 1$ -OL1 and $\phi 5$ -OL1 contacts are grounded, the NAND gates U11a and U10a see only one logic ONE input each and thus produce logic ONE outputs to the bus 79. The remaining NAND gates of the circuit 81 are also receiving only one logic ONE input each and thus also produce logic ONE outputs to the bus 79. The NAND gate U2a thus sees all logic ONE inputs and, accordingly, produces a logic ZERO output which furnishes one control input, to the AND gate U1a. The occurrence of the overlap one display (OL1) during this time period causes the overlap one AC to DC sensor and converter 51 to produce a signal in conductor 71 which supplies a logic ONE input to the AND gate U1a. Since, however, the second input to this AND gate is ZERO, the U1a AND gate produces a ZERO output signal, indicating that overlap one is permissible. If the controller attempts to display a phase which is not permissible during the overlap one interval, at least one of the NAND gates U11a–U11d, U10a–U10d will receive two logic ONE inputs. For example, if the controller 14 advances to the phase two interval, the phase two AC to DC sensor and converter circuit 42 produces an output signal on the conductor 62 which is sensed by the NAND gate U11b across resistor R6 as a logic ONE input. Since the $\phi 2$ -OL1 terminal is not grounded, the NAND gate U11b thus sees two logic ONE inputs and produces a logic ZERO output. The NAND gate U2a thus senses a combination of logic ONE and logic ZERO inputs and, accordingly, produces a logic ONE output. If the overlap one display continues during this second time interval, the logic ONE signal from the overlap one AC to DC sensor and converter 51 is also supplied as an input to the AND gate U1a and this gate produces a logic ONE output which, through conductor 75, resistor R173 and conductor 60 provides a logic ONE input

to the OR gate U5a of the timer circuit controlling the CR1 relay. Accordingly, the occurrence of the overlap one display during the phase two display interval is sensed as a conflict.

The conflict monitor also monitors the operating voltage level of the controller 14, a relay coil CR3-C being connected, through input terminals P9-P and P9-N, to the controller circuitry. As long as the voltage across the terminals P9-P and P9-N remains at the proper level for operation of the controller circuitry, the relay coil CR3-C remains energized holding relay contacts CR3-1 and CR3-2 in their normal positions. The contact CR3-1 is normally open, disconnecting pilot lamp PL1 from the AC power source and this lamp is, accordingly, not lit as long as the controller operating voltage level is maintained. In the event the voltage across the terminals P9-P and P9-N drops below the level required for proper operation of the controller circuitry, relay coil CR3-C releases, causing contacts CR3-1 and CR3-2 to move to their reverse positions. Lamp PL1 is thus connected to the AC power supply and terminal P9-M is disconnected from terminal P9-K and connected to terminal P9-L, causing the traffic signal to operate in a flashing mode.

From the above description of the conflict monitor and the operation thereof, it should be apparent that the present invention provides a system for monitoring the operation of a traffic signal which provides a degree of flexibility of signal display combinations which is not present in the conflict monitor systems of the prior art. This flexibility is achieved by the provision, in the conflict monitor, of the barrier check inhibit circuitry permitting the controller to intentionally effect otherwise conflicting phase displays and of the overlap input control circuits permitting variation of permissible phase combinations during overlap intervals.

While a preferred embodiment of the invention has been illustrated and described in detail, the invention is not limited thereto or thereby. Rather, reference should be had to the appended claims in determining the scope of the invention.

What is claimed is:

1. In a traffic control system for controlling traffic movement over a plurality of traffic flow paths at least certain of which conflict with one another and having a traffic signal providing right-of-way and stop indications to each traffic flow path and a controller actuating said traffic signal; a conflict monitor, comprising:

a plurality of detector circuits, each detector circuit being associated with a different one of said traffic flow paths and producing an output signal during the time interval in which said traffic signal displays a right-of-way indication to said traffic flow path;

a plurality of first logic elements, each first logic element being connected to two of said detector circuits to receive the output signals therefrom, the detector circuits connected to any one of said first logic elements being associated with conflicting traffic flow paths, each first logic element producing an output signal whenever both detector circuits connected thereto produce output signals;

a logic network connected to all of said detector circuits to receive the output signals therefrom, said network producing an output signal whenever an output signal is received from at least one detector circuit of a first group of detector circuits and an output signal is received from at least one detector

circuit of a second group of detector circuits, each detector circuit of the first group being associated with a traffic flow path which conflicts with each traffic flow path with which the detectors of the second group are associated; and

circuit means for interrupting normal operation of said traffic signal, said circuit means being responsive to the output signals of each of said first logic elements and of said logic network.

2. The conflict monitor of claim 1 further including means actuated by said controller for disabling said logic network.

3. The conflict monitor of claim 1 wherein said logic network includes first and second OR gates receiving, respectively, the output signals of the detector circuits of said first and second groups as input signals and an AND gate receiving the output signals of said OR gates as input signals, the output signal of said AND gate being the output signal of said logic network.

4. The conflict monitor of claim 3 wherein said controller includes means for blocking said OR gate output signals from said AND gate.

5. The conflict monitor of claim 1 wherein said circuit means includes relay means for effecting interruption of said traffic signal operation and a relay actuating circuit responsive to the output signals of said first logic elements and of said logic network.

6. The conflict monitor of claim 5 wherein said relay actuating circuit includes timing means for delaying relay actuation until said last mentioned output signals have been present for a predetermined time interval.

7. The conflict monitor of claim 1 wherein said traffic signal provides overlap displays and said conflict monitor further includes

a plurality of additional detector circuits, one additional detector circuit being associated with each overlap display, each of said additional detector circuits furnishing an output signal during the interval in which the corresponding overlap display is actuated;

a plurality of programmable circuits, one programmable circuit being associated with each overlap display, each programmable circuit receiving the output signal of the corresponding additional detector circuit and producing, in response thereto, control signals indicating the permissible combinations of right-of-way indications during the corresponding overlap; and

a second logic network receiving said output signals of each of said first mentioned detector circuits, said output signals of said additional detector circuits and said control signals, said second logic network producing an output signal whenever output signals are received from said first mentioned and said additional detector circuits in the absence of a control signal, said second logic network output signal being supplied to said circuit means as an input signal thereto.

8. In a traffic control system for controlling the movement of traffic along a plurality of paths through an intersection with at least certain of said paths being in conflict with one another and having a signal light and a controller actuating the signal light to provide normal and overlap signal indications; a conflict monitor, comprising:

a plurality of first detector circuits, one circuit being provided for each normal indication and producing

an output signal during the time interval in which said normal indication is displayed;

a first logic circuit receiving the output signals of said first detector circuits and producing an error signal whenever at least two first detector circuit output signals corresponding to conflicting traffic movement paths are present;

an output circuit actuated by said error signal and operable to interrupt normal operation of said signal light;

a plurality of second detector circuits, one circuit being provided for each overlap indication and producing an output signal during the time interval in which said overlap indication is displayed;

a plurality of programmable circuits, one programmable circuit being associated with each overlap signal indication and receiving the output signal of the corresponding one of said second detector circuits to produce, in response thereto, control signals indicating the permissible normal signal indications during the respective overlap; and

a second logic circuit receiving the output signals of said first detector circuits, the output signals of said second detector circuits and said control signals, said second logic circuit producing an error signal whenever at least one first detector output signal and at least one second detector output signal are received in the absence a control signal corresponding to the associated normal and overlap indications, said error signal providing an actuating input to said output circuit.

9. The conflict monitor according to claim 8 wherein said first logic circuit includes a plurality of AND gates, each AND gate receiving the output signals of two of said first detector circuits corresponding to conflicting normal indications, the output signal of any AND gate comprising said error signal.

10. The conflict monitor according to claim 9 wherein said first logic circuit further includes at least two OR gates, each OR gate receiving the output signals from a group of said first detector circuits, said groups being mutually exclusive and each normal indication associated with a detector circuit of one group being in conflict with each normal indication associated with a detector circuit of the remaining groups, each OR gate producing an output signal whenever an output signal from at least one detector circuit of the corresponding group is present, and an additional AND gate receiving the output signals of each of said OR gates, said additional AND gate producing an output signal whenever at least two OR gate output signals are present, said AND gate output signal comprising said error signal.

11. The conflict monitor according to claim 10 wherein each of said gates comprises a current type operational amplifier.

12. The conflict monitor according to claim 8 wherein said second logic circuit comprises a plurality of logic networks, one logic network being provided for each overlap indication, each logic network receiving said output signals of each of said first detector circuits and said control signals for the corresponding overlap function and operable to produce an output signal whenever a first detector circuit output signal is received in the absence of the corresponding control signal, and an AND gate for each overlap indication, each of said AND gates receiving the output signal of the

corresponding second detector circuit and the corresponding logic network, the output signal of each of said AND gates constituting said error signal.

13. The conflict monitor according to claim 12 wherein each logic network comprises a plurality of first NAND gates, one NAND gate being provided for each normal indication and receiving the output signal of the corresponding first detector circuit as an input signal, each logic network including circuit means normally providing a second input signal to each of said first NAND gates, said programmable circuits being such that said control signals remove the second input signals from the corresponding NAND gates, each network further including an additional NAND gate receiving the output signals of each of said first NAND gates as input signals, the output signal of said additional NAND gate being the output signal of said logic network.

14. The conflict monitor according to claim 13 wherein each of said gates comprises a current type operational amplifier.

15. A conflict monitor for a traffic control system of the type having a traffic light for displaying normal phase and overlap signals to control traffic movement through an intersection, certain of said normal phase movements being in conflict with one another, said system including a controller operating said traffic light; the conflict monitor comprising:

a plurality of first input circuits, one input circuit being provided for each normal phase and producing an output signal whenever said normal phase signal is displayed;

a first solid state logic network comprised of a plurality of AND gates each of which receives said output signals of two of said input circuits associated with conflicting phases and producing an output signal whenever said two phases are in conflict;

a second solid state logic network having a pair of OR gates receiving, respectively, said output signals of first and second groups of said input circuits with the groups being arranged so that any one phase of either group is in conflict with any phase of the other group, and an AND gate responsive to the outputs of said OR gates to produce an output signal in the event a conflict occurs between any phase of one group and any phase of the other group;

means under the control of said signal controller for disabling said second logic network in the event a normally conflicting signal indication is to be intentionally displayed;

a relay operable to switch the signal operation from a sequencing mode to a flashing mode;

a timing circuit responsive to the output of each of said AND gates and operable to actuate said relay; an additional input circuit associated with each overlap function and producing an output signal whenever said overlap indication is being displayed;

a programmable circuit associated with each overlap function, each programmable circuit receiving the output signal of the corresponding additional input circuit and producing, in response thereto, control signals indicating compatible normal phases during the corresponding overlap; and

an overlap monitoring circuit for each overlap function including a solid state logic network receiving the output signals of said first input circuits, the

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output signals of said additional input circuit associated with the corresponding overlap function and the control signals of said programmable circuit associated with the corresponding overlap function, each overlap monitoring circuit including an AND 5 gate producing an output signal in the event a non-

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permissible phase display occurs during said overlap, the output signal of each of these AND gates also providing an actuating input to said timing circuit.

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