**Title:** SYSTEM FOR OPERATING A LAMP

The invention relates to a system for operating a lamp comprising encoding means for perturbing part of a predetermined number of half periods of the sinusoidal supply voltage, the number of half periods forming a control period, and a ballast circuit with input terminals (1', 2') coupled to the encoding means for receiving the perturbed voltage. The ballast circuit comprises means (A, B, C, E) for generating a lamp current out of the perturbed voltage, means (G) coupled to the means for generating a lamp current, for controlling an operating characteristic of the lamp in dependency of a control signal, and decoding means (I) for generating the control signal depending on the shape of the control period. The perturbations applied by the encoding means change the amplitude of the sinusoidal supply voltage of only a part of each perturbed half period of the supply voltage, thus preventing light flickering.
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System for operating a lamp.

The invention relates to a system for operating a lamp comprising
- two input terminals for connection to a source of a sinusoidal supply voltage,
- encoding means coupled to said input terminals for perturbing part of a predetermined number of half periods of the sinusoidal supply voltage, said predetermined number of half periods of the sinusoidal supply voltage together forming a control period,
- a ballast circuit equipped with
- ballast input terminals that are coupled to said encoding means during lamp operation for receiving the perturbed sinusoidal supply voltage,
- means I for generating a lamp current out of the perturbed sinusoidal supply voltage,
- means II coupled to means I for controlling an operating characteristic of the lamp in dependency of a control signal,
- decoding means for generating the control signal depending on the shape of the control period.

The invention also relates to encoding means and to a ballast circuit for use in such a system.

Such a system is known from U.S. 5,068,576. In the known system the encoding means completely cuts or reduces the magnitude of an entire half period, so that there is a missing pulse or a pulse of significantly reduced voltage in the rectified DC output of the of a rectifier comprised in the ballast circuit. In the disclosed ballast the operating characteristic of the lamp that is controlled is the light output. The time period between successive missing pulses represents a dimming command. For example, time "n" between missing pulses may represent a 70% dim level while time "m" between missing pulses represents a 90% dim level. A missing pulse means an interruption of the supply voltage and will cause a lamp operated by the ballast to flicker. In the disclosed step-dimming ballast, the flicker is not so objectionable as the user expects a significant and abrupt change in the light
output of the lamp when switching from one light level, e.g. 90% to the next, e.g. 75%. However, where a continuous dimming effect is desired, i.e. where the light should be smoothly adjustable in very small increments, the cutting of entire pulses from the mains supply (and the resulting flicker) would be objectionable to the user.

The invention aims to provide a system for operating a lamp comprising an improved communication between encoding means and the ballast circuit which overcomes the above-mentioned disadvantage.

A system for operating a lamp as described in the opening paragraph is therefore according to the invention characterized in that the perturbations applied by the encoding means change the amplitude of the sinusoidal supply voltage of only a part of each perturbed half period of the sinusoidal supply voltage.

In this way the encoded perturbations in the line voltage in the coded technique according to the invention can be chosen small enough so that lamp flicker is avoided even with encoded signals on the supply voltage.

It has been found that, depending on the configuration of the ballast circuit, the part of the half period that is perturbed can be chosen between 10% and 50% of a half period, preferably between 10% and 25%.

Preferably also the perturbation is a phase cut.

The phase cuts can be chosen less than 45 degrees, preferably about 30 degrees. In this way the encoded perturbations in the line voltage in the coded technique according to the invention can be very small so that lamp flicker is very effectively avoided.

Use of a constant phase cut as perturbation enables a relatively simple implementation for the encoding and decoding circuitry.

Preferably the decoding means comprise means for differentiating the perturbed sinusoidal supply voltage. Decoding by differentiating the waveform allows the perturbation to be small to minimize disturbances in the supply voltage signal.

In a favourable embodiment of a system for operating a lamp according to the invention, the means for controlling the operating characteristic of the lamp increase said operating characteristic by a predetermined amount when a first shape of the control period is detected by the decoding means and decrease the operating characteristic of the lamp by a predetermined amount when a second shape of the control period is detected by the decoding means.
The means for controlling an operating characteristic of the lamp can for instance be dimming means for controlling the light output of the lamp. No perturbations are introduced on the line voltage unless a change in the operating characteristic of the electric lamp is desired. This has the advantage that when lamp operation is to be kept constant, no distortions are imposed on the mains voltage, so that flicker of the lamp is completely avoided. This is significant, since for general lighting purposes the amount of time that a lamp remains at the same light level far exceeds the very limited time frame in which the light level is actually changing. This is in contrast to triac and electronic dimmers where at intermediate light levels, phase cuts are continuously imposed on every cycle of the mains voltage.

Said control period can be formed by two successive perturbed half periods of the supply voltage and the unperturbed half periods therebetween, and the signal can depend on the time duration of the control period. On the other hand said control period may comprise a fixed number of half periods of the sinusoidal supply voltage. In this latter case the signal may depend on the amount of perturbations in a control period. In that case the encoding and decoding means can be of relatively simple construction. Additionally it is possible that the control period represents a binary figure, each unperturbed half period of the control period corresponding to a "0" (zero) and each perturbed half period corresponding to a "1" (one). This way many commands can be accommodated in a control period. Of course an equivalent possibility is that the control period represents a binary figure, each unperturbed half period of the control period corresponding to a "1" (one) and each perturbed half period corresponding to a "0" (zero).

These and other objects, features and advantages of the invention will become apparent from the following drawings, detailed description and appended claims.

In the drawing Fig. 1 is a block diagram of an embodiment of a ballast circuit that is part of a system for operating a lamp according to the present invention;

Fig. 2 shows decoding means comprised in the embodiment shown in Fig. 1;

Fig. 3 shows an embodiment of encoding means suitable for use with a ballast circuit as shown in Fig. 1 in a system for operating a lamp according to the invention;

Fig. 4 shows the shape of signals that are present in the embodiment a system for operating a lamp shown in Fig. 1, 2 and 3, and
Fig. 5 shows a flow chart for controlling the operation of the encoding means shown in Fig. 3.

The fluorescent lamp ballast circuit, shown in Figure 1 includes an EMI and triac damping filter "A" connected to full bridge input rectifier "B", which together convert a sinusoidal AC power line voltage into a rectified, filtered DC voltage at an output thereof. The pre-conditioner circuit "C" includes circuitry for active power factor correction, as well as for increasing and controlling the DC voltage from the rectifier circuit B, which DC voltage is provided across a pair of DC rails RL1, RL2. The ballast circuit includes a DC-AC converter, or inverter, "E" and a controller "G" which controls the inverter. The inverter E is a half-bridge configuration which under control of the half-bridge controller, or driver, circuit G provides a high frequency lamp current to the lamp L coupled to the inverter E. In the embodiment shown in Fig.1 the means I for generating a lamp current are formed by filter "A", rectifier "B", preconditioner circuit "C" and inverter "E". Controller G forms means II for controlling an operating characteristic (the light output) of the lamp in dependency of a control signal.

A dimming interface circuit "I" is connected between an output of the rectifier circuit B and a control input of ballast circuit present at the controller G to control dimming of the lamp. The dimming interface circuitry provides a dimming voltage signal (the control signal) to the controller G and forms the decoding means for generating a signal depending on the shape of the control period.

A detailed description of the operation of all parts of the ballast circuit shown in Fig. 1 except for the decoding means is given in U.S. Application serial no. 08/414,859 and will not be repeated here.

In the coded communication according to the invention between the encoding means and the decoding means of the embodiment of a system for operating a lamp shown in Fig. 1, 2 and 3, a selected number of line cycles or fundamental periods, forms a control period. The occurrence signature of preselected perturbation within the control period is indicative of a control command, for example to change an operating characteristic of the lamp, such as the light level. The "occurrence signature" of the perturbation within the control period may simply be the number of times that the perturbation occurs within the control period. The occurrence signature may also be the location pattern of the perturbation within the control period. For example, the perturbation may be encoded to from a binary
number within the control period.

In an attractive embodiment for dimming, a first fixed number of perturbations represents a command to increase the light level by a pre-selected incremental amount and a second, different number of perturbations represents a command to lower the light level by the pre-selected incremental amount. A third number of cuts in the control period represents the command to keep the light level the same. Favorably, no (zero) cuts per control period represents the command to maintain a constant light level. This has the advantage that when no change is desired, there are no distortions introduced into the power line waveform. Also, since no distortions are introduced there are no adverse effects on THD, power factor or component stress. The perturbation is a phase cut in the nominal waveform of the fundamental periods, since this type of perturbation is easy to implement by controlling the firing of a triac.

Figures 4(a) to 4(c) represent three power line waveforms from a wall controller forming encoding means illustrating this particular dimming implementation. The control period selected is three (3) full line cycles at the encoding means or wall controller, which after rectification is six (6) half-wave cycles at the interface circuit in the ballast. Figure 4(d) is a waveform on the receiver side, i.e. of the dimming interface, and is the differential of the power line waveform of Figure 14(c). If there is no light intensity change requirement, the power line waveform will not be modified as shown in Figure 4(a). Thus, no additional distortion will be added into the line. In this case, there would be no pulse on the differential receiver waveform since the line voltage is a smooth sine signal. A control signal to decrease the light is represented by a phase cut in one positive side waveform during every three line cycles (Figure 4(b)), which would result in one pulse on the receiver waveform after decoding (differentiation) by the receiver. A control signal to increase the light level is represented by two cuts in the control period (Figure 4(c)) such that the receiver waveform will have two pulses during every three line cycles, as illustrated in Fig. 4(d).

In the ballast, the light will remain unchanged if no pulse is detected by the receiver in the rectified power line waveform. If one pulse or two pulses are detected during every three line cycles (six half-wave cycles after rectification), the light will change one step, i.e. by the pre-selected increment, to the corresponding direction.

Experience shows that continuous dimming can be mimicked if the number of steps between the lowest and highest light levels is large enough; in other words, if the increment by which the light is changed each time is very small. In the following embodiment, the number of steps is selected to be 100. If an increase or decrease control
signal is generated continuously by the wall controller, it will take about 5 seconds to change the light intensity from the lowest level to the highest level.

The main function of the wall controller or encoding means for the coded dimming technique is to generate the control patterns illustrated in Figures 4(a)-4(c). The circuit diagram of a suitable transmitter, in the form of a wall controller, is shown in Figure 3.

Two input terminals W1 and W3 are for connection to the white (neutral) and black (hot) lines of the power line, respectively. Output terminal W2 connects to the red output line which carries the encoded, hot AC signal to the ballast. A triac WU1 is connected between the terminals W1 and W2. A step-down transformer WT1 has each end of its primary winding WP1 connected to a respective one of the terminals W1 and W3. The ends of the secondary winding WS1 are connected to respective nodes W4, W5 of a full-bridge rectifier formed by the diodes WD1-WD4. The cathodes of the diodes WD1 and WD2 are connected to node W4 and the anodes of the diodes WD3 and WD4 are connected to node W5. The cathode of the diode WD3 and the anode of the diode WD1 are connected at node W6 and the cathode of the diode WD4 and the anode of the diode WD2 are connected at node W7.

The triggering of the triac WU1 is controlled by an 8-bit microcontroller IC1 with a built-in oscillator. A suitable controller for IC1 is the Motorola MC68HC05k1.

The microcontroller IC1 has two ports A, B. Port A has eight terminals and Port B has two terminals. There are four push button switches WS1 - WS4 to control the following functions: on, off, light increase and light decrease. The microcontroller IC-1 reads the status of these switches through its terminals PA4-PA7 of port A.

The node W7 of the rectifier is connected to terminal IC1's power supply VDD via line WRL2 which includes a 5V voltage regulator WU2. An electrolytic capacitor WC1 is connected between the lines WRL3 and WRL2 at the input (A) side of regulator WU2 to filter the DC ripple from the rectifier. A capacitor WC2 is connected between these same lines at the output side (B) of regulator W2 to filter noise. The zener diode WD5 bridges lines WRL3 and WRL5, with its cathode connected to the latter line. Terminals RST (reset) and IRQ (interrupt request) are also connected to the +5V output of regulator WU2. The ceramic resonator XT is connected across oscillator terminals OSC1 and OSC2, with the components WC3, WC4, and WR2 being specified by the resonator manufacturer to ensure proper operation of the resonator XT.

The microcontroller IC1 needs a line voltage zero-crossing signal as a
reference to trigger the triac WU1. This signal is provided by the resistor WR1 and the zener diode WD5, and is input at terminals PB0 and PB1. Since the voltage at the cathode of the diode WD5 is only 4.7V, which is much less than the power line peak voltage, it provides the logic signal "1" and "0" on terminals PB0 and PB1 when the line voltage is crossing zero. Controller IC1 sends the triac trigger signal out through terminals PA0 through PA3 via line WRL4 to the triac WU1. The resistor WR3 limits the current to the triac WU1 from the triac trigger signal. These terminals are parallel connected to increase drive reliability. If the microcontroller IC1 sends out a trigger signal immediately upon detection of the line voltage zero-crossing, there is no modification for the power line waveform. This provides the waveform of Fig. 4(a) for a constant light level. To provide the phase cut in either one or two half-cycles to generate the signals to increase or decrease the light level (as shown in Figures 4(b) and 4(c)) the trigger signal is delayed about 1.39ms after the zero-crossing for the respective half-cycle. This provides a small phase cut of about 30 degrees.

Figure 5 is a program flow chart for the wall controller. After initializing port directions, the program goes into a loop that reads the status of the four switches WS1 - WS4. If a switch is activated, the program will perform the corresponding function. For example, when switch WS4 (down key) is pressed, the wall controller will produce the waveform of Fig. 4(b) to dim the light and when the switch WS3 (up key) is pressed the waveform of Fig. 4(c) will be produced to increase the light level. When switch WS1 (on key) is pushed, power will be supplied to the connected lamp controller without any perturbations imposed on the AC power line signal. When switch WS2 is pressed, the AC power line signal is completely interrupted so that no power is supplied to the connected ballast.

Figure 2 is a schematic of the decoding means or receiver, or interface circuit, in the ballast circuit. The heart of the interface circuit is the microcontroller IC2 (for example, a Z86C04 from Zilog, Inc.) which converts the dimming control signals to a corresponding PWM (Pulse Width Modulation) output. The microcontroller IC2 has an inputs P31 which accepts the coded dimming signals. The PWM output (dim) signal is formed on terminal P27 and is converted to a DC signal present at terminal Z7 for input to the half-bridge driver at the 'dim' input of controller "G" to adjust the power to the lamp. Node A (also ref. Z8) of the rectifier circuit B is connected to ground (ref. Z9) via a voltage divider network consisting of the resistors GR1, GR2 and GR3. The input P31 is connected to a node B through a differential circuit formed by GC2 and GR5. A zener diode GD6 parallel connects with GR5 to protect the input of the microcontroller IC2. The microcon-
controller is powered at terminal VCC with a 5V voltage source, in this case from voltage
regulator U3. An external ceramic resonator XL1 (2MHZ) is connected between the clock
terminals X1, X2. The clock terminals are connected to ground via the capacitors GC3 and
GC4, respectively, which ensure proper resonator operation. The capacitor GC5 is connected
between ground and the voltage supply to suppress noise. The resistors GR6, GR7 and
capacitors GC6 and GC7 smooth the PWM output signal from terminal P27 to an average
DC signal for input to the dim input of the controller G.

When power turns on, i.e. the mains voltage from the wall controller is
provided at ballast input terminals 1',2', the microcontroller IC2 is initialized and the output
P27 is set at a default PWM value for a default light level, for example 85% light output.
The microcontroller input threshold level is about 2.5V. This means that it is logic "1" if
the input is above 2.5V and logic "0" if the input is below 2.5V. A logic "1" will be
received on terminal P31 only when the voltage on P31 exceeds 2.5V. The differentiating
circuit provides a pulse to terminal P31 of greater than 2.5V (logic "1") whenever the
sinusoidal half-cycle includes a phase cut as with the coded dimmer (Fig. 4(d)). The rectified
DC output fed to the interface circuit is 120 HZ pulsed DC. If a standard ON/OFF wall
switch is installed instead of any dimming control device, the PWM output signal is set to
the default level, since the power line is unmodified and the microcontroller U2 will not
detect any pulses at its inputs.

The microprocessor IC2 includes an 8-bit register named PWM which
controls the substantially square wave shaped PWM output signal present at the PWM
register output at P27. A timer 0 in the microcontroller determines the duration of t_h (the
time interval during which the PWM output signal is high) and t_l (the time interval during
which the output signal is low) based on the PWM value in the register. After the timer 0
times out, an interrupt 4 will be generated. In the interrupt subroutine, the first test is the
current PWM register output status. If the current PWM register output is logic "0", then it
sets the PWM register output to 1 and installs the PWM value into timer 0. If the current
PWM register output is logic "1", it sets the PWM register output to logic "0" and installs
(255-pwm) into timer 0. The time to invoke the next interruption is proportional to the value
installed into the timer 0. The time of t_h plus t_l is set to be independent of the PWM value so
that the PWM signal frequency is a constant. Thus, with a larger PWM value, the PWM
register has more time to stay in logic "1" condition and provides a higher average output
dimming control voltage at pin 27. The dimming control voltage range is set from 0.4V to
3V which means the PWM duty cycle should be 8% to 60%, since logic "0" is zero volts
and logic "1" is 5 volts.

A pulse on the terminal P31 invokes a subroutine "interrupt 1". The
"interrupt 1" procedure increases the value of a register named "pulse number" by 1. The
coded dimming control (CDL) loop installed in the microcontroller IC2 checks the value in
the register "pulse number" every 50ms. Since 50ms equals 3 line cycles, the value of the
register "pulse number" will determine if the light level should change. When the value in
the register "pulse number" equals zero (0) there is no pulse, so no change in the light level
or in the PWM value occurs. When the register "pulse number" equals one (1), the PWM
value is decreased until it reaches the preset minimum value. When the register "pulse
number" equals two (2) the PWM increases until it reaches a preset maximum value. Thus,
the interface circuitry enables the ballast to automatically accept dimming inputs from the
wall controller and produces a DC signal, input to the controller G to control the light level
of the fluorescent lamps.

Under non-dimming conditions, the disclosed ballast maintains a power
factor >0.99, THD <10%, and a crest factor <1.6, so the circuit satisfies both the need
for a dimmable ballast while also providing a high power factor and keeping THD, EMI and
component stress very low even at the lowest dimming levels.
CLAIMS:

1. A system for operating a lamp comprising
   - two input terminals for connection to a source of a sinusoidal supply voltage,
   - encoding means coupled to said input terminals for perturbing part of a predetermined number of half periods of the sinusoidal supply voltage, said predetermined number of half periods of the sinusoidal supply voltage together forming a control period,
   - a ballast circuit equipped with
   - ballast input terminals that are coupled to said encoding means during lamp operation for receiving the perturbed sinusoidal supply voltage,
   - means I for generating a lamp current out of the perturbed sinusoidal supply voltage,
   - means II coupled to means I for controlling an operating characteristic of the lamp in dependency of a control signal,
   - decoding means for generating the control signal depending on the shape of the control period,
characterized in that the perturbations applied by the encoding means change the amplitude of the sinusoidal supply voltage of only a part of each perturbed half period of the sinusoidal supply voltage.

2. A system as claimed in claim 1, wherein the part of each half period is between 10% and 50% of a half period, preferably between 10% and 25%.

3. A system as claimed in claim 1 or 2, wherein the perturbation is a phase cut.

4. A system as claimed in claim 1, 2 or 3, wherein the decoding means comprise means for differentiating the perturbed sinusoidal supply voltage.

5. A system as claimed in one or more of the previous claims, wherein the means for controlling the operating characteristic increase the operating characteristic of the lamp by a predetermined amount when a first shape of the control period is detected by the decoding means and decrease the operating characteristic of the lamp by a predetermined amount when a second shape of the light output is detected by the decoding means.
6. A system as claimed in one or more of the previous claims, wherein said control period is formed by two successive perturbed half periods of the supply voltage and the unperturbed half periods therebetween, and the dimming signal depends on the time duration of the control period.

7. A system as claimed in claim 1, 2, 3, 4 or 5, wherein said control period comprises a fixed number of half periods of the sinusoidal supply voltage.

8. A system as claimed in one or more of the previous claims, wherein the control period represents a binary figure, each unperturbed half period of the control period corresponding to a "0" (zero) and each perturbed half period corresponding to a "1" (one).

9. A system as claimed in one or more of the previous claims, wherein the control period represents a binary figure, each unperturbed half period of the control period corresponding to a "1" (one) and each perturbed half period corresponding to a "0" (zero).

10. A system as claimed in claim 7, wherein the signal depends on the number of perturbed half periods of the sinusoidal supply voltage in a control period.

11. A system as claimed in one or more of the previous claims wherein the operating characteristic of the lamp is its light output.

12. Encoding means suitable for use in a system according to one or more of the previous claims.

13. Ballast circuit suitable for use in a system according to one or more of the previous claims.
FIG. 5

Initialize ports

read switch conditions

off key?

N

down key?

N

up key?

N

on key?

N

condition = on?

Y

all trig signal are not modified

Y

set condition = off

N

generate one modified trig signal in 3 line cycles

N

generate two modified trig signal in 3 line cycles

N

set condition = on
### INTERNATIONAL SEARCH REPORT

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC6: H05B 41/36, H05B 37/02

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04B, H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE, DK, FI, NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
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<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<td>X</td>
<td>US 5227762 A (D. GUIDETTE ET AL), 13 July 1993 (13.07.93), column 2, line 63 - column 11, line 23, figures 1-11</td>
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<td>A</td>
<td>US 4329678 A (J. M. HATFIELD), 11 May 1982 (11.05.82), column 3, line 18 - column 11, line 45, figures 1-7</td>
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<td>A</td>
<td>US 4024528 A (L. M. BOGGS ET AL), 17 May 1977 (17.05.77), figure 2, abstract</td>
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Further documents are listed in the continuation of Box C.

See patent family annex.

**Date of the actual completion of the international search**

18 December 1996

**Date of mailing of the international search report**

18-12-1996

Name and mailing address of the ISA:

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