### FIG. 3
**Input Message Segment**

<table>
<thead>
<tr>
<th>Digit Position</th>
<th>Information</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SCAN POSITION</td>
<td>0-15</td>
</tr>
<tr>
<td>2</td>
<td>AMOUNT ROW 14</td>
<td>0-9</td>
</tr>
<tr>
<td>3</td>
<td>AMOUNT ROW 13</td>
<td>0-9</td>
</tr>
<tr>
<td>4</td>
<td>AMOUNT ROW 12</td>
<td>0-9</td>
</tr>
<tr>
<td>5</td>
<td>AMOUNT ROW 11</td>
<td>0-9</td>
</tr>
<tr>
<td>6</td>
<td>AMOUNT ROW 10</td>
<td>0-9</td>
</tr>
<tr>
<td>7</td>
<td>AMOUNT ROW 9</td>
<td>0-9</td>
</tr>
<tr>
<td>8</td>
<td>AMOUNT ROW 8</td>
<td>0-9</td>
</tr>
<tr>
<td>9</td>
<td>AMOUNT ROW 7</td>
<td>0-9</td>
</tr>
<tr>
<td>10</td>
<td>AMOUNT ROW 6</td>
<td>0-9</td>
</tr>
<tr>
<td>11</td>
<td>AMOUNT ROW 5</td>
<td>0-9</td>
</tr>
<tr>
<td>12</td>
<td>WINDOW MACHINE TENS</td>
<td>0-9</td>
</tr>
<tr>
<td>13</td>
<td>WINDOW MACHINE UNITS</td>
<td>0-9</td>
</tr>
<tr>
<td>14</td>
<td>CONTROL ROW 4</td>
<td>0-9</td>
</tr>
<tr>
<td>15</td>
<td>CONTROL ROW 3</td>
<td>0-9</td>
</tr>
<tr>
<td>16</td>
<td>CONTROL ROW 2</td>
<td>0-9</td>
</tr>
<tr>
<td>17</td>
<td>CONTROL ROW 1</td>
<td>0-9</td>
</tr>
<tr>
<td>18</td>
<td>LONGITUDINAL BIT CHECK DIGIT</td>
<td></td>
</tr>
</tbody>
</table>

### FIG. 4
**Output Message Segment**

<table>
<thead>
<tr>
<th>Digit Position</th>
<th>Information</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SCAN POSITION</td>
<td>0-15</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>AMOUNT ROW 13</td>
<td>0-9</td>
</tr>
<tr>
<td>4</td>
<td>AMOUNT ROW 12</td>
<td>0-9</td>
</tr>
<tr>
<td>5</td>
<td>AMOUNT ROW 11</td>
<td>0-9</td>
</tr>
<tr>
<td>6</td>
<td>AMOUNT ROW 10</td>
<td>0-9</td>
</tr>
<tr>
<td>7</td>
<td>AMOUNT ROW 9</td>
<td>0-9</td>
</tr>
<tr>
<td>8</td>
<td>AMOUNT ROW 8</td>
<td>0-9</td>
</tr>
<tr>
<td>9</td>
<td>AMOUNT ROW 7</td>
<td>0-9</td>
</tr>
<tr>
<td>10</td>
<td>AMOUNT ROW 6</td>
<td>0-9</td>
</tr>
<tr>
<td>11</td>
<td>AMOUNT ROW 5</td>
<td>0-9</td>
</tr>
<tr>
<td>12</td>
<td>LIGHTS</td>
<td>0-12</td>
</tr>
<tr>
<td>13</td>
<td>AUX. CONTROL DIGIT</td>
<td>0-7</td>
</tr>
<tr>
<td>14</td>
<td>CONTROL ROW 4</td>
<td>0-9</td>
</tr>
<tr>
<td>15</td>
<td>CONTROL ROW 3</td>
<td>0-9</td>
</tr>
<tr>
<td>16</td>
<td>CONTROL ROW 2</td>
<td>0-9</td>
</tr>
<tr>
<td>17</td>
<td>CONTROL ROW 1</td>
<td>0-9</td>
</tr>
<tr>
<td>18</td>
<td>LONGITUDINAL BIT CHECK DIGIT</td>
<td></td>
</tr>
</tbody>
</table>

### FIG. 5

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Representation</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Flag</td>
<td>C</td>
<td>F</td>
<td>R</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

### FIG. 6

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000000</td>
<td>NO DATA</td>
</tr>
<tr>
<td>101000</td>
<td>REQUEST TO TRANSFER</td>
</tr>
<tr>
<td>1010100</td>
<td>READY</td>
</tr>
<tr>
<td>1010010</td>
<td>OK</td>
</tr>
<tr>
<td>1010001</td>
<td>REWRITE</td>
</tr>
</tbody>
</table>
REMOTE CONTROLLER INPUT SECTION

Outputs to CLA

ICA1 - Data Bit (2^0)
ICA2 - Data Bit (2^1)
ICA3 - Data Bit (2^2)
ICA4 - Data Bit (2^3)
ICA5 - Parity Bit
ICA6 - Request to Input
ICA7 - Data On Line

Inputs from CLA

JCA1 - Start Input
JCA2 - Input OK
JCA3 - Input Error
JCA4 - System On
JCA5 - Request for Character
JCA6 - Interlock

Outputs to Window Machine

JWM1 - Selection of Window Machine #1
JWM2 - Selection of Window Machine #2
JWM3 - Selection of Window Machine #3
JWM4 - Selection of Window Machine #4
JWM5 - Selection of Window Machine #5
JWM6 - Selection of Window Machine #6
JWM7 - Selection of Window Machine #7
JWM8 - Selection of Window Machine #8

FIG. 23
JWM9 - Selection of Window Machine #9
JWM10 - Selection of Window Machine #10
JWM11 - Selection of Window Machine #11
JWM12 - Selection of Window Machine #12
JWM13 - Selection of Window Machine #13
JWM14 - Selection of Window Machine #14
JWM15 - Selection of Window Machine #15
JWM16 - Selection of Window Machine #0
JWM41 - Window Machine #1 Ready to Interrogate
JWM42 - Window Machine #2 Ready to Interrogate
JWM43 - Window Machine #3 Ready to Interrogate
JWM44 - Window Machine #4 Ready to Interrogate
JWM45 - Window Machine #5 Ready to Interrogate
JWM46 - Window Machine #6 Ready to Interrogate
JWM47 - Window Machine #7 Ready to Interrogate
JWM48 - Window Machine #8 Ready to Interrogate
JWM49 - Window Machine #9 Ready to Interrogate
JWM50 - Window Machine #10 Ready to Interrogate
JWM51 - Window Machine #11 Ready to Interrogate
JWM52 - Window Machine #12 Ready to Interrogate
JWM53 - Window Machine #13 Ready to Interrogate
JWM54 - Window Machine #14 Ready to Interrogate
JWM55 - Window Machine #15 Ready to Interrogate
JWM56 - Window Machine #0 Ready to Interrogate

FIG. 24
JWM21 - Row 15 Control Row #1
JWM22 - Row 16 Control Row #2
JWM23 - Row 17 Control Row #3
JWM24 - Row 14 Control Row #4
JWM25 - Row 11 Amount Row #1
JWM26 - Row 10 Amount Row #2
JWM27 - Row 9 Amount Row #3
JWM28 - Row 8 Amount Row #4
JWM29 - Row 7 Amount Row #5
JWM30 - Row 6 Amount Row #6
JWM31 - Row 5 Amount Row #7
JWM32 - Row 4 Amount Row #8
JWM33 - Row 3 Amount Row #9
JWM34 - Row 2 Amount Row #10 (Totals)
JWM35 - Row 13 Units Machine #
JWM36 - Row 12 Tens Machine #
JWM37 - End of Segment
JWM38 - Input Error

Input from Window Machine
IWM1 - Answer Digit 1
IWM2 - Answer Digit 2
IWM3 - Answer Digit 3
IWM4 - Answer Digit 4
IWM5 - Answer Digit 5

FIG. 25
Sept. 12, 1967  E. J. GRILLMEIER, JR., ETAL  3,341,820
ON-LINE BRANCH FOR DATA PROCESSING SYSTEMS
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IWM6 - Answer Digit 6
IWM7 - Answer Digit 7
IWM8 - Answer Digit 8
IWM9 - Answer Digit 9
IWM10 - Answer Digit 0
IWM20 - Answer Ready

Error Register
AE11 - Request to Input and No Answer in 350 msec.
AE12 - No Echo from Central in 350 msec. after sending data or Error from Central or Window Machine Error.

Switches
SF - Run Switch
SR - Reset Switch
ST - Test Switch

Relay
DRW - Reset During Power Sequence

Longitudinal Bit Register
AL11 - Sum Check Bit (2^0)
AL12 - Sum Check Bit (2^1)
AL13 - Sum Check Bit (2^2)
AL14 - Sum Check Bit (2^3)

Clocks
CPI - Program Counter Clock

FIG. 26
CTI - Main Timing Clock
CCI - Row Counter Clock
CSI - Scan Counter Clock
CXI - Test Counter Clock
CE - Error Counter Clock

Decimal to Binary Decode
DDI1 - \(2^0\) Bit
DDI2 - \(2^1\) Bit
DDI3 - \(2^2\) Bit
DDI4 - \(2^3\) Bit
DDI1A - Even Bit
DEI1 - Error Combinations

Miscellaneous Drive
DMI1 - Reset During Warm-Up or Reset in Test Mode Operation
DMI2 - Reset Term
DMI3 - End of Segment in Test Mode with Error
DMI4 - Input Error
DMI5 - Request for Character
DMI6 - Error Register Full

Reset Drivers
DRI2 - Reset Program Counter
DRI3 - Reset Error Counter "A"
DRI4 - Reset Row Counter
DRI5 - Reset Error Counter "B"

FIG. 27
Row Counter

FCI1 - Flip-Flop ($2^0$) Bit
FCI2 - Flip-Flop ($2^1$) Bit
FCI3 - Flip-Flop ($2^2$) Bit
FCI4 - Flip-Flop ($2^3$) Bit
FCI5 - Flip-Flop ($2^6$) Bit

Error Counter "A"

FEA1 - Flip-Flop ($2^0$) Bit
FEA2 - Flip-Flop ($2^1$) Bit
FEA3 - Flip-Flop ($2^2$)
FEA4 - Flip-Flop ($2^3$)

Error Counter "B"

FEB1 - Flip-Flop ($2^0$) Bit
FEB2 - Flip-Flop ($2^1$) Bit

Program Counter

FPI1 - Flip-Flop ($2^0$) Bit
FPI2 - Flip-Flop ($2^1$) Bit
FPI3 - Flip-Flop ($2^2$) Bit

FPI(0) - Reset Block
FPI(1) - Scan for Window Machine Ready
FPI(2) - Request to Input Data
FPI(3) - Delay Block
FPI(4) - Read Keyboard
FPI(5) - Answer Block

FIG. 28
FPI(6) - Delay Block
FPI(7) - End of Segment Block

Scan Counter
FSI1 - Flip-Flop (2^0) Bit  FSI(0) to FSI(15) inclusive
FSI2 - Flip-Flop (2^1) Bit  represent Scan Counter
FSI3 - Flip-Flop (2^2) Bit  Outputs for Counts 0 to 15 inclusive.
FSI4 - Flip-Flop (2^3) Bit

Test Counter
FTI1 - Flip-Flop (2^0) Bit  FTI(0) to FTI(6) inclusive
FTI2 - Flip-Flop (2^1) Bit  represent Test Counter
FTI3 - Flip-Flop (2^2) Bit  Outputs for Counts 0 to 6 inclusive.

Sync Memory
GCI1 - Gates Program Counter
GCI2 - Gates Program and Row Counter in Error Conditions
GCI3 - Gates Scan Counter

Window Machine Release
JWM37 - End of Segment
JWM38 - Input Error

Time Delays
TDI1 - Window Machine Select (15 msec.)
TDI2 - Echo Delay (350 msec. retrig.)

Lamps
BEI - Input Error Retry

FIG. 29
INPUT EQUATIONS

Error Register
\[ aEi1 = FPI(2) \cdot TD12' \cdot (SE' + ST') \]
\[ oaei1 = FPI(1) \cdot CPI + SR \cdot ST + DRW \]
\[ aEi2 = (SE' + ST') \cdot TD12' \cdot [FPI(5) + FPI(7)] + CT \cdot JCA3 \cdot [FPI(4) + FPI(5)] + IA7 \cdot FPI(4) \cdot FCI(0)' \cdot FCI(1)' \cdot FCI(18)' \cdot (DEII + IWM20') \]
\[ oaei2 = FPI(1) \cdot CPI + DRW + SR \cdot ST \]

Longitudinal Bit Register
\[ aLi1 = CCI \cdot ICA1 \cdot FCI(0)' \]
\[ oali1 = CCI \cdot [ICA1 + FCI(0)] \]
\[ aLi2 = CCI \cdot ICA2 \cdot FCI(0)' \]
\[ oali2 = CCI \cdot [ICA2 + FCI(0)] \]
\[ aLi3 = CCI \cdot ICA3 \cdot FCI(0)' \]
\[ oali3 = CCI \cdot [ICA3 + FCI(0)] \]
\[ aLi4 = CCI \cdot ICA4 \cdot FCI(0)' \]
\[ oali4 = CCI \cdot [ICA4 + FCI(0)] \]

Clocks
\[ CPI = CTI \cdot (GCI1 + GCI2) \]
\[ CTI = TTS \cdot [FPI(3)' \cdot FPI(4)' \cdot FPI(5)' + GCI2'] + GCI2' \cdot [FPI(3) \cdot JCA5] + FPI(4) \cdot FCI(0)' \cdot ICA7 + FPI(5) \cdot JCA2 + FPI(4) \cdot FCI(0) \cdot TTS \]
\[ CCI = FPI(3) \cdot CPI + CTI \cdot [FPI(4) \cdot FPO(2)' \cdot FCI(0)' + GCI2 \cdot FCI(0)'] \]
\[ CSI = TTN \cdot FPI(1) \cdot IWM20' \]
\[ CXI = FPI(4) \cdot JCA5 \cdot [DDI1 + DDI2 + DDI3 + DDI4 + FTO(0)] + CTI \cdot FPI(4)' \]
\[ CE = FPI(0) \cdot CPI \]

FIG. 30
Sept. 12, 1967  E. J. GRILLMEIER, JR., ET AL  3,341,820
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Filed Oct. 13, 1964

Decimal to Binary Decode

\[ \text{DDI}_1 = \text{IWM}_1 + \text{IWM}_3 + \text{IWM}_5 + \text{IWM}_7 + \text{IWM}_9 \]
\[ \text{DDI}_2 = \text{IWM}_2 + \text{IWM}_3 + \text{IWM}_6 + \text{IWM}_7 \]
\[ \text{DDI}_3 = \text{IWM}_4 + \text{IWM}_5 + \text{IWM}_6 + \text{IWM}_7 \]
\[ \text{DDI}_4 = \text{IWM}_6 + \text{IWM}_9 \]
\[ \text{DDI}_1a = \text{IWM}_2 + \text{IWM}_4 + \text{IWM}_6 + \text{IWM}_8 + \text{IWM}_10 \]
\[ \text{DEI}_1 = (\text{DDI}_1a \oplus \text{DDI}_1)' \]

Miscellaneous Drives

\[ \text{DMI}_1 = \text{DRW} + \text{SR} + \text{ST} \]
\[ \text{DMI}_2 = \text{DMI}_1 + \text{FPI}(1) + \text{CPI} \]
\[ \text{DMI}_3 = \text{FPI}(7) \cdot \text{ST}' (\text{AEI}_1 + \text{AEI}_2) \]
\[ \text{DMI}_4 = \text{AEI}_1 + \text{AEI}_2 \]
\[ \text{DMI}_5 = \text{FPI}(4) + \text{JCA}(5) \]
\[ \text{DMI}_6 = \text{FEA}(9) + \text{FEB}(3) \]

Reset Drives

\[ \text{DRI}_2 = \text{DRW} + \text{SR} + \text{ST} + \text{GCI}_2 + \text{FEA}(9)' + \text{FEB}(3)' (\text{AEI}_1 + \text{AEI}_2) + \text{FPI}(0) + \text{GCI}_2 \]
\[ \text{DRI}_3 = \text{DRW} + \text{SR} + \text{ST} + \text{AEI}_1 + \text{FEA}(9) + \text{FEB}(3) + \text{AEI}_2 + \text{AEI}_1' \cdot \text{AEI}_2' \]
\[ \text{DRI}_4 = \text{DRW} + \text{SR} + \text{ST} + \text{GCI}_2 + \text{FCI}(18) \]
\[ \text{DRI}_5 = \text{DRW} + \text{SR} + \text{ST} + \text{AEI}_2 + \text{FEA}(9) + \text{FEB}(3) + \text{AEI}_1' \cdot \text{AEI}_2' \]
\[ \text{DRI}_6 = \text{DRW} + \text{SR} + \text{ST} + \text{FPI}(4)' + \text{FTI}(6) \]

Row Counter

\[ \text{FCI}_1 = \text{CCI} \cdot \text{DRI}_4' \]
\[ \text{ofFCI}_1 = \text{CCI} \]

FIG. 31
fCI2 = CCI DRI4' FCI1
ofCI2 = CCI (FCI1 + DRI4)
fCI3 = CCI DRI4' FCI1 FCI2
ofCI3 = CCI (FCI1 FCI2 + DRI4)
fCI4 = CCI DRI4' FCI2 FCI3
ofCI4 = CCI (FCI1 FCI2 FCI3 + DRI4)
fCI5 = CCI DRI4' FCI1 FCI2 FCI3 FCI4
ofCI5 = CCI (FCI1 FCI2 FCI3 FCI4 + DRI4)

Error Counter "A"

fEA1 = CE DRI3'
ofEA1 = CE
fEA2 = CE FEA1 DRI3'
ofEA2 = CE (FEA1 + DRI3)
fEA3 = CE (FEA1 FEA2 DRI3')
ofEA3 = CE (FEA1 FEA2 + DRI3)
fEA4 = CE (FEA1 FEA2 FEA3 DRI3')
ofEA4 = CE (FEA1 FEA2 FEA3 + DRI3)

Error Counter "B"

fEB1 = CE AEI2 DRI5'
ofEB1 = CE (AEI2 + DRI5)
fEB2 = CE FEB1 AEI2 DRI5'
ofEB2 = CE (FEB1 AEI2 + DRI5)

Program Counter

fPI1 = CPI DRI2'

FIG. 32
ofPI1 = CPI
fPI2 = CPI FPI1 DRI2'
ofPI2 = CPI (FPI1 + DRI2)
fPI3 = CPI FPI1 FPI2 DRI2'
ofPI3 = CPI (FPI1 FPI2 + DRI2)

Scan Counter

fSI1 = CSI
ofSI1 = CSI
fSI2 = CSI FSI1
ofSI2 = CSI FSI1
fSI3 = CSI FSI1 FSI2
ofSI3 = CSI FSI1 FSI2
fSI4 = CSI FSI1 FSI2 FSI3
ofSI4 = CSI FSI1 FSI2 FSI3

Test Counter

fTI1 = CXI DRI6'
ofTI1 = CXI
fTI2 = CXI DRI6' FTI1
ofTI2 = CXI (FTI1 + DRI6)
fTI3 = CXI DRI6' FTI1 FTI2
ofTI3 = CXI (FTI1 FTI2 + DRI6)

CLA Input
ICA1 = DDI1 + FCI(1) FSI1 + ALI1 FCI(18) + DEO1

FIG. 33
ICA2 = DDI2 + FCI(1) FSI2 + ALI2 FCI(18) + DEO2
ICA3 = DDI3 + FCI(1) FSI3 + ALI3 FCI(18) + DEO3
ICA4 = DDI4 + FCI(1) FSI4 + ALI4 FCI(18)
ICA5 = [(ICA1 + IIA2) ⊕ (ICA3 + ICA4)]'
ICA6 = GCI3 AEI1' AEI2'
ICA7 = JCA5 [ST' + FTI(0) JCA6'] [FPI(4) FCI(0) + FPO(2) (AEO1 + AE02 + AE03 + AE04)]

Sync Memory

gCI1 = CTI [FPI(1) TDI1' GCI3 + FPI(2) AEI1' (JCA1 + JCA6' ST) + FPI(3) + FPI(4) FCI(0) AEI2' + FPI(6) GCI2' + FPI(7) IWM20' TDI1' + (ST' + SF') [FPI(0) FCI(0) JCA4 JCA1' GCI2']]
goCI1 = CTI FPI(4)'
gCI2 = TTS [JCA5' FPI(6)' FPI(0)' FPI(1)' FPI(7)' TDI1' (AEI1 + AEI2) + DRW + SR ST]
goCI2 = TTS DRW' (SR' + ST') [FPA(9)' FEB(3)' + FPI(6) + FPI(7)]
goCI3 = CTI FPI(1) FPO(4) IWM20 DRW' (SR' + ST')
goCI3 = CTI [FPI(0) FPO(4)' + FPI(5) AEI1' AEI2' + FPI(7) (GCI1 + GCI2) + DRW + SR ST]

Window Machine Select

JWM1 = IWM20 FSI(1)
JWM2 = IWM20 FSI(2)
JWM3 = IWM20 FSI(3)
JWM4 = IWM20 FSI(4)
JWM5 = IWM20 FSI(5)

FIG. 34
Window Machine Ready Interrogate

JWM41 = FSI(1)
JWM42 = FSI(2)
JWM43 = FSI(3)
JWM44 = FSI(4)
JWM45 = FSI(5)
JWM46 = FSI(6)
JWM47 = FSI(7)
JWM48 = FSI(8)
JWM49 = FSI(9)
JWM50 = FSI(10)
JWM51 = FSI(11)
JWM52 = FSI(12)
JWM53 = FSI(13)
JWM34 = FSI(14)
JWM35 = FSI(15)
JWM36 = FSI(0)

Row Select
JWM21 = FCI(15)
JWM22 = FCI(16)
JWM23 = FCI(17)
JWM24 = FCI(14)
JWM25 = FCI(11)
JWM26 = FCI(10)
JWM27 = FCI(9)
JWM28 = FCI(8)
JWM29 = FCI(7)
JWM30 = FCI(6)
JWM31 = FCI(5)
JWM32 = FCI(4)
JWM33 = FCI(3)
JWM34 = FCI(2)
JWM35 = FCI(13)
JWM36 = FCI(12)

Window Machine Release
Input OK
JWM37 = FPI(7) AEI1' AEI2' + ST FPI(7) (AEI1 + AEI2)

Input Error
JWM38 = FPI(7) ST' (AEI1 + AEI2)

FIG. 36
Time Delays

Window Machine Select

tDI1 = gCI3 GCI3' + FPI(7) ST' (AEI1 + AEI2)

Echo Delay

tDI2 = IGA6' FPI(5)' FPI(7)' + FPI(4) + FPI(6)

Switches

SF = ST703
SR = SP701
ST = ST701

Relays

DRW = K203

FIG. 37
REMOTe CONTROLLER OUTPUT
SECTION

Outputs from CLA

JCA101 - Data Bit (2^0)
JCA102 - Data Bit (2^1)
JCA103 - Data Bit (2^2)
JCA104 - Data Bit (2^3)
JCA106 - Request to Output
JCA107 - Clock Data
JCA108 - Transmission Error

Input to CLA

ICA102 - Answer Output OK
ICA103 - Answer Output Error

Outputs to Window Machine

JWM101 - Selection of Window Machine #1
JWM102 - Selection of Window Machine #2
JWM103 - Selection of Window Machine #3
JWM104 - Selection of Window Machine #4
JWM105 - Selection of Window Machine #5
JWM106 - Selection of Window Machine #6
JWM107 - Selection of Window Machine #7
JWM108 - Selection of Window Machine #8
JWM109 - Selection of Window Machine #9
JWM110 - Selection of Window Machine #10
JWM111 - Selection of Window Machine #11
FIG. 39
JW148' - Digit 8
JW149' - Digit 9

JWM152 - System On
JWM160 - Auxiliary Control Digit (2^0)
JWM161 - Auxiliary Control Digit (2^1)
JWM162 - Auxiliary Control Digit (2^2)

JWM171 - Lamp Control Digit (2)
JWM172 - Lamp Control Digit (2)
JWM173 - Lamp Control Digit (2)
JWM174 - Lamp Control Digit (2)
JWM175 - Lamp Reset

JWM190 - Window Machine Trip

Inputs from Window Machine
IWM101 - Window Machine Ready
IWM102 - Window Machine On Line

Data Register
ADO1 - Data Bit (2^0)  ADO(0) to ADO(9) inclusive
ADO2 - Data Bit (2^1)  represent digital values
ADO3 - Data Bit (2^2)  0 to 9 inclusive of the
ADO4 - Data Bit (2^3)  output data.

Error Register
AE01 - Window Machine Busy

FIG. 40
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AE02 - Window Machine Not There
AE03 - Error Before Window Machine Select
AE04 - Error After Window Machine Select

Longitudinal Bit Register
AL01 - Sum Check Bit (2^0)
AL02 - Sum Check Bit (2^1)
AL03 - Sum Check Bit (2^2)
AL04 - Sum Check Bit (2^3)
AL00 represents the output of the Longitudinal Bit Register when it is set to zero.

Select Register
AS01 - (2^0) Bit
AS02 - (2^1) Bit
AS03 - (2^2) Bit
AS04 - (2^3) Bit
AS05 - Select
AS(0) to AS(15) inclusive represent values corresponding to the window machine numbers in the branch.

Clocks
CCO - Row Counter Clock
CLO - Longitudinal Bit Register Clock
CPO - Program Counter Clock
CTO - Main Timing Clock

Blow-Out SCR
DBO - SCR Blow-Out Pulse

Firing SCR
DFO - SCR Firing Pulse

FIG. 41
Error Encode

DEO1 - \( (2^0) \) Bit
DEO2 - \( (2^1) \) Bit
DEO3 - \( (2^2) \) Bit

Row Counter

FCO1 - Flip-Flop \( (2^0) \) Bit
FCO2 - Flip-Flop \( (2^1) \) Bit
FCO3 - Flip-Flop \( (2^2) \) Bit
FCO4 - Flip-Flop \( (2^3) \) Bit
FCO5 - Flip-Flop \( (2^4) \) Bit

\( \text{FC(0) to FCO(18) inclusive} \) represent the decoded output values of the Output Row Counter for Counts 1 to 18 inclusive.

Program Counter

FP01 - Flip-Flop \( (2^0) \) Bit
FP02 - Flip-Flop \( (2^1) \) Bit
FP03 - Flip-Flop \( (2^2) \) Bit
FP0(0) - Delay Block
FP0(1) - Answer Back Block
FP0(2) - Type Error Transmission Block
FP0(3) - Reset Block
FP0(4) - Request to Output Block
FP0(5) - Load Keyboard Block
FP0(6) - Delay Block or Error Override
FP0(7) - Trip Window Machine

Sync Memory

GC01 - Gates Program Counter

FIG. 42
GC02 - Gates Program Counter and Blow-Out in Test Mode During Reset
GC03 - Prevents Output OK and Type of Error Answer During Warm Up

Miscellaneous Drives
DM02 - No Error Override of Not in Test
DM03 - Data Character 10 or Greater
DM04 - Row Count One through Three
DM05 - Parity or Last Clock Indication
DM06 - Clock Data in Row Count #1
DM07 - Prevents Error Encode Answer During Warm Up
DM08 - Output Error Indication
DM09 - Program Count 0 or 2
DM10 - Program Count 5 and Row Count Other Than 0
DM11 - Program Count 5 and Row Count 0
DM12 - Program Count 5 and Row Count Other Than 18
DM13 - Detect SCR Not Turned Off
DM14 - Error Indication Before Window Machine Select
DM15 - Error Indication

Reset Drives
DR01 - Reset Program Counter
DR02 - Reset Row Counter

Echo Output
ICA102 - Output OK
ICA103 - Output Error

FIG. 43
Lamps

Bon - System On
Bit - Interlock

Switches

SE - Error Override

Time Delays

TD01 - Clock Detector (60 msec. retrig.)
TD02 - Error Override (49 msec.)
TD03 - Lamp Reset (25 msec.)
TD04 - Deionization (500 usec.)
TD05 - Firing Pulse (55 usec.)
TD06 - Inhibit (1 msec.)

FIG. 44
Data Register

\[ a_{D01} = JCA107', JCA101 \]
\[ o_{aD01} = JCA107', JCA101' \]
\[ a_{D02} = JCA107', JCA102 \]
\[ o_{aD02} = JCA107', JCA102' \]
\[ a_{D03} = JCA107', JCA103 \]
\[ o_{aD03} = JCA107', JCA103' \]
\[ a_{D04} = JCA107', JCA104 \]
\[ o_{aD04} = JCA107', JCA104' \]

Error Register

\[ a_{E01} = IWM101', IWM102, TD05, FCO(1), (SE' + ST') \]
\[ o_{aE01} = FPO(3) \]
\[ a_{E02} = IWM102', TD05, FCO(1), (SE' + ST') \]
\[ o_{aE02} = FPO(3) \]
\[ a_{E03} = (SE' + ST') \ TRS \left\{ FPO(5), FCO(1), FCO(2), FCO(3) \right\} \]
\[ (JCA108 + TD01') + JCA107, JCA104, FCO(3), FCO(12)', FCO(18)' \]
\[ (JCA102 + JCA103) \]
\[ o_{aE03} = FPO(3) \]
\[ a_{E04} = (SE' + ST') \left\{ FPO(5), TRS, FCO(0)', FCO(1)', FCO(2)', FCO(3)' \right\} \]
\[ TD01' + IWM101' + IWM102' + JCA108 + JCA107, JCA104, FCO(12)' \]
\[ FCO(18)' (JCA102 + JCA103) + FCO(18)TD05ALO(0) \]
\[ o_{aE04} = FPO(3) \]

Longitudinal Bit Register

\[ a_{L01} = CLO ADO1 FPO(3)' \]

**FIG. 45**
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oaL01 = CLO \left[ AD01 + FPO(3) \right]
aL02 = CLO AD02 FPO(3)'
aL02 = CLO \left[ AD02 + FPO(3) \right]
aL03 = CLO AD03 FPO(3)'
aL03 = CLO \left[ AD03 + FPO(3) \right]
aL04 = CLO AD04 FPO(3)'
aL04 = CLO \left[ AD04 + FPO(3) \right]

Select Register
aS01 = JCA107 JCA101 FLO(1)
aaS01 = FPO(3)
aS02 = JCA107 JCA102 FCO(1)
aaS02 = FPO(3)
aS03 = JCA107 JCA103 FCO(1)
aaS03 = FPO(3)
aS04 = JCA107 JCA104 FCO(1)
aaS04 = FPO(3)
aS05 = FPO(5) FCO(1) JCA107
aaS05 = FPO(0)

Clocks
CCO = FPO(4) CPO + FPO(5) FCO(0) + TD05 + TRS FPO(5) (AE01 + AE02 + AE03 + AE04) + DRW + SR ST
CLO = JCA107 FPO(5) FCO(0) + CPO FPO(3)
CPO = CTO \left[ CCO1 + DR01 FPO(0) \right]

FIG. 46
CTO = DRW' (SR' + ST') JCA5 [FPO(0) + FPO(2)] + TRS [FPO(1) +
FPO(3) + FPO(4) + FPO(5) + FPO(6) + FPO(7) + DRO1]

Blow-Out SCR

DBO = CPO GC01 (AE01 + AE02 + AE03 + AE04) [FPO(5) + FPO(6)] +
JCA107 FPO(5) + TRS FPO(0) GC02

Firing Pulse SCR

DF0 = TD05 [FPO(5) FCO(18) AE01' AE02' AE03' + TD02]

Error Encode

DE01 = FPO(2) GC03' AE04' (AE01 AE02' + AE03)
DE02 = FPO(2) GC03' AE04' (AE02 + AE03)
DE03 = FPO(2) GC03' AE04

Miscellaneous Drives

DM02 = SE' + ST'
DM03 = JCA107 JCA104 FCO(13)' FCO(18) (JCA102 + JCA103)
DM04 = FCO(1) + FCO(2) + FCO(3)
DM05 = FPO(5) (JCA108 + TD01')
DM06 = JCA107 FCO(1)
DM07 = FPO(2) GC03' AE04'
DM08 = AE01 + AE02 + AE03 + AE04
DM09 = FPO(0) + FPO(2)
DM10 = FPO(5) FCO(0)'
DM11 = FPO(5) FCO(0)
DM12 = FPO(5) FCO(18)'

FIG. 47
DMO13 = SW TD02' \left[ FP0(5)' + TD01 \right] \\
DMO14 = AE01 + AE02 + AE03 \\
DMO15 = FP0(5) (AE01 + AE02 + AE03 + AE04) + DRW + SR ST \\

Reset Drives \\
DR01 = FP0(5) (AE01 + AE02 + AE03) + GCD2 + DRW \\
DR02 = FP0(5) (AE01 + AE02 + AE03 + AE04) + FC0(18) + DRW + SR ST \\

Row Counter \\
FC01 = CCO DR02' \\
ofC01 = CCO \\
FC02 = CCO FC01 DR02' \\
ofC02 = CCO (FC01 + DR02) \\
FC03 = CCO FC01 FC02 DR02' \\
ofC03 = CCO (FC01 FC02 + DR02) \\
FC04 = CCO FC01 FC02 FC03 DR02' \\
ofC04 = CCO (FC01 FC02 FC03 + DR03) \\
FC05 = CCO FC01 FC02 FC03 FC04 DR02' \\
ofC05 = CCO (FC01 FC02 FC03 FC04 + DR02) \\

Program Counter \\
FP01 = CPO DR01' \\
ofFP01 = CPO \\
FP02 = CPO FP01 DR01' \\
ofFP02 = CPO (FP01 + DR01) \\
FP03 = CPO FP01 FP02 DR01' \\
ofFP03 = CPO (FP01 FP02 + DR01) \\

FIG. 48
Sync Memory
\[ gC01 = CTO\ DRW'\ (SR' + ST')\ \left[ FPO(0)\ FCO(0)\ JCA4 + FPO(1)\ JCA106' \right. \]
\[ + FPO(2) + FPO(3) + FPO(4)\ JCA106 + FPO(5)\ FCO(0)\ TD01' \]
\[ + FPO(6)\ TD02' + FPO(7)\ TD01' \]
\[ ogC01 = CTO\ FPO(1)' \]
\[ gC02 = TRS\ FPO(0)'\ TD01'\ SR\ ST \]
\[ ogC02 = TRS\ FPO(0) \]
\[ gC03 = DRW + SR\ ST \]
\[ ogC03 = FPO(3) \]

Echo Output
\[ ICA102 = FPO(1)\ JCA106\ GCO3'\ AE01'\ AE02'\ AE03'\ AE04' \]
\[ ICA103 = FPO(1)\ JCA106\ GCO3' (AE01 + AE02 + AE03 + AE04) \]

Row Select
\[ JW121' = DFO\ \left[ FCO(15) + AE04\ FCO(0) \right] \]
\[ JW122' = DFO\ FCO(16) \]
\[ JW123' = DFO\ FCO(17) \]
\[ JW124' = DFO\ FCO(14) \]
\[ JW125' = DFO\ FCO(11) \]
\[ JW126' = DFO\ FCO(10) \]
\[ JW127' = DFO\ FCO(9) \]
\[ JW128' = DFO\ FCO(8) \]
\[ JW129' = DFO\ FCO(7) \]
\[ JW130' = DFO\ FCO(6) \]
\[ JW131' = DFO\ FCO(5) \]

FIG. 49
JW132' = DFO FCO(4)
JW133' = DFO FCO(3)

Digit Lines
JW141' = ADO(1) DFO FCO(0)'
JW142' = ADO(2) DFO FCO(0)'
JW143' = ADO(3) DFO FCO(0)'
JW144' = ADO(4) DFO FCO(0)'
JW145' = DFO [ADO(5) FCO(0) + FCO(0) AEO4]
JW146' = ADO(6) DFO FCO(0)'
JW147' = ADO(7) DFO FCO(0)'
JW148' = ADO(8) DFO FCO(0)'
JW149' = ADO(9) DFO FCO(0)'

Window Machine Select
JWM101 = ASO(1) AS05
JWM102 = ASO(2) AS05
JWM103 = ASO(3) AS05
JWM104 = ASO(4) AS05
JWM105 = ASO(5) AS05
JWM106 = ASO(6) AS05
JWM107 = ASO(7) AS05
JWM108 = ASO(8) AS05
JWM109 = ASO(9) AS05
JWM110 = ASO(10) AS05
JWM111 = ASO(11) AS05

FIG. 50
JWM112 = ASO(12) ASO5
JWM113 = ASO(13) ASO5
JWM114 = ASO(14) ASO5
JWM115 = ASO(15) ASO5
JWM116 = ASO(0) ASO5

Lamp and Relay Control

Auxiliary Control Digits
JWM160 = AD01 FCO(14)
JWM161 = AD02 FCO(14)
JWM162 = AD03 FCO(14)

Window Machine Trip
JWM190 = ASO5 FPO(7) TD01

Lamp Digits
JWM171 = AD01 FCO(13) + AEO4 ASO5
JWM172 = AD02 FCO(13) + AEO4 ASO5
JWM173 = AD03 FCO(13)
JWM174 = ADO4 FCO(13)
JWM175 = TD03 TD06 (JWM171 + JWM172 + JWM173 + JWM174)

Lamps
JWM152 = JCA4 JCA6
BON = JCA4
BIT = JCA6

FIG. 51
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Time Delays

tD01 = [FP0(5) TDO6 AE01' AE02' AE03' AE04' FCO(18)'] + FP0(4) + FP0(6) (SR' + ST')
tD02 = FP0(5) FCO(0) GC01 (AE01 + AE02 + AE03 + AE04)
tD03 = FCO(12) TDO4
tD04 = FP0(5) [JCA107 FCO(0)'] + CPC
tD05 = TDO4'
tD06 = FP0(5) [JCA107 FCO(0)'] + CPC

Switches

SE = (ST 702)

FIG. 52
TRANSMITTER SECTION

Transmitter Register

FT0 - Flip-Flop #0
FT1 - Flip-Flop #1
FT2 - Flip-Flop #2
FT3 - Flip-Flop #3
FT4 - Flip-Flop #4
FT5 - Flip-Flop #5
FT6 - Flip-Flop #6
FT7 - Flip-Flop #7

Control Memories

GRI - Request to Input Memory
GTS - Transmitter Sync. Memory

Miscellaneous Drives

DNF - No Flag Bit in Transmitter Register
DNT - NOD Character in Transmitter Register
DRI - Request to Input
DER - Output Error
DOK - Output OK
DLD - Load Data
DTE - Transmitter Register Empty

Timing Elements

TTN - Normal Transmitter One Shot (55 msec.)

FIG. 53
TTS - Special Transmitter One Shot (55 msec.)
CT - Transmitter Clock

RECEIVER SECTION

Receiver Register
FRO - Flip-Flop #0
FR1 - Flip-Flop #1
FR2 - Flip-Flop #2
FR3 - Flip-Flop #3
FR4 - Flip-Flop #4
FR5 - Flip-Flop #5
FR6 - Flip-Flop #6

Control Memories
GRO - Request to Output Memory
GSI - Start Input Memory

Miscellaneous Drives
DPC - Odd Parity Check
DNR - NOD Character in Receiver Register
DRO - Request to Output Character in Receiver Register
DSI - Start Input Character in Receiver Register

Timing Elements
TRN - Normal Receiver One Shot (55 msec.)
TRS - Special Receiver One Shot (55 msec.)
CR - Receiver Clock

FIG. 54
Inputs to CLA from Input/Output Section

ICA1  - Data Bit (2⁰)
ICA2  - Data Bit (2¹)
ICA3  - Data Bit (2²)
ICA4  - Data Bit (2³)
ICA5  - Odd Parity Bit
ICA6  - Request to Input
ICA7  - Data On Line
ICA102 - Answer Output OK
ICA103 - Answer Output Error

Outputs from CLA to Input/Output Section

JCA1  - Start Input
JCA2  - Answer Input OK
JCA3  - Answer Input Error
JCA4  - System On
JCA5  - Request for Character
JCA6  - Interlock
JCA101 - Data Bit (2⁰)
JCA102 - Data Bit (2¹)
JCA103 - Data Bit (2²)
JCA104 - Data Bit (2³)
JCA106 - Request to Output
JCA107 - Character Present
JCA108 - Error In Transmission

FIG. 55
Communication Line to/from Data Set

RS - Request to Send
SD - Send Data
DCR - 1 KC Receiver Clock
SCT - 2 KC Transmitter Clock
DCT - 1 KC Transmitter Clock
CS - Clear to Send
CO - Carrier On
LT - Interlock
NS - New Sync
RD - Receive Data

Transmitter Logic Equations

Transmitter Register

\[ \text{fT0} = \text{fT0}' \text{ TTN FT1} \]
\[ \text{ofT0} = \text{fT0} \text{ TTN FT1}' \]
\[ \text{FT1} = \text{FT1}' \text{ CT (FT2 + DLD)} \]
\[ \text{ofT1} = \text{FT1} \text{ CT FT2}' \]
\[ \text{FT2} = \text{FT2}' \text{ CT (FT3 + DRI DTE + DER DTE + DOK DTE + DLD ICA3)} \]
\[ \text{ofT2} = \text{FT2} \text{ CT FT3}' \]
\[ \text{FT3} = \text{FT3}' \text{ CT (FT4 + DRI DTE + DLD ICA1)} \]
\[ \text{ofT3} = \text{FT3} \text{ CT FT4'} \]
\[ \text{FT4} = \text{FT4'} \text{ CT (FT5 + DLD ICA2)} \]
\[ \text{ofT4} = \text{FT4} \text{ CT FT5'} \]
\[ \text{FT5} = \text{FT5'} \text{ CT (FT6 + DOK DTE + DLD ICA3)} \]

FIG. 56
ofT5 = FT5 CT FT6
FT6 = FT6' CT (FT7 + DER DTE + DLD ICA4)
ofT6 = FT6 CT FT7'
FT7 = FT7' CT (DTE + DNF + DMI1)
ofT7 = FT7 CT DMI1'

Control Memories

gR1 = CT DTE DRI
goR1 = ICA6' + DMI1
gTS = DNT DMI1'
goTS = CT DMI1

Miscellaneous Terms

DNF = FTO' FT1' FT2' FT3' FT4' FT5' FT6' FT7'
DNT = FTO FT1' FT2' FT3' FT4' FT5' FT6' FT7'
DRI = JCA5' GRI' ICA6
DER = DRI' JCA5' ICA103
DOK = DRI' JCA5' ICA102
DLD = JCA5 ICA7
DTE = TTS DNT

Timing Elements

TTN = SCT
TTS = SCT'
CT = TTN + DTE

FIG. 57
Receiver Logic Equations

Receiver Register

\[ \begin{align*}
    f_{R0} &= f_{R0}' CR f_{R1} \\
    o_f f_{R0} &= f_{R0} CR \\
    f_{R1} &= f_{R1}' CR f_{R2} f_{R0}' \\
    o_f f_{R1} &= f_{R1} CR (f_{R2}' + f_{R0}) \\
    f_{R2} &= f_{R2}' CR f_{R3} f_{R0}' \\
    o_f f_{R2} &= f_{R2} CR (f_{R3}' + f_{R0}) \\
    f_{R3} &= f_{R3}' CR f_{R4} f_{R0}' \\
    o_f f_{R3} &= f_{R3} CR (f_{R4}' + f_{R0}) \\
    f_{R4} &= f_{R4}' CR f_{R5} f_{R0}' \\
    o_f f_{R4} &= f_{R4} CR (f_{R5}' + f_{R0}) \\
    f_{R5} &= f_{R5}' CR f_{R6} f_{R0}' \\
    o_f f_{R5} &= f_{R5} CR (f_{R6}' + f_{R0}) \\
    f_{R6} &= f_{R6}' CR f_{R6} f_{R0}' \\
    o_f f_{R6} &= f_{R6} CR (RD' + f_{R0})
\end{align*} \]

Control Memories

\[ \begin{align*}
    g_{RO} &= DRO \\
    o_g g_{RO} &= CT (DTR DTE + DOK DTE + DMI1) \\
    g_{SI} &= DSI \\
    o_g g_{SI} &= CT (ICA6' + DMI1)
\end{align*} \]

Miscellaneous Terms

\[ DPC = \left\{ (f_{R0} \oplus f_{R1}) \oplus (f_{R2} \oplus f_{R3}) \oplus (f_{R4} \oplus f_{R5}) \right\} \oplus f_{R6} \]

FIG. 58
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DNR = FRO FR1' FR2' FR3' FR4' FR5' FR6'
DRO = FRO FR1' FR2 FR3 FR4' FR5' FR6' DMI1'
DSI = FRO FR1' FR2' FR3' FR4 FR5' FR6' DMI1'

Timing Elements

TRN = DCR'
TRS = DCR
CR = TRN + FRO TRS

Communication Lines to Input and Output Section

JCA1 = GSI ICA6
JCA2 = FRO FR1' FR2 FR3' FR4' FR5 FR6'
JCA3 = FRO FR1' FR2 FR3' FR4' FR5' FR6
JCA4 = GO GS
JCA5 = DTE DRI' DOK' DER'
JCA6 = IT
JCA101 = FR3
JCA102 = FR4
JCA103 = FR5
JCA104 = FR6
JCA106 = GRO
JCA107 = FRO FR1 CR
JCA108 = DPC' FRO + FRO FR1' DNR' DRO' DSI' JCA2' JCA3'

FIG. 59
Communication Lines to and From Dataphone

RS = DMIL'
SD = GTS FTO
DCR = DCRP CO + SCT CO'

FIG. 60
FIG. 63

Fig. 79 ICA1

Fig. 79 ICA2

Fig. 79 ICA3

Fig. 79 ICA4

Fig. 79 ICA5

Fig. 79 ICA6

Fig. 79 ICA7

Fig. 92 ICA102

Fig. 92 ICA103
FIG. 75
FIG. 76A
FIG. 86A

FIG. 17A
FIG. 97A
### FIG. 70
- FR0
- FR1
- FR2
- FR3
- FR4
- FR5
- FR6
- ALO1
- ALO2
- ALO3
- ALO4
- GC01b
- FT0
- FT1
- FT2
- FT3
- FT4
- FT5
- FT6
- FT7
- AL11a
- AL12a
- AL13a
- AL14a

### FIG. 82
- AS01a
- AS02a
- AS03a
- AS04a
- AS05a
- AD01a
- AD02a
- AD03a
- AD04a
- AE05
- AE06
- AE07
- FS11a
- FS12a
- FS13a
- FS14a
- GC11a
- GC12a
- GC13a
- TD12
- AE13
- AE14
- AE15
- TD01

### FIG. 102
FIG. 104

WAVE FORMS FOR NORMAL OUTPUT MESSAGE
INPUT ROW COUNTER AND TEST COUNTER TIMING WAVE FORMS
FIG. 109  MAIN INPUT TIMING WAVE FORMS

CTI
GCI 1
CPI
FP1 1
FP1 2
FP1 3
GSI
FSI 1
FSI 2
FSI 3
FSI 4
GSI 3
TDI 1
CGI
ICA 7
FGI 1
FGI 2
FGI 3
FGI 4
FGI 5
ICA 6
ON-LINE BRANCH FOR DATA PROCESSING SYSTEMS

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Claims. (Cl. 340—172.5)

This invention relates generally to a data processing system, and more particularly relates to a system comprising a central data processing station and a plurality of branches remote from the central station and in "on-line" communication therewith, whereby information can be entered into the system from any of the branches, processed immediately by the central station, and returned in processed form to the originating branch to be utilized there.

More specifically, the present invention is directed to the means utilized in a branch sub-system for accepting information from an external source, translating the information into a form suitable for transmission to the central station of the system, receiving information transmitted from the central system, and utilizing the transmitted information. In addition, numerous means are provided for preventing incorrect operations of the system, for preventing utilization of erroneous data, and for handling special conditions which may arise.

Although this invention has many applications, it is particularly adapted for use by banking organizations having a number of branch banks and a central bank location in which is housed the central data processing station, where permanent records of all of the bank's individual accounts are maintained. The system of the present invention makes it possible for an individual account holder to have performed any desired transaction, such as deposit, withdrawal, interest entry, etc., at any one of the bank's branches, with the central data processing system performing the necessary computations and maintaining the centrally stored account record in up-to-date condition. Furthermore, each branch may contain a number of teller stations, each provided with an input-output device, which may take the form of a window posting machine, so that a number of customers can be served simultaneously at each branch's sub-system location.

In conventional banking facilities, using conventional banking procedures, window posting machines have long been used to record the deposits and withdrawals of customers at tellers' windows. When used alone, these machines extend the balance and print the necessary information about each transaction on the customer's passbook, the bank's ledger card, the machine's internal audit tape, and a transaction slip. In addition, the window posting machines maintain running totals of such transaction classifications as deposits, withdrawals, checks, interest, etc. These totals can be read out at any time or at the end of any period of operation. Thus, the history and the current status of each account are contained on the customer's passbook and the bank's ledger card. Also, a history of the day's activity at each window is printed on the audit tape. A summary of this activity, by classification is contained in the machine totals and activity counters.

All of this information is utilized by the bookkeeping, accounting, and auditing functions of the organization. In particular, interest has to be calculated at the end of the interest period for each account. It requires many hours of overtime for bank employees to first compute the interest from the ledgers and then prepare the account activity information and then post the new balance result to the card. The teller must also update the customer's passbook from the ledger card at his first opportunity. This method of interest computation is subject to error, both in the calculation and in the manual interest postings. Because the ledger cards, which occupy a great deal of floor space, must be easily accessible to the teller, in larger banks the customer can only go to the window that has access to his card.

To eliminate some of these problems, punched paper tape recorders, actuated by the window machines, have been added by many banks. As a by-product of the transaction posting of the window machine, the paper tape recorder punches information required for the ledger card. Later, the taped information is converted to punched cards for the back-office tabulating system, which updates the bank's records. This eliminates the need for ledger cards on the banking floor and allows the customer to use any window. Also, interest is calculated on a daily basis as a part of the mechanized updating of the bank's records.

This system still has disadvantages, however. The teller must manually post the interest to the customer's passbook from an interest card provided by the back office, at the end of each period. Again, the teller has no convenient access to the bank's record of accounts for reference purposes. These disadvantages are eliminated by the "on-line" savings bank system of the present invention.

In this on-line system, all window machines directly communicate with a data processor at the bank's central accounting location. The window machine sends transaction messages to the data processor, which performs the necessary calculations, updates the bank's records, and sends a message back to the window machine to automatically update the customer's passbook and complete the transaction. The advantages of this system are:

(1) The customer may use any window at any of the bank's branches for any normal transaction.

(2) The teller operates without leaving the window.

(3) The window machine automatically posts the updated interest on the first presentation of the customer's passbook.

(4) The window machine indicates such account conditions as stop, dormant, hold, and uncollected funds.

(5) The data processor detects and eliminates errors caused by incorrect old balances, incorrect account numbers, incorrect interest, and no-book transactions.

(6) The data processor eliminates the need for space-consuming reference files on the banking floor.

(7) The data processor calculates and accumulates anticipated interest as a part of the bank's account-updating routine.

(8) The system makes available current balances and account conditions to any teller's window.

A simple deposit or withdrawal transaction illustrates on-line operation. The customer presents his passbook and transaction slip at any teller's window. The teller verifies the amount of the transaction and enters the old passbook balance into the window machine. This is transmitted to the central processor in the form of a message segment. He then enters the transaction amount and the account number, which are transmitted to the central processor in successive message segments. The central processor receives the message segment for each entry when the teller depresses the proper operating key of the window machine. When the processor receives the account number (which indicates the end of the message), it begins processing the transaction. First, the processor compares the passbook balance with the bank's balance. When they agree, the processor applies the transaction to update the bank's records and sends a series of message segments to the window machine that causes it to post the necessary entries on the passbook and the transaction slip. These message segments also activate the window machine totals and cause the window ma-
chine to extend the balance to complete the transaction. When the processor finds that the passbook balance and the bank's balance do not agree, it applies any unposted interest or no-book transactions to the passbook balance to produce agreement. The processor then processes the transaction and sends a series of message segments to the window machine that cause it to update the passbook and post the necessary entries and extensions to complete the new transaction. When the processor is unable to produce agreement or finds some special account condition, an indicator light on the window machine informs the teller of this situation.

The central processor of the on-line system of the present invention communicates with only a single window machine at a time. A system of scanning insures that each machine, in turn, can send or receive a single message segment. When the processor receives from a window machine the final segment of a message, it assembles it with the previously received segments and acts on the message. It sends to the window machine, in periodic segments, a message in reply. The window machine unlocks when it receives the last segment of a message from the processor. Each branch sub-system consists of the teller's window machines in the branch, plus special controller equipment to receive message input and output for these machines. The branch sub-system equipment is the subject of the present invention.

The window posting machine serves as the input-output device for the branch sub-system. The teller sends messages to the processor by depressing the proper amount and operating keys on the keyboard of the window machine. The processor sends messages to the window machine by depressing the keys of the window machine through solenoids located beneath the keyboard. The window machine may also be operated off-line in the conventional manner.

When operating on-line, each window machine is connected to a separate window machine controller that gates the transaction information inputs and outputs. The controller also provides internal decoding and memory functions for machine control and accounts status information.

A number of window machine controllers are connected to a remote controller, which transmits and receives all transaction and control information over the communications sub-system. This remote controller scans and selects its window machines for communication with the central processor. It also performs such internal operations as encoding and decoding, parity and sum checking, and program and column counting. The remote controller is connected to the communications subsystem through a device such as the Bell System Digital Sub-Set Model 201A.

Accordingly, it is an object of the present invention to provide a data processing system including at least one remote branch sub-system capable of performing an input-output function, and of communicating with a central data processing station.

Another object is to provide, in a data processing system, a branch sub-system having a plurality of input-output devices which can be selectively connected to a central data processing system for transmission of information in both directions.

Another object is to provide, in a data processing system, a branch sub-system capable of successively scanning a number of input-output devices connected thereto for connecting one of said devices, when properly conditioned, to a central data processing station for transmission of information.

Another object is to provide, in a data processing system, a branch sub-system capable of selectively connecting one of a group of input-output devices to a central data processing station for transmission of information, and capable of detecting erroneous information and initiating corrective measures.

Another object is to provide, in a data processing system, a branch sub-system capable of selectively connecting one of a group of input-output devices to a central data processing station for the transmission of information, and capable of converting the information from one form to another for such transmission.

Another object is to provide, in a data processing system, a branch sub-system capable of selectively connecting one of a group of input-output devices to a central data processing station for the transmission of information, and capable of controlling the selected input-output device to cause recording of the information transmitted from the central data processing station.

Another object is to provide, in a data processing system, a branch sub-system capable of selectively connecting one of a group of input-output devices to a central data processing station for the transmission of information, and capable of serially reading out row information storage means associated with the selected input-output device to sense therefrom the information which is to be transmitted to the central data processing station.

With these and incidental objects in view, the invention includes certain novel features of construction and combinations of parts, a preferred form or embodiment of which will hereinafter be described with reference to the drawings which accompany and form a part of this specification.

In the drawings:

FIG. 1 is a schematic block diagram showing the on-line banking system as a whole, with the various branches associated with the central station;

FIG. 2 is a perspective view showing a typical branch layout;

FIG. 3 is a chart showing the input message segment format;

FIG. 4 is a chart showing the output message segment format;

FIG. 5 is a chart showing the data character format;

FIG. 6 is a chart showing different control characters which may be used in controlling the system;

FIG. 7 is a perspective view of a window machine, or input-output device, several of which may be used in each branch sub-system;

FIG. 8 is a view showing a keyboard of the window machine of FIG. 7;

FIGS. 9A and 9B comprise a view showing the selector switches and relay rack forming a part of the window machine;

FIG. 10 is an end view of the structure of FIGS. 9A and 9B;

FIGS. 11A, 11B, and 11C, taken together, show one portion of the operating circuitry of the window machine;

FIGS. 12A and 12B, taken together, show another portion of the operating circuitry of the window machine;

FIG. 13 shows the circuit for energizing the keyboard solenoids of the window machine, with associated circuitry;

FIG. 14 shows a program board utilized in the operating circuitry of the window machine;

FIG. 15 shows certain additional circuitry of the window machine;
FIGS. 16A and 16B, taken together, show a portion of the operating circuitry of the window machine controller;
FIGS. 17A and 17B, taken together, show another portion of the operating circuitry of the window machine controller;
FIGS. 18 and 19 show further portions of the operating circuitry of the window machine controller;
FIGS. 20A and 20B, taken together, show a simplified block diagram of the various elements of the remote controller;
FIG. 21 is a chart showing the input program format;
FIG. 22 is a chart showing the output program format;
FIGS. 23 to 29 inclusive contain definitions of the various logic terms employed in the input section of the remote controller;
FIGS. 30 to 37 inclusive contain equations for the logic terms employed in the input section of the remote controller;
FIG. 38 to 44 inclusive contain definitions of the various logic terms employed in the output section of the remote controller;
FIGS. 45 to 52 inclusive contain equations for the logic terms employed in the output section of the remote controller;
FIGS. 53 to 60 inclusive contain definitions and equations for the various logic terms employed in the CLA section of the remote controller;
FIGS. 61 to 72 inclusive are logic block diagrams of the CLA section of the remote controller;
FIGS. 73 to 84 inclusive are logic block diagrams of the input section of the remote controller;
FIGS. 85 to 96 inclusive are logic block diagrams of the output section of the remote controller;
FIGS. 97 and 97A, taken together, constitute a circuit diagram of a power supply which is suitable for use with the present invention;
FIGS. 98 to 98G inclusive, taken together, constitute a circuit diagram of the keyboard operating solenoid motor of the window machine and the associated control circuitry;
FIG. 98H is a diagram showing the manner in which FIGS. 98 to 98G inclusive are arranged with respect to each other to form the circuit diagram;
FIGS. 99, 99A, 100, 101, 102, and 103 are diagrams showing various testing and simulation circuits which, in the illustrated embodiment, are included as an integral part of the branch sub-system;
FIG. 104 to 114 inclusive are timing diagrams showing the relationship of various types of signals in different types of operations of the system;
FIG. 115 is a circuit diagram of a branch to data sub-set level converter, together with its block diagram representation;
FIG. 116 is a circuit diagram of a data sub-set to branch level converter, together with its block diagram representation;
FIG. 117 is a circuit diagram of an input level converter, together with its block diagram representation;
FIG. 118 is a circuit diagram of an output level converter, together with its block diagram representation;
FIG. 119 is a circuit diagram of a logic inverter, together with its block diagram representation;
FIG. 120 is a circuit diagram of a power inverter, together with its block diagram representation;
FIG. 121 is a circuit diagram of a drive inverter, together with its block diagram representation;
FIG. 122 is a circuit diagram of an NPN inverter, together with its block diagram representation;
FIG. 123 is a circuit diagram of a special NPN inverter, together with its block diagram representation;
FIG. 124 is a circuit diagram of an OR gate, together with its block diagram representation;
FIG. 125 is a circuit diagram of an AND gate, together with its block diagram representation;
FIG. 126 is a circuit diagram of a flip-flop, together with its block diagram representation;
FIG. 127 is a circuit diagram of an exclusive OR circuit, together with its block diagram representation;
FIG. 128 is a circuit diagram of an OR inverter circuit, together with its block diagram representation;
FIG. 129 is a circuit diagram of an AND inverter circuit, together with its block diagram representation;
FIG. 130 is a circuit diagram of a logic latch, together with its block diagram representation;
FIG. 131 is a circuit diagram of a five-volt power supply, together with its block diagram representation;
FIG. 132 is a circuit diagram of a special relay driver, together with its block diagram representation;
FIGS. 133, 134, and 135 are circuit diagrams of AND and diode circuits, together with their block diagram representations;
FIG. 136 is a circuit diagram of a decimal-to-binary encoder, together with its block diagram representation;
FIG. 137 is a circuit diagram of a clamping diode circuit, together with its block diagram representation;
FIGS. 138A and 138B, taken together, are a circuit diagram of the binary-to-decimal encoder No. 1, together with its block diagram representation;
FIGS. 139A and 139B, taken together, are a circuit diagram of the binary-to-decimal encoder No. 2, together with its block diagram representation;
FIG. 140 is a circuit diagram for 60 and 350 millisecond retriggerable one-shots, together with block diagram representations for these devices;
FIG. 141 is a circuit diagram of a 55 millisecond one-shot, together with its block diagram representation;
FIG. 142 is a circuit diagram for 500 and 1000 microsecond one-shots, together with block diagram representations for these devices;
FIG. 143 is a circuit diagram for 25 and 50 millisecond one-shots, together with block diagram representations for these devices;
FIG. 144 is a circuit diagram of a latch, together with its block diagram representation;
FIG. 145 is a circuit diagram of a blow-out circuit, together with its block diagram representation;
FIG. 146 is a circuit diagram of a sense circuit, together with its block diagram representation;
FIG. 147 is a circuit diagram of a solenoid driver circuit, together with its block diagram representation;
FIGS. 148 and 149 are circuit diagrams of OR diode circuits, together with block diagram representations of these circuits;
FIG. 150 is a circuit diagram of an AND resistor circuit, together with its block diagram representation;
FIGS. 151 and 152 are circuit diagrams of OR resistor circuits, together with their block diagram representations;
FIG. 153 is a circuit diagram of a latch, together with its block diagram representation;
FIG. 154 is a circuit diagram of a minus five-volt supply, together with its block diagram representation;
FIG. 155 is a circuit diagram of a plus five-volt supply, together with its block diagram representation;
FIG. 156 is a circuit diagram of a power source, together with its block diagram representation;
FIG. 157 is a circuit diagram showing certain data sub-set simulator circuits, together with its block diagram representation; and
FIG. 158 is a circuit diagram of an indicator lamp circuit, together with its block diagram representation.

Referring now to FIG. 1 of the drawings, there is shown a schematic diagram illustrating one arrangement by which a branch sub-system embodying the present invention can be incorporated into an on-line data processing system which includes a number of such branches, together with a central data processing station. It will be appreciated that the present invention can be implemented in many different ways and that the branch sub-system ap-
paratus disclosed herein constitutes only one of many possible variations which may be employed.

As shown in the diagram, the system includes a plurality of branch sub-systems 100 and a central station 101. Since the present invention relates to the branch sub-system, per se, and not to the overall system, or to the central station, the system as a whole and the central station will be described only in general terms, and the specific description will be confined to the branch sub-system. For a more detailed description of the system as a central station, reference may be made to the copending United States patent application Ser. No. 335,184, filed Jan. 2, 1964, inventors Robert M. Tink et al.

The central station 101 includes a data processor 102, which may be any suitably programmed, modern, high-speed digital data processor, together with the necessary peripheral equipment, including one or more random access memory devices 103. One such suitable data processor is the Class 315 computer, manufactured by The National Cash Register Company, Dayton, Ohio, United States of America, and available with the necessary peripheral equipment.

Connected to the data processor are one or more buffers 104, up to sixteen of which may be used in the illustrated embodiment. Each buffer has an internal memory capable of storing one message segment used in communicating between the central station and a branch sub-system. Input lines to the central station are continuously monitored, and when a remote location, or branch sub-system, has data for the data processor 102, the data is transferred into the buffer memory. The processor 102 is notified, and when it is ready, the data is transferred from buffer to processor. When the processor has information for a remote location, the out-going data is transferred to the buffer memory, and the processor is released to perform other work. The buffer selects the line to the remote location and transfers the data when the sub-system is ready to receive. A sum check character accompanies each message segment to assure accurate transfer of data.

Physically associated with each buffer and internally connected thereto are a number of CLA (Communication Line Adapter) units, corresponding to the number of remote branch sub-systems (which may be any number up to eight in the illustrated embodiment) which are connected to the buffer in the system. During an output operation, in which information is transmitted from the central data processing station 101 to one of the branches, one function of the CLA unit is to convert the normal parallel-bit characters from the buffer into serial-bit characters for transmission over telephone lines. During an input operation, in which information is transmitted from one of the remote sub-systems to the central processing station, the serial-bit characters from the telephone lines are converted by the CLA unit into parallel-bit characters for transmission to the buffer. This conversion is necessary because data transmission over telephone lines is always in serial-bit form.

Connected to each CLA unit of each buffer is a suitable telephone line terminal device or data sub-set 105, such as the Bell System Digital Sub-Set Model 201A, which is a modulator-demodulator designed to transmit and receive data over a switched voice-frequency telephone circuit for a private line at a transmission rate of 2000 bits per second. Each telephone line terminal device 105 is connected over telephone lines to a remote branch sub-system 100, to enable communication to take place between the various branch sub-systems and the central data processing station.

As shown in Fig. 1, each remote branch sub-system 100 is connected over telephone lines 106 to one of the telephone line terminal devices 105 associated with one of the buffers 104 of the central data processing station 101. In the sub-system, the telephone lines terminate in another suitable telephone line terminal device 107, which also may be a Bell System Digital Sub-Set Model 201A.

The terminal device 107 in each branch sub-system is connected to a remote controller 108, which integrally contains a CLA unit for the purpose of character conversion. Each remote controller 108 can accommodate a number (up to sixteen in the illustrated embodiment) of window machines 109, each with an associated window machine controller 110. The remote controller 108, acting upon information received from its associated buffer 104, can select any one of the window machines 109 in its branch sub-system. When not communicating with a window machine 109 or with the central data processing station 101, the remote controller 108 "locks on" to the requesting window machine 109 and connects it to the buffer 104.

The window machine 109 acts as an input device for transmitting information from the teller's window in the branch sub-system to the data processor 102 at the central station 101, which will then directly access, on a random basis, the account balances and return information to the window machine 109, which will then update the record media relating to the account, and post the current transaction. The window machine 109 can be operated off-line as a conventional window machine if communication with the central station 101 is interrupted. After communication is restored, the off-line transactions printed upon an audit tape by the window machine 109 are re-entered by the window machine operator, or teller, in a re-entry operation, for transmission to the central station 101 to update the bank's accounts.

A window machine controller 110 is interconnected between the remote controller 108 and each window machine 109, and contains the wiring configuration and the control switching necessary to permit each window machine 109 to communicate with the remote controller 108. The window machine controller 110 prevents transmission of signals from the remote controller 108 to the window machine 109 associated with the controller if said window machine is busy with another operation. Any window machine 109 or window machine controller 110 can be taken out of service at any time without interfering with the overall on-line banking system operation. The only limiting condition is that the part of the window machine controller 110 containing the numerical designation of the window machine 109 must remain in the circuit, or else the remote controller 108 will be prevented from selecting other window machines.

The controller 110 associated with each window machine 109 is located below the counter 111. All of the controllers in the sub-system are connected to a single remote controller 108, which may be located in the vicinity of the banking floor, and connected to a digital sub-set device 107, from which the telephone lines 106 extend to the central station 101. It may be noted that if a branch location is sufficiently large, more than one remote controller 108 may be required, in order to provide for the necessary number of window machines 109.

INPUT AND OUTPUT MESSAGE FORMAT

Every transaction that is handled in an on-line mode from a branch sub-system requires an input message and an output message. Input and output are both determined with respect to the central processor. Thus, a message sent from the keyboard of the window machine through the remote controller to the central processor by the machine operator, or teller, is considered to be an input message. A message sent from the central processor through the remote controller to the keyboard of the
window machine is considered to be an output message. Both types of messages consist of one or more message segments. During input operations, the window machine transmits a segment each time that it cycles. The account number segment always indicates to the central processor the end of the input message. An input message cannot have more than five segments in the illustrated embodiment of the present invention. During output operations of the window machine, each message segment from the central station 101 causes a message cycle that can, in addition, be followed by a second balance or sub-balance cycle, which is also initiated by that message segment. A balance cycle always indicates to the window machine the end of the output message.

FIG. 3 shows the information arrangement of an input message segment from the branch sub-system. Each segment consists of sixteen decimal digits. The first digit is the window machine position, or window machine scanner position number, and has a value which may be anywhere from zero to fifteen, inclusive. This identifies the window machine position. The second digit is normally zero. Digits three to eleven inclusive are the values of the nine window machine amount rows (keyboard rows 5 to 13 inclusive). When a tenth high-order digit (row 14) occurs during the transmission of machine totals, this digit occupies the second digit position in the message. Generally, digits twelve and thirteen are the two window machine numbers that may have a value from 00 through 99. Digits fourteen to seventeen inclusive are the four window machine control rows. The last digit, number eighteen, is the longitudinal bit check value. It represents the sum of the bits of all of the previous digit values of the segment, taken without carry, and is used as a transmission accuracy check.

FIG. 4 shows the information arrangement of an output message segment. Each segment again consists of eighteen decimal digits whose arrangement is similar to those of the input segment. The first digit is the window machine scanner position number. The second digit is normally zero. Digits three to eleven inclusive and fourteen to seventeen inclusive operate the solenoid actuator keyboard. Digit twelve lights one of twelve window machine indicator lights and has a value of zero to twelve inclusive. Digit thirteen, the automatic cycle digit, specifies a second cycle of operation of the window machine that causes a balance or a sub-balance cycle of operation of the window machine to follow the first cycle. This digit may have a value of zero to seven inclusive, with the following significance: 0: none; 1: balance; 2: sub-balance; 3: auditor over-ride; 4: auditor over-ride; 5: no over-ride; 6: spare; 7: spare. It will thus be seen that this digit can specify a second cycle in the case of a balance or sub-balance operation, to follow the first cycle, or, alternatively, can specify no second cycle, or can require the operator to over-ride or to void an operation. The last digit, number eighteen, is the longitudinal bit check digit.

FIG. 5 shows the information arrangement of a digit of a message segment. Each digit consists of seven bits, or binary digits. A "one" bit in the flag bit position indicates the beginning of the digit. A "zero" in the control position indicates that the digit is a data character. The parity bit maintains an odd parity. The four data bits provide a binary value of the digit. 

In addition to data characters that make up digits of the message segments, the branch sub-system sends and receives character strings, which are shown in FIG. 6. There are five different control characters which may be used. The first is 1000000, which is a "no data" character used for timing purposes to maintain synchronization between the local and central adapters, and which is always employed when no other information is being transmitted, so that there will always be a signal carried on the line. The second control character is a "request to transmit" character, which is a request by the sender to transmit information to the receiver. In the case of a transmission by the central station, this is the only signal preceding the transmission of data. The "request to transmit" signal is in form 1011000. The third control character is a "ready" signal, in form 1010100, and is a signal transmitted by the branch to indicate that it is all right for the branch to proceed with the sending of information. The fourth control character is an "OK" character having the form 1010010, which indicates in either the input or the output direction that the last data transmission was satisfactory. The fifth data character is a "write," or error, character, having the form 1010001, indicating that the last transmission was in error in some respect.

Input segments leave the branch sub-system serially by bit and serially by digit at a rate of 2000 bits per second in the illustrated embodiment of the present invention. Output segments enter the branch sub-system serially by bit and serially by digit at a rate of 1000 bits per second.

WINDOW MACHINE CONTROLLER

The window machine controller 110 is a unit of the on-line branch sub-system which is provided to enable each window machine 109 of a branch to communicate with the remote controller 108 of that branch. As has been previously described, a window machine controller 110 is provided for each window machine in the branch.

The window machine controller 110 is essentially an electrical device consisting of a plurality of relays, or transmission elements, and a plurality of associated electrical components which operate with the remainder of the branch circuitry to control the transmission of information, and to exercise certain other controls over the operation of the associated window machine. If desired, the various components of the window machine controller 110 could be packaged integrally with the associated window machine 109, but in the illustrated embodiment, the components of the window machine controller have been separately packaged for convenience, and to facilitate removal of a window machine from the branch sub-system.

As shown in FIGS. 1 and 2, all of the various window machine controllers of the branch are connected by cables to the remote controller 108 in such a manner that all of the information transmitted from the remote controller 108 is, in effect, transmitted to all of the window machine controllers 110. However, gating means in the various window machine controllers prevent such information from being passed on to any but the one selected window machine.

The operating circuitry of the window machine controller is shown in FIGS. 16A, 16B, 17A, 17B, 18, and 19. FIGS. 16A, 16B, and 18 show mainly the input control circuitry, while FIGS. 17A, 17B, and 19 show mainly the output control circuitry. It will be noted that all of the various horizontally-disposed conductors in FIGS. 16A and 17A bearing reference identifications and representing individual lines in the cables connecting the branch window machine controllers 110 to the remote controller 108 have vertically-disposed conductors connected thereto bearing the same reference identifications.

These vertically-disposed conductors represent individual lines in cables which extend to the next adjacent window machine controller of the branch sub-system. This illustrates the manner in which the various input and output lines or conductors connecting the remote controller and the window machine controllers are connected to transmit the necessary information within the branch sub-system.

In addition to these conductors, which will be subsequently described in greater detail, the window machine controller contains a terminal board TBC, which is diagrammatically shown in separate sections in FIGS. 16B and 17A. This terminal board is wired to represent the number (of the sixteen possible in each branch) of the window machine that it controls.
The relays K102, K105, and K108 are energized when the scanner of the remote controller finds a Ready Interrogate circuit completed, thus indicating that a specific window machine is ready for an input operation. Since the window machine select lines are scanned simultaneously and in the same sequential order as the Ready Interrogate lines, the circuit through the terminal board for the Window Machine Select line of the machine in question is completed, resulting in energization of the three relays K102, K105, and K108.

Energization of these relays closes contacts controlled by said relays in the digit lines in the window machine controller, as will be described subsequently.

Also shown in FIGS. 15A and 16B are ten Digit lines. These lines are designated at their left extremities, representing the interface or connection between the window machine controller 110 and the remote controller 108, by reference characters JWMI1 to JWMI10, and by individual circled letter designations. At the right extremities, representing the interface or connection between the window machine controller 110 and the window machine 109, they are designated by reference characters IMI1 to IMI10 inclusive, and by the same circled letter designations as on the left. These lines represent the ten positions zero-eliminate and 1 to 9 inclusive of the various rotary row switches (FIGS. 12A and 12B), corresponding to the amount and control rows of the window machine.

Each of these lines is controlled by a set of contacts of one of the three relays K102, K105, and K108, described above, said contacts being opened to interrupt the lines, except when the relays are energized. These contacts close when the relays K102, K105, and K108 are energized. This establishes continuity in these lines in the window machine controller to enable the remote controller, by pulsing the subsequently-described Input Row Select Lines, to read out the information contained in each rotary row switch in the window machine. This readout is accomplished by virtue of the fact that the wiper of each rotary switch will be set to one of its contact positions, which position in turn is connected to one of the Digit lines. The information is thus transmitted from the window machine through the window machine controller 110 back to the remote controller 108, and from there to the central data processing station 101, as will be described subsequently.

A fourth group of lines, shown in FIGS. 16A and 16B, are sixteen Row Select lines. These lines are designated at their left extremities, representing the interface or connection between the remote controller 108 and the window machine controller 110, by reference characters JWMI1 to JWMI16, and by individual circled letter designations. At their right extremities, representing the interface or connection between the window machine controller 110 and the window machine 109, they are designated by the reference characters JWMI1 to JWMI16, and by the same circled letter designations as on the left. A diode 113 is connected into each of these lines in order to limit the current flow therethrough to one desired direction.

Fourteen of these lines—namely, JWMI1 to JWMI14 inclusive—extend to the wipers or commons of the rotary row switches in the window machine. The two remaining lines JWMI15 and JWMI16 terminate in positions H11 and E11 of program board TB501 (FIG. 14) of the window machine, which is wired in an interjection. Since these units and ten number of this particular machine in the entire system.

As the row counter of the remote controller 108 advances sequentially, each of the sixteen Row Select lines of the window machine controller 110 will be pulsed sequentially, beginning with the line that terminates at the row 14 rotary switch SR514A (FIG. 12A). The Digit line selected by the position of the row switch will also be pulsed, and this pulse on the selected Digit line will be transmitted back to the remote controller over the selected Digit line, since the contacts in
controller. The energizing circuit for the relay K208 extends from the line JWM152 over the relay K208 to the line HWM1, which is connected to a source of minus 20-volt D.C. power.

The System On line JWM152 is common to all window machine controllers, and therefore the relay K208 energizes in each window machine controller and remains energized for as long as the entire system remains in an "on-line" condition and is able to transmit.

Relay K208 energizes the window machine controlling the opening of the contacts K208A01 (FIG. 19) in the window machine controller to prepare a path for illumination of three machine status lamps in the window machine. These lights are the READY lamp IS14 (FIG. 12A), the PARTIAL MESSAGE lamp IS16, and the PROCESSOR CONTROL lamp IS18. The READY lamp lights when the window machine is in an "on-line" mode and the crossfooter, or add-subtract totalizer, has been cleared. The PARTIAL MESSAGE lamp lights after an input segment has been introduced into the remote controller from the window machine. The PROCESSOR CONTROL lamp lights after an end-of-message operation has taken place in the input mode of operation of the system.

The complete circuits for energization of these lamps will be described in the subsequent explanation of the operating circuitry of the window machine.

An Answer Ready line is provided in the window machine controller 110, originates in the window machine 109 and extends through the window machine controller to the remote controller 108. This line is designated at its left extremity, representing the interface or connection between the remote controller 108 and the window machine controller 110, by reference character JWM20 (FIG. 16A) and by an individual circled letter designation. At the right extremity, representing the interface or connection between the window machine controller 110 and the window machine 109, the line is designated by the reference character JWM (FIG. 16B) and by the same circled letter designation at the left. While the Answer Ready line is common to all window machine controllers, only a window machine which is ready for an input operation and which is being interrogated by a pulse on its associated Ready Interrogate line affects this line. This line is connected to the contacts K507A02 (FIG. 11A) of the relay K507 in the window machine, the connection being represented in FIG. 11A by the terminal 80. Said contacts are also connected to the Ready Interrogate line J19, the connection being represented by the terminal 81. When an input signal has been introduced by the teler into the window machine, the relay K507 is energized closing the contacts K507A01, which couples the Answer Ready line to the Ready Interrogate line J19. The subject window machine is then selected by the remote controller when the scan counter of the remote controller sequentially counts to the Ready Interrogate line which is programmed to this particular window machine.

The various output control lines and the associated control relays included in the window machine controller will now be described.

A first group of output control lines, shown in FIG. 17A, are the Window Machine Select lines. These are eight lines JWM116 through JWM118 inclusive, or alternatively JWM109 to JWM116 inclusive, included in each output cable between the remote controller 108 and the window machine controller 110, terminating in the latter at the H and J sections on the back of the terminal board TBC1. These lines are common to all window machines, but only the selected window machine is affected by the signal on the selected line.

A jumper wire is used to connect one of the eight Window Machine Select line positions on the board TBC1 to a board position which is connected over a parallel combination of a resistor 114 and the normally closed contacts K3010B01 to a conductor 88. By means of the jumper wire,
wire, each window machine is assigned an output Window Machine Select position from one to eight on one output cable, and from nine to sixteen on the other output cable. Each of these output key number positions corresponds to a position of the output select register in the remote controller. The position selected on the H and J sections of the board TBC1 by the jumper wire should correspond to the positions selected on the other sections of the board TBC1 for the same window machine in connection with lines previously described above.

Between the conductor 88 and a conductor 89 are connected in parallel a diode 90 and eight Window Machine Select relays K301 to K308 inclusive. The conductor 89 is connected to a source of minus 20-volt D.C. potential. Therefore, when the central data processing station sends an output message to a specific window machine in a branch, a register in the remote controller sends a signal over the Window Machine Select line corresponding to the window machine in question, completing the circuit described above to energize the output Window Machine Select relays K301 to K308 inclusive in the Window Machine controller corresponding to the selected window machine.

Additional groups of lines, shown in Figs. 17A and 17B, are thirteen Output Row Select lines and nine Output Digit Select lines. The Output Digit Select lines are energized at their left extremities, representing the interface or connection between the window machine controller and the remote controller 108, by reference characters JWM121 to JWM133 inclusive, and by individual circled letter designations. At their right extremities, representing the interface or connection between the window machine controller and the window machine, they are designated by the reference characters JMW121 to JMW133 inclusive, and by the same circled letter designations as on the left. These lines are utilized, in a manner which will be more specifically described subsequently, to select the row on the window machine keyboard in which a key is to be depressed.

The Output Digit Select lines are designated at their left extremities, representing the interface or connection between the window machine controller and the remote controller, and the remote controller 108, by reference characters JMW141 to JMW149 inclusive, and by individual circled letter designations. At their right extremities, representing the interface or connection between the window machine controller and the window machine, they are designated by the reference characters JMW141 to JMW149 inclusive, and by the same circled letter designations as on the left. These lines are used in cooperation with the Output Row Select lines in selection of the key to be depressed on the solenoid-operated keyboard of the window machine. The manner in which keys on the keyboard of the window machine are selected and depressed will be subsequently described in greater detail.

Examination of Fig. 17B discloses that a set of contacts controlled by one of the relays K301 to K308 inclusive is interposed in each one of the Output Row Select lines and Output Digit Select lines. It will therefore be seen that these lines are interconnected, so that no signal can be transmitted thereon, until such time as the window machine to which the window machine controller corresponds has been selected and the relays K301 to K309 inclusive have been energized over the circuit described above in connection with the Window Machine Select lines. When these relays are energized, the various Window Machine Select relay contacts in the Output Row Select lines and the Output Digit Select lines are closed, so that the path for transmission of signals to the window machine for selection of keys to be depressed on the window machine keyboard is completed. The Output Row Select lines are connected to the output row counter in the remote controller, and, as said output row counter advances, each Row Select line is pulsed, beginning with the line which terminates at amount row 9 of the window machine key-board. When a Row Select line is pulsed which requires an amount key to be depressed, the Digit line representing the amount key in this row is also pulsed, causing the amount key to energize in a manner which will be described subsequently.

Four Lamp Bit lines are shown in Figs. 17A and 17B and are provided in the window machine controller to control Lamp Decode relays K202, K206, K207, K203, and K201, in said window machine controller. The Lamp Bit lines are designated at their left extremities, representing the interface or connection between the window machine controller and the remote controller 108, by reference characters JWM171 to JWM174 inclusive, and by individual circled letter designations.

Connected into the Lamp Bit lines are relay contacts K307AC3, K307AC4, K308AC1, and K308AC2, controlled by the Window Machine Select relays previously described. These relay contacts prevent transmission of signals over the Lamp Bit lines except when the Window Machine Select relays have been energized in the manner described above. These Lamp Bit lines control the determination of what indicator lamp shall be illuminated on the window machine. The transmission of a signal over a Lamp Bit line to a selected window machine controller causes energization of the corresponding Lamp Bit relay K201, K202, K203, K206, or K207, over a circuit which extends from the selected line over the relay to a conductor 91, which is connected to a minus 20-volt D.C. source. A diode 92 is connected in parallel with each of the relays K201, K202, K203, K206, and K207.

A predetermined combination of signals on the Lamp Bit lines causes the corresponding relays to be energized, and causes transferring of contacts controlled by said relays in a lamp decode relay tree, shown in Fig. 19, which decodes the binary code input to one of twelve output lines. Each of these lines represents an individual lamp upon the window machine indicator panel and controls the illumination of said lamp, in a manner which will be described subsequently.

Energization of the relays K201, K203, K206, and K207 also causes closing of contacts K201AC1, K203AC1, K207AC1, and K206AC1 in the lines JWM171, JWM172, JWM173, and JWM174, respectively. Each of these lines also contains a diode 93, shown to the right of the relay contacts mentioned above. These lines are connected together between the diodes and one side of relay contacts Q208C1, controlling the relay K205. Closing of these various contacts establishes holding circuits for maintaining the corresponding relays in energized condition, said circuits extending over the Lamp Reset line 1M35 to ground.

A relay K310 (Fig. 17B) is provided in the window machine controller circuitry and is adapted to be energized when the Window Machine Select relays K301 to K308 inclusive are energized. The energizing circuit for the relay K310 extends from the common 89, to which a source of minus 20-volt D.C. potential is applied, over the relay K310, and contact 1M35 to ground connection. It will be seen that, when the relay K308 is energized, the contacts K308AC3 close, thus causing the relay K310 to energize. Energization of the relay K310 causes certain contacts in the control circuitry of the window machine controller to be transferred, for purposes which will be described subsequently.

A Lamp Reset line JWM175 (Fig. 16A) is provided in the window machine controller. This line extends from the remote controller and terminates in the window machine controller. The Lamp Reset line JWM175 is connected to one side of a relay K310AC3, and the other side of which is connected to a minus 20-volt D.C. source. Interposed in the line JWM175 are contacts K310AC3, controlled by the relay K310. It will be seen that, when the relay K310 is energized, so that the contacts K310AC3 are closed, and when a signal is applied on the Lamp Reset line JWM175, the relay K206 is energized over the circuit de-
scribed above. A diode 94 is connected in parallel with the relay K205.

Energization of the relay K205 opens the contacts K205BC1 (FIG. 17B) to interrupt the holding circuit for the lamp decode relays K201, K203, K206, and K207 to deenergize any of these relays previously energized, and thus extinguish any lamps in the window machine previously turned on. A Trip line JVM190 (FIG. 16A) is provided in the window machine controller. This line extends from the remote controller to the window machine controller and functions to control the energization of a relay K204 in the window machine controller. Relay contacts K310AC2, controlled by the relay K310, are interposed in the Trip line, to prevent energization of the relay K204 unless the relay K310 is energized. The energizing circuit for the relay K204 extends from the Trip line JVM190 over the contacts K310AC2, over the parallel combination of the relay K204 and a diode 95, to a minus 20-volt d.c. source. Energization of the relay K204 causes the contacts K204AC1 (FIG. 18) to close, which completes an energizing circuit for the Trip solenoid L540 in the window machine, thereby allowing the window machine to be tripped to perform a cycle of operation, for utilizing an output segment of information.

Three Auxiliary Control Bit lines JVM160, JVM161, and JVM162 (FIGS. 16A and 16B) are provided in the window controller. These lines originate in the remote controller and terminate in the window machine controller. Interposed in these lines are relay contacts controlled by the Window Machine Select relays K306 and K307. These lines JVM160, JVM161, and JVM162 represent the binary bits for the auxiliary control digits, and are connected to one side of Auxiliary Control Digit relays K101, K103, and K106, respectively, so that signals on the lines are effective to energize said relays. The energizing circuits for the relays extend from the lines, over the previously-mentioned relay contacts controlled by the relays K306 and K307, over the relays K101, K103, K106, each in parallel with a diode 96, to a minus 20-volt d.c. source.

Contacts controlled by the relays K101, K103, K106 are included in an Auxiliary Control Digit relay tree, shown in FIG. 18, which decodes the binary input on the lines JVM160, JVM161, and JVM162 to one of seven output lines. Each of these output lines controls a relay in the window machine, as will be described subsequently. A Window Machine Ready line is provided in the window machine controller to the remote controller. This line is connected to the left by reference character JVM101 (FIG. 17A) and on the right by reference character 1M101 (FIG. 17B). A diode 97 is interposed in this line for purposes of isolation. This line is used to transmit a signal from the window machine to the remote controller to indicate that the window machine is in proper condition to receive a message from the remote controller.

A Window Machine On-Line line JVM102 is provided in the window machine controller, said line originating in the window machine controller and terminating in the remote controller. The Window Machine On-Line line has been interposed therein, as shown in FIG. 17B, an isolation diode 98 and contacts K309AC1, which are controlled by a relay K309. This line is connected through sections 31 of the program board T81 to the Window Machine Select relays K306 or JVM108 to JVM109, and in such a way that, when the contacts K309AC1 are closed, a signal appearing on one of the above lines also appears on the line JVM102 associated with the selected window machine.

The relay K309 (FIG. 17B) is connected into the operating circuitry of the window machine, so that when the window machine is in operating condition, the power on, the relay K309 is energized, and the contacts K309AC1 are closed, to complete the path over the line JVM102. A signal from the window machine, effected by closing of contacts in the machine, is transmitted over the Window Machine On-Line line to the remote controller to indicate that the selected window machine is in an "online" mode of operation.

Further reference will be made to various portions of the operating circuitry of the window machine controller in connection with the subsequent descriptions of other portions of the branch circuitry which cooperate with the window machine controller circuitry in the performance of certain functions.

WINDOW MACHINE

A perspective view of a suitable window machine 109 for employment in the branch sub-system of the present invention is shown in FIG. 7. This machine utilizes the basic construction disclosed and claimed in United States Patent No. 2,774,298, issued Dec. 18, 1956, inventors Everett M. Placke, Willis E. Eickman, and Charles S. Nagy, and in United States Patent No. 2,616,623, issued Nov. 4, 1952, inventors Mayo A. Goodbar, Everett H. Placke, and Carl G. Falkner. Reference may be had to these patents for a detailed description of the basic construction of the window machine. Modifications to the standard machine construction permit operation with the other elements of the on-line system. These modifications include a top lock keyboard, various control switches and relays, and a recorder assembly, all of which will be described subsequently.

As shown in FIG. 7, the present machine has three printing sections. The left-hand section is provided with a table 117 for receiving a transaction slip on which the record of the transaction may be validated. The center section is provided with a table 118 for receiving the passbook which is carried by the customer, and the right-hand section is provided with a printing mechanism (not shown) for printing, on an audit strip which is retained in the machine, all of the data entered in the pass-book and on the transaction slip. A window 119 is provided, so that the entries on the audit strip may be viewed by the machine operator.

The book printing mechanism and the transaction slip printing mechanism are provided with feelers to throw off the printing and feeding mechanisms in the event that no book or transaction slip is placed on the table in position to receive an entry.

The window machine 109 is provided with a keyboard 120, also shown in FIG. 8, which is a relay key for releasing depressed keys of the keyboard, four rows of control keys designated generally by the reference character 122, nine rows of amount keys designated generally by the reference character 123, and a plurality of indicator lights arranged in three vertically disposed panels 124, 125, and 126.

A top lock keyboard especially adapted for use with the window machine forming part of the on-line branch sub-system of the present invention is disclosed and claimed in the United States patent application Ser. No. 308,382, filed Sept. 12, 1963, inventors George C. Beason and Calvin E. Stichwhe. With this construction, the keyboard of the window machine is formed in three parts. The top lock keyboard contains the key tips that are depressed by the teller to index transactions into the machine. A solenoid keyboard, which is beneath the top lock keyboard, contains solenoids for each key that the central processor or the remote controller can operate during an output operation. The key stems of the top lock keyboard rest on the plunger of the solenoid keyboard. These plungers, in turn, rest on the key stems of the main keyboard, which key stems are used to control the actual entry of information into the window machine.

A brief description of the manner in which the various control keys of the four control rows are used, and the functions performed by them, both in an on-line mode of operation and in an off-line mode of operation, appears below.
Balance key (row 1)  
(On line)

Input.—The teller does not normally depress the Balance key during a transaction.

Output.—The central processor causes the Balance key to be operated through a solenoid to extend the balance, following the last message segment, to complete the transaction. This initiates a machine cycle to cause the following functions to be performed:

(a) Clear plus side of add-subtract totalizer.
(b) Consecutively feed forms in validating printer.
(c) Printing of data by audit, validating, and pass-book printers.
(d) Ejection of forms from validating and pass-book printers.
(e) Release and reset last line lock.
(f) Unlock all top-locked keys and reset the lock-out of Balance Pick Up or No Book key.

Sub Balance key (row 1)  
(On line)

Input.—The teller does not normally depress the Sub Balance key.

Output.—The central processor may cause the Sub Balance key to be operated through a solenoid to print a sub-balance following any message segment where additional segments will be posted. The teller may also depress the Sub Balance key when a machine is in a last-line-lock condition to cause printing of a balance on the last line of the pass-book before starting a new page. In either case, a machine cycle is initiated in which the following functions are performed:

(a) Read the plus side of the add-subtract totalizer.
(b) Consecutively feed forms in the validating printer.
(c) Printing of data by audit, validating, and pass-book printers.
(d) Release the last line lock.

Over Ride key (row 1)  
(On line)

Input.—The teller does not normally depress the Over Ride key.

Output.—The remote controller operates the Over Ride key through a solenoid when it detects an output error. The teller depresses the Over Ride key in response to a “hold” condition on an account, such as an insufficient balance. This allows the central processor to proceed with the output message. A second type of “hold” condition requires the supervisor to unlock the Total key before the Over Ride key is effective to operate the window machine. A third type of “hold” condition does not allow the depression of the Over Ride key. Depression of the Over Ride key initiates a machine cycle in which the following functions are performed:

(a) Printing of data by the audit printer.
(b) Release of last line lock.

Total key (row 1)  
(On line)

Input.—The teller cannot normally depress the Total key to send a message to the processor. This key is under lock control and can be used by a supervisor when the Total key lock 127 is unlocked. It may be used to override a special condition signal from the processor 102. The supervisor depresses the Total key to read out and clear the ten accumulating totals associated with control keys in rows 2 and 3 at the end of the day or other operating period. When a key associated with the total to be
read out is depressed, together with depression of the Total key, a machine cycle is initiated in which the following functions are performed:

(a) Read and clear the associated totalizer.
(b) Transfer the amount of the total to the add-subtract totalizer.
(c) Consecutively feed the forms in both printers.
(d) Printing of data by the audit, validating, and pass-book printers.

Output.—The central processor cannot operate the Total key through a solenoid.

(Off line)

The supervisor depresses the Total key under the same conditions as in on-line operation. This initiates a machine cycle in which the same functions are performed as listed above for on-line operation in the input mode.

**Sub Total key (row 1)**

(On line)

**Input.**—The teller depresses the Sub Total key to read out the ten accumulating totals associated with control keys in rows 2 and 3. This does not send a message to the central processor. When a key associated with the total to be read out is depressed together with the Sub Total key, a machine cycle is initiated in which the following functions are performed:

(a) Read the associated totalizer.
(b) Consecutively feed forms in both printers.
(c) Printing of data by audit, validating, and pass-book printers.

Output.—The computer cannot operate the Sub Total key through a solenoid.

(Off line)

The teller depresses the Sub Total key under the same conditions as in on-line operation. This initiates a machine cycle in which the same functions are performed as listed above for on-line operation in the input mode.

**Receive key (row 1)**

(On line)

**Input.**—The teller cannot depress the Receive key.

Output.—The central processor operates the Receive key through a solenoid to allow other operating keys to affect the accumulating totals and the add-subtract totalizer, and also to permit printing by the validating and pass-book printers. This control function is exercised by the Receive key due to the fact that it is desirable to have all printing in the pass-book printer and the validating printer, as well as all total accumulation, controlled by the central processor, which eliminates the need to make corrections in the pass-book and total accumulation, in the event that an error is made in indexing information, or in the event of a special condition which prohibits posting to the account. In an on-line mode of operation, the Receive key can therefore be energized only by the central processor, since the top lock keyboard of the window machine is locked against manual depression of the Receive key, which must be depressed to allow any transaction key to effect printing by the pass-book or validating printer, or to effect operation of the add-subtract totalizer or the accumulating totalizer.

(Off line)

The supervisor of the branch locks down the Receive key to allow other operating keys to affect the accumulating totals and the add-subtract totalizer and also to permit printing by the validating and pass-book printers. This is necessary when the operator first enters the transaction information, because the machine receives no output message from the central processor when it is operating off line.

**Balance Pick Up key (row 2)**

(On line)

**Input.**—The teller depresses the Balance Pick Up key to enter the amount of the old balance in a transaction. The Balance Pick Up, Plus-Minus, or No Book keys lock out the Balance Pick Up key until the teller depresses one of the O Draft, Void, B Account Number, or A Account Number keys. The Balance Pick Up key initiates a machine cycle in which the following functions are performed:

(a) Add to the add-subtract totalizer.
(b) Printing of data by the audit printer.

Output.—The central processor cannot operate the Balance Pick Up key through a solenoid. It can, however, unlock this key when it operates the Balance key.

(Off line)

The teller depresses the Balance Pick Up key to operate the machine in the same manner as described above for on-line operation in the input mode.

**B Account Number (row 2)**

(On line)

**Input.**—The teller depresses the B Account Number key to enter the account number for the transaction, identify the teller, and signal the central processor that this is the last message segment. Depression of this key initiates a machine cycle in which the following functions are performed:

(a) Consecutively feeding of forms in validating printer.
(b) Printing of data by the audit printer.
(c) Lock all top-locked keys.

Output.—The central processor cannot operate the B Account Number key through a solenoid.

(Off line)

The teller depresses the B Account Number key to operate the machine in the same manner as described above for on-line operation in the input mode.

**Duplicate W Drawal key (row 2)**

(On line)

**Input.**—The teller does not normally depress the Duplicate W Drawal key.
Output.—The central processor operates the Duplicate W Drawal key through a solenoid to update the pass-book and thus account for a previous "no book withdrawal" transaction. This initiates a machine cycle in which the following functions are performed:

(a) Subtract from add-subtract totalizer.
(b) Add to its own total (the Duplicate Deposit key also adds to this total).
(c) Consecutive feeding of forms in both the validating and pass-book printers.
(d) Printing of data by the audit, validating, and pass-book printers.

(Off line)

The teller depresses the Duplicate W Drawal key to operate the machine in the same manner as described above for on-line operation in the output mode.

Plus key (row 2)

(On line)

Input.—The teller depresses the Plus key to perform additions which are not part of an on-line transaction. This key does not send a message to the central processor, and locks the Balance Pick Up and No Book keys until one of the Balance, O Draft, Void, B Account Number, or A Account Number keys is depressed. The Plus key initiates a machine cycle in which the following functions are performed:

(a) Add to add-subtract totalizer.
(b) Consecutively feed the validating printer.
(c) Printing of data by the audit printer.

Output.—The central processor operates the Plus key in response to an inquiry which requires addition to the add-subtract totalizer. This initiates a machine cycle in which the same functions are performed as those given for the input mode, except that it also causes printing by the validating printer.

(Off line)

The teller depresses the Plus key to operate the machine in the same manner as described above for on-line operation in the input mode except that printing is also caused to take place by the validating printer.

Minus key (row 2)

The teller and the central processor use the Minus key to operate the machine in the same manner as the Plus key, because the Minus key causes subtraction from, instead of addition to, the add-subtract totalizer.

Eject key (row 2)

(On line)

Input.—The teller depresses the Eject key along with the Spec Check or Check keys to indicate that a check is being cashed. He also uses this key to eject forms from the printers. Depression of the Eject key initiates a machine cycle in which the following functions are performed:

(a) Printing of data by the audit printer.
(b) Ejection of forms from the validating and pass-book printers.
(c) Release of the last line lock.

Output.—The central processor operates the Eject key to perform the same functions as those given for the input mode, and to cause printing by the audit printer of information identifying an indicator lamp illuminated to inform the teller of the status of an account.

(Off line)

The teller depresses the Eject key to perform the same functions as those given for on-line operation in the input mode.

Account Number key (row 2)

The teller uses the A Account Number key to operate the machine in the same manner as has been described for the B Account Number key.

No Book key (row 2)

(On line)

Input.—The teller depresses the No Book key together with depression of a deposit or withdrawal key to indicate that the transaction is not being recorded in a pass-book. Any of the Balance Pick Up, Plus, Minus, or No Book keys lock out the No Book key until the teller depresses one of the O Draft, Void, B Account Number, or A Account Number keys. The key with which the No Book key is used initiates the machine cycle and determines what functions are to be performed during that cycle.

Output.—The central processor operates the No Book key to perform the same functions as those described above for the input mode.

(Off line)

The teller depresses the No Book key under the same conditions as given for on-line operation in the input mode.

Duplicate Deposit key (row 2)

This key has a function similar to that of the Duplicate W Drawal key except that it adds to the add-subtract totalizer instead of subtracting therefrom.

B Deposit key (row 3)

(On line)

Input.—The teller depresses the B Deposit key together with an amount, to designate the transaction as a deposit and to identify the teller. The No Book, O Draft, Void, Spec Check, or Check keys, which may be used with the B Deposit key, further identify conditions of the deposit. Depression of the B Deposit key initiates a machine cycle in which the following functions are performed:

(a) Consecutively feed forms in both the pass-book printer and the validating printer.
(b) Printing of data by the audit printer.

Output.—The central processor operates the B Deposit key, together with an amount, to designate the transaction as a deposit and to identify the teller during posting. The No Book, Trans, Spec Check, or Check keys may be operated with the B Deposit key to further identify the conditions of the deposit. Depression of the B Deposit key, when the Receive key is depressed, initiates a machine cycle in which the following functions are performed:

(a) Add to the add-subtract totalizer.
(b) Add to the B Deposit total.
(c) Consecutive feeding of forms in both the validating and pass-book printers.
(d) Printing of data by the audit, validating, and pass-book printers.

(Off line)

The teller depresses the B Deposit key under the same conditions as given above for on-line operation in the output mode.

B W Drawal key (row 3)

(On line)

Input.—The teller depresses the B W Drawal key, together with an amount, to designate the transaction as a withdrawal, and to identify the teller. The No Book or Trans key may be operated with the B W Drawal key to further identify the conditions of the withdrawal. De-
pression of the B W Drawer key initiates a machine cycle in which the following functions are performed:
(a) Consecutive feeding of forms in both the validating and pass-book printers.
(b) Printing of data by the audit printer.

Output.—The central processor operates the B W Drawer key together with an amount to designate the transaction as a withdrawal, and to identify the teller during posting. The No Book or Trans keys may be operated with the B W Drawer key to further identify the conditions of the withdrawal. Depression of the B W Drawer key, when the Receive key is depressed, initiates a machine cycle in which the following functions are performed:
(a) Subtracts from add-subtract totalizer.
(b) Adds to the total for the B W Drawer key.
(c) Consecutive feeding of forms in both the validating and pass-book printers.
(d) Printing of data by the audit, validating, and pass-book printers.

(Off line)
The teller depresses the B W Drawer key under the same conditions as given above for on-line operation in the output mode.

B Other key (row 3)
The teller of the window machine operates the B Other key to identify various miscellaneous receipts. Keys in control row 4, when used with the B Other key, further describe the operation. Depression of the B Other key initiates a machine cycle in which is similar in functions performed to the cycle initiated by the depression of the B Deposit key.

Interest key (row 3)

(On line)

Input.—The teller does not normally depress the Interest key.

Output.—The central processor operates the Interest key through a solenoid to post interest that has accrued from a previous period. This initiates a machine cycle, when the Receive key is depressed, in which the following functions are performed:
(a) Add to the add-subtract totalizer.
(b) Add to the total for the Interest key.
(c) Consecutive feeding of forms in both the validating and pass-book printers.
(d) Printing of data by the audit, validating, and pass-book printers.

(Off line)
The teller does not normally depress the Interest key.

W Drawer Correct key (row 3)

(On line)

Input.—The teller depresses the W Drawer Correct key with the original incorrect amount, in order to correct a previously-posted withdrawal transaction error. The keys in control row 4 may be used in conjunction with the W Drawer Correct key in order to further describe the conditions of the operation. Depression of the W Drawer Correct key initiates a machine cycle in which the following functions are performed:
(a) Consecutive feeding of forms in both the validating and pass-book printers.
(b) Printing of data by the audit printer.

Output.—The central processor operates the W Drawer Correct key together with the original incorrect amount to post the correction of a previously-posted withdrawal transaction. The keys in control row 4 may be depressed in conjunction with this key in order to further describe the condition. Depression of the W Drawer Correct key, when the Receiving key is depressed, initiates a machine cycle in which the following functions are performed:
(a) Add to the add-subtract totalizer.
(b) Add to the total of the W Drawer Correct key.
(c) Consecutive feeding of forms in both the validating and pass-book printers.
(d) Printing of data by the audit, validating, and pass-book printers.

(Off line)
The teller depresses the W Drawer Correct key to cause the same machine functions to be performed as those given above for on-line operation in the output mode.

Deposit Correct key (row 3)
The teller and the central processor use the Deposit Correct key to operate the window machine in a manner similar to that described for the W Drawer Correct key except that it causes subtraction from instead of addition to the add-subtract totalizer.

A Other key (row 3)
The teller and the central processor use the A Other key in the same manner as the B Other key, except that it identifies a different teller.

A W Drawer key (row 3)
The teller and the central processor use the A W Drawer key in the same manner as the B W Drawer key except that it identifies a different teller.

A Deposit key (row 3)
The teller and the central processor use the A Deposit key in the same manner as the B Deposit key except that it identifies a different teller.

Descriptive keys (Row 4)
The teller and the central processor use these keys together with the various motorized control keys to further describe various transaction conditions. These descriptive keys generally take the machine functions of the control key with which they are used, but provide an additional printing symbol. Such captions as School Sav., Safe Dep., Xmas, Ins., Mtge., TI. Ck Mo, Trans, Spec Check, and Check may appear on these keys.

Three of the above-described row 4 keys are of particular interest and will therefore be described in additional detail below.

The Trans (transfer) key is a key used in an on-line mode of operation to signal the processor that money being withdrawn from the account being processed is actually being transferred to another account. This key is used with the B Deposit, Deposit Correct, A Deposit keys to signal that the deposit being made is a transfer and should carry with it any anticipated interest accrued in the original account. In an off-line mode of operation, this key is used to provide visual identification that one of the above-described situations is present.

The Check and Spec Check keys of row 4 are used, in an on-line mode of operation, with the B Deposit, Deposit Correct, and A Deposit keys in an input operation to indicate that the deposits are made up of checks which have not yet been collected. Each of these keys represents a different length of delay in time before the money thus deposited will be available for withdrawal. These keys may be used with the Eject key to indicate that a check is being cashed and that an amount equal to the amount of the check should be made unavailable in the customer's account until the check has been collected. These keys are used with the Receive key and with the B Deposit, Deposit Correct, and A Deposit keys to print in the pass-book printer for visual identification in the customer's pass-book that the amount of this deposit is not immediately available. These keys perform the same function in
the off-line mode as described above in connection with the Receive key, the B Deposit key, the Deposit Correct key, and the A Deposit key.

In addition to the four rows of control keys 122 described above, the keyboard 120 of the window machine 109 also includes nine rows of amount keys 123. The amount rows are standard in construction and function, except that they are provided with solenoid energizing means so that they may be operated automatically by the central data processor, as will be described subsequently. Also it may be noted that two left-most amount rows may be used for branch number indexing purposes. When an account number for an account being processed is entered into a window machine by a teller, the machine automatically emits a branch number as a prefix to that account number, as part of the input message to the central processor. If the account is an account which was originated in another branch, that branch number must be indexed in the two left-most amount rows. Keys depressed in these rows will take precedence over the branch number normally emitted by the window machine. In this connection, it may be noted that branch numbers must exclude the use of zeros. This restriction is necessary because it is not possible to override an emitted digit with a zero in the event of an inter-branch transaction; i.e., at branch 15 there would be no way to post an account from branch 10, since the keyboard provides no way to depress a zero to override the five which is normally emitted in the example given.

The three vertically disposed indicator panels 124, 125, and 126 are positioned to the left of the amount key rows on the keyboard 120, as viewed in FIG. 8. Each of these panels includes a plurality of individual indicator lights which provide information to the machine operator concerning various operating conditions which may occur in the system. A group of indicator lights in the panel 124 indicates conditions detected by the window machine. The groups of indicator lights in the panels 125 and 126 indicate conditions which are primarily detected in other areas of the on-line system, and sent to the window machine as part of the output message segments from the central processor. A summary of the various indicator lights and the conditions which the indicate is included below.

The READY indicator light in the panel 124 indicates that the window machine is ready to accept the first segment of an input message.

The PARTIAL MESSAGE indicator light in the panel 124 indicates that the window machine is ready to accept additional segments of an input message. This light comes on after the first message segment has been entered into the window machine.

The PROCESSOR CONTROL indicator light in the panel 124 indicates that the message is completed and the machine is ready to receive an output message segment. This light goes off at the end of the output message, and the READY indicator light again lights.

The FORM MISSING indicator light in the panel 124 indicates that a form has not been inserted in one of the printers of the window machine, or that the last line of a form has been reached.

The ON LINE indicator light in the panel 124 indicates that the machine is switched to on-line operation. In addition to this light, the operator must check the READY, the PARTIAL MESSAGE, and the PROCESSOR CONTROL lights to determine that the machine can actually communicate with the central processor.

The OFF LINE indicator light of the panel 124 indicates that the machine is switched to off-line operation.

The SEND ERROR indicator light of the panel 125 indicates that equipment at the central location or the remote controller has detected an input message segment error. This condition requires the teller to void and re-enter the message.

The ENTRY ERROR indicator light of the panel 125 indicates that the teller has incorrectly entered an input message segment into the machine. This condition requires the teller to void and re-enter the message.

The RECEIVE ERROR indicator light of the panel 125 indicates that the equipment at the central location or the remote controller has detected an output message segment error. This condition requires the teller to void the message.

The ERROR UPDATE indicator light of the panel 125 indicates that the central processor is sending output message segments to correct a pass-book that has been previously posted in error. An audible alarm alerts the teller of this updating.

The REFERR indicator light of the panel 125 indicates that the customer's account is not available from the central processor.

The OVERDRAFT indicator light of the panel 125 indicates that the machine add-subtract totalizer is in a minus condition or that the central processor finds the account being processed to be overdrawn.

The six additional indicator lights located in the panel 126 may be programmed at the central processor to indicate various special account conditions.

On the left side of the window machine, as viewed in FIG. 8, is positioned a receiver 130 in which are located several additional controls, as well as an additional lock 131, controlled by a supervisory person at the branch.

This lock 131, when locked, prevents movement of a three-position slide 132, which exercises certain controls over the operation of the window machine. In a first position of the slide, designated LOCKED in FIG. 8, the window machine is locked in a condition in which all power is off and the machine cannot operate. In a second position of the slide, designated OPERATE in FIG. 8, power is applied to the machine and it is permitted to cycle. In a third position of the slide, designated DATE JOURNAL in FIG. 8, the supervisor of the branch is permitted to adjust a dater adjustment knob 133, for setting of the date. A visible date 134 is provided, so that the supervisor can tell which date has been set. In the third position of the slide 132, the supervisor is also permitted to operate the on-line off-line knob 135, which is located next to the dater adjustment knob 133 and which sets the machine to operate in either the on-line or the off-line mode of operation. In addition, the third position of the slide 132 allows access to the audit tape. The teller's key, which also fits this lock 131, only permits the teller to turn the machine on and off by using the first two positions of the slide.

Located above the slide 132, as viewed in FIG. 8, is a trip key 136, which may be used when it is necessary to trip the machine manually.

In connection with the control exercised by the on-line off-line knob 135, the following may be noted. When the machine is in the on-line mode of operation, rotary switches which are provided in association with each amount and control row of the window machine, and which will be further described subsequently, will be sensed after each machine cycle, and that portion of the message will be sent to an assembly area of the central processor, where the entire message will be assembled. The on-line off-line knob 135 permits a single machine to operate in an off-line mode, while the rest of the machines in the branch are operating in an on-line mode. To operate in an off-line mode with a window machine, it is necessary to lock down the Receive control key in Row 1, in addition to having the knob 135 in the off-line position.

As described in the previously-cited patents which disclose the basic construction of the window machine employed in the illustrated embodiment of the present invention, a key lock line (not shown) in the machine controls the locking and releasing of keys during a cycle of machine operation. Detents in the various rows of keys act as links between the key stems of the main keyboard and the key lock line. Detents also prevent the depression of illegal
combinations of keys and link the key stems with the zero stop control line that is located at the front of the keyboard. An auxiliary key lock line, which prevents the teller from removing the key, has been provided for each row of teller keys in which a message is transmitted from the central station to the window machine, is associated with the top lock keyboard.

The digit values of the depressed keys are transmitted to other parts of the machine by means of differential actuator racks. In one form, each row of output operation in which a message is transmitted from the control station to the window machine, is associated with the top lock keyboard.

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An accumulating totalizer is provided for each of the keys in the control row 3, and one additional totalizer is provided for accumulating a combined total of entries associated with the Duplicate Withdrawal and Duplicite Deposit keys in control row 2. Each of these totalizers is mounted on a single shaft and are of the type referred to in the art as “interposed totalizers.” The construction and selection of the interposed totalizers is like that shown and described in the above-mentioned Goodbar et al. United States Patent No. 2,616,625, and therefore no detailed description thereof is given herein. The add-subtract totalizer is mounted on the upper totalizer line and includes a mechanism for selecting the add and subtract sides of the two-wheel totalizers, which are geared together in a manner well known in the art. A brief summary of the manner in which the ten accumulating totalizers are controlled in the on-line and off-line modes of operation will now be given. In the on-line mode, no totalizers are affected when a message is entered into the window machine by a teller. Totalizers are affected only when the central processor sends a message back to the window machine. This is accomplished by having the processor message energize the Receive key in control row 1, which engages individual totalizers. The tenth totalizer, called Group Total 3, accumulates a single total for all duplicate postings, whether they are deposits or withdrawals. In on-line mode of operation, the Receive key of control row 1 must be locked down, and all transactions will affect accumulation totalizers on entry.

A brief summary of the manner in which the add-subtract totalizer is controlled in the on-line and off-line modes of operation will now be given. In the on-line mode, the add-subtract totalizer is affected only by the Balance Pick Up key on entry of a message. Depression of the Receive key by a processor message will enable the transaction keys to affect the add-subtract totalizer designated by the individual transaction keys. The add-subtract totalizer will be cleared by the Balance, Overdraft, and Void keys, and will be read, but not cleared, by the Sub Balance key. The add-subtract totalizer is affected by the Plus and Minus keys. These keys do not input information to the processor, and they lock out the Balance Pick Up and No Book keys until the Account Number key has been depressed, or the add-subtract totalizer has been cleared. In an off-line mode of operation, the Receive key must be depressed, and all transaction keys will affect the add-subtract totalizer as designated by the individual transaction keys.

The window machine differential actuator racks position the type wheels of the three printers through the front transmission line. This transmission line permits the digit values of the racks to be printed in the appropriate columns of the three printers, while a back transmission line permits the digit values of the racks to control machine operation. A brief description of each of the three printers in the window machine anönue will now be given.

The audit tape printer prints the details of each operation made by the machine. Each transaction appears on the audit tape two times when the window machine is operating in an on-line mode: once when entered into the machine by the teller, and once when the message is returned by the processor as the pass-book is printed upon. The audit tape is under lock control.

The pass-book printer, in the on-line mode of operation, is so controlled that no manual entries will be printed. Depression of the Receive key will cause transaction keys to effect printing by the pass-book printer on the pass-book if said pass-book has been inserted. A slip feeder will prevent printing if no pass-book is inserted. Posting beyond the last line of a pass-book is prohibited. This printer has the ability to post in the Data, Withdrawal, Deposit, Interest, Balance, and Transaction columns on a pass-book, and also has the ability to skip over the center fold of a pass-book. It will print eight digits in the Withdrawal column; nine digits in the Deposit column; six digits in the Interest column; and nine digits in the Balance column. The two low-order digits are underlined to designate cents. The printer also prints symbols from the four transaction rows in the Transaction columns.

When the machine is operating in an off-line mode, the Receive key is locked down, this printer will print transaction on entry, and the slip feeder will operate in the same manner as in a conventional window machine of this type.

The validating printer, in the on-line mode of operation, is controlled so that the account number is the only operator entry which will cause printing by this printer. The Account number will print in the Balance column. Depression of the Receive key will cause the transaction keys to effect printing by the validating printer if a slip has been inserted. A slip feeder prevents printing if no slip has been inserted. The validating printer has the ability to post in the Date, Withdrawal, Deposit, Interest, Balance, and Transaction columns on an inserted form, and has the same columnar capacity as the pass-book printer. For the validating printer to print in the off-line mode of operation, the Receive key must be locked down. Transactions will print on entry. This printer has the ability to post a ledger card. It is used to validate teller’s checks, money orders, deposit tickets, withdrawal slips, cash checks, and inquiry slips.

The window machine differential actuator racks also position the rotary read-out switches for each row (both amount and control) in accordance with the differential positions of the rows. These switches, and their association with the differential actuator racks of the window machine, are shown in FIGS. 9A, 9B, and 10. As may be seen in FIGS. 9A and 9B, each differential actuator rack 142 for the four control rows has three selector switches 143 associated therewith, certain of which switches are not utilized in the illustrated embodiment, while each differential actuator rack 142 for the amount rows 1 to 9 inclusive has one selector switch 143 associated therewith.

The selector switches designated by the reference characters SR501A, SR501B, and SR501C (FIG. 12B) are set by the control row 1 of the keyboard; switches SR502A and SR502B are set by the control row 2 of the keyboard; the switches SR503A and SR503B are set by the control row 3 of the keyboard; the switches SR504A and SR504B are set by the control row 4 of the keyboard; and the switches designated by the reference characters SR505A to SR514A inclusive are set by the amount rows 1 to 10 inclusive. It may be noted that amount rows 10 and 11 is known as an overflow row, and therefore it is not associated with a row of amount keys on the keyboard.
Three shafts 144, 145, and 146 form the main support for the selector switches. These shafts are mounted at each end in machine side frames 147 and 148. These selector switches, which have twelve positions, is similar to the construction of the ten-position selector switches disclosed in United States Patent No. 2,878,872, issued Mar. 24, 1959, to John H. Burns et al., and consequently will not be described in detail here.

Each selector switch includes a common having a terminal 149, twelve contacts 150, including one position not used and one for each of the eleven differential positions (eliminate, zero, and 1 to 9 inclusive) of the differential rack, and a rotatable wiper to engage the common with the contact 150 corresponding to the position of the related differential rack. The wiper is connected to a gear 151 for unitary movement therewith, said gear meshing with a gear 152, rotatable on a shaft 153, supported by the side frames 147 and 148. The gear 152 is integral with a gear 141, which meshes with the rack 142.

As previously indicated, each differential mechanism of control rows 1 to 4 inclusive, sets three selector switches. Therefore, three switch assemblies, comprising a set of twelve contacts 150, a common, and a wiper, are provided for each of these rows, and the three wipers are connected to operate simultaneously. In each of the amount rows 1 to 4 inclusive, the differential mechanisms sets only one selector switch. Therefore, only one switch assembly, comprising a set of twelve contacts 150, a common, and a wiper, is provided for each of these rows. The switch assemblies are held on the shafts 144 and 145, and on the center shaft 146, in the proper lateral alignment by suitable securing means.

After being set differentially by the differential mechanisms of the four control rows and the ten amount rows, the wipers are aligned and held in set position by aligner pawls 154, which are rocked into engagement with the gears 151 when an aligner shaft 155 is rocked by the arm 156 thereon, which is pivotally connected to a link 157, connected in turn to one arm 158 of a cam follower 159 rotatably mounted on a shaft 160, and provided with two rollers, 161 and 162, which engage a cam 163 mounted on the printer cam line 164 of the window machine.

The configuration of this cam is such that the aligners are moved out of engagement with the gears at the proper times to permit the storage switches to be set, and then moved into engagement with the gears to maintain the storage switches in the desired setting.

As may be seen in FIGS. 12A and 12B, the contacts 150, when in contact positions representing values of 1 to 9 inclusive, for all of the amount row rotary switches, and for the control row switches SR501A, SR502A, SR503A, and SR504A, are connected to nine common digit lines 167. It will be noted that all of the contacts of the various switches in the “one” position are connected to a “one” digit line 167; all of the contacts of the various switches in the “two” position are connected to a “two” digit line 167, etc. With respect to the “0” and “eliminate” contact positions of the various switches, it will be noted that these are connected to the operating circuit in various arrangements to the particular control to be exercised. The switches SR501B, SR501C, SR502B, SR503B, and SR504B, controlled by the racks of the control rows 1 to 4 inclusive of the window machine, are connected into the operating circuit in such a manner as to enable them to exercise a desired control over various types of window machine operations, as will be described subsequently.

The common digit lines, representing contact positions 0 to 9 inclusive, are permanently connected to the back of positions A10 and A1 to A9, respectively, of a program board TB501, shown in FIG. 14. This board, in the illustrated embodiment, is provided with ninety-six positions in coordinate arrangement, so that each individual position is identifiable by a letter and number combination. As may be seen in FIG. 14, certain of the positions are bussed together. At the front of the board, suitable receptacles are provided, so that the various positions can be connected by jumper wires, for purposes which will appear subsequently. At the back of the program board, certain positions are provided with conductors for connection to other components of the system circuitry. Positions D1 to D10 inclusive of program board TB501 are connected at the back to digital input lines 1 to 9 inclusive and 0, respectively, which carry input signal information from the window machine to the window machine controller. Positions H1 and E11 of the program board are connected at the back to window machine number lines for units and tens, respectively, which carry window machine number information from the window machine to the window machine controller. Jumper wires on the front of the program board TB501 are used to connect positions E11 and E11 to desired digit positions A1 to A9 or D1 to D9 to provide digit values for a window machine number. In FIG. 14, an exemplary connection of jumper wires is shown to provide for a number 15, for example. The terminals A11 and C11 are also jumped to digit lines to provide digits for a branch code number, and are connected at their backs to contacts of the branch code switch SC509 for controlling the transmission of a branch code signal by the window machine. Also, positions D12 and D12 are connected at their backs to terminals 165 and 166 for connection to other portions of the operating circuit.

An “add” operation illustrates a typical window machine operating cycle. During each such cycle, the main cam line of the window machine makes one revolution. This cam line provides timing and drive for the various phases of the machine operation. Some operations require two machine cycles. Zero to 360 degrees of main cam line rotation is the reference for a cycle in all timing during the following discussion.

In an operating cycle, the transaction racks transmit information from the control rows of the keyboard directly to the read-out switches. Also, through the front transmission line they position the symbol-printing type wheels and through the rear transmission line they set up control conditions for the printers and the totalizers. These control conditions determine where printing occurs and which total is selected.

The adding racks transfer amount information directly to the totalizers and set the printer racks to their corresponding digit values. The printing racks in turn set the read-out switches and position the type wheels of the printers through the front transmission line.

Before the cycle begins, the adding racks are in home position, but the printing racks and the transaction racks are at the digit positions which they occupied at the end of the previous cycle. Thus the read-out switches and the printers also retain the values of the previous message segment. At the beginning of the cycle, the transaction racks move toward their home positions and have reached their new digit positions by 95 degrees of the cycle. This permits the proper totalizer to be selected from 100 to 125 degrees of the cycle, which is before the adding racks begin the adding operation.

The printing racks also begin to return to home position at the beginning of the cycle, and the adding racks begin to move toward their new digit values. After the adding racks have reached their new digit values, they become engaged with the printing racks, which are then in home position at the rear of the machine. Between 150 degrees and 200 degrees of the cycle, the adding racks return to their home position, which is toward the front of the machine, and take with them the printing racks. During this movement between 150 and 200 degrees, the adding racks add into the engaged totalizer, and the printing racks set the amount type wheels through the front transmission line. The printing racks also set their re-
spective read-out switches. After this point, printing occurs. In addition, the read-out switches can be read at any time until the machine is cycled for another segment of information to be transmitted to or from the central data processing station.

In addition to the read-out switches described previously, a number of other different types of switches have been added to the mechanism of the window machine to permit on-line operation. Each of these switches is briefly described below. A specific description and showing of the mechanical association of each switch with the mechanism of the window machine is not provided, since the manner in which these switches are connected to the various mechanisms of the window machine would be obvious to one skilled in the art, and a showing and description of each such switch and associated mechanical structure would unnecessarily enlarge and complicate this disclosure. These switches appear in the electrical circuitry contained in this disclosure, and the manner in which they cooperate in controlling the functioning of the system will be described subsequently.

A motor switch SC41 is mounted on the window machine operating motor. This switch, when closed, completes the circuit path to operate the motor. The fall, or completion of rotation, of the key lock actuates the switch for the beginning of the machine cycle. The contacts open again at approximately 357 degrees of the cycle.

A last line switch SC54 is mounted on the "last line" bracket in the window machine and serves to energize the "last line" relay when a form in the book or validating printer reaches the last line space of that form. The switch operates through a linkage that closes the switch contacts until the last line lock of the window machine restores.

A last line release switch SC55 is mounted on the front tie bar of the window machine. This switch energizes the "last line" solenoid when the last line lock releases. Any key of the window machine keyboard that releases the last line lock closes the contacts through the zero stop control line of the window machine. The contacts of the switch SC55 reopen at approximately 243 degrees of the machine cycle.

A power switch SC91 is mounted inside the left printer frame of the window machine. This switch connects power to the machine and operates through a linkage from the control lock mechanism.

A trip switch SC502 is mounted on a bracket on the right side frame of the machine. This switch partially controls the presser shoe actuating path for the trip solenoid. It operates through a switch arm from any motorized key of the window machine keyboard. The contacts of this switch remain closed as long as the depressed key remains depressed, and subsequently release at 243 degrees of the machine cycle.

A motor link switch SC503 is mounted on the rear of the back plate of the window machine. This switch insures that there is no output flag, or signal, when the machine is cycling. It operates from a switch arm linked associated with the key lock line. The contacts of this switch operate before the main cam line begins rotation, and close again after the cam line stops its revolution.

An output mode switch SC504 is mounted on a bracket at the end of the key lock line. This switch energizes the output mode relays when the teller operating the window machine sends the account number segment to the printer. This switch operates at 100 degrees of the account number cycle of operation when the keyboard top locks. The contacts open on a cycle that restores the keyboard, such as a balance or void cycle.

An OFF-line switch SC505 is mounted on a bracket on the left printer frame of the window machine. This switch either lights the OFF LINE indicator light or partially completes a path for the ON LINE and READY lights. It operates through a linkage from the on-off line knob 135.

A remote switch SC506 is mounted on a bracket on the left printer frame of the window machine. This switch either partially completes a path for 115 volts D.C. current to the control relays during on-line operation, or partially completes a path for 115 volts D.C. current to the trip solenoid during off-line operation. It operates through a linkage from the on-off line knob in the same manner as the switch SC505.

A slip feeder switch SC508 is mounted on the base of the window machine. This switch, when its contacts are closed, lights the FORM MISSING light and opens the output flag circuit when no book is present in the book printer during a machine cycle. A feeder closes the light circuit contacts and opens the output flag contacts. The contacts of this switch restore when the teller inserts a book into the printer and cycles the machine.

A branch code switch SC509 is mounted outside the left printer frame of the machine. The switch permits the machine to automatically send a predetermined branch code when there is nothing in the two high-order amount rows of the machine during an account number operation. The Account Number key operates the contacts of this switch through a selecting plate.

An input flag switch SC520 is mounted on the recorder assembly of the window machine. This switch gates, or controls, the rise of the input flag signal. It operates through a cam arm operating from the main cam line. The contacts of this switch close at 235 degrees, and open at 260 degrees of the machine cycle.

An automatic cycle switch SC521 is mounted on a bracket on the recorder assembly of the window machine. This switch gates, or controls, the automatic trip relay and the Lamp Reset line. It is operated by the main cam line at 325 degrees and restores at 350 degrees.

An auxiliary trip switch SC522 is mounted on a bracket on the recorder assembly of the window machine. This switch prevents the trip solenoid from energizing during most of a cycle. It is operated by the main cam line, so that the contacts open at five degrees and close at 340 degrees of the machine cycle.

A trip release switch SC523 is mounted on a bracket on the recorder assembly of the window machine. This switch deenergizes the trip relays and controls the energization of the ACD drop relay. It is operated by the main cam line at five degrees and restores at 340 degrees.

A machine status switch SC524 is mounted on the recorder assembly of the window machine. This switch grounds the Lamp Reset line and switches ON LINE and READY to PARTIAL MESSAGE or PROCESSOR CONTROL. Any motorized key operates the switch in the first cycle of the transaction. The contacts restore on a cycle that restores the keyboard, such as a balance or void cycle of operation.

An overdraft trip switch SC525 is mounted on the recorder assembly of the window machine. This switch energizes the overdraft relay whenever the net value in the add-subtract totalizer is negative. It operates through a linkage associated with the add-subtract totalizer and restores when the net value of said totalizer becomes positive.

A total lock switch SC530 is mounted on the keyboard of the window machine. This switch permits the supervisor to override a "hold" condition. It is actuated through a linkage from the total mechanism.

A Re-Entry key switch SC531 is mounted on the keyboard of the window machine. This switch permits the user to override a "hold" condition. It operates from the stem of the Re-Entry key.

An Over Ride key switch SC532 is mounted on the keyboard of the window machine. This switch permits the user to override a "hold" condition. It operates from the stem of the Over Ride key.

A void key switch SC533 is mounted on the keyboard of the window machine. This switch permits the machine
to cycle in a void condition regardless of the transaction conditions unless the select gate of the window machine controller is raised. It operates from the stem of the Void key.

The auxiliary key lock line switch SC534 is mounted on the keyboard. This switch drops, or controls, the output flag signal when the teller operates a lever locked key or prevents the output flag signal from being raised until all keys are in their fully restored position. It operates through the auxiliary key lock line from the lever on the keyboard.

A fluorescent lamp switch SP540 is mounted on the keyboard instead of the window machine. This pushbutton switch turns on and off the lamp that is located over the printing table of the machine.

Located in the recorder assembly portion of the window machine, on a support 168 fixed on a plate 169 extending between the side frames 147 and 148, are a plurality of relays designated K501 to K505 inclusive, K507 to K516 inclusive, and K518 to K522 inclusive. When the window machine is operating in an on-line mode, the relays K501 to K505 inclusive, K507 to K516 inclusive, K518, K519, K521, and K522 are gated, or controlled, through the switch SC506 to a 115-volt D.C. power supply. The relay K520 has a 50-volt D.C. power supply controlled through the window machine. When the window machine is operating in the off-line mode, the relays K501 to K505 inclusive, K507 to K510 inclusive, K513 to K516 inclusive, and K518 to K522 inclusive are prevented from functioning, while the relays K511 and K512 are still connected to the 115-volt D.C. power supply.

A listing of the various relays, and their identification according to function, the contacts which they control, and the functions which these contacts perform, appears below. The manner in which these relays cooperate in the functioning of the system will be described subsequently.

**Relay Assignments**

- **K501**: Auxiliary Control Digit 1—Balance
  - K501AC1—Holding Contacts
  - K501AC2—Controls Relay K522
  - K501AC4—Controls Balance Key Solenoid
- **K502**:
  - K502AC1—Holding Contacts
  - K502AC2—Controls Relay K522
  - K502AC4—Controls Sub-Balance Key Solenoid
- **K503**:
  - K503AC1—Holding Contacts
  - K503AC2—Controls Relay K514
- **K504**:
  - K504AC1—Holding Contacts
  - K504AC2—Controls Relay K503
  - K504BC3—Contacts Relay K510
- **K505**:
  - K505AC1—Holding Contacts
  - K505BC2—Contacts Relay K510
- **K507**:
  - K507BC1—Controls Window Machine Ready Line
  - K507BC2—Controls Input Flag Signal
- **K508**:
  - K508BC1—Controls Switching Circuit for Auxiliary Control Digits 1 to 5 Inclusive Relays K501 to K505
- **K509**:
  - K509AC1—Controls Circuit for Relays K501 to K505 Inclusive
  - K509AC2—Controls Solenoid L540 (Output)
  - K509BC4—Controls Solenoid L540 (Input)
- **K510**:
  - Trip By-Pass
  - K510AC1—Controls Solenoid L540
- **K511**:
  - K511AC1—Controls FORM MISSING Lamp
  - K511BC4—Controls Window Machine Ready Line
- **K512**:
  - Overdraft
  - K512AC1—Controls OVERDRAFT Lamp

The window machine performs various functions before a transaction begins, and during the input and output phases of the transaction. Various electrical components including relays, switches, solenoids, and program boards contained in the window machine, some of which have been previously described, cooperate to enable the machine to perform these functions. In order that the circuitry which utilizes these components may best be explained, certain portions of the circuitry will now be described, after which a description will be given of the manner in which the circuitry functions during several different types of operations of the window machine.

In order to function, the window machine must be connected to a suitable source of power (a 115-volt, 60-cycle source in the illustrated embodiment) and must be set either for on-line operation or for off-line operation, according to the conditions under which the machine is to operate.

To set the window machine for off-line operation, the lock 131 (FIG. 8) for the slide 132 must be unlocked, and the slide moved to "Date Journal" position. The knob 135 is then shifted to "off" position, which causes the OFF LINE lamp in the panel 124 to be illuminated. The slide 132 is then moved to "Operate" position and locked. The Receive key of control row 1 must be used or locked down if the totalizers and printers are to operate in this off-line mode. The lock 127 is used to lock down the Receive key.

To set the window machine for on-line operation, the knob 135 is shifted to "on" position, using the same procedure described above, which causes the ON LINE indicator in the panel 124 to be illuminated. The slide 132 is then moved to "Operate" position and locked. The Receive key must not be locked down during on-line operation. It may be restored from its locked-down position by operation of the total lock 127 or the Release key 121.

The window machine power supply is shown in FIG. 11C. When the teller turns power to the window
machine by moving the slide 132 (FIG. 8) from “Locked” position, the contacts SC501B1 and SC501B2 (FIG. 11C), controlled by said slide, are closed.

Let it be assumed that the machine is operating in the off-line mode. As may be shown in FIG. 11C, the contacts SC501B1 and SC501B2 makes the 115-volt A.C. 60-cycle power applied to the plug 175 available to the circuits for the motor 176, the table light 1519, the transformer T501, and the bridge rectifier CR501. Now, when the motor switch SC41A1 is closed in a conventional operation from the plug 175 through the motor winding 174 and the motor relay 178 energizes the motor relay, causing its contacts 179 to close, completing a 115-volt A.C. path which extends from the contacts SC41A1 through the motor start winding 177 and a start capacitor 180. This capacitor then charges, causing high current to flow through the start winding 177. This short-duration high current through the start winding assists in initiating the movement of the motor armature. As the motor increases speed, the current in the motor winding 174 and in the motor relay 178 decreases. As the current decreases through the motor relay, the magnetic field decreases, and the motor relay contacts 179 open. The start winding 177 and the capacitor 180 are then removed from the motor circuit. Arcing of the motor relay contact points is suppressed by an arc suppressor 181, which functions in a conventional manner. The off-shade resistor 182 and the two-microfarad capacitor 183 are connected serially in the motor circuit in parallel with the motor windings in order to provide smoother operation.

Closure of the contacts SC501B1 and SC501B2 also prepares an illuminating circuit for the table light 1519, said circuit being from the plug 175 through the contacts SC501B1, one filament of the light 1519, the contacts SP540A1, the other filament of the light 1519, the contacts SP540A2, a ballast L501, the contacts SC501B2, and back to the plug 175. This circuit is completed by closing the contacts SP540A1 and SP540A2, which are controlled by a manually-operable button on the window machine.

Closure of the contacts SC501B1 and SC501B2 also applies 115-volt A.C. power across the primary winding 157 of the transformer T501. This transformer steps down 115-volt A.C. power to 6.3 volts A.C., which is used to supply the 6.3-volt A.C. power required for the indicator light circuits of FIG. 12A.

Closure of the contacts SC501B1 and SC501B2 also applies 115-volt A.C. power across the bridge rectifier CR501. This is a full-wave bridge rectifier which rectifies 115-volt A.C. to 115-volt D.C.

As previously mentioned, when the window machine is in the off-line mode of operation, the OFF LINE indicator is illuminated. The Form Missing and Overdraft indicators may also be illuminated. As may be seen in FIG. 12A, the secondary 183 of the transformer T501 supplies 6.3 volts A.C. potential to the indicator lamp circuits, which includes the lamps 1501 to 1518 inclusive.

In FIG. 12A, not all of these lamps are shown, the lamps 1507 to 1512 inclusive being omitted in order to conserve space, and because these lamps function in the same way as the remaining lamps which are shown.

The on-line off-line switch SC505 is actuated mechanically from the on-line off-line knob 135. The contacts SC505B2C (FIG. 12A) are closed when the machine is in the off-line mode, and a lamp circuit is then completed which extends from one side of the secondary winding 138 (FIG. 12A) of the transformer T501 through the contacts SC505B2C, and the OFF LINE lamp 1515, to the other side of the secondary winding 138 of the transformer T501. The OFF LINE lamp is illuminated so long as the on-line off-line knob 135 is in an “off” position and the control lock slide 132 is not in the “Locked” position.

The contacts of the machine status switch SC524A transfers only during a balance or void operation. These contacts remain in a transferred state until any motorized control key, other than a Balance or Void key, is used. A balance or void key causes the machine status switch contacts SC524B2 (FIG. 12A) to close. During this operation, the slip feeder mechanism in the book printer of the window machine feeds for the presence of a book. The book is normally not inserted before the balance pick-up operation, and the slip feeder switch contacts SC508B2 (FIG. 12A) therefore remain closed. This causes illumination of the FORM MISSING lamp 1517 over a circuit which extends from one side of the secondary winding 158 (FIG. 12A) through contacts SC524B2, contacts SC508B2, and through the FORM MISSING lamp 1517, to the other side of the secondary winding 158.

Following a balance pick-up operation, the teller will normally index the transaction information into the keyboard and press the appropriate transaction key. Following the transaction operation, the teller then will normally index the account number information into the keyboard, place the pass-book in the book printer of the window machine, and press the appropriate account number key. The slip feeder operates during this operation and senses the book, setting the in-feed mechanism of the window machine and opening the contacts SC508B2. The circuit to the FORM MISSING lamp 1517 will therefore open, and this lamp will be extinguished.

Let it be assumed that the teller has to make several transaction operations on the pass-book, and that the first transaction was made on line 23 of the pass-book. This series of transactions will cause a last line lock-up condition and will transfer the contacts of the last line switch SC54 (FIG. 11C). This closes the contacts SC54A1 (FIG. 11C) and completes an energizing circuit, which extends from a common 189 connected to the plus side of the rectifier CR501, over the contacts SC54A1, a conductor 190, and the relay KS11 (FIG. 11B), to a common 191 connected to the other side of the rectifier CR501. This circuit energizes the relay KS11 and causes its contacts to transfer. The contacts KS11A1C1 (FIG. 12A) in the energizing circuit for the FORM MISSING lamp 1517 close and cause said lamp to be illuminated, over a circuit which extends from one side of the secondary winding 158 (FIG. 12A) of the transformer T501 through the contacts SC524B2, the contacts KS11A1C1, and the lamp 1517, to the other side of the secondary winding 158. This causes the FORM MISSING lamp to be illuminated and provides an indication of this condition on the panel 124 of the window machine. It is then possible for the teller to sub-balance the machine, eject the form, insert a new form, and sub-balance again to relieve the last line lock-up condition that was set in the machine. During this operation, the circuit to the relay KS11 is broken when the last line switch contacts SC54A1 open, and the contacts KS11A1C1 in the FORM MISSING lamp circuit then also open, causing the FORM MISSING lamp 1517 to be extinguished.

Should an overdraft condition arise during the posting of an account by the window machine, the OVERDRAFT lamp 1506 will be illuminated. In an overdraft condition of the machine, the overdraft trip line (not shown) is tripped, and an arm (not shown) on said line moves away from the overdraft trip switch SC525, allowing the contacts SC525B1 (FIG. 11B) to close, which completes a circuit extending from the second rectifier CR501 over the common 189, a conductor 192, the contacts SC525C1, the overdraft relay KS12, and the common 191, to the other side of the rectifier CR501. This energizes the relay KS12, and causes the contacts KS12A1C1 (FIG. 12A) to close. Closure of these contacts completes a circuit which extends from one side of the secondary winding 158 (FIG. 12A) of the transformer T501, over the contacts KS12A1C1, and the OVERDRAFT lamp 1506, to the other side of the secondary winding 158.
winding 188, to illuminate said OVERDRAFT lamp and thus provide a visual indication to the operator of the window machine that an overdraft condition exists.

In an off-line mode of operation, the window machine is tripped to initiate a cycle of operation when a motorized control key is depressed. This tripping of the machine is effected by energization of the trip solenoid L540 (FIG. 11C). Depression of any motorized key causes the trip switch SC502 to actuate so that the contacts SC502A1C1 are closed. This completes an energizing circuit which extends from one side of the rectifier CR500 over the common 189, the contacts SC506B1C1, the solenoid LS40, the closed contacts SC522A1 of the auxiliary trip switch SC502, and the common 191, to the other side of the rectifier CR501.

Energization of the solenoid LS40 causes a release pawl (not shown) to be moved, by means of linkage connecting the solenoid with the release pawl, from the path of the release arm (not shown), which permits the key lock line of the window machine to trip, to commence a cycle of operation of the window machine.

When the window machine is posting on the last line of an account book, the machine lock mechanism will be operated by the last line feeler, and the machine lock arm will be moved and will prevent the tripping of the machine for a cycle of operation. The last line switch SC54A1 will also be closed. The Over Ride and Sub Balance keys will operate the window machine in the last line condition but will not cause the book to be ejected. The Void, Eject, and Balance keys will operate the machine and will cause the book to be ejected. When the last line condition exists and any of these five control keys are used, the contacts SC54A1 of the last line switch LS45 are opened, causing the last line solenoid LS42 (FIG. 11C) to be energized. The energizing path extends from one side of the rectifier CR501 over the common 189, the contacts SC55A1, the solenoid LS42, and the common 191 to the other side of the rectifier CR501. When the solenoid LS42 is energized, the mechanical interference with the key lock line of the window machine is removed, and the key lock line is then free to move, to initiate a cycle of operation of the window machine.

As has been previously described, when the window machine is to be operated in the on-line mode, the knob 135 (FIG. 8) is moved to its “on” position, which actuates the on-line switch SC505 and the remote switch SC506 to close the contacts SC505A2C2, SC506A1C1, and SC506A2C2. The contacts SC506A1C1 (FIG. 11C), when closed, prepare the energizing circuits for the relays K501 to K516 inclusive, K518, to K519, K521, and K522, as well as the circuit to the associated window machine controller 110 (FIG. 1).

When the entire system is functioning in an on-line mode, the ON LINE indicator in the panel 124 of the window machine is illuminated. This is effected by illumination of the ON LINE lamp 1513 (FIG. 12A) over a circuit which extends from one side of the secondary winding 188 of the transformer T501, over the contacts SC505A2C2 and the lamp 1513, to the other side of the secondary winding 188.

The FORM MISSING lamp 1517 is illuminated when a form missing from its proper location in association with the appropriate printer of the window machine in the same manner in an on-line mode of operation, as has been previously described in connection with the off-line mode of operation. Reference may accordingly be had to the previous description of the energizing circuit for the Form Missing lamp for an explanation of how and when this lamp is illuminated in an on-line mode of operation.

The READY lamp 1514, when illuminated, indicates that the window machine add-subtract totalizer has been cleared to the top, and that the proper condition to have an input entry indexed thereon by a teller. The window machine status switch SC524 is actuated only after a balance or void operation of the window machine, and its contacts SC524A1C3 are closed at such a time. The system on relay K208 in the window machine controller associated with the window machine is energized at this time, and the contacts K208A1C1 are closed. With the status switch SC524 actuated, and the system in an "on" condition, the READY lamp is illuminated to provide an appropriate indication on the panel 124 of the window machine.

The energizing circuit for the lamp 1514 extends from one side of the secondary winding 188 (FIG. 12A) of the transformer T501, over the contacts SC505A2C2, to a terminal 195, which is connected to a corresponding terminal 193 (FIG. 19) in the associated window machine controller 110, over contacts K208A1C1 in the associated window machine controller 110, to a terminal 194, which is connected to a terminal 196 (FIG. 12A) in the window machine, over the contacts SC524A3C3, and the READY lamp 1514 will remain illuminated until such time as the machine status switch SC524 is not actuated in a machine cycle of operation, which takes place after the first input segment is transmitted from the window machine.

The PARTIAL MESSAGE lamp 1516 is used to indicate that the teller has initiated a segment using any motorized control key other than Balance, Void, or Account Number. It also indicates that one or more input segments have been transmitted. The machine status switch SC524 contacts will transfer when any motorized key other than Balance, Void, or Account Number is used, and the contacts SC524A3C3 will close. With the system on contacts, which are controlled by the relay K208 in the controller 110, closed, and with the contacts SC524A3C3 closed, the PARTIAL MESSAGE lamp 1516 will be illuminated and will provide appropriate indication on the panel 124 of the window machine. The energizing circuit for this lamp extends from one side of the secondary winding 188 (FIG. 12A) of the transformer T501 over the contacts SC505A2C2, the terminal 195, the terminal 193, the contacts K208A1C1 in the controller 110, the terminal 194, the terminal 196, the contacts SC524A3C3, the contacts K519B1C1, and the lamp 1516, to the other side of the winding 188. The lamp 1516 remains in an on condition until a void or account number operation of the window machine takes place.

The PROCESSOR CONTROL lamp 1518 is used to indicate that an account number operation has been made and that the window machine is in an output mode, waiting for the output segment or segments from the processor. The PROCESSOR CONTROL indication appears in the panel 124 of the window machine. This indication also lets the teller know that the lamp 1518 is not available for use and is mechanically locked out to prevent teller interference. The contacts SC524B3C3 of the machine status switch SC524 are closed at this time, as previously described in connection with the PARTIAL MESSAGE lamp 1516.

During the cycle of operation of the window machine in an account number operation, the output mode switch SC504 transfers at approximately 205 degrees of cam line rotation, closing the contacts SC504B1C1 (FIG. 11B). These contacts remain closed until a balance or void operation takes place. When these contacts are energized, the relay K519 (FIG. 11B) is energized over a circuit which extends from the rectifier CR501 (FIG. 11C) over the common 189, the contacts SC506A1C1, the common 189, the contacts SC504B1C1, the relay K519, and the common 191, to the other side of the rectifier CR501.

The energizer of the relay K519 causes the contacts K519B1C1 (FIG. 12A) to close, and the contacts K519B1C1 (FIG. 12A) to open. It will be recalled that the contacts K519B1C1 are in the energizing circuit for the PROCESSOR CONTROL lamp 1518, and their closer condition is the proper indication for that lamp. This circuit extends from one side of the secondary winding 188 of the transformer T501 over the contacts SC505A2C2, the terminal 195, the terminal 193,
the contacts K208AC1 in the controller 110, the terminal 194, the terminal 196, the contacts SC524BC3, the contacts K519AC1, and the lamp 1518, to the other side of the winding 188. This illuminates the PROCESSOR CONTROL lamp 1518, which remains illuminated until a void or balance operation of the window machine takes place. Indicator lamps 1501 to 1506 inclusive (FIG. 12A) are located to illuminate the SEND ERROR, ENTRY ERROR, RECEIVE, ERROR UPDATE, REFER, and OVERDRAFT indicators, respectively, in the panel 125 of the window machine controller. A buzzer 197 is connected in parallel with the ERROR UPDATE lamp 1504 and emits a sound audible to the machine operator when the lamp 1594 is illuminated. The OVERDRAFT lamp 1506 can be illuminated in an on-line mode of operation from the central processor, as well as in the off-line mode, as previously described. Each of these lamps has one side of its filament connected to one side of the secondary winding 188 of the transformer T501, while the other side of the filament is connected to one of the terminals 201, 202, 203, 204, 205, and 206, respectively, which terminal, in turn, is connected to a corresponding terminal in the associated window machine controller 110. A circuit extends from the corresponding terminals in the window machine controller 110 through a series, or “tree,” of contacts of a group of relays in the controller 110 (FIG. 19), over the contacts 110, the terminal 195 (FIG. 12A), and the contacts SC505SC2, to the other side of the secondary winding 188.

Signals on these terminals for selective illumination of these lamps are provided by the energization of selected ones of the relays in the associated window machine controller 110, under control of the branch remote controller 108 and the central processor, as will be described subsequently. For example, if the central processor has sent a signal to illuminate the REFER relay 1505, a current path is completed from one side of the secondary winding 188 over the contacts SC505AC2, the terminal 195, a corresponding terminal in the window machine controller 110, a path through certain contacts of the relays described above, a second terminal in the window machine controller 110, the terminal 205, and the lamp 1505, to the other side of the winding 188. This causes the lamp 1505 to be illuminated.

Not specifically shown in FIG. 12A or 12B, but also included in the illustrated embodiment of the present invention, are a plurality of lamps 1507 to 1512 inclusive. Captions for these lamps are normally located in the panel 126 of the window machine 109 and are assigned to indicate particular account status conditions which the bank using the system may require. Illumination of these six lamps is accomplished in the same manner as the illumination of the lamps 1501 to 1506 inclusive, through combinations of relay contacts in the associated window machine controller 110.

OPERATION OF WINDOW MACHINE CIRCUITY

In order best to describe certain aspects of the operating circuitry of the input-output device, or window machine, certain typical on-line operations of said device will now be described.

A first such on-line operation is a balance pick-up operation, which constitutes an input of data to the central data processing station from the window machine. To make such an operation, the window machine tiler indexes a passbook to a page on which is presented to him by an account holder into the window machine via the window machine keyboard, and then depresses the Balance Pick Up key of the window machine. This causes the trip solenoid L540 to be energized over a circuit which extends from the plus side of the rectifier CR501 (FIG. 11C) over the common 139; the contacts SC506AC1; K509BC4; K513BC2; SC506AC2; the solenoid L540; the contacts SC522AC2; controlled by the auxiliary trip switch, and closed at this time; the contacts SC502AC1, controlled to be closed by the depression of any motorized control key; and the common 191, to the minus side of the rectifier CR501.

Energy flow of the solenoid L540 causes initiation of a cycle of operation of the window machine. At five degrees of rotation of the main cam line of the window machine, the contacts SC522AC2 open and break the energizing circuit for the solenoid L540 until the contacts SC522AC2 again close at 340 degrees of rotation of said cam line.

During this machine cycle, the input mode relay K513 (FIG. 11B) and the auxiliary input mode relay K507 (FIG. 11A) are energized over a circuit which extends from the plus side of the rectifier CR501 over the common 189; a terminal 214 (FIG. 11A) and a corresponding terminal 215 (FIG. 18) in the window machine controller; the closed contacts K107BC1; over a terminal 216 in the controller and a corresponding terminal 217 (FIG. 12B) in the window machine operating circuitry; the wiper of switch SR501B set to position 1X (said switch being associated with the control row 1 and being set at position 1X when no key in that control row is depressed); the wiper of switch SR502B set to position 1 (said switch being associated with control row 2 and being set to position 1 when the Balance Pick Up key in control row 2 is depressed); over a connector 219 (FIGS. 11B and 12B) in the controller 110, the terminal 195 (FIG. 12A), and the contacts SC502AC1, which close at 235 degrees of the machine cycle and open at 260 degrees of said cycle; over the input mode relay K513 and the auxiliary input mode relay K507, in parallel; and over the common 191 to the other side of the rectifier CR501.

During the operation such that the contacts SC520A1 are closed, the relays K507 and K513 are energized. This causes the contacts K513AC1, controlled by the relay K513, to close and to provide a holding circuit for maintaining the relays K507 and K513 in energized condition. This holding circuit is identical to the energizing circuit previously described, except that the contacts K513AC1 are employed in this circuit, said contacts being in parallel with the contacts SC520A1, as may readily be seen in FIG. 11B. Energization of the relay K513 also causes the contacts K513BC2 (FIG. 11C) to open, thus preventing the trip solenoid L540 from energizing again during this input segment. The contacts K507AC2 (FIG. 11A) also close to complete the input flag circuit, which extends through the circuitry of the window machine and the window machine controller. This circuit comprises two lines in the branch system, which lines are coupled by the contacts K507AC2 when closed. The remote controller in the branch can then send a signal through the input flag Ready Interrogate line to cause the scan counter in the remote controller to stop, as will subsequently be described in detail. The input select gate relays in the window machine controller are then energized, completing digit line circuits between the remote controller and the rotary read-out switches of the window machine.

As has been previously described, there are fourteen rotary switch assemblies in the illustrated embodiment of the window machine, including ten switch assemblies for the amount rows, each containing a single switch, and four switch assemblies for the four control rows, each containing three rotary switches. It will be recalled that the rotary switches are positioned by the racks in the various rows.

In an input operation, the remote controller 108 senses the rows sequentially by selecting one row at a time under control of a row counter in the remote controller, as will be described subsequently. As each row is selected by the row counter, a circuit is completed which extends from a base reference potential, which may be ground, in the remote controller, through the selected row through the window machine controller 110, to the wiper of, or common, of the rotary switch for the selected row, said rotary switches being shown in the operating circuitry
of FIGS. 12A and 12B. The wiper of the selected rotary switch will be in one of eleven available positions (0 to 9 inclusive and "eliminate," with the twelfth position of the switch not being utilized), according to the information indexed into the window machine keyboard.

The circuit continues from the selected contact position of the selected rotary switch over the corresponding digit line 167, through the program board TB501 (FIG. 14) back to a corresponding digit line in the window machine controller TB502. The digit lines in the window machine controller TB502 correspond to the positions previously described, and also to a decimal-to-binary encoder in the remote controller 108. The decimal digit information for that row is then converted to binary information and transmitted to the central processing station, as will be described subsequently.

The remote controller 108 also senses the window machine number from the window machine 109. The row counter in the remote controller has two counts, which select the tens window machine number select line and the units window machine number select line. The select tens and units machine number lines are connected to the position E11 and H11, respectively, of the program board TB501. In the example shown in broken lines in FIG. 14, of the jumper wires effecting this number selection, a number 15 will be read out.

The read-out of the fourteen row switches and the twodigit programmed window machine number constitutes sixteen of the digits of the input segment shown in FIG. 3 and previously described.

The remote controller 108 transmits this balance pick-up segment to the central data processing station. An Input OK signal is sent from the central station, indicating that the segment was received correctly and OK. The remote controller now sends an Input OK signal to the window machine controller 110. The Input OK signal in the window machine controller 110 energizes the end-of-segment relay K107 (FIG. 16B). The contacts K107BC1 (FIG. 18) then open and break the 115-volt D.C. path to the input mode relays K507 and K513 (FIGS. 11A and 11B) in the window machine operating circuitry.

The energization of the relay K507 causes its contacts K507AC2, connecting the input flag Ready Interrogate gate line to the input flag Answer Ready line, to open, thus terminating the window machine input flag circuit. The PARTIAL MESSAGE lamp IS16 and the FORM MISSING indicator lamp IS17 are illuminated.

TRANSACTION OPERATION (A DEPOSIT OPERATION)

Following the balance pick-up operation and the return of an input OK signal from the central processing station, the teller indexes the amount of the transaction to the transaction operation on the window machine keyboard. The window machine is caused to trip by energization of the solenoid LS40, as was described in connection with the balance pick-up operation. The input mode relays K507 and K513 are again energized when the input flag switch contacts SC520A1 close, as described in connection with the balance pick-up operation.

The energizing circuit for the relays K507 and K513 extends from the plus side of the rectifier CR501 (FIG. 11C) over the common 189; the terminal 214 (FIG. 11A) and the corresponding terminal 215 (FIG. 18) in the window machine controller; over contacts K107BC1 in the window machine controller 110; over the terminal 216 in the controller and the corresponding terminal 217 (FIG. 12B) in the window machine operating circuitry; the wiper of switch SR502B to position 1X (said switch being associated with control row 1 and being set to position 1X when no key is depressed); the wiper of switch SR502B set to position 2X (said switch being associated with control row 2 and being set to position 2X during this operation); the wiper of switch SR503B set to position 9 (said switch being associated with control row 3 and being set to position 9 by depression of the A deposit key); over a connector 219 (FIGS. 11B and 12B); over the input flag switch contacts SC520A1, which close at 235 degrees of the machine cycle and open at 260 degrees of the machine cycle; over the input mode relay K513 and the auxiliary input mode relay K507 in parallel; and over the common 191 to the other side of the rectifier CR501.

The contacts K513AC1 (FIG. 11B) close to provide a holding circuit for the input mode relays K507 and K513.

The contacts K513BC2 in the trip solenoid circuit for energization of the solenoid SR503B, when the indicator said solenoid from energizing. The input flag is again completed by closing of the contacts K507AC2 to couple the input flag Ready Interrogate line to the input flag Answer Ready line.

The remote controller then is once more maintained in connection with this window machine, when said window machine is pulsed by the scan counter. The input select gate in the window machine controller is closed, as will subsequently be described, completing the digit line circuits. The second input segment is now read from the rotary read-out switches in the window machine, through the program board, in the same manner as previously described.

When the window machine controller receives the Input OK signal from the remote controller, the relay K107, which is the end of segment relay in the window machine controller, is once more energized, causing the contacts K107BC1 (FIG. 18) to open and break the 115-volt D.C. supply to the input mode relays K507 and K513. The input flag circuit then opens, and the inhibition of the trip solenoid energizing circuit is removed by closing of the contacts K513BC2. The PARTIAL MESSAGE indicator lamp IS16 and the FORM MISSING indicator lamp IS17 (FIG. 12A) are illuminated.

ACCOUNT NUMBER OPERATION (A ACCOUNT NUMBER)

An account number operation is an input operation which provides an indication of "end of message" to the central data processing station, and which prepares the window machine to receive an output message from the central data processing station.

To commence an account number operation, the teller indexes the account number on the window machine keyboard, inserts the account holder's pass-book in the book printer of the window machine on the desired print line, and depresses one of the Account Number keys, such as the A Account Number key K540.

Depression of this key causes the solenoid LS40 to be energized, in the same manner as previously described, to initiate an operation of the window machine. The input mode relay K513 and the auxiliary input mode relay K507 are energized once again when the input mode switch contacts SC520A1 close. The energizing path for these relays extends from the plus side of the rectifier CR501 (FIG. 11C) over the common 189; over the terminal 214 (FIG. 11A) and a corresponding terminal 215 (FIG. 18) in the window machine controller; over contacts K107BC1 in the window machine controller 110; over the terminal 216 in the controller and the corresponding terminal 217 (FIG. 12B) in the window machine operating circuitry; the wiper of switch SR501B set to position 1X (said switch being associated with control row 1 and being set to position 1X when no key is depressed); the
wiper of switch SR502B set to position 7 (said switch being associated with control row 2 and being set to position 7 when the A Account Number key is depressed); over the connector 212 (FIG. 11B and 12B); over the input flag switch contacts SC520A1, which close at 235 degrees of the machine cycle and open at 260 degrees of the machine cycle; over the input mode relay K513 and the auxiliary input mode relay K507 in parallel; and over the common 191 to the other side of the rectifier CR501. The relays K507 and K513 are energized over the circuit described above and complete the input flat circuit and inhibit the trip circuit, as in the previous descriptions. In addition, a holding circuit for these relays is completed, as has been previously described.

During this account number operation, the branch code switch SC509 is actuated at approximately 135 degrees of rotation of the main cam line by a transaction row 2 selecting pawl pitman (not shown) that is moved to feel a low spot in the account number positions of a selecting plate in the window machine, in a manner which is conventional. A stud on this pitman acts to close the contacts SC509A1 (FIG. 14) and SC509A2 (FIG. 14) of the branch code switch SC509. Let it be assumed that in this account number operation there are no keys depressed in amount rows 9 or 8, thus the account number being processed belongs to the branch at which it is being processed. When these two amount rows are sensed by the remote controller, a previously programmed branch code number is read out and transmitted to the remote controller, and from there to the central data processing station. The read-out circuit extends over the same path as previously described, from the row counter of the remote controller, through the window machine controller, to the wiper of the selector switch SR513A1 (FIG. 12A) associated with amount row 1 of the window machine. This wiper is set to the "eliminate" position, since no key is depressed in that row of the keyboard. The circuit extends from the "eliminate" contact position of the switch SR513A1 over a connector 221 (FIGS. 12A and 14) to the branch code switch contacts SC509AC2, which are now closed, to the position A11 of the program board TB501. A jumper wire (not shown) is used to connect the position A11 to a desired position in row A of the program board TB501 to provide the tens digit for the branch code number. The circuit continues over this jumper wire, and then over the corresponding digit line, through the controller, to the machine accumulator back to the decimal-to-binary encoder in the remote controller. From here, the information is transmitted to the central data processing station.

Amount row 8 is read out in the same manner as described above, for amount row 9, with the circuit extending from the "eliminate" contact position of the switch SR512A over a connector 222 and the closed branch code switch contacts SC509AC1 to the position C11 of the board TB501, in order to sense the programmed units digit for the branch code number of the branch in which the window machine being interrogated is located.

The programmed branch code number in an account number operation will not be read out in the above-described manner if amount keys in amount rows 9 and 8 are depressed. This feature gives the window machine teller the ability to index a branch code number of a branch in amount rows 8 and 9 when the branch at which the account is being processed is not the branch that issued the pass-book. In such a case, it will be seen that the wiper for the rotary switch for amount row 8, and the wiper for the rotary switch for amount row 9, are both positioned to the digits corresponding to the depressed keys on the window machine keyboard, and the read-out of these switches is then carried out in a normal manner to provide the branch code number to the central data processing station.

The remainder of the amount read-out switches on which the account number information is stored are sensed in a conventional manner.

During this account number operation of the system, the window machine is also being conditioned for an output mode, in preparation for receiving information from the central data processing station. As previously mentioned, the account book of the account being processed is in the printer of the window machine. Also, at approximately 295 degrees of rotation of the cam line of the window machine during the account number operation, the keyboard is top-locked against teller interference by means of the mechanism described in the previously cited United States patent application Ser. No. 308,382. In addition, during the operation of the system for transmitting the account number data to the central processing station, the processor control lamp 1518 of the window machine is illuminated. As the "top lock" mechanism of the window machine is actuated, the armature of the output mode switch SC504 is moved, causing its contact to open. When the contacts SC504BC1 (FIG. 11B) close, the output mode relays K509 and K519 are energized.

The current path to energize the relays K509 and K519 extends from the plus side of the rectifier CR501 (FIG. 11C) over the common 189; the contacts SC509AC1, a continuation of the common 189; the contacts SC504BC1; the relays K509 and K519 in parallel; and the common 191, back to the negative side of the rectifier CR501.

Energization of the output mode relay K509 causes contacts controlled thereby to transfer. The contacts K509AC4 (FIG. 11C) close, to prepare the trip circuit for the solenoid 1540 for automatic trip operation, while the contacts K509BC4 (FIG. 11C) open to interrupt an alternate path in that circuit. The contacts K509AC1 (FIG. 11A) close to prepare an energizing circuit for the five automatic cycle digit relays K501, K502, K503, K504, and K505.

The energization of the auxiliary output mode relay K519 causes its contacts to transfer. The contacts K519AC1 (FIG. 12A) close to illuminate the PROCESSOR CONTROL lamp 1518. The contacts K519BC1 (FIG. 12A) close to extinguish the PARTIAL MESSAGE lamp 1517. The contacts K519AC4 (FIG. 15) close to prepare the output flag circuit for completion of a path therefrom.

When the window machine controller receives the Input OK signal for the account number message segment, the end of segment relay K107 in the control circuit is energized. This causes the contacts K107BC1 to open, thus deenergizing the relays K507 and K513. The contacts K513BC2, controlled by the relay K513, close and remove the interruption in the energizing circuit for the trip solenoid 1540 (FIG. 11C). Also, as the relay K507 is deenergized, the contacts K507BC1 (FIG. 15) close in the output flag circuit.

The output flag circuit is utilized in output operations of the system, in which information from the central processing station is transmitted to the individual window machines. It is therefore necessary that this circuit be conditioned for operation prior to the commencement of an output operation. That portion of the output flag circuit in the window machine operating circuitry is shown in FIG. 15 and extends between terminals 223 and 224. The circuit at this time is completed over the path shown in FIG. 15 which includes the contacts K521B1, which are controlled by the trip relay K521, and which are closed at this time, since said relay is not energized; the contacts K519AC4, controlled by the auxiliary output mode relay K519, which are also closed at this time, since said relay is not energized; the contacts K507BC1, controlled by the auxiliary input mode relay K507, and which are closed at this time, since said relay is not energized; the contacts SC534AC1, which are
part of the auxiliary key lock switch and which are closed in the top lock operation of the keyboard; the contacts SC50B2, controlled by the total lock switch SC509 and not containing the contacts K511B4, controlled by the last line relay K511 and closed at this time; the contacts SC50A1A, controlled by the slip feeder switch SC508 and closed when an account book is in the printer of the window machine; the contacts SC503A1C, controlled by the motor links switch SC503 and not containing the contacts K511B4, controlled by the last line relay K511 and closed at this time; the contacts SC505A1C, controlled by the on-off line switch and closed in the on-line mode; to the terminal 224. It will be noted in the circuit that the contacts SC507A1C are also shown. These contacts are controlled by the slip feeder mechanism for the ledger card or similar document, which may be placed in the corresponding printer in the window machine. As is shown in Fig. 15, these contacts are not connected into the circuit, but may be connected into the circuit if desired, in series with the contacts SC508A1C. Also shown in Fig. 15, in parallel with the contacts SC508A1C, are contacts ST510A2, which are employed for test purposes when it is desired to operate the system without a book being inserted in any of the window machine printers. These contacts can then be closed and will effectively by-pass the contacts SC508A1C. In addition, it will be noted that two terminals, 165 and 166, connecting to terminals 165 and 166 in the program board TB501 shown in Fig. 14, are connected to the circuit in Fig. 15. These terminals are employed so that the contacts SC508A1C can also be by-passed simply by placing a jumper wire between positions D12 and J12 in the program board TB501. This expedient may be employed when the system is being serviced, and it is not desired to have to close any of the contacts previously mentioned, namely, SC507A1C, SC508A1C, or ST510A2. It will also be noted that contacts K518A1C are provided in parallel with the combination of the contacts K511B4 and ST510A2. These contacts are controlled by the auxiliary re-entry relay K518, to by-pass the combination of the contacts K511B4 and SC508A1C in suitable circumstances.

With the output flag circuit completed between the terminals 223 and 224, the system is now conditioned for an output operation, which will next be described.

OUTPUT OPERATION

The central processor 102 can only transmit output information to a window machine which has requested information via input segments, and which is in an output operation mode.

The central processor compares the balance pick-up information transmitted by the window machine to the processor with the balance in the file for that particular account. If the balances do not agree, the processor then examines the account file for items which have not been posted to the account pass-book, such as interest, no book, and error update items. When unposted items are to be posted to the pass-book, the processor makes the necessary computations to determine the validity of the pass-book balance. If the manipulated balance agrees, the processor then initiates output segments to the window machine. The first output segment or segments contain the unposted item or items, information to cause depression of the Receive key, and an Automatic Sub-Balance signal. When the pass-book has been updated with these items, the processor then transmits an output message segment containing the present position and an Automatic Balance signal. The processor posts information contained in particular segments to the account file prior to transmission of the information contained in these segments to the window machine, but has the facility to correct this posting as to any segment or segments which may not be successfully transmitted to the window machine via output messages.

If the balance from the pass-book agrees with the balance in the account file, the processor sends an output segment to the window machine. This segment contains a current transaction, the Receive key signal, and an Automatic Balance signal. The output segment represents the current transaction to be automatically indexed into the key-board and also causes the Receive key to be pulled down. The Receive key selects the totalizers and printers to operate, and causes the transaction to be recorded on the pass-book and in the totalizers when a trip signal is sent to the window machine closed at this time. The add-subtract totalizer is then engaged, and the transaction is added to the balance pick-up information in the add-subtract totalizer, and into the transaction totalizer. The auxiliary control digit (1) in the output segment causes the window machine to prepare to automatically balance following the output transaction operation.

A typical output operation will now be described with reference to the manner in which the window machine functions during such an operation. For purposes of illustration, it will be assumed that the window machine is in the "on-line" mode, ready for an output operation, with the account pass-book in the book printer of the window machine. It will also be assumed that the previous input operation from the window machine for the account being processed included a balance pick-up of $20.00; an "A" deposit entry of $6.00; and an "A" account number entry of No. 061. It follows that the account file balance and the pass-book balance agree.

In response to the input information pertaining to the account which was transmitted from the window machine to the central processor 101 in preceding input message segments, the processor will transmit to the window machine an output message segment to cause an "A" deposit entry of $6.00 to be made by the window machine on the pass-book.

This information is transmitted from the central processing station 101 (Fig. 1) to the remote controller 108, which is in the system branch, and is receiving by the remote controller 108 to the window machine 109 processing the account, through the associated remote controller 110.

The remote controller selects the appropriate window machine by applying a signal to the appropriate Window Machine Select line JWM101 to JWM116 (Fig. 17A). This causes energization of the relays K301 to K308 inclusive and K310 in the associated window machine controller, as previously described, to close the contacts controlled by said relays to connect the row and digit select lines to the row and digit drive lines. It also causes a signal to be returned to the remote controller 108, which is connected to the Window Machine Ready line JWM101 (Fig. 17A) over the output flag circuit of Fig. 15, from the Window Machine Ready Interrogate line JMI100 (Fig. 17B); and causes a signal to be returned to the remote controller on the Window Machine On-Line JWI102 (Fig. 17A), as has been previously described.

With these signals received by the remote controller, the row counter therein will be advanced each seven milliseconds, as will be described, until a significant digit is received in the output message segment. In the illustrative example, the first significant digit to be received in the output message segment is a "6" in the "dollars" row (which is the seventh keyboard row from the right side of the machine, as viewed from above). Reference to the output message segment chart of Fig. 4 discloses that this is in digit position 9 of the output message segment. It may be noted that any digit greater than 0 in the output message segment is followed by six "No Data" characters (see Fig. 6), which allows a total of forty-nine milliseconds for a key solenoid to be actuated.

As will now be described in greater detail, the remote controller 108 now causes the simultaneous firing of the row 7 solenoid driver and the digit six solenoid grunder simultaneously. A completed circuit is maintained for forty-nine milliseconds to cause the key solenoid to be energized, and 50-volt D.C. power is thus applied to the $6.00 key solenoid L76 (Fig. 13), causing the solenoid...
plunger to be pulled downwardly, depressing the $6.00 key.

The energizing circuit for the solenoid L16 is from a plus 50-volt D.C. source in the remote controller 108 over the Select Row 7 line JW1127 (FIG. 17A); the contacts K302A/C4 (FIG. 17B); the Row 7 Drive line JM1127; a terminal 240 on the board TB29 (FIG. 13), which is common to all key solenoids in row 7; a diode CR506; a solenoid L16; a common return to a terminal 241 on a board TB29; the Digit 6 Drive line JM1146 (FIG. 17B); the contacts K308AC4; and the Select Digit 6 line JW1146 (FIG. 17A) to a return to the Digit 6 solenoid grounder in the remote controller 108.

The next digit to be received is a one in position 13 of the output message segment (FIG. 4). This causes the window machine to prepare to balance automatically following this output operation. The binary-coded auxiliary control digit is sent from the remote controller to the selected window machine controller on the three Auxiliary Control Bit lines JW1160, JW1161, and JW1162 (FIG. 16A) in position 13 of the output message segment. The auxiliary control bit relays K101, K102, and K103 (FIG. 16A) are energized in accordance with the signals received in the corresponding line, and the contacts controlled by said relays, arranged in a decoding network shown in FIG. 18, close in accordance with the signals received to complete a 115-volt D.C. circuit, and also complete several Auxiliary Control Digit lines JM1161 to JM1167 inclusive.

In this example, the Auxiliary Control Digit No. 1 line JM1161 has 115 volts D.C. power supplied to it, and causes energization of the relay K501 (FIG. 11A) in the electrical circuitry of the window machine over a circuit which extends from the line JM1161 over a terminal 242 (FIG. 11A); the relay K501; contacts K509AC1; contacts K508BC1; contacts K520BC1; and the common 191 to the minus side of the rectifier CR501 (FIG. 11C).

Energization of the relay K501 causes the contacts K501A/C1 (FIG. 11A) to close and provide a holding path for maintaining the relay K501 energized, which path extends from the common 189 through the contacts K501A/C1 and the relay K501, over the contacts K509AC1, K508BC1, K529BC1, and the common 191, back to the rectifier CR501.

K501A/C2 (FIG. 11C) also close upon energization of the relay K501 and prepare an energizing circuit for energization of the automatic trip relay K522.

In addition, the contacts K501A/C4 (FIG. 13) close upon energization of the relay K501 and prepare an energizing circuit for energization of the balance key solenoid L11.

The next significant character to be received by the window machine in this output message segment is a digit 8 in output message segment position 15, which energizes the Receive key solenoid L18 to depress the Receive key in Row 1 of the window machine keyboard.

The energizing circuit for the solenoid L18 extends from a plus 50-volt D.C. source in the remote controller 108 over the Select Row 1 line JW1121 (FIG. 17A); the contacts K301AC2; the Row 1 drive line JM1121; terminal 243 of Board TB21, which is common to all Row 1 key solenoids; a diode CR18; the solenoid L18; a common return to a terminal 244 on the board TB20; the Digit 8 Drive line JM1148 (FIG. 17B); the contacts K306AC2; and the Select Digit 8 line JW1148 (FIG. 17A); to a return to the digit 8 solenoid grounder in the remote controller 108.

During the forty-nine milliseconds that the Receive key solenoid circuit is complete, current flows from a plus 50-volt D.C. supply in the remote controller through the arc suppression diode CR18, through the Receive key solenoid L18, to ground in the remote controller; this is described above. The Receive key solenoid is thus effective to depress the Receive key of the accounting machine keyboard in control row 1.

In the illustrated example, since no key is to be depressed in row 2 of the accounting machine keyboard, position 16 of the output message segment is zero, and the duration of its signal is only seven milliseconds.

In position 17 of the output message segment, relating to control row 3, a digit nine is contained, which will cause the A Deposit key to be depressed in the same manner as has been previously described for the other keys of the keyboard in the illustrated example. The A Deposit key is a motorized transaction key. When this key is depressed, the trip switch contacts SC506AC1 (FIG. 11C) are closed to complete a portion of the operating circuit for the trip solenoid L540. It may be noted that at this time the relay K509 is energized, and the relay K513 is deenergized. It may also be noted that the auxiliary trip switch SC522A1 is closed at home position.

When the output message is checked and found to be OK by checking circuitry in the remote controller, an "Output OK" signal is sent to the central data processing station 101, and a Trip signal is sent over line JW1190 (FIG. 16A) to the window machine controller 110. This Trip signal is sent to a circuit extending from the line JM1190 over the relay contacts K310AC2 and the relay K204 to a minus 20-volt D.C. potential source, and energizes the relay K204 in the window machine controller. Energization of the relay K204 causes the contacts K204AC1 (FIG. 18) to close, which completes a circuit for energizing the auxiliary trip relay K516 and the trip relay K521 in the window machine operating circuitry. This energizing circuit extends from a source of 115-volt D.C. potential applied at the terminal 216 of FIG. 18, over the contacts K204AC1; to the trip line JM1190; over a terminal 245 in the window machine controller circuitry; a corresponding terminal 246 in the window machine circuitry (FIG. 11B); over the relays K516 and K521 in parallel; and over the common 191, to the negative side of the rectifier CR501, thus energizing the relays K516 and K521.

Energization of the relays K516 and K521 causes the contacts K516AC1 and K521A/C2 (FIG. 11B) to close, to complete holding circuits for the relays K516 and K521, said holding circuits extending from the common 189 over the contacts SC523A1, the contacts K516AC1 and K521A/C2 in parallel, and the relays K516 and K521 in parallel, to the negative common 191.

Energization of the relays K516 and K521 also causes the contacts K516BC4 and K521B/C1 (FIG. 15) to open in the output flag circuit. Should the remote controller now attempt to transmit an output message, this open circuit will indicate "busy" and that the machine is not in condition to receive an output message.

In addition, energization of the relays K516 and K521 causes the contacts K516AC2 and K521A/C3 to close to complete the circuit for energizing the trip solenoid L540 (FIG. 11C). This circuit extends from the positive common 189 over the contacts SC506AC1; the contacts K509AC4; the contacts K516AC2 and K521A/C3 in parallel; and the contacts K513BC2; the contacts SC506AC2; the trip solenoid L540; the contacts SC522A1; and the contacts SC502AC1, to the negative common 191.

Energization of the window machine trip solenoid L540 is effective to cause the window machine to be tripped to commence the output transaction operation ("A" Deposit, $6.00).

During the operation of the window machine, at five degrees of rotation of the cam line, the trip release switch contacts SC523A1 (FIG. 11B) open and break the holding circuit for the relays K516 and K521, thereby causing deenergization of these relays. By 270 degrees of rotation of the cam line during this operation, the keys, the key lock line, and the auxiliary key lock line of the window machine are restored, and the amount of the deposit has been added to the old balance accumulated on the add-
51 subtractor totalizer of the window machine. In addition, the
transaction row 1 rotary switch SR510CC (FIG. 12B) is
positioned to position 8; namely, the Receive key position,
by the trip circuit of operations 322 degrees of rotation of
the cam line, the automatic cycle switch con-
tacts SC521A1 (FIG. 12B) are closed by a cam on the
printer cam line. When these contacts close, the auto trip
relay K522 (FIG. 11C) is energized over a circuit which
extends from the positive common 189 over the contacts
K512BC4 (FIG. 11C); K501AC2; K517BC4; the relay
K522; a terminal 247 (FIG. 11C), which is connected to a
terminal 248 (FIG. 12B); the switch SR501C, with the
wiper set to position 8; the contacts SC521A1, to a termi-
nal 249 (FIGS. 11B and 12B), which is connected to
the negative common 191.

The auto trip relay K522 remains energized during the
25 degrees of rotation of the cam line that the auto cycle
switch contacts SC521A1 are closed. Each degree of the
cam line rotation equals approximately 2.4 milliseconds,
when the window machine is running at 120 degrees of
cam line rotation of approximately 68 operations per minute. When the relay K522 is energized, the contacts K522A1 (FIG. 13) close and complete an energizing circuit for the Balance key solenoid L11 (FIG. 13). This circuit extends from a plus 50-volt D.C. supply, represented in FIG. 13 by terminal 250; the solenoid L11, the contacts
K501AC4; the contacts K522A1; to a 50-volt D.C. re-
turn, represented in FIG. 13 by the terminal 251.

The Balance key solenoid L11 is energized over the
above circuit for at least 49 milliseconds, and causes the
Balance key of the window machine to be depressed to
initiate a second cycle of window machine operation, this
time a balance cycle. The trip switch contacts SC502AC1
(FIG. 11C) close when the balance key is depressed, and
prepare the energizing circuit for the trip solenoid L540.
At the same time that the Balance key solenoid circuit
is completed by closing of the contacts K522A1, as de-
scribed above, the contacts K522A3 (FIG. 11B) also close
and complete the circuit for the trip and auxiliary trip relays
K516 and K521 over a circuit which extends from the
positive common 189 over the contacts K522A3 and the
relays K516 and K521 in parallel to the negative com-
mon 191. Energization of the trip relay K521 causes the
contacts K521A13 to close in the energizing circuit for this
trip solenoid L540. At 340 degrees of rotation of the
cam line during the "A" Deposit operation of the window
machine, the auxiliary trip switch contacts SC522A1 close
in the energizing circuit for the trip solenoid L540 to
complete the energizing circuit for said solenoid, thereby
tripping the window machine for the auto balance oper-
ation.

At five degrees of rotation of the cam line during the
balance operation, the auxiliary trip switch contacts
SC522A1 open in the energizing circuit for the trip sole-
noid L540 to interrupt said circuit. At the same time,
the trip release switch contacts SC522A1 (FIG. 11B)
open to deenergize the auxiliary trip and trip relays K516
and K521. At 355 degrees of rotation during the balance
operation of the window machine, the output mode switch contacts SC504BC1 (FIG.
11B) open and interrupt the energizing circuit for the
output mode relays K509 and K519. The contacts K509AC1 (FIG. 11A) open in the energizing circuit for
the auxiliary control digit 1 relay K501, to cause deener-
gization of said relay.

At the conclusion of the balance operation of the win-
dow machine, the add-subtract totalizer is cleared, the
pass-book has been printed upon and ejected, the top
lock mechanism of the window machine has been relaxed,
and the window machine is in the home position, with
the ON LINE and READY lamp indicators lighted.

SEND ERROR

A "Send Error" indication results in the event that the
remote controller attempts to send an input message seg-
ment to the central data processing station without suc-
cess. A certain number of "retries" of transmission of the
message segment are permitted, since the difficulty may
be simply an error in transmission which can be cleared
up by a subsequent attempt. However, if the given num-
ber of retries, which can be determined according to the
design of the machine, is not successful, then the "Send Error" indication is utilized.

A "Send Error" signal, denoting unsuccessful trans-
mission of an input message segment, is detected in the
remote controller 108, or in the buffer of the central data
processing station 101, by checks for proper encoding,
parity, longitudinal bit sum, and characters greater than
nine.

Unsuccessful transmission of an input segment causes
the appearance of a signal at the "true" logic level on the
input error line JWM38 (FIG. 16A). In the window ma-
chine controller 110, when the line JWM38 goes true, the
relay K104 (FIG. 16B) is energized, the energizing
circuit extending from the line JWM38 over the closed
contacts K102AC4 and the relay K104, to a minus 20-
volt D.C. source.

Energization of the relay K104 causes the contacts
K104BC2 (FIG. 16B), which are normally closed, to
open, in the Ready Interrogate line JIM9, thus breaking
the input flag circuit, consequently:

This causes the signal on the Answer Ready line, desig-
nated in FIG. 16B as IM20 and in FIG. 16A as JW20,
to go to a false logical level, which allows the remote
controller 108 to resume scanning.

The contacts K104AC1 (FIG. 16B) are closed by ener-
gization of the relay K104 and provide a holding path for
maintaining said relay in an energized condition,
said holding path extending from ground, as in-
dicated at the terminal 252 (FIG. 12B), over the two
switches SC521B2 and SC524B1 in parallel, which are
closed in the home position of the window machine, over
a terminal 253, to the JIM3 line in FIG. 16B, over the
connectors 73 and 74 (FIGS. 16B and 17B), over the
relay contacts K104AC1, and the relay K104, to a minus
20-volt D.C. power source.

The contacts K104AC4 (FIG. 19) are closed by ener-
gization of the relay K104 and complete a path for il-
iminating the SEND ERROR lamp I501 (FIG. 12A),
said circuit path extending from the 6.3-volt A.C. line
193 in FIG. 19 over the contacts K104AC4, the line
JIM71, a terminal 201 (FIG. 12A), and the lamp I501,
to one side of the windings 188 of the transformer
secondary T901.

The window machine teller must now use the Void key
in another operation, to return the window machine to an
"On-Line Ready" status in order to reset the SEND
ERROR lamp I501.

At approximately 140 degrees of the void operation,
the machine status switch contacts SC524B1 open, break-
ing one of the parallel hold circuits which have been
previously described for maintaining the relay K104 in
energized condition. At 325 degrees of the cycle of ma-
chine operation, the auto cycle switch contacts SC521B2
also open, thereby breaking the holding path for the rel-
ay K104. As this relay is deenergized, the contacts
K104AC4 open, and the SEND ERROR lamp I501 is
extinguished. The contacts K104BC2 close in the input
flag circuit. The remote controller 108 recognizes the
input request from this window machine, and the Void
operation is sensed from the window machine and sent to
the central processing station 101.

The condition which caused a Send Error indication
on an input segment may also cause a Send Error indi-
cation when the teller attempts to void the previous trans-
action. If this is the case, at 320 degrees of the void op-
eration, the Send Error lamp I501 is reset, as described
above, and the input flag circuit is completed by closing
of the contacts K104BC2. The input error line JWM38
again goes true when an input error is detected, causing
the relay K104 to be energized once more over the circuit described above. The contacts SC524B1 are open and remain open. The contacts SC521B2 are closed again at 350 degrees of the void operation. With the contacts SC521B2 closed, and the relay K104 energized, the contacts K104AC1 are closed, holding the relay K104 energized. The SEND ERROR lamp 1501 is illuminated. The window machine 109 has been cleared, but the central processing station will not have received the void message segment. Each void operation to follow will reset the SEND ERROR lamp 1501, and the input errors will continue to light the SEND ERROR lamp 1501 until the window machine makes a successful void input operation.

ENTRY ERROR

An “Entry Error” indication results after the window machine 109 has completed an input operation and is in an output mode. The central processing station compares old balances and checks for data to update the pass-book. When the balances do not agree, the processor sends an output message to the remote controller 108 for the branch in which the window machine is located. The message contains the digit 2 in the penny row (11th character) in the lamp digit position (12th digit character), and digit 6 in transaction Row 2 (Eject key) position. This causes key 2 in the penny row to be depressed by its corresponding key solenoid.

The Lamp Digit 2 in the message will cause the line JVM172 (FIG. 17A), from the remote controller to the window machine controller, to go true, which provides a ground connection for energization of the relay K203 (FIG. 17B). The path extends from ground over the conductor 91, the relay K203, the contacts K30BAC1, and the line JVM172 to a minus 20-volt D.C. source. This relay K203 is energized, which contacts the contacts K203AC3 (FIG. 19) to close, to complete a signal to the Lamp Digit 2 line JVM172. The circuit for applying the signal to the line JVM172 extends from the 6.3-volt A.C. line HMG (FIG. 19), designated by reference character 193, over the contacts K207BC2, K201BC4, K203AC3, and K202DC4, to the line JVM172. This signal is applied to the terminal 202 (FIG. 12A), and the circuit path continues from the terminal 202 over the ENTRY ERROR lamp 1502 to one side of the secondary winding 188 of the transformer TS01. The ENTRY ERROR lamp 1502 is thus illuminated, to indicate the existing condition to the window machine operator.

Energization of the relay K203 causes the contacts K203AC1 (FIG. 17B) to close, which completes a holding circuit for maintaining the relay K203 in an energized condition. This holding circuit extends from an electronic ground connection over the contacts K205BC1, a diode 93, the contacts K203AC1, the relay K203, and the common 91 to the minus 20-volt line HWM1 (FIG. 17A). The relay K203 will remain energized until the lamp set relay K205 is energized, at which time the contacts K205BC1 will open, thereby deenergizing the relay K203. Following energization of the relay K203, the Flot key is pulled down, in a manner previously described, by its keyboard solenoid, and a Trip signal causes the window machine to be tripped, to initiate a cycle of operation. When the window machine operates, the add-subtract totalizer and the back counter will not be affected because the Receive key was not depressed in this operation. The account pass-book is ejected, and the audit tape is printed upon by the window machine to record the operation. The line of print on the audit tape will include a “Received” and a 2 in the penny row position. The Delta symbol indicates an eject operation. The 2 in the penny row describes the reason for the eject operation by indicating the lamp digit which was used during this eject operation, which in the illustrated example is Lamp Digit No. 2.

The operator must now make a void operation, which will clear the add-subtract totalizer and return the window machine to the “Ready” status. Following this, the operator will introduce the complete input message into the window machine once more.

RECEIVE ERROR

Should an error be detected in an output message after a key of the window machine could have been depressed by its corresponding solenoid, the remote controller will cause the Lamp Bit lines JVM171 and JVM172 (FIG. 17A) to go true. These lines provide ground connections for energizing the relays K201 and K203 (FIG. 17B), respectively, over circuits extending from the lines JVM171 and JVM172, contacts K30BAC2 and K30BAC1, the relays K201 and K203, and the common 91 to the minus 20-volt D.C. line HWM1. Energization of the relays K201 and K203 causes the contacts K201AC1 and K203AC1 (FIG. 17B) to close, and establish holding circuits for maintaining the respective relays K201 and K203 in an energized condition. The contacts K201AC4 and K203AC4 (FIG. 19) close in the Lamp Digit decoding network, while the contacts K201BC4 and K203BC4 open in that network. The combination of closed contacts in said network is then effective to complete a 6.3-volt A.C. circuit which extends from the line 193 of FIG. 19 over the contacts K207BC2, K201AC4, K203AC4, K206BC3, to line JVM173, which is connected to terminal 203 (FIG. 12A), over the RECEIVE ERROR lamp 1503, to one side of the secondary windings 188 of the transformer TS01. This causes the RECEIVE ERROR lamp 1503 to be illuminated to provide an appropriate signal indication on the window machine to advise the operator thereof of the condition existing.

At the same time, appropriate signals on the Digit 5 solenoid ground line JVM145 and the transaction row 1 driver JVM112 (FIG. 17A) are transmitted to the window machine in the manner previously described and cause energization of the appropriate keyboard solenoid to depress the Over Ride key in row 1 of the window machine keyboard. An appropriate signal on the Trip line JVM (FIG. 16A) then causes the window machine to be tripped for an operating cycle. In this cycle, the audit printer of the window machine operates to print the number represented by the keys which had been depressed prior to the detected error. An appropriate symbol is also printed to indicate the use of the Over Ride key.

ERROR UPDATE

The Error Update feature is a provision included in the system to correct errors caused by the incorrect posting of a transaction amount by the teller. This type of error will be detected when the teller attempts to prove the totals of the window machine against the cash on hand at the end of an operating period, such as at the end of a day. The teller, in the normal procedure of operating the branch, will then set the window machine to an on-line condition, and correct the error in the normal manner, using "no book," "deposit correction," or "withdrawal correction" procedure. This information will correct the account file. "No book" operations are retained as update items in the account file. A "no book" correction will also have a coded character to denote "error update."

The next time the customer presents the pass-book, the central data processing station will automatically output the segments of data to the branch to update the customer's pass-book. An "error update" message segment will have a digit 4 in the lamp digit position of the output message segment.

When the lamp digit portion of the "error update" message is received, the Lamp Bit line JVM173 (FIG. 17A) goes to a true condition. This provides a ground connection for energization of the relay K207 (FIG. 17B), and said relay then is energized over a circuit which extends from the line JVM173 over the contacts.
K307AC4, the relay K207, and the common 91, to the minus 20-volt D.C. line HWM1.

Energy of the relays K207 causes the contacts K207AC2 to close, and the contacts K207BC2 to open, in the Lamp Digit decoding network of FIG. 19. A circuit is then completed from the 6.3-volt A.C. line 193 of FIG. 19 over the contacts K207AC2, K206BC2, K203BC2, and K201BC3 to the Lamp Digit 4 line J174, which is connected to the terminal 204 of FIG. 12A, over the ERROR UPDATE lamp J504, to one side of the secondary winding 188 of the transformer T501. This causes the ERROR UPDATE lamp J504 to be illuminated, thus providing appropriate indication to the teller of the error signal received from the bank.

At the same time that the lamp J504 is illuminated, the Error Update buzzer 197 (FIG. 12A), also designated J520, is energized, to provide an audible indication to the teller of an error update operation.

**HOLD CONDITIONS**

The lamps J505 to J512 inclusive (FIG. 12A) are used to denote account status conditions. The lamps J505 and J506 are labeled REFER and OVERRRAFT, respectively. The lamps J507 to J512 inclusive are labeled as shown by the bank according to individual requirements of the system employed by the bank for maintaining accounts. The "refer" indication is used to show that a special condition exists on the account being processed which requires the teller to communicate with the central data processing station 101 before the processing of the account by means of one or more output messages to the selected window machine can be completed.

Each of these "hold" conditions will require special attention by the teller or by the supervisor or auditor of the branch. The individual bank will dictate the policy to control each hold condition, for determination of who should make the appropriate decision; the teller or the supervisor. It may also be desired that the decision is not to be permitted to be made by the branch. The output message for a "hold" condition will contain an Auxiliary Control Digit or ACD character that will allow the teller or the supervisor to override the "hold" condition or alternatively will force the bank branch to disallow the transaction. The "Teller Override," "Auditor Override," and "No Override" characters will be designated as ACD3, ACD4, and ACD5, respectively.

In each instance, a "hold" output message will contain an amount in the cent and dime rows to describe the lamp to be used (5 to 12 inclusive); a lamp digit (5 to 12 inclusive); an ACD3, ACD4, or ACD5 character; and an Eject key signal (digit 6, transaction row 2). The lamp digit will cause the proper lamp to be illuminated in the same manner as described in connection with previous lamp digit illuminating circuits. The ACD3, ACD4, and ACD5 characters will set the ACD relays in the window machine and will condition the machine for "teller override," "auditor override," or "no override" conditions, respectively.

**AUXILIARY CONTROL DIGIT 3**

The Auxiliary Control Digit 3 character is used with a hold condition which requires only a teller override operation to relieve the hold condition. The output message segments from the data processing station 101 to set this condition consists of the cent and dime (or units and tens) row amounts to describe the hold lamp to be illuminated (5 to 12 inclusive), a lamp digit (5 to 12 inclusive), the Auxiliary Control Digit 3 character, and a signal to cause energization of the keyboard solenoid controlling depression of the Eject key.

When the Auxiliary Control Digit 3 signal is received by the remote controller 108, the ACD Bit lines JWM160 and JWM161 (FIG. 16A) are made true, which causes the relays K101 and K103 to be energized over circuits extending from said lines over the contacts K306AC4 and K307AC1, and the relays K101 and K103, to a minus 20-volt D.C. line.

Energy of the relays K101 and K103 causes the contacts K101AC1, K101AC2, K101AC3, K101AC4, K103AC1, and K103AC4 to close, and causes the contacts K101BC1, K101BC2, K103BC1, and K103BC3 to open in the ACD decoding circuit of FIG. 18. A path is thus completed through the network of FIG. 18, extending from a 115-volt D.C. line HM5 at terminal 216 over the contacts K106BC1, K103AC4, and K101AC4 to the Auxiliary Control Digit 3 line J163.

The signal on the line J163 is applied to a terminal 259 (FIG. 11A) for energization of the ACD3 relay K503 (FIG. 11A) over a circuit which extends from the terminal 259 over the relay K503, the contacts K509AC1, the contacts K508BC1, and the contacts K520BC1, to the negative common 191.

Energy of the relay K503 causes the contacts K503AC1 (FIG. 11A) to close, to complete a holding circuit for maintaining the relay K503 in energized condition. Said holding circuit extends from the positive common 189 over the relay contacts K503AC1, the relay K503, and the contacts K509AC1, K508BC1, and K520BC1 to the negative common 191.

The contacts K503AC2 are closed by energization of the relay K503, in the circuit for energization of the relay of the override input relay K514 (FIG. 11B). Closing of the contacts K503AC2 completes an energizing circuit for energizing the override input relay K514 over a circuit which extends from the positive common 189 of FIG. 11A over the terminal 214, over the terminal 216 on line HM5 (FIG. 18), over the contacts K107BC1, over a terminal 215 on the line J317, over a terminal 260 (FIG. 11B), over the contacts K529BC4, which are closed at this time, over the contacts K503AC2, and over the relay K514, to the negative common 191.

Energization of the relay K514 closes the contacts K514AC2 (FIG. 12B) to prepare a circuit for enabling a subsequent override input operation to be made from the window machine to the central data processing station 101.

Energization of the relay K514 also causes the contacts K514AC1 (FIG. 11B) to close, to complete a holding circuit for maintaining the relay K514 in energized condition.

Following the output operation described above, the teller may "void" the previous transaction, or he may "override" the hold condition established by the preceding output message segment. In the illustrative example, it will be assumed that the teller chooses, after examining the pass-book, to "override" the hold condition. In order to do this, the teller must put the pass-book into the book printer of the window machine, move the lever lock of the window machine upward, and press the Over Ride key in row 1 of the accounting machine keyboard while maintaining the lever lock held upward.

The movement of the lever lock described above causes the contacts SC534BC2 (FIG. 11A) to close. As soon as the Over Ride key of row 1 is depressed, the contacts SC532BC4 (FIG. 11A) close and complete an energizing circuit for energization of the override relay K515 (FIG. 11A). This circuit extends from the positive common 189 over the contacts K509AC4 (FIG. 11C) over a conductor 261, over the contacts SC534BC2, over the contacts SC532BC1, and over the relay K515 to the negative common 191, for energization of said relay.

Energization of the relay K515 causes the contacts K515AC4 (FIG. 11A) to close, in the energizing circuit of the ACD drop relay K508. This completes an energizing circuit for the relay K508, extending from the positive common 189 over the relay K508, the contacts SC523BC2, which are closed at this time, and the contacts K515AC4, to the negative common 191.

Energization of the relay K508 causes the contacts K508BC1 (FIG. 11A) to open, thereby interrupting the energizing circuit for the relay K503, and causing said relay to be deenergized.
As the Over Ride key of the accounting machine keyboard is fully depressed, the contacts SCS02AC1 (FIG. 11C) are closed, which completes an energizing circuit for the trip bypass relay K510 (FIG. 11A). The energizing circuit for the relay K510 extends from the positive common 189 over the contacts K509AC4 (FIG. 11C), the common 261, the contacts K515AC1 (FIG. 11A), the contacts K504BC3, the contacts K505BC2, a resistor 262, the relay K510, a common 263, and the contacts SCS02AC1, to the negative common 191. Energization of the relay K510 causes the contacts K510AC1 (FIG. 11C) to close, completing the circuit for energizing circuit for LS40 (FIG. 11C), said circuit extending from the positive common 189 over the contacts K510AC1, the contacts SC506AC2, the solenoid L540, the contacts SCS22A1, and the contacts SC502AC1, to the negative common 191.

It may be noted that energization of the trip bypass relay K510 is prevented during an output operation by closing of the contacts K301AC1 (FIG. 17B), which are connected to lines JM103 and JM104. The lines JM103 and JM104, in turn, are connected to terminals 270 and 271 (FIG. 11A), connected to opposite sides of the relay K504AC1. It will be seen that when the relay K301 is energized, in an output operation, the contacts K301AC1 are closed, thereby shorting the relay K510 and preventing its energization.

Energization of the trip solenoid K540 is effective to initiate the machine operation. As the machine operates, the input flag switch contacts SCS202A1 (FIG. 11B) close to complete an energizing circuit for energizing the input mode relays K507 (FIG. 11A) and K513 (FIG. 11B). In this circuit, it will be recalled, the contacts K514AC2 (FIG. 12B) are now closed, due to energization of the relay K514, as previously described. This energizing circuit for the relays K507 and K513 extends from the terminal 214 (FIG. 11A), connected to the positive common 189, to a terminal 216 (FIG. 18) on the line HMS, to which the terminal 214 is connected, over the contacts K107BC1, a terminal 215, shown in FIG. 18 as associated with the End of Segment line JMS3, a terminal 217 (FIG. 12B) to which the End of Segment line is connected, the wiper of the storage switch SR501B, which in this operation is set to position 5, corresponding to the Over Ride key position of row 1 of the window machine keyboard, the contacts K104AC2, the connector 219, shown in FIGS. 12B and 11B, the contacts SCS202A1, and the relays K507 and K513 in parallel, to the negative common 191. The input mode relays K507 and K513 are thus energized. An input message containing the “override” information is then transmitted to the central data processing station to permit the processing of the account to continue with a subsequent output message.

**AUXILIARY CONTROL DIGIT 4**

The Auxiliary Control Digit 4 character is used with a “hold” condition which requires an auditor override procedure to relieve the hold condition. The term “auditor override” is used to designate a requirement that, for every key which he alone carries. The output message to set this particular hold condition will include an ADC4 character.

When the ADC4 character is received by the remote controller, the ACB Bit line JW162 (FIG. 16A) to the window machine controller is made true. This results in the energization of the relay K106 (FIG. 16A) over a circuit which extends from the line JW162 over the contacts K307AC2 and the relay K106, to a minus 20-volt D.C. line. Energization of the relay K106 causes the contacts K106BC1 to close and the contacts K106BC1 to open in the Automatic Control Digit decoding circuit shown in FIG. 18. A path is thus completed through this circuit which extends from the 115-volt D.C. line HMS, to which the reference character 216 is applied; over the contacts K106AC1; the contacts K103BC1; and the contacts K101BC2; to the Auxiliary Control Digit 4 line JM164. Application of potential to the line JM164 causes energization of the ACB4 relay K504 (FIG. 11A) over a circuit which runs over line JW162 over a terminal 263A (FIG. 11A), the relay K504, the contacts K509AC1, the contacts K508BC1, and the contacts K520BC1, to the negative common 191.

Energization of the relay K504 causes the contacts K504AC1 (FIG. 11A) to close to complete a holding circuit for maintaining the relay K504 in energized condition, said holding circuit extending from the positive common 189 over the contacts K509AC4 (FIG. 11C), the conductor 261, the normally-closed total lock switch SC530B1, the contacts K504AC1, the relay K504, the contacts K509AC1, the contacts K508BC1, and the contacts K520BC1, to the negative common 191.

Energization of the relay K504 also causes the contacts K504AC2 (FIG. 11A) to close to complete a circuit for energizing the relay K503, said circuit extending from the positive common 189 over the contacts K504AC2, the relay K503, the contacts K508BC1, the contacts K508BC1, and the contacts K520BC1, to a negative common 191.

Energization of the relay K503 causes it to establish a holding circuit for maintaining said relay energized, over the contacts K503AC1, as has been previously described in connection with the ACB3 description.

The contacts K504BC3 (FIG. 11A) open in the energizing circuit for the trip by-pass relay K510, and thereby prevent tripping of the window machine for an operation using the Over Ride key.

In order to permit an override operation of the window machine, following an output message from the central data processing station in which an ACB4 character appears, the branch supervisor, or auditor, must place the auditor key in the total lock of the window machine and turn the key, then return it to the “locked” position. When the lock is operated, the total lock switch contacts SC530B1 (FIG. 11A) are mechanically opened, which interrupts the energizing circuit for the relay K504 and causes the deenergization of said relay. The contacts K504AC1 and K504AC2 thereby open, and the contacts K504BC3 close once more will be seen that returning of the contacts SC530B1 to their closed position does not result in the re-energization of the relay K504, since the contacts K504AC1 are now open. Since the contacts K504BC3 are now closed once more, the relay K510 can be energized to permit the machine to be tripped for an override operation. Operation of the window machine from this point on is similar to the description of machine operation in the description of the Automatic Control Digit 3 character.

**AUTOMATIC CONTROL DIGIT 5**

The Automatic Control Digit 5 is used with hold conditions (as determined by bank policy of the bank utilizing the system) to prevent any activity in the account in which the hold condition appears. The output message to set this condition will include a digit 5 in the ACD portion of the message.

When the ACD character is received, the remote controller causes the ACD bit lines JW160 and JW162 (FIG. 16A) to the window machine controller to be made true. This causes energization of the relays K101 and K106 over energizing circuits extending from the lines JW160 and JW162 over contacts K306AC4 and K307AC2, the relays K101 and K106 (FIGS. 16B and 16A) to a minus 20-volt D.C. line, to cause said relays to be energized. The various contacts controlled by these relays in the ACD decoding circuit of FIG. 16 are transferred, so that a path is completed through a circuit, which extends from the terminal 216 of the 115-volt D.C. line HMS over the contacts K106AC1, K103BC1, and
K101AC2, to the Auxiliary Control Digit 5 line JM165. The 115-volt D.C. potential on this line is applied to the terminal 264 of FIG. 11A to cause energization of the relay K505 over a path extending from the terminal 264, over the relay K505, the contacts K509AC1, the contacts K508BC1, and the contacts K520BC1 to the negative common 191. Energization of the relay K505 causes the contacts K505AC1 to close and complete a holding circuit for maintaining the relay K505 energized. Said holding circuit extends from the common 189 over the relay contacts K505AC1 (FIG. 11A), the relay K505, the contacts K509AC1, the contacts K508BC1, the contacts K520BC1 to the negative common 191.

Energization of the relay K505 also causes the contacts K505BC2 (FIG. 11A) to open in the energizing circuit for the trip by-pass relay K510. This prevents energization of the relay K510 and therefore sets a "no override" condition in the window machine. As a result, the window machine operator must use the Void key to return the window machine to an on-line ready status.

AUTOMATIC OVERRIDE

An automatic override feature is provided in this system and is used to automatically release any depressed keys on the window machine keyboard, and to deenergize any ACD digit relays in the window machine, when the remote controller 108 detects any one of several different types of output errors after a key could possibly have been depressed and before a trip signal has been transmitted to the window machine during an output operation.

When an error is detected during this period, the remote controller causes the Output Digit 5 line JWM145 and the Output Control Row 1 line JWM121 (FIG. 17A) in the window machine controller to go true. These signals are transmitted through the window machine controller and cause the override key of row 1 of the window machine keyboard to be depressed by energizing its solenoid L15 in the manner previously described.

It will be recalled that the solenoid L15 is energized by application of a plus 50-volt signal over the appropriate line to the terminal 243 of board T1 (FIG. 13), and at the same time connecting a terminal 265 of the solenoid L15 to a solenoid grounder in the remote controller. An examination of FIG. 13 will show that an error drop relay K520 is connected to the solenoid L15 in parallel with both, over a resistor 267. The relay K520 is energized at the same time that the solenoid L15 is energized, by virtue of the fact that the relay is connected at one side to the terminal 243 and is connected at its other side over a terminal 266 to the same solenoid grounder line as is the solenoid L15 of the terminal 265.

Energization of the relay K520 causes the contacts K520BC1 (FIG. 11A) to open, deenergizing any and all of the ACD relays K501 to K505 inclusive which may have been energized during the preceding output message segment.

The deenergization of the relay K520 causes the contacts K520BC4 to be opened in the energizing circuit for the override input relay K514, thus causing said relay to be deenergized in the event that it was energized during the preceding output message segment.

Following depression of the Over Ride key by the solenoid L15, a trip signal is sent to the window machine from the remote controller on line JWM190 (FIG. 18) to energize the relay K204. This closes the contacts K204AC1 (FIG. 18) to apply 115 volts D.C. to energize the auxiliary trip and trip relays K516 and K521 (FIG. 11B) which in turn are effective to close the contacts K516AC2 and K521AC3 (FIG. 11B) in the energizing circuit for the trip solenoid L540, so that said trip solenoid is energized in the manner previously described.

The window machine is thus tripped for a cycle of operation, and during said cycle will cause information corresponding to any depressed keys to be printed.
The contacts K502AC2 (FIG. 11C) are closed by energization of the relay K502 and prepare an energizing path for energization of the auto trip relay K522.

Energization of the relay K502 causes the contacts K502AC3 (FIG. 12B) to close to prepare an energizing circuit for energizing a relay K508 subsequently. Following the energization of the relay K502, the appropriate control keys in rows 4, 1, 2, and 3, including in all cases the Receive key in row 1, are depressed by energization of their respective solenoids according to the information contained in the output message segment.

Following the energization of these solenoids, the window machine is tripped for a cycle of operation, in the same manner as has been previously described. At 325 degrees of the interest operation, the auto cycle switch SC521A1 (FIG. 12B) is closed. At this time, the row 1 rotary switch SR501C (FIG. 12B) is in digit position 8 corresponding to the position for the Receive key. A circuit is then completed for energization of the automatic trip relay K522, said circuit extending from the positive common 189 over the contacts K512BC4, K502AC2, the relay K522, the relay K521, the terminal 249 of FIGS. 12B, 12C, and 12F, the relay switch SR501C, set to position 8, the switch SC521A1, the terminal 249 of FIGS. 12B and 11B, to the negative common 191. The relay K522 is thus energized.

Energization of the relay K522 causes the contacts K522A3 (FIG. 11B) to close to energize the trip relays K516 and K521 (FIG. 11B). The contacts K516A2 and K521A3 (which are controlled by the relays K516 and K521, then close to prepare an energizing circuit for the trip solenoid L540 (FIG. 11C).

Energization of the relay K522 also closes the contacts K522A2 and K522A1, which are in parallel to reduce arcing, and which close to provide a 50-volt D.C. power supply for energizing the sub-balance solenoid L12 (FIG. 13). This circuit extends from a plus 50-volt D.C. terminal 250 over the solenoid L12, the contacts K502AC4, and the contacts K522A1 and K522A2, in parallel, to a 50-volt return terminal 251. Energization of the solenoid L12 causes the Sub-Balance key in control row 1 of the window machine keyboard to be depressed for a second operation, which is an automatic sub-balance operation, following the interest operation of the window machine which is just being completed at this time. It will be realized that the previously-depressed Receive key in row 1 has been released at this stage of the interest operation.

Depression of the row 1 Sub-Balance key mechanically causes the contacts SC522A1, (FIG. 11C) to close, completing a circuit to energize the trip solenoid L540, said circuit being over the path previously described. It may be noted that the auxiliary trip switch contacts SC522A1, in the energizing circuit for the solenoid L540, are closed by this time in the cycle of operation of the window machine.

Near the end of the sub-balance operation, the relay K508 (FIG. 11A) is energized over a circuit which extends from the negative common 191 over the terminal 249 (FIGS. 11B and 12B); the contacts SC521A1; the switch SR501C; the terminal 2 on row 12 which is the trip solenoid balance position; the contacts K502AC3; a terminal 269 (FIGS. 12B and 11A); and the relay K508 to the positive common 189. Energization of the relay K508 causes the contacts K508BC1 (FIG. 11A) to open to drop out any energized AC/D relays K501 to K505 inclusive, which in this case is the relay K502.

Initiation of an automatic sub-balance operation of the window machine by energization of the trip solenoid L540 as described above results in the printing, by the window machine printing mechanism, of a sub-total amount on the pass-book, on the audit strip, and on the transaction slip, so that the various update operations are indicated separately.

The sub-balance operation will not affect the output mode relays K509 and K519, and these relays remain energized following a sub-balance operation, which they would not do in case of a balance operation, in which these relays are deenergized. The window machine is thus left in the output mode of operation under processor control. Upon completion of the sub-balance operation, the window machine will be ready to accept another output operation.

In the last of a series of updating operations, it will be seen that the ACDI character, rather than the ACD2 character, will be used, so that the relay K501, rather than the relay K502, is energized to cause a balance operation, rather than a sub-balance operation, to be made. Use of a balance operation at this time terminates the output mode of the window machine.

**RE-ENTRY OPERATION**

As has been previously described, a re-entry operation is used when it is necessary to re-enter information used to post the various customers' pass-books during a time when the operation of the particular window machine used was in an offline mode. This is necessary in order to update the bank's records at the central data processing station, and to ensure that the customer's records and the bank's records are in agreement. In making re-entry operations, the Re-Entry key of row 1 in the window machine keyboard is depressed and is locked down during the re-entry operation. Re-entry operations are identical to normal on-line input and output operations except that no document need be placed in either of the window machine printers in order for the operation to take place. From the standpoint of the window machine operating circuitry, the only difference between a re-entry operation and a normal entry operation is that the contacts SC531AC1 (FIG. 11B) are closed by depression of the Re-Entry key. This completes an energizing circuit for the relay K518, said circuit extending from the positive common 189 (FIG. 11C) over the contacts K509AC4, the common 261, the contacts SC531AC1, and the relay K518 to the negative common 191.

Energization of the relay K518 causes the contacts K518A1, (FIG. 15) to close in the output flag circuit, thereby by-passing the contacts SC507AC1 and SC508AC1, which are controlled by slip feeders in the printers of the window machine. This permits the circuit of FIG. 15 to be completed even though no documents have been inserted into either of these printers.

The necessary re-entry operations can thus be carried out to provide the central data processing station with the required information.

**REMOTE CONTROLLER GENERAL ORGANIZATION**

As has been previously stated, the remote controller 108 is a unit of the on-line branch sub-system which is connected to a number of window machines 109 through their associated window machine controllers 110 to enable individual window machines of a branch sub-system to communicate with and to be controlled by the central data processing station. Usually, only one remote controller 108 is required for each branch. However, in the case of an exceptionally large branch, having many window machines, more than one remote controller may be required, depending upon the number of window machines utilized. In the illustrated embodiment of the invention, a single remote controller can accommodate up to sixteen window machines.

The remote controller 108 is essentially a combination of electrical components in circuit arrangements capable of performing the required functions in the operation of the on-line system.

A simplified block diagram of a remote controller 108, showing its connections to the associated data sub-set 107 and the associated window machine controllers 110, appears in FIGS. 20A and 20B, which are best viewed when taken together, with FIG. 20A positioned above...
FIG. 20B. The lines representing connections to and from the window machine controllers 110 extend to the right of the dashed outline of the remote controller 108 in FIGS. 20A and 20B. A brief description of the elements represented by the various blocks in the diagram will first be given, followed by a brief explanation of the operation of the remote controller. Following this, the logical design employed in the illustrated embodiment, including the elements which may be used to make up the various blocks of the remote controller, will be described. It may be noted that descriptive legends are associated with the various lines extending to, between, and from the various blocks of FIGS. 20A and 20B. These lines generally represent the logic levels used by the remote controller to control the various components of the machine. In some cases, the names of such lines having the same or a similar function.

Referring now specifically to the communication link adator (CLA) section of the remote controller, the Output Level Counter functions to convert the logic levels used by the data sub-set (minus 5 volts and plus 5 volts, in the illustrated embodiment) to the logic levels used by the remote controller (minus 8 volts and 0 volt in the illustrated embodiment). Similarly, the Input Level Converter of the CLA converts the logic levels used by the remote controller to the logic levels used by the data sub-set.

The transmit Shift Register of the CLA is an eight-flip-flop register, in the illustrated embodiment. Each character of the input message segment is loaded into these flip-flops in parallel and is shifted out in a serial bit stream to the data sub-set so that it can be transmitted over a telephone line to the central data processing station.

The Receive Shift Register of the CLA is a seven-flip-flop register. Each character of an output message segment from the central data processing station is shifted in as a serial bit stream from the data sub-set, and is unloaded from this register in a parallel form.

The Control Character Decoder of the CLA consists of four separate diode decoding matrices for decoding the four control characters which may be transmitted from the central data processing station to the branch subsystem.

The Parity Decoder of the CLA is an "exclusive or" network by means of which each character that is shifted into the Receive Shift Register is checked for the proper parity.

The Scan Counter of the input section of the Remote Controller 108 is a four-flip-flop counter which counts from zero to fifteen and then resets to zero. These sixteen counts represent the six-digit window machine select lines in the remote controller. As soon as the Scan Counter counts to a number corresponding to a window machine which is ready to deliver an input message to the central data processing station, it stops. After the data has been successfully sent to the central station, the Scan Counter is reset.

The Input Program Counter of the input section of the remote controller is a three-flip-flop counter which counts from zero to seven and then resets to zero. This counter controls the sequence of operation in the input section of the remote controller.

The block designated Error Registers A and B of the input section of the remote controller represents two registers, each of which contains two flip-flops. These two registers are used at different points in the sequential operation of a program counter to count the number of retries which may be made on various operations. When an error is detected in an input message segment to the central data processing station, the buffer of the central station will send an Input Error signal to the remote controller, which will read the switches of the window machine again, and then re-transmit the input message segment. The Error Registers are effective to tally the number of times any segment is re-tried. If the input segment is not successfully received, the central station after three re-tries, the remote controller sends a signal to the window machine which causes the illumination of the SEND ERROR lamp. The remote controller will then terminate its connection to the particular window machine from which it received the information, will resume scanning, and will reset the Error Register which has been used.

The Input Row Counter of the input section of the remote controller is a five-flip-flop counter which determines the format of the input message segment. Each program count from one to eighteen corresponds to one of the eighteen characters in an input message segment. With each count of the Input Row Counter, a data character is transmitted to the central data processing station. Sixteen of the characters in the message segment are sensed from the window machine. The other two characters are inserted into the input message segment by the remote controller. The Input Row Counter is reset to zero after the count of eighteen has been reached.

The Decimal-to-Binary Encoder of the input section of the remote controller is a circuit which employs a diode encoding network to cause decimal digits which are read from the window machine to be changed into a four-bit binary-coded-decimal code.

The Longitudinal Bit Check Register of the input section of the remote controller is a four-flip-flop register which causes a longitudinal bit check digit to be generated. This check character or digit is generated from all four bits of each of the first seventeen characters in the input message segment. The resulting character is inserted as the last character in the input segment. The buffer of the central data processing station generates a longitudinal bit check digit for the input message segment and transmits it with the last character of the input message segment. In this manner, the central data processing station is provided with a character to verify that the message received is the same as the message which was sent by the branch.

The Longitudinal Bit Check Register of the output section of the remote controller is a four-flip-flop register. As each digit of the output message segment is received from the central data processing station by the remote controller at the branch, the remote controller accumulates a longitudinal bit check digit on the first seventeen characters of the output message segment. This digit is compared with the longitudinal bit check character inserted by the buffer into the eighteenth character position of the output message segment. If these two characters agree, the window machine is sent a trip signal by the remote controller. If they do not agree, an Output Error Signal is sent to the inquiry buffer at the central data processing station.

The Output Select Register of the output section of the remote controller consists of four independent latches, or memory elements. These elements are not interconnected. The Output Select Register takes the window machine number from the central data processing station in binary-coded-decimal format and converts this number to decimal format through an attached decoding network for energizing the appropriate output select relays in the window machine controller corresponding to the selected window machine.

The Output Data Register of the output section of the remote controller is a four-flip-flop register which contains the four data digits from the binary-coded-decimal format in which they are received from the Receive Shift Register to decimal form for operating the grounder portion of the solenoid energizing matrix to cause the appropriate keys to be depressed on the keyboard of the window machine.

The Output Row Counter of the remote controller is a five-flip-flop counter which counts from one to eighteen. This counter is advanced as each character of the output message segment is received, and controls the driver portion of the solenoid energizing matrix.
The block designated Solenoid Matrix Drivers of the diagram of FIG. 20B, in the output section of the remote controller, represents the driver circuits associated with the solenoid matrix for causing energization of solenoids to depress keys on the keyboard of the selected window machine.

The block designated Solenoid Matrix Grounders in the block diagram of FIG. 20B, in the output section of the remote controller, represents the grunder circuits associated with the solenoid matrix for energizing solenoids to depress keys on the keyboard of the selected window machine.

The Output Program Counter of the output section of the remote controller is a three-flip-flop counter which counts from zero to seven, and which is used for control of the output section, stepping from one program count to the next.

A general explanation of the manner in which the remote controller, shown diagrammatically in FIGS. 20A and 20B, functions during normal on-line operation will now be given, with the aid of the charts of FIGS. 22 and 22, which show, respectively, the input program format and the output program format utilized in the remote controller to effect the transmission of information between the central data processing station and a given window machine of a given branch sub-system. A normal input message consists of a balance length, which is a transaction segment (deposit or withdrawn), and an account number segment, while a normal output message consists of a transaction segment which includes instructions for the window machine to make an automatic new balance operation at the end of the transaction operation.

It may be noted that proper timing sequences in the operation of the remote controller are maintained by clock signals provided to the various elements of the remote controller from the associated branch data sub-set.

The sequence in which the input segment is transmitted is determined by the format of the Input Program Counter and the Input Record Counter. This format is shown in FIG. 21 and is described in detail below.

The zero position of the Input Program Counter is a "reset" position. The Program Counter is operated to step out of this position when the entire on-line system is on and able to transmit.

The 1 position of the Input Program Counter is a "scan" position. In this position of the Input Program Counter, the Scan Counter in the remote controller will continually pulse each window machine scan position of the sixteen window machines until it finds a window machine which is ready to input, at which time the eighth To Input signal is sent to the central data processing station.

The 2 position of the Input Program Counter is a "start" position, in which the central data processing station sends a Start Input signal, to inform the remote controller that it has recognized the request to input and is ready to receive the input segment.

The 3 position of the Input Program Counter is a "delay" position, in which a Request For Character signal is generated, indicating that the remote controller wishes to sense the rotary switches of the window machine.

The 4 position of the Input Program Counter is a "read keyboard" position. In this position, the Input Row Counter will advance, so that the eighteen characters of the input segment can be sensed from the window machine and transmitted to the central data processing station. As has been previously described, the first character of the input range segment represents the window machine scan position number; the second through eleventh characters represent amount rows 10 through 1; the twelfth and thirteenth characters represent the tens and units of the window machine number in the system; the fourteenth through seventeenth characters represent control rows 1, 2, and 3, respectively; and the eighteenth character represents the sum check digit that is used in the central data processing station to check the longitudinal sum of the data bits transmitted. The Input Program Counter remains in count 4 until the Input Row Counter counts to zero.

The 5 position of the Input Program Counter is the "echo" position, in which an echo signal is received from the central data processing station that the input was O.K., or that the input was in error.

The 6 position of the Input Program Counter is the "delay" position, which is a momentary delay position. A main timing clock pulse will immediately step the Input Program Counter to the next position.

The 7 position of the Input Program Counter is the "end of segment" position. In this position, an End Of Segment signal is sent to the window machine, which causes the window machine to be disconnected from the remote controller, so that the Scan Counter can resume its scanning.

A typical input sequence will now be described. After the first segment of information, comprising a balance pick-up operation, has been introduced into the window machine by the tiller, the account number, the deposit or withdrawn, the transaction segment (deposit or withdrawn), and the Ready Interrogate line are connected in the window machine. The Input Program Counter is in count 1 at this time, and the Scan Counter is running. When the Scan Counter in the remote controller finds the selected Window Machine Ready line "high," or "true," the Scan Counter is stopped, an input request is caused, and an input To Input signal to be generated. The window machine selects relays within the window machine controller are next energized, and the contacts from these relays prepare the window machine row and digit select lines for a read-out operation. At this time, the Input Program Counter advances from position one to position two. At the time the Scan Counter was stopped, a Request To Input signal was sent to the CLA section of the remote controller. The CLA section builds a Request To Input control character and loads it in parallel into the Transmit Shift Register, which, it will be recalled, is an eight flip-flop register. This register is empty when the first flip-flop is on and all others are off, and only at this time can the character be loaded. The first flip-flop contains the "flag bit" (when the register is empty), which indicates that this is the start of a character. The six bits of a character to be transmitted will be loaded in parallel into the second through seventh flip-flops. At the same time that this character is loaded, a "flag bit" for the next character is loaded into the eighth flip-flop. The loaded character is then shifted out to the data sub-set in a serial bit stream. This is done by generating each flip-flop to attain the state of its adjacent higher order flip-flop, until the "flag bit" that was set into the eighth flip-flop has been shifted to the first flip-flop. This indicates that the character has been transmitted, and the register is once again empty.

The Transmit Shift Register shifts the Request To Input character out serially to the Level Converter in which the voltage levels are converted from the remote controller logic levels of zero and minus 8 volts to the data sub-set logic levels of plus 5 volts and minus 5 volts. The Request To Input character is then dialed by the telephone lines via the data sub-set to the central data processing station. After the Request To Input character is accepted in the central data processing station, a Start Input control character is returned over the output telephone line to the output section of the branch data sub-set. This control character is fed into the Level Converter for the data sub-set in which logic levels are converted to those used by the remote controller. The Start Input character is then shifted into the Receive Shift Register serially.

The Receive Shift Register contains seven flip-flops and is loaded serially and unloaded in parallel. The first bit of any character is always a "flag bit," so that when shifting a character into the Receive Shift Register, the "flag bit" will enter the Receive Shift Register first. The character is loaded serially by shifting each bit into the flip-flops of the Receive Shift Register in a high order to
low order direction. In this manner, each flip-flop attains the state of its adjacent higher order flip-flop, until the "flag bit" reaches the first flip-flop. This indicates that the complete seven-bit character has been shifted in, and that the data holding register is full. When two input character completely occupies the Receive Shift Register, it is unloaded in parallel into the Control Character Decoder. The character is then decoded, and the resulting signal is applied to the Input Program Counter, advancing it from its position 2, which is a "start" position, to position 3, which is a "delay" position.

A Request For Character signal is generated when the Transmit Shift Register is empty, and said signal is applied to the Input Program Counter. The Input Program Counter advances from position 3 to position 4, which is the "read keyboard" position, and the Input Row Counter advances from position 0 to position 1, in which it reads the window machine scan position. A Data On Line signal is generated with the Input Program Counter in position 4 and the Input Row Counter in position 1. In conjunction with the Request For Character signal, this will generate an Odd Data signal.

The data to be loaded into the Transmit Shift Register at this time is the window machine scan position number. The outputs of the four Scan Counter flip-flops, in conjunction with the output of the Input Row Counter flip-flops, set the row count 1, since the Scan Count is set to agree with the scan position of the window machine. For example, with window machine No. 15 selected, all four flip-flops of the Scan Counter are set. The outputs of these flip-flops, in row count 1, set all of the data bit lines true, representing window machine scan position No. 15. A parity signal is generated as the result of all four data bit lines being true, due to the fact that an odd number of bits is required in the Transmit Shift Register to satisfy parity. The signals on the four data bit lines are also transmitted as input to the four flip-flops of the Input Longitudinal Bit Check Register. Since all four data bit lines are true, each flip-flop of the Input Longitudinal Bit Check Register is set. Each flip-flop in this register adds, without carry, its associated data bit line output, each time a data digit is to be transmitted. In this manner, a sum of all data bits of the seventeen digits transmitted for a given segment is contained in the Input Longitudinal Bit Check Register, and the contents of this register are inserted as the eighteenth character of the input segment.

With the Load Data signal, the window machine scan position from the four flip-flops of the Scan Counter, and this four-bit configuration is loaded in parallel into the Transmit Shift Register. The parity bit, a bit that identifies the character as a data character, and a flag bit which identifies the start of the next character are also loaded into the Transmit Shift Register with the four data bits. This is the first seven-bit character of the eighteen-character input segment, and is shifted out of the Transmit Shift Register serially to the Level Converter and then over the telephone line via the data sub-set. When the Transmit Shift Register is empty, another Request For Character signal is generated. Another Data On Line signal is also generated, which will cause the Input Row Counter to advance to count 2, in which, as may be seen in FIG. 21, row 14, which is amount row 10, of the window machine is read out. The Input Program Counter remains in program count 4 until all eighteen characters of the input segment have been transmitted.

In row count 2, the row select line 1 selects the high amount row rotary switch, that of row 14, is pulsed via the select gate of the window machine controller. Since there are no amount keys in row 14, the rotary switch common remains at the eliminate position on a balance pick-up element, and the zero digit line of the window machine is also pulsed. The signal on this line is fed into the Decimal-to-Binary Encoder, where the output of the ten digit select lines is encoded into a four-bit binary configuration. Since only the zero line has a signal, the output of the Decimal-to-Binary Encoder is a binary zero, in which case all of the four data bit lines are false, or off. A binary zero represents an even number of data bits, and a parity bit is therefore required. It is loaded into the Transmit Shift Register with the zero digit when the Load Data signal is generated. The flip-flops of the Input Longitudinal Bit Check Register are not effective at this time, due to the fact that all four data bit lines are false. A Load Data signal is generated by the Data On Line and Request For Character signals, and the Input Row Counter is set to position 2. The flag bit, the data character bit, the parity bit, and the zero data digit are loaded into the Transmit Shift Register in parallel. This seven-bit character is then shifted out of the Transmit Shift Register serially to the Input Level Converter, and over the telephone line via the data sub-set.

When the Transmit Shift Register is again empty, another Request For Character signal and Data On Line signal are generated. The Input Row Counter advances to row count number 3, which calls for reading of row 13. When the row 13 select line is pulsed, the digit select line, representing the position of the rotary switch, is also pulsed. Let it be assumed that the rotary switch common is in position 2. The signal on the number 2 digit select line is then fed into the Decimal-to-Binary Encoder, which results in an output of a binary digit 2. Since the digit 2 represents an odd digit, a parity bit is also generated. The appropriate flip-flop of the Input Longitudinal Bit Check Register is set, due to the presence of a signal on its corresponding line. The rest of the flip-flops are not affected. A Load Data signal causes a flag bit, a data character bit, and the data digit to be loaded into the Transmit Shift Register in parallel. After this seven-bit character has been shifted out over the telephone line, the Transmit Shift Register will again be empty, and another Request For Character signal and Data On Line signal will be generated.

The preceding sequence is repeated until all of the amount and control row rotary switches of the window machine, as well as the window machine number programmed into the terminal board of the window machine, have been read out. It may be noted that control row 3 of the window machine is the seventeenth character of the input segment to be transmitted.

With the Input Row Counter in count 18, the sum check digit, contained in the flip-flops of the Input Longitudinal Bit Check Register, is read out and transmitted as the eighteenth character of the input segment. The output of each Input Longitudinal Bit Check Register flip-flop, in conjunction with the output of the Input Row Counter representing row count 18, is fed to each of the four data bit lines. The data digit thus received is added, without carry, back into the Input Longitudinal Bit Check Register in the following manner:

Each data bit line sends a signal to its respective flip-flop in the Input Longitudinal Bit Check Register, from which it received the signal originally. The data bit line input to each Input Longitudinal Bit Check Register flip-flop causes each flip-flop that was set to be reset, which results in the register being reset to zero. Parity will be generated if required, on the sum check digit in the same manner as on the other data digits.

A Load Data signal causes a flag bit, a data character bit, a parity bit if required, and the sum check data digit to be loaded in parallel into the Transmit Shift Register. The seven-bit character is shifted out of the Transmit Shift Register serially over the telephone line via the data sub-set. The Transmit Shift Register is then again empty, which causes another Request For Character signal to be generated. A parity line signal is also generated, which advances the Input Row Counter from position 18 to position zero. With the Input Row Counter in zero, the Input Program Counter advances to count 5, which is the "answer back" position.
When the central data processing station successfully receives this input segment within 350 milliseconds, an Input O.K. control character is returned over the telephone line to the output section of the branch data sub-set. The character is shifted into the Receive Shift Register serially, after the voltage levels of the signals have been converted from the data sub-set logic levels to the remote controller logic levels by the Output Level Converter. When this character completely occupies the Receive Shift Register, it is unloaded in parallel, and its encoding is then loaded into the resulting signal is sent over the Answer Input O.K. line to the Input Program Counter, advancing it from count 5 (answer back) to count 6 (delay count). The Input Program Counter immediately advances to program count 7 (end of segment count) with the next main timing clock pulse.

With the Input Program Counter in count 7, the output line from the Input Program Counter that represents program count 7 is true. The signal over this line is fed to the End Of Segment line in the input select gate of the window machine controller, which energizes the end of segment relay K513 in the window machine controller. A contact from this relay opens in the input motor relay circuit in the window machine, relaxing the relays K513 and K507. The contacts from the relay K507 open, to break the Window Machine Relay Ready line and the Window Machine Ready Interrogate line. With these lines broken, the control counter starts scanning for another window machine which is ready to input. The window machine trip inhibit condition in addition is removed when the input mode relay K513 is relaxed, and this permits the machine counter to introduce another input segment into the window machine via the keyboard.

A transaction operation, such as a deposit or withdrawal, follows the balance pick-up operation, and represents the second segment of the input message. The sequence is the same as described above for the first segment, except for the control row read-out.

An account number operation always follows the last transaction segment, and represents the end of the message. During the account number machine cycle, the auxiliary key lock line in the top lock keyboard of the window machine is positioned. This line locks the key in the top section of the window machine keyboard, and actuates the output mode switch SC504 and the auxiliary key lock line switch SC534 in the window machine. The output mode switch completes the circuit to the output mode relays K519 and K509. The auxiliary key lock line switch, in conjunction with other contacts from the relay K513, prepares the output flag circuit. Other contacts of the relay K519 prepare an alternate path in the window machine trip circuit.

The description of the communications sequence for the account number segment begins in Program count 4, which is the "read keyboard" count, and row count 3, which is the "read tens branch number" count, since, up to this point, the sequence for the account number segment is the same as that described for the initial balance pick-up segment. With the Input Row Counter in count 3, the branch which is programmed in the terminal board in the window machine, is read out. The tens and units branch numbers programmed in the program board of the window machine can be overridden if the operator indexes keys in amount rows 8 and 9 of the window machine when entering the account number, in which case the keys will take preference. Here it will be assumed that branch No. 22 is programmed in the window machine program board and that no keys have been indexed in amount rows 8 and 9. The rotary switch common for row 13, which is amount row 9, is made with its zero position, which in turn is wired via the branch code number switch to the tens branch number in the digit select line section of the terminal board. When amount row 9 is pulsed, the number 2 digit select line carries a signal to the Decimal-to-Binary Encoder, where the ten digit select lines are encoded into a four-bit binary configuration. The output of the encoder in this case is a binary two. A parity bit is not generated, since the binary digit two represents an odd bit configuration. The appropriate flip-flop of the Input Longitudinal Bit Check Register receives the signal from the corresponding data bit line, which sets the flip-flop if it is reset, and resets it if it is set. If it is assumed that all flip-flops were previously set, this flip-flop is reset at this time. A Load Data signal causes a flag bit, a data character bit, and the data digit to be loaded into the Transmit Shift Register in parallel. When this character has been shifted out of the Transmit Shift Register and over the telephone line, the Transmit Shift Register is again empty, and another Request For Character signal and Data On Line signal is generated.

The Input Row Counter then advances to count 4, for reading of the units branch number, which is accomplished in the same way as described for the tens branch number. The rest of the amount row rotary switches, representing the account number, and the control row rotary switches, are read out; and the Input Program Counter advances, in the same manner as described for the first segment.

When the Input Program Counter advances to count 7, which is the "end of segment" count, output, on the End Of Segment line to the window machine controller, which energizes the segment relay K507. Contacts from this relay break the input mode relay circuit to the window machine, relaxing the relays K513 and K507. Contacts from the relay K507 break the Window Machine Ready and the Window Machine Ready Interrogate lines in the window machine controller, which causes the remote controller to drop the window machine and resume scanning. The window machine trip inhibit condition is removed when the relay K513 relaxes. However, the operator cannot depress keys due to the top lock condition of the window machine keyboard. Another set of contacts from the relay K507 closes, completing the output flag circuit. The Window Machine Ready line and the Window Machine Select line for this machine, which in the illustrated example is number 15, are coupled in the window machine controller.

When the central data processing station receives the account number segment, it recognizes it as the end of the message. The customer's account is accessed and the balances are compared, after which a Request To Output control character is returned over the output telephone line to the branch data sub-set.

This concludes the description of the transmission of the input message from the selected window machine to the central data processing station.

The sequence in which an output message segment is received by the branch will now be described. This sequence is controlled by the format of the Output Program Counter and the Output Row Counter, which is shown in FIG. 22. The Program counts are briefly summarized below.

Position 4 of the Output Program Counter is the "request" position. A Request To Output signal is received in this position, indicating that the central data processing station is ready to output to the solenoid keyboard of the window machine.

Position 5 of the Output Program Counter is the "load keyboard" position. The Output Row Counter advances in this position, so that the eighteen characters of the Output Segment can be received. The Output Program Counter remains in count 5 until the Output Row Counter steps to zero.

Position 6 of the Output Row Counter is the "delay" position, which is used to override errors if an output error has occurred after a selection of the window machine.

Position 7 of the Output Row Counter is the "trip" position, in which a trip signal is sent to the window machine.
Position 0 of the Output Program Counter is a "delay" position, in which the Program Counter waits until a Request For Character signal from the input section is generated.

Position 1 of the Output Program Counter is the "answer back" position, in which an O.U.K. signal or an Output Error signal is sent, indicating that the output segment was received correctly or incorrectly.

Position 2 of the Output Program Counter is a position which calls for a particular type of error to be transmitted. It is used to start the type of error which may occur on an output message is coded and transmitted.

Position 3 of the Output Program Counter is the "reset" position, in which the Error Register and the Output Select Register are reset.

As has been previously mentioned, the output segment consists of eighteen characters. The first character represents the window machine select position number, which is the same as the window machine scan position number sent to the central data processing station in the input segment. The second through eleventh characters represent the amount rows 10 through 1, which the window machine keyboard. The twelfth character represents the lamp digit, which illuminates one of the twelve status lights on the window machine keyboard. The thirteenth character represents the auxiliary control digit, which controls the automatic second cycle and override conditions in the window machine. The fourteenth digit describes the ACD digit that causes an automatic new balance operation following the transaction. The fourteenth through seventh characters represent control rows 4, 1, 2, and 3, respectively. The eighteenth character is the sum check digit, which is the longitudinal sum of the bits transmitted from the output segment.

When the central data processing station sends the Request To Output control character to the output section of the branch data sub-set, it is fed into the Level Converter and shifted into Receive Shift Register serially. When this character completely occupies the Receive Shift Register, it is unloaded in parallel into the Control Character Decoder. The resulting signal is sent to the Output Program Counter and to the Output Row Decoder, advancing the Output Program Counter to its position 5, which is the "window machine select" position. It may be noted that the Output Program Counter waits in count 5 for a Request To Output signal throughout the input message. The Output Program Counter remains in count 5 until all eighteen characters of the output segment have been received and the Output Row Counter advances to zero.

In position 1 of the Output Row Counter, the window machine select position is received from the central data processing station as the first character of the output segment. It will be assumed here that the window machine select position is No. 15. This data character consists of a flag bit, a data character bit, a parity bit, and four data digit bits. When the Window Machine Select character fills the Receive Shift Register, a Character Present signal is generated.

The Receive Shift Register is unloaded in parallel, and the outputs of the four Receive Shift Register data digit flip-flops set the four data digit lines true. The Character Present signal, in conjunction with the signals on the four data bit lines and the line from the Output Row Counter for count 1, sets the four latches of the Output Select Register. The outputs of these latches are fed into a binary-to-decimal decoder which is included in the Output Select Register, where the binary configuration representing the number 15 is decoded into a decimal number 15. The No. 15 window machine select line is then true, which sends a signal to the No. 15 window machine select position of the program board in the corresponding window machine controller. The window machine No. 15 has its output

Window Machine Ready line coupled to the window machine select position No. 15 of said program board.

With this circuit completed, the window machine select relays in the window machine controller energize. The contacts from these relays transfer and prepare the output row and digit select lines, so that the window machine solenoid keyboard can be loaded. The seven bits of the window machine select character are checked for proper parity. The signals on the four data digit lines are fed to the Output Data Register flip-flops, which flip-flops are turned on. The outputs of the Output Data Register flip-flops are added to the Output Longitudinal Bit Check Register to create a sum check digit. It should be noted that each time a character is shifted into the Receive Shift Register, a Character Present signal is generated. This signal, in conjunction with the signal on the Output Program Counter line for count 5, and the Output Row Counter lines from 1 to 18, causes a firing pulse, which controls the advancement of the Output Row Counter. Accordingly, a firing pulse is generated with the Window Machine Select character just received, and advances the Output Row Counter to count 2, which is the count in which row 14 of the window machine is loaded.

The second character to be received also contains a zero data digit, since there are no amount keys in row 14, which is amount row 10 of the window machine keyboard. This character is shifted into the Receive Shift Register and unloaded in parallel, after which it is handled in the same manner as the description that follows for the third character. A firing pulse is again generated, and the Output Row Counter advances to position 3, in which row 13 of the window machine keyboard is loaded.

Let it be assumed that amount key No. 2 is to be selected in row 13 (amount row 9). When the third character has been completely shifted into the Receive Shift Register, a Character Present signal is generated, and the Receive Shift Register is unloaded in parallel. The seven bits of the character are checked for proper parity. The outputs of the four data digit flip-flops of the Receive Shift Register set the appropriate one of the four data digit lines true, and the other three lines remain false. The signals on the data digit lines are fed to the flip-flops of the Output Data Register, which is set to agree with the data digit line signals. The outputs of the flip-flops of the Output Data Register are added without carry to the Output Longitudinal Bit Check Register flip-flops to build the sum check digit. Other outputs from the flip-flops of the Output Data Register are fed to the binary-to-decimal decoding means, where the binary digit 2 is decoded to a decimal digit 2. The signals on the data digit lines are present at the Solenoid Grounder for the digit 2 line. The output of the Output Row Counter line for row count 3 (the count in which row 13 of the window machine keyboard is loaded), in conjunction with the firing pulse, will turn on the solenoid driver of the Solenoid Matrix Drivers for row 13 (which is amount row 9 of the window machine keyboard). This coincidence of signals energizes the No. 2 key solenoid in amount row 9. The central data processing station sends six "no data" characters after each significant digit, in the illustrated embodiment, to allow time for the key solenoid to pull in the selected amount key, before the next character is sent to the Receive Shift Register.

The fourth through eleventh characters, representing amount rows 8 through 1, are received and routed as described above for the third character.

The twelfth character of the output message segment contains the lamp digit which selects one of the twelve account and error status lights displayed on the window machine indicator panels. Assume that no lamp is to be selected in this output message. In this case, a zero lamp digit is received as the twelfth character.

The thirteenth character, in this example, contains the auxiliary control digit for an automatic new balance, which is auxiliary control digit 1. When this character is
shifted into the Receive Shift Register, a Character Present signal is generated, and the register unloads in parallel. The seven bits of this character are checked for proper parity. The outputs from the four data digit flip-flops of the Receive Shift Register, the receive data digit lines. The signals on the data digit lines are fed to the four flip-flops of the Output Data Register, to turn on the appropriate flip-flop. Outputs from the Output Data Register are fed to the Output Longitudinal Bit Check Register to build the sum check digit. Other outputs from its flip-flops are fed to the appropriate relay drivers for the auxiliary control digit relays in the window machine controller. This causes the appropriate auxiliary control digit relay in the window machine controller to energize, and the contacts of this relay transfer in the auxiliary control digit decoding tree in the window machine controller, where the binary digit is decoded, to set one of the seven auxiliary control digit lines true.

The output from the decoding tree sends a signal over the No. 1 auxiliary control digital line, to energize the auxiliary control digit No. 1 relay in the window machine. The contacts of this relay transfer, as previously described in the window machine section of the description of the invention, and prepare the new balance key solenoid circuit. This relay in the window machine acts as a memory for the auxiliary control digit instruction until the window machine receives the transfer from the auxiliary control digit relay. The firing pulse is generated with the thirteenth character, which advances the Output Row Counter to count 14. All control rows are loaded in the same manner as described for amount row 9. It should be noted that the Receive key in control row 1 and the B deposit key in control row 3 are pulled down and remain in the illustrated example. When the eighteenth character, containing the sum check digit, is shifted into the Receive Shift Register, a Character Present signal is generated, and the Receive Shift Register is unloaded in parallel. The seven bits of this character are checked for proper parity. The outputs from the four data digit flip-flops of the Receive Shift Register are fed to the data digit lines. These lines are set according to the binary configuration of the sum check digit. Each data digit line transmits a signal to its respective flip-flop of the Output Longitudinal Bit Check Register, which adds the sum check digit received from the central data processing station to the digit built from the data digits of the seventeen characters received in this output message. All flip-flops of the Output Longitudinal Bit Check Register are reset when the Sum Check Digit is added, which proves that the data digits of the eighteen characters were received as they were transmitted. The Output Row Counter advances to count zero, which in turn advances the Output Program Counter to count 6 which is a "delay" count.

The Output Program Counter steps out of count 6 to count 7, which is a "trip" count, with the next main timing clock pulse. With the Output Program Counter in count 7, a Trip signal is generated and sent over the Trip line to the selected window machine controller, which energizes the trip relay K204. The contacts of this relay transfer and complete the trip relay circuit to the window machine, energizing the relays K521 and K516. The contacts from these relays transfer, completing the circuit to energize the trip solenoid L540, which releases the window machine for the deposit operation. During the deposit transaction, the row 1 rotary switch common of the window machine is set to terminal 8, which corresponds to the Receive key position. At 32 degrees inclusive, and the end of the windcycle switch SW521 closes in the row 1 rotary switch common circuit, completing the circuit to energize the automatic trip relay K522. The contacts of this relay transfer and, in conjunction with the contacts from the ACD1 relay, complete the circuit to energize the New Balance key solenoid and trip the window machine for a new balance operation, during which the auxiliary key lock line restores and transfers the output mode switch SC504 in the output mode relay circuit, and the auxiliary key lock line switches SC334 in the output flag circuit. The output mode relays K519 and K509 deenergize when the output mode switch opens, and their contacts will therefore transfer. A set of contacts of the relay K509 open in the ACD relay hold circuit, deenergizing the ACD1 relay. Other contacts controlled by the relay K519 reset in the window machine trip circuit, and set contacts from the relay K519 open in the output flag circuit. When the auxiliary key lock line switch opened in the output flag circuit, the Window Machine Ready line was broken.

The Output Program Counter has continued to advance during the window machine operations and will have stepped to count 4, which is the "request" position, before the window machine has completed its operations. The Output Program Counter steps into count zero (the "delay" count) on the next timing pulse after sending the Trip signal to the window machine. The Request For Character signal from the input section of the remote controller steps the Output Program Counter to count 1, which is the "answer back" count. In Program Count 1, an Output O.K. control character is transmitted to the central data processing station. This signal resets the Request To Output memory latch, which in turn advances the Output Program Counter to count 2, in which the "send type of error" command is given. The Output Program Counter advances to the "reset" count 3 when a Request For Character signal is generated in the input section of the remote controller. Since error conditions are not being considered in this illustrative operation, it can be assumed that all functions are normal. In Program Count 3, the Output Select Register latches are reset, which removes the signal from the No. 15 window machine select line and the program board in the window machine controller. In so doing, the window machine is dropped, and the central data processing station resumes scanning its other branches. It should be noted that the Error Register is also normally reset in count 3. The Output Program Counter then advances to count 4, which is the "request" count, with the next main timing clock pulse, and remains in that count until another Request To Output Control character is received from the central data processing station. This concludes the description of the operation of the system in an output message segment operation, and also concludes the general description of the system operation.

REMOTE CONTROLLER LOGICAL DESIGN

The various functional parts of the remote controller 108 which are shown in block form in FIGS. 20A and 20B may be mechanized by any appropriate combination of logical elements, according to the specific requirements of the particular system to be designed. In the illustrated embodiment of the invention, the logical equations of FIGS. 23 to 60 inclusive have been evolved to provide a remote controller having the necessary functional relationships to the remainder of the system to enable the desired operations to be performed. These logical equations, in turn, have been implemented in a form shown in the logical block diagrams of FIGS. 61 to 103 inclusive. Associated timing diagrams are presented in FIGS. 104 to 114 inclusive. It will, of course, be realized that the structural organization of the controller is not limited to the particular logical design given in the equations of FIGS. 23 to 60 inclusive and shown in the design of FIGS. 61 to 103 inclusive, the various forms of the logical block diagrams, which is in the scope of the present invention may be employed. A description with now be given, in terms of the logic employed, of typical operating sequences of the branch sub-system, such as the input and output operations, which have been previously described with reference to the input
and output programs shown diagrammatically in FIGS. 21 and 22, and various types of error sequences.

In this description, references will be made from time to time to specific logical equations and, to a lesser extent, to logical block diagrams and flow charts. However, to avoid unnecessary detail, not every logical equation or logical block diagram of the drawings will be specifically referred to, since the specific equations and diagrams used in the various operating sequences may readily be determined by one skilled in the art.

It should also be noted that in some instances, for convenience in design, the block diagram implementation of particular logical equations will differ somewhat from the exact form of the logical equation, as is commonplace in logical design. Many different variations in stating and implementing the logical equations are available, and the invention accordingly is not deemed to be limited to any single variation. To give one example, it is well known that a logical network employing AND gates may readily be interchanged with one employing OR gates to achieve the same result, by the proper manipulation of terms.

Also, for convenience the following description, the letter combinations, or letter and number combinations (such as TTS or JCA1), used to identify the various logical terms, are also used to identify the signals for these terms, the lines on which these signals appear, and components such as flip-flops and one-shots which provide signals for these terms. Examination of FIGS. 23 to 60 inclusive will show that a definition is provided for each term employed. It may be noted that the inverse of a given term is designated by the addition of a prime (') mark to that term; thus JCA1 is the inverse of JCA5. Also it may be noted that the inputs for setting the various flip-flops and one-shots bear the same designations as those used for the flip-flops and one-shots, except that the initial letter is lower-case rather than upper-case. The inputs for resetting the various flip-flops bear the same designation as those for setting the flip-flops, with the addition of a lower-case “o” preceding the rest of the designation.

Timing elements

To aid in the understanding of the logic employed in these operating sequences, the various clocks and other timing elements used to maintain proper synchronization of the various operating elements of the system will first be described. Reference may be had to the various timing diagrams of FIGS. 104 to 114 inclusive for a graphical representation of the relationship of the various timing elements to each other and to the other components of the sub-system.

A first such timing element is the 1-kc, Receiver Clock DCR. In the illustrated embodiment, this is a square wave signal at one-kilohertz frequency which originates in the data sub-set. The amplitude of this signal as it comes from the data sub-set is from plus 5 volts to minus 5 volts, which is converted by a level converter in the remote controller to the logic levels used therein of zero volts and minus 8 volts.

As transmitted from the data sub-set, this signal is designated DCRP. After being converted to the logical levels for the remote controller, this signal is inverted and applied to an OR gate, together with the inverted Carrier On signal CO'. During normal run conditions, the signal CO is maintained at a constant level of plus 5 volts from the data sub-set, and is converted to zero volts and then inverted to minus 8 volts in the remote controller, before being applied to the OR gate with the signal DCR. This inverter may be seen in the logical block diagram of FIG. 72, while the logical equation is given in FIG. 60.

The inverted signal CO' does not affect the OR gate during normal run conditions, and the output of this OR gate therefore follows the DCR input.

Another OR gate is provided for use when the remote controller is in a test mode. As shown in FIG. 72, the inputs to this gate are the inverted signal SCT of the 2-kc, Transmitter Clock SCT (which will be described subsequently) and the inverted CO. This gate is at zero volts potential during normal run conditions.

The second OR gate does not affect the signal DCR during normal run conditions. However, when the remote controller is operating in test mode, the plus 5-volt signal CO from the data sub-set is switched to minus 5 volts, and the inverted signal SCT is switched off. The CO signal, converted to minus 8 volts, permits the SCT signals to create the DCR and DCR' signals in test mode. The CO' signal is switched during test mode to a converted and inverted zero-volt signal which, applied to the OR gate with the DCR signal, overcomes the effect of the DCR signal.

A second timing element is the 1-kc, Normal Receiver Timing Element TRN, derived from a 55-microsecond one-shot which changes the wave form of the signal DCR' to a 55-microsecond pulse, once every millisecond. The equation for this is shown in FIG. 59, and the block diagram appears in FIG. 69.

A third timing element is the 1-kc, Special Receiver Timing Element TRS, derived from a 55-microsecond one-shot which changes the wave form of the signal DCR to a 55-microsecond pulse, once every millisecond. The equation for this is shown in FIG. 59, and the block diagram appears in FIG. 69.

A fourth timing element is the 2-kc, Transmitter Clock SCT. This is a signal at a 2-kilohertz frequency originating in the data sub-set. The plus 5-volt and minus 5-volt amplitude of this signal is converted to zero volts and minus 8 volts in the remote controller. The signal SCT is, of course, an inversion of the signal SCT. The Clock SCT is defined in FIG. 56 of the logical equations, and the block diagram appears in FIG. 72. With the test switch shown in FIG. 72 in an “on” condition, the 1-kilohertz input of the signal DCT from the data sub-set is fed to the level converter, and the 2-kilohertz input is switched off. The signals SCT and SCT' then become signals of 1-kilohertz frequency.

A fifth timing element is the 2-kc, Normal Transmitter Timing Element TTN, derived from a 55-microsecond one-shot which changes the wave form of the signal SCT to a 55-microsecond pulse twice every millisecond. The equation for this is shown in FIG. 57, and the block diagram appears in FIG. 69.

A sixth timing element is the 2-kc, Special Transmitter Timing Element TTS, derived from a 55-microsecond one-shot which changes the wave form of the signal SCT to a 55-microsecond pulse twice every millisecond. The equation for this is shown in FIG. 57, and the block diagram appears in FIG. 69.

A seventh timing element is the Transmitted Clock CT. This is a 2-kc, gated clock which is used to control the flip-flops of the Transmit Shift Register. Each CT pulse is 55 microseconds in duration and is derived from the Normal Transmitter Timing Element TTN. An additional CT pulse is generated 250 microseconds after every seventh TTN pulse. This extra pulse is produced as a result of the Transmit Shift Register being empty, which occurs every 3.5 milliseconds. Each time the Transmit Shift Register is empty, a DNT pulse is generated. This pulse is synchronized by the Special Transmitter Timing Element TTS, which occurs 250 microseconds after each TTN pulse. When the DNT and TTS pulses are in coincidence, a 55-microsecond pulse DTE is generated, which is identified as the Transmitter Register being empty. This pulse is applied to an OR gate with the pulse TTN, which causes an additional CT pulse after every seventh TTN pulse. The equation for the Transmitter Clock CT is given in FIG. 57, and the block diagram appears in FIG. 69.
An eighth timing element is the Receiver Clock CR. This is a 1-kc, gated clock which is used to control the flip-flops of the Receive Shift Register. Each CR pulse is 55 microseconds in duration and is derived from the Normal Receiver Timing Element TRN, which is a 55-microsecond one-shot. An additional CR pulse is generated 500 microseconds after every seventh TRN pulse. This extra pulse is produced as a result of the Receive Shift Register being full, which occurs every seven milliseconds. Each time the Receive Shift Register is full, its low-order flip-flop FR0 will be set. The output of the flip flop FR0 is synchronized by the Special Receiver Timing Element TRS, which occurs 500 microseconds after each TRN pulse. When the pulses FR0 and TRS are in coincidence, an additional CR pulse of 55 microseconds' duration is generated. The equation for the Receive Clock CR is given in Fig. 59, and the block diagram appears in Fig. 69.

**Input operating sequence**

The input operating sequence, previously described with reference to the block diagram of Figs. 20A and 20B, will now be described in terms of the logic employed.

When power is turned on in the remote controller, a warm-up period of twenty seconds occurs, which allows time for the power supplies to develop the several different voltages required in the system. The data sub-set receives its operating voltages from the remote controller power supply, and, in turn, provides the remote controller with the clocks previously described to control its counters and registers.

When the branch data sub-set and the associated data sub-set at the central data processing station are both in an on-line condition, a Carrier On signal CO and a Clear to Send signal CS are sent to the remote controller and are combined to produce a System On signal JCA4 according to the equation $JCA4 = CO \cdot CS$. The arrangement of logical elements to produce this signal is shown in Fig. 67.

During the warm-up period, a Master Reset signal DRW controlled by contacts of the relay K203 is generated and is applied to the Input and Output Program Counters, the Input and Output Row Counters, the Error Registers, and a Test Counter, if one is included in the system, to assure that these counters are reset to zero by the time the power is fully up.

When the branch system is on-line with the central data processing station, and its power is fully up, the Input Program Counter advances from Count zero to Count 1. The System On signal JCA4 controls the Input Program Counter Clock signal CPI at this time, and the Master Reset Drive signal DR12 permits the Input Program Counter flip-flops to be set after warm-up of the remote controller. The equation for causing the first flip-flop of the Input Program Counter to be set is $F1 = CI \cdot DR12$.

When the first input message segment (normally a balanced pick-up segment) has been introduced by the teller into the window machine, the input mode relays K507 and K513 energize, and the contacts K507A2 close in the Input Flag circuit. This couples the Window Machine Ready Interrogate Line JM19 to the Window Machine Ready Line IM20 in the associated window machine controller. In the example being given, a jumper wire connects line JM19 to position 15 of the board TBCI in the window machine controller, representing window machine number 15 in the branch.

With the Input Program Counter in Count 1, the Scan Counter is advanced when the Scan Counter Clock signal CSI is pulsed, as may be seen by the input equations for the various flip-flops of the Scan Counter given in Fig. 53. The Scan Counter clock signal CSI, in turn, is controlled by the Window Machine Ready signal JWM20 at this time, according to the logical equation $CSI = TTN \cdot FP1(1) \cdot IWM20$.

When the Scan Counter advances to Count 15, the output line representing Count 15 in the associated Binary-to-Decimal Decoder is fed through a level converter, where the minus 8-volt input level is converted to zero volts, to provide a ground for the No. 15 Window Machine Ready Interrogate line JWM55, as expressed by the logical equation $JWM55 = FSI(15)$.

The line JWM55 terminates at position 15 of board TBCI where the line JM19 is connected by its jumper wire. Therefore the lines JM19 and IM20 also are at ground potential, since they are coupled at this time by the closed contacts K507A2.

The signal on the line IM20 is then fed to another level converter, where the voltage level is converted from ground potential to minus 8 volts. The minus 8-volt output from this level converter is then inverted, to provide the Answer Ready signal IWM20. The signal IWM20 goes false, in the Scan Counter Clock gate, which prevents the Scan Counter from advancing further under control of its clock, according to the previously-mentioned equation $CSI = TTN \cdot FP1(1) \cdot IWM20$.

Another output from the level converter, associated with the line JWM20, and the output FSI(15) from the Scan Counter, representing Count 15, are fed to a special relay driver (designated by one of the blocks LM in Fig. 81) for the No. 15 Window Machine Select line JWM15, according to the logical equation $JWM15 = FSI(15) \cdot IWM20$.

The line JWM15 is thus at ground potential, which is effective to cause energization of the window machine select relays in the window machine controller, via the jumper wire connected to position No. 15 of the Select section of the board TBCI.

The signal of zero volts potential level on the line JWM20 is also effective to cause an input signal to be applied to the "on" trigger of the flip-flop which generates the term GC13, according to the equation $GC13 = CFI \cdot FP1(1) \cdot FPO(4) \cdot IWM20 \cdot DRW'(SR' \cdot ST')$

The change of signal level of the output GC13 of the flip-flop, in conjunction with the signal GC13' being true, operates a Time Delay one-shot to generate a signal TD11, which allows time for the window machine relays to energize. The equation for the input to the Time Delay one-shot is $TD11 = GC13 \cdot GC13'$. Energization of the window machine select relays causes their contacts to contact, to prepare the various row and direct select lines, so that the window machine rotary switches can be read-out.

The Sync Memory flip-flop which generates the signal GC1 is set by the signals GC13 and TD11 going true in the expression $CRI(1) \cdot FP1(1) \cdot TD11' \cdot GC13$, which forms a part of the equation for gC11 found in Fig. 34. This produces an output signal GCI to complete the gate for the Input Program Counter Clock CPI according to the equation $GCI = CTI(1) \cdot GC11 + GC12$ given in Fig. 30.

At the fall of the signal for the term CPI, the 2nd flip-flop FP11 of the Input Program Counter is reset, and the 2nd flip-flop FP12 is set, to establish a condition representing Count 2. The equations for setting and resetting these two flip-flops are found in Figs. 32 and 33.

The term GC13 also appears in the equation for the Request to Input Term ICA6 given in Fig. 34. When the signal GC13 goes true, the signal ICA6 goes true and the signal ICA6' goes false. This triggers a 350-millisecond Echo Delay one-shot, which generates a signal for the Echo Delay TD12 according to the equation given in Fig. 37.

Also, the signal ICA6 going true causes the Request to Input Driver line IC16 given in Fig. 35 to go true according to the equation $DRI = JC45' \cdot GR1 \cdot IC16'$. The signal DRI is used in conjunction with the Transmitter Empty signal DTE to set the Parity Bit, 2nd Data
Bit, and Flag Bit flip-flops of the Transmit Shift Register at the fall of the signal for the transmit Shift Register Clock signal CT. This, in effect, builds a Request to Input character in the Transmit Shift Register. The three flip-flops mentioned above generate output signals F12, F13, and F17. The equations for setting these flip-flops are given in FIGS. 56 and 57, and the equation for the Transmitter Clock CT is also given in FIG. 57.

Each succeeding Transmitter Clock Signal CT shifts the contents of each flip-flop of the Transmit Shift Register to its adjacent lower-order flip-flop until the Flag Bit that was set in the flip-flop FT7 reaches the flip-flop FT0. At this time, the Transmit Shift Register is empty.

As the bits of the Request to Input character are shifted out of the Transmit Shift Register, the signals are sent over the Send Data line to a line converter for appropriate conversion of voltage levels and subsequent transmission over telephone lines to the central data processing station.

Within 350 milliseconds from the time that the Request to Input control character was transmitted (before the one-shot generating the signal TD12 times out), the central data processing station must send back a Start Input control character to provide a signal JCA1. It may be noted that the Time Delay one-shot for the signal TD12 will be retrigged in Count 4 of the Input Program Counter.

The Start Input character is shifted serially into the Receive Shift Register in 7 milliseconds. When this character completely occupies the Receive Shift Register, the flip-flops FR0, FR2, and FR4, corresponding to the Flag, Parity, and 21 Data Bit positions are set, and the remaining flip-flops are reset.

The next Receiver Clock signal CR occurs 500 microseconds after the CR signal which shifted the Flag bit into the flip-flop FR0, and causes the Receive Shift Register to be unloaded.

The outputs from the seven flip-flops of the Receive Shift Register are combined in a logical network to produce a start Input Drive signal DS1 when the Register contains a Start Input character, according to the logical equation \( DS1 = FR6' FR' FR3' FR3' FR5' FR5' FR6' DM11' \).

The signal DS1 is effective to set the Start Input Control Memory Latch, which controls the signal GSI. The signal GSI going true, in conjunction with the signal IC6 being true, results in the Start Input signal JCA1 going true according to the equation JCA1 = GSI IC6.

Other outputs from the seven flip-flops of the Receive Shift Register are fed to an Exclusive OR network shown in FIG. 68, which checks the character for proper parity, according to the equation for the Parity Check Drive signal DPC given in FIG. 58.

The signal JCA1 completes a gate to set the Sync Memory flip-flop for the signal GCI1 according to the expression FPI(2) JCA1 CTI included in the logical equation for GCI1 found in FIG. 34.

Signals GCI1 and CTI generate another Input Program Counter clock pulse CPI, which advances the Input Program Counter to Count 3, in which the flip-flop FPI1 is set and the flip-flop FPI2 remains set. The Control Mercury Latch signal GR1 is set, and the Request to Input Drive signal DRI went false when the signal GRI' went false.

A Request for Character signal JCA5 is generated (with the signal DRI' being true) each time that the Transmitter Empty signal TD1E goes true, according to the equation JCA5 = DTE DRI' DOK DER' given in FIG. 59.

Another Main Timing Clock signal CTI is generated by a true signal JCA5, in conjunction with the true output EPI(3) of the Input Program Counter in Count 3 in accordance with the expression FPI(3) JCA5 in the equation for the term CTI given in FIG. 30.

The true signal CTI completes gates to produce true signals CPI and GCI1 in accordance with equations given in FIGS. 30 and 34. This, in turn, advances the Input Program Counter to Count 4, by resetting the flip-flops FPI1 and FPI2, and by setting the flip-flop FPI3, according to the equations given in FIG. 33. It may be noted that the Time Delay one shot TD12 is retrigged in program Count 4, indicating that the central data processing station received a Request to Input signal JCA6 and returned a Start Input signal JCA1.

When an Input Program Counter Clock signal CPI pulses the Input Program Counter, it also, in conjunction with a signal FPI3, generates a Column Counter Clock signal CCI according to the equation shown in FIG. 30. This advances the Input Row Counter from Count 0 to Count 1. It will be recalled that the Input Row Counter was set to Count 0 during system warm-up by the Master Reset signal DRW. The Reset Drive signal DRW' allows the flip-flops of the Input Row Counter to be set following warm-up, as may be seen in the Input Row Counter equations in FIGS. 31 and 32.

The Transmitter Empty signal DTE again goes true 3.5 milliseconds after the Input Program Counter has advanced to Count 4 and causes another Request for Character signal JCA5 to be generated. The signal JCA5 in conjunction with Program Count 4 and Row Count 1 signals, causes the generation of a Data On Line signal ICAD, in accordance with the equation given in FIG. 34.

A Load Data signal DLD is generated by signals ICAD and IC5 in accordance with the equation \( DLD = ICAD IC5 \), given in FIG. 57. Each succeeding signal DTE, while the Input Program Counter is in Count 4, will simultaneously cause the Input Row Counter to advance, and the Transmit Shift Register to be loaded, due to the fact that the signals IC5 and C5 follow the signal DTE; the signal ICAD follows the signal ICAS; and the signal DLD follows the signals ICAD and IC5. Therefore the signal DTE that loads the first character into the Transmitter Shift Register also advances the Input Row Counter to Count 2. During the 3.5 milliseconds time required to shift out the first character, the second character is being sensed from the storage switches of the window machine.

The first character to be loaded into the Transmitter Shift Register is a character representing Scan Position No. 15. The output of each flip-flop of the Scan Counter, in conjunction with the output signal IC5, and the Binary-to-Decimal Decoder of the Input Row Counter, is effective to provide a true signal on each of the four Data Bit lines ICA1, ICA2, ICA3, and ICA4, according to the logical equations for the terms corresponding to these lines found in FIGS. 33 and 34.

An Exclusive OR network is used to check the four Data Bit line outputs to determine whether or not a Parity bit is needed. Since all four lines are true, a Parity signal IC5 is generated in accordance with the equation for IC5 given in FIG. 34.

The signals on the four Data Bit lines are also applied as inputs to the four flip-flops AL11, AL12, AL13, and AL14 of the Input Longitudinal Bit Check Register. At the next fall of the Row Counter Clock signal CCI, the four Input Longitudinal Bit Check Register flip-flops will be set, in accordance with the logical equations for these flip-flops given in FIG. 30.

When the Transmitter Register Empty signal DTE went true, it caused the generation of an additional Transmitter Clock signal CT 250 microseconds after the Flag Bit reached the flip-flop FT0 of the Transmit Shift Register, in accordance with the logical equation \( CT = DTE' \). This signal CT provides the Transmitter Clock pulse necessary to load the Transmit Shift Register.

The Load Data signal DLD, generation of which was previously described, in conjunction with the Data Bit
signals ICA1, ICA2, ICA3, and ICA4, and the Parity Bit signal ICA5, is effective to set the flip-flops FT1 to FT6 inclusive of the Transmit Shift Register at the full of the clock signal CT in accordance with the equations for the flip-flops given in FIGS. 56 and 57. The flip-flop FT7 of the Transmit Shift Register is also set on this clock pulse by the true Transmitter Empty signal DTE, in accordance with the equation for FT7 shown in FIG. 57.

At the same time that the Transmit Shift Register is loaded, the Main Timing Clock signal CTI goes true, in accordance with the expression FPI(4) FCI(0)′ ICA7 included in the equation for CTI found in FIG. 30. This, in turn, generates another pulse for the Row Counter Clock CCI in accordance with the expression CTI FPI(4) FCI(0) FPO(2)′ included in the equation for CCI found in FIG. 30. The pulse CCI advances the Input Row Counter to Count 2 by resetting the flip-flop FC11 and setting the flip-flop FC12 according to the equations of CCI(1)=CCI, and FC12=CCI DRI′ FC1.

With a character representing the window machine scan position No. 15 loaded into the Transmit Shift Register, the character is shifted out serially in 3.5 milliseconds with the next seven Transmitter Clock pulses CT. During this time, the second character is being sensed from the row 14 rotary switch of the window machine in a manner which will be described later.

The output of the flip-flop FC12 of the Input Row Counter is fed to a Binary to Decimal Encoder, the output of which is fed to a level converter, which converts the minus 8-volt input to a potential of zero volts. The zero-volt output from the level converter provides ground potential for the Row 14 Select line JWMM3. The signal on this line pulses the common, or wiper, of the row 14 rotary switch, which is set to the “eliminate” position. Therefore the Zero Answer Digit line IWM10 is also at ground potential.

The outputs of the ten Answer Digit lines IWM1 to IWM10 inclusive are fed to a Decimal to Binary Decoder, where the decimal zero is decoded into a binary zero. The binary lines are fed through level converters to the four Data Digit lines DD1 to DD14 inclusive. The signals on the Data Digit lines are fed to the Data Bit lines ICA1 to ICA4 inclusive, to set all four of these lines false, in accordance with their equations, which are given in FIGS. 33 and 34.

The Data Bit lines are applied to the Exclusive OR Parity network to determine whether or not a Parity Bit signal ICAS should be generated according to the equation given in FIG. 34. Since all four Data Bit lines are false, a signal is generated for the Parity Bit signal ICAS.

It may be noted that the Input Longitudinal Bit Check Register is not affected by the zero digit. When the Flag Bit that was set in the flip-flop FT7 of the Transmit Shift Register is shifted to the flip-flops FT5, a true Transmitter Empty signal DTE is again generated, and true signals ICA5, ICA7, and DLD are generated.

The flip-flops FT1, FT2, and FT7, corresponding to the Data Character Bit, Parity Bit, and Flag Bit, of the Transmit Shift Register are set at the fall of the Transmitter Clock signal CT, which loads the second character into the Transmit Shift Register according to the equations for these flip-flops given in FIGS. 56 and 57.

At the same time that the second character is loaded into the Transmit Shift Register, the Main Timing Clock signal CTI goes true, generating another Input Row Counter Clock signal CCI, in accordance with the equation given in FIG. 30 for CCI, to advance the Input Row Counter to Count 3, which sets the flip-flop FC12 remains set, as may be seen by the equations for these terms given in FIGS. 31 and 32.

While the second character is being shifted out of the Transmit Shift Register, the third character is being sensed from the row 13 storage switch of the window machine in a manner which will now be described.

The output from the Binary to Decimal Encoder for the Input Row Counter in Count 3 is fed to a level converter which converts minus 8 volts to zero volts. The zero-volt output from the level converter provides ground potential for the Row 13 Select line JWMM3. The signal on the line JWMM3 is fed to the common, or wiper, of the row 13 storage switch of the window machine, and it will be assumed for this example that the wiper is set to position 2 of the switch. The No. 2 Answer Digit line IWM12 is therefore also at ground potential. The signal on this line is fed to a Decimal to Binary Decoder. The other nine Answer Digit lines are also connected to the Decimal to Binary Decoder, but their potential is at a minus 20-volt level. The decimal digit 2 is decoded into a binary digit 2, and a signal is fed over the 2′ binary line through a level converter to the 2′ Data Digit Line DD12. The Data Digit lines are then checked, according to the equations listed under “Decimal to Binary Decode” in FIG. 31, to verify that the character which they are transmitting is a proper one.

The signal on the line DD12 is applied to the 2′ Data Bit line ICA2 in accordance with the equation for ICA2 given in FIG. 34. Next, a determination is made, according to the equation in FIG. 34 for the Parity term ICAS, as to whether or not a parity character is generated. Since only the signal on line ICA2 is true, odd parity is satisfied, and the signal ICAS therefore remains false.

The flip-flop AL2 in the Input Longitudinal Bit Check Register is set at the time of the next Row Counter Clock Signal CCI according to the equation acI3=RCCI ICA2 FCI(0)′.

The Load Data signal DLD and the Data Bit 2′ signal ICA2 set the flip-flop FT4 of the Transmit Shift Register at the fall of the Transmitter Clock signal CT. The flip-flops FT1 and FT7, representing the Data Character Bit and the Flag Bit, are also set at the fall of the same CT signal. The equations for setting these flip-flops are given in FIGS. 56 and 57. This third character, which is thus loaded into the Transmit Shift Register, is shifted out of said Register, over the telephone lines to the central data processing station, in the same manner as has been described for the preceding characters.

Sensing of information from the storage switches of the window machine, loading of the Transmit Shift Register, and transmission of the characters to the central data processing station proceed in the manner described above through the operation of the character characterizer. When the seventeenth character, representing control row 3 of the window machine, has been loaded into the Transmit Shift Register, signals ICAS, ICA7, and DLD are generated, causing a Main Timing Clock signal CTI to generate a signal for the Row Counter Clock CCI, according to the equation given in FIG. 30, and advance the Input Row Counter to Count 18, which is the Read Sum Check Digit Count.

With the Input Row Counter in Count 18, the Sum Check Digit for the input message segment is sensed from the flip-flops AL11, AL12, AL13, and AL14 of the Input Longitudinal Bit Check Register. The output FCI(18) of the Binary to Decimal Encoder for Count 18 of the Input Row Counter, in conjunction with the outputs from the Input Longitudinal Bit Check Register flip-flops, sets the signal levels on the Data Bit lines ICA1, ICA2, ICA3, and ICA4 to agree with the Sum Check Digit stored in the flip-flops of the Input Longitudinal Bit Check Register in accordance with the “CLA Input” equations given in FIGS. 33 and 34. For example, it is assumed that the Input Longitudinal Bit Check Register contains a Sum Check Digit of 13, then the signal level is true on lines ICA1, ICA3, and ICA4. It may be noted that a true signal does not appear on
line ICA5 due to the odd number of bits in the Sum Check Digit, which satisfies the Parity requirements. The Transmitter Empty signal DTE following the transmission of the character generates an additional Transmitter Clock signal CT, which, in conjunction with signals DLD, ICA1, ICA3, and ICA4, loads the Sum Check Digit into the Transmit Shift Register. Flip-flops FT1, FT3, FT5, FT6, and FT7 are set, according to the equations given in FIGS. 56 and 57, to provide a Sum Check Digit character consisting of a Data Character Bit, a 2nd Data Bit, a 2nd Data Bit, a 2nd Data Bit, and a Flag Bit.

The transmitter Empty signal DTE, which caused the eighteenth character to be loaded into the Transmit Shift Register, also causes the generation of a signal ICA5, which in turn causes the generation of a Data On line signal ICA7, as shown in the equation given in FIG. 34. This causes the generation of a Main Timing Clock signal CTI, which causes the generation of a Row Counter Clock signal CCI. The equations for these latter equations are given in FIG. 30.

At the fall of the signal CCI, the signals on the lines ICA1, ICA3, and ICA4 are reset to the flip-flops ALI1, ALI3, and ALI4 of the Input Longitudinal Bit Check Register, in accordance with the equations for these flip-flops given in FIG. 30. The Input Row Counter is also reset to Count zero with the same signal CCI used to reset the flip-flops of the Input Longitudinal Bit Check Register. This is accomplished by resetting the flip-flops FC12 and FC15 in accordance with the equations given in FIG. 32. It may be noted that a true signal DR14 is generated, and is used in this reset in the flip-flops FC12 and FC15, by the output of the Input Row Counter in Count 18.

When the Input Row Counter is set to Count zero, and an output representing that count goes true, a signal for the Main Timing Clock CTI also goes true in accordance with the expression FPI(4) FCI(0) TTS, included in the equation for CTI found in FIG. 30.

The Sync Memory flip-flop GC11 is set in accordance with the expression FPI(4) FCI(0) CTI included in the equation for gCTI found in FIG. 34. A true signal for the Input Program Counter Clock CPI is then generated in accordance with the equation
\[ \text{CPI} = \text{CTI}(\text{GCC1}+\text{GCC2}) \]
and this, in turn, is effective to set the Input Program Counter flip-flop FPII in accordance with the Equation fPI1 = CPI DRI11, which advances the Input Program Counter to Count 5.

When the output FPI(4) of the Input Program Counter representing Count 4 goes false, the Time Delay one shot TD12 is triggered, and commences a 350-millisecond delay period, in accordance with the equation td12 = ICA6 FPI(5) FPI(7) + FPI(4) + FPI(6). The central data processing station must now return an Input O.K. Answer signal JCA2 before the one shot TD12 times out, in order to avoid an error indication.

Let it be assumed that the input message segment was O.K., and that the central data processing station has transmitted back to the branch in Input O.K. control character. When the Input O.K. control character has been completely shifted into the Receive Shift Register, the flip-flops FR0, FR2, and FR5, representing the Flag Bit, the Party Bit, and the 2nd Data Bit are set, and the Input O.K. signal JCA2 goes true in accordance with the equation
\[ \text{JCA2} = \text{FR0} \text{FR1} \text{FR2} \text{FR3} \text{FR4} \text{FR5} \text{FR6} \]
With the signal JCA2 true, and the Input Program Counter output FPI(5) true, the Main Timing Clock signal CTI also goes true in accordance with its equation given in FIG. 30. Since the signal GCC1 is also still true, an Input Program Counter Clock signal CPI is generated in accordance with the equation
\[ \text{CPI} = \text{CTI}(\text{GCC1}+\text{GCC2}) \]
This advances the Input Program Counter to Count 6, by resetting flip-flop FPII and setting flip-flop FPI6. The flip-flop FPI3 remains set. Equations for these flip-flops are found in FIGS. 32 and 33.

The Sync Memory flip-flop GC13 is reset at the fall of the same Main Timing Clock signal CTI, which advances the Input Program Counter to Count 6, in accordance with the expression FPI(5) AEI1' AEI2' CTI included in the equation for opGC13 found in FIG. 34. This, in turn, causes the Request to Input signal ICA6 to go false in accordance with the equation
\[ \text{ICA6} = \text{GC13} \text{AEI1'} \text{AEI2'} \]
The Sync Memory flip-flop GC12 is also reset at the fall of the same Main Timing Clock signal CTI which advances the Input Program Counter to Count 6, in accordance with the equation opGC11 = CTI FPI(4)'.

When the Input Program Counter advances to Count 6, and the output signal FPI(6) goes true, the Time Delay one shot TD12 is retriggered in accordance with the equation
\[ \text{td12} = \text{ICA6} FPI(5) FPI(7) + FPI(4) + FPI(6) \]
The Input Program Counter advances to Count 7 with the next Main Timing Clock pulse CTI, by the setting of the flip-flop FPI1, while the flip-flops FPI2 and FPI3 remain set. The pulse CTI is generated in accordance with the expression TTS FPI(3) FPI(4) FPI(5) included in the equation for CTI given in FIG. 30. The Sync Memory flip-flop GC11 is set by the pulse CTI in accordance with the expression CTFI FPI6 GC12 included in the equation for gCTI given in FIG. 34. Setting of the flip-flop GC11, in turn, is effective to generate an Input Program Counter Clock signal CPI in accordance with the equation CPI = CTI(GC11+GC12). This signal then sets the flip-flop FPI1 in accordance with the equation fPI1 = CPI DRI11.

The Time Delay TD12 starts to time out when the signals FPI(7)' and FPI(6) go false, in accordance with the equation for d12 found in FIG. 37. Now the signal IWM20 must go false to retrigger the Time Delay TD12 before it completely times out, or an error indication will be set.

With the Input Program Counter in Count 7, an End of Segment signal JVM37 is sent from the remote controller to the window machine controller to interrupt the Window Machine Ready line IWM20. The signal JVM37 is generated in accordance with the equation given in FIG. 35, and particularly the signal FPI(7) (indicating the output of the Input Program Counter in Count 7), and the signals AEI1' and AEI2' (indicating that no error is present).

The signal on the End of Segment line JVM37 is fed to the relay K107 in the window machine controller, which causes this relay to be energized, thereby opening the contacts K107BC1. These contacts are in the energizing circuits for the relays K507 and K513 in the window machine, and said relays are thus deenergized. The contacts K507AC2, controlled by the relay K507, open in the circuit which includes the lines JMN19 and IM20. This interrupts the Answer Ready line and causes the signal on the Window Machine Ready line JVM20 to go false, which retriggers the Time Delay TD12 and thus prevents the setting of an error indication.

Also the Input Program Counter is advanced to Count zero by the signal JVM20 (which is the inverse of signal JVM37) going true. A true signal from the Special Transmitter one shot TTS generates a true signal for the Main Timing Clock CTI in accordance with the expression TTS FPI(3) FPI(4) FPI(5) included in the equation for CTI found in FIG. 30. The true signal CTI, in
conjunction with the true signal IWM20', and the true signal FPI(7) of the Input Program Counter in Count 7, sets the Sync Memory flip-flop GCI1 in accordance with the expression CFI FPI(7) IWM20' TD1' included in the equation for gCII found in FIG. 34. An Input Program Counter Clock signal CPI is generated in accordance with the equation CPI = CFI (GCI1 + GCI2). The signal CPI is now effective to reset the flip-flops FPI1, FPI2, and FPI3, according to the resetting equations for these flip-flops given in FIGS. 31 and 32, thereby advancing the Input Program Counter to Count zero.

When the Input Program Counter advances to Count zero, the signal FPI(7)' goes true, representing the inverse of the output of the Input Program Counter in Count 7. This retriggered the Time Delay one shot TD12 according to the equation

\[ iD12 = ICA6' FPI5'(S) FPI7' + FPI(4) + FPI(6) \]

The Input Program Counter advances to Count 1 on the next pulse of the Main Timing Clock CT1 which is generated according to the expression TTS FPI(3)' FPI(4)' FPI(5)' included in the equation for CTI found in FIG. 30. The Sync Memory flip-flop GCI1 is again set in accordance with the expression CTI FPI(8) FCI(8) JCA4 included in the equation for gCII found in FIG. 34. A true pulse is generated for the Input Program Counter Clock CPI in accordance with the equation

\[ CPI = CFI (GCI1 + GCI2) \]

and this pulse is effective to set the flip-flop FPI1 of the Input Program Counter according to the equation

\[ FPI1 = CPI DR12' \]

thus advancing said Counter to Count 1.

Pulsing commences for the Scan Counter Clock CSI when the Input Program Counter is advanced to Count 1, which causes a true signal FPI(1) in accordance with the equation CSI = TTS FPI(1) IWM20'. The Scan Counter resumes counting, and the Input Program Counter remains in Count 1, until another window machine is found which provides a true IWM20 signal which stops the Scan Counter from advancing.

Output operating sequence

The output operating sequence, previously described with reference to the block diagram of FIGS. 20A and 20B, will now be described in terms of the logic employed.

After power has been turned on in the system, and the warm-up period has been completed, the Output Program Counter Reset Drive signal DRO1 goes false, which permits the Output Program Counter flip-flops to be set. Advancement of the Output Program Counter from Count zero to Count 1 is accomplished by setting the 2nd flip-flop FPO1.

An output Program Counter Clock pulse CPO is required to set the flip-flop FPO1, and the pulse CPO is generated by a combination of a Sync Memory signal GCO1 and a Main Timing Clock Signal CTO. The Sync Memory flip-flop is set in accordance with the expression CTO DRW' FPO(0) FCO(0) JCA4 included in the equation for gCO1 found in FIG. 49. The Main Timing Clock signal CTO is generated in accordance with the expression DRW' JCA5 FPO(0) included in the equation for CTO given in FIG. 47. The signal GCO1 and CTO are combined to produce an Output Program Counter Clock pulse in accordance with the equation for CPO given in FIG. 46.

The signal CPO is combined with the signal DRO1' to set the flip-flop FPO1 in accordance with the equation

\[ FPO1 = CPO DR01' \]

given in FIG. 48. It may be noted that the flip-flops of the Output Program Counter are shown in the logical block diagram of FIG. 90.

The Output Program Counter then advances to Counts 2, 3, and 4 with each succeeding Output Program Counter Clock signal CPO, which in each case is controlled by the same main signals as given above. However, the signal combinations for producing the main signals CTO and GCO1 in accordance with the equations in FIGS. 47 and 49 are different for each count. To advance the Output Program Counter from Count 1 to Count 2, the expression for generating a signal CTO is TRS FPO(1), and the expression for generating a signal GCO1 is CTO DRW' FPO(1) JCA106'. To advance the Output Program Counter from Count 2 to Count 3, the expression for generating a signal CTO is DRW' JCA5 FPO(2), and the expression for generating a signal GCO1 is CTO DRW' FPO(2).

To advance the Output Counter from Count 3 to Count 4, the expression for generating a signal CTO is TRS FPO(3), and the expression for generating a signal GCO1 is CTO DRW' FPO(3).

The Output Program Counter thus advances to Count 5 and remains there until a Request to Output Character is received from the central data processing station. The Request to Output Character includes a Flag Bit, a Parity Bit, and a 2's Data Digit Bit. When this character has been entered into the Receive Shift Register, a Request to Output character in the Receiver Register signal DRO is generated in accordance with the equation given in FIG. 59.

The signal DRO is effective to set the Request to Output Memory latch GRO, shown in the block diagram of FIG. 65, in accordance with the equation gRO = DRO. Setting of the latch GRO provides a true Request to Output signal JCA106 in accordance with the equation

\[ JCA106 = GRO \]

The Output Program Counter now advances to Count 5. In this case, the expression for generating a signal CTO is TRS FPO(4), and the expression for generating a signal GCO1 is FPO(4) JCA106 CTO.

The Output Row Counter is reset to Count zero during the warm-up period in accordance with the equations in FIG. 48 by a Reset Row Counter signal DRO2 which is true when the Master Reset signal DRW is true. The same Output Program Counter Clock signal which advanced the Output Program Counter to Count 5 also advances the Output Row Counter from Count zero to Count 1. An Output Row Counter Clock signal CCO is generated in accordance with the expression FPO(4) CP0 included in the equation for CCO given in FIG. 46. A true signal CCO then sets the Output Row Counter flip-flop FCO1 in accordance with the equation

\[ FCO1 = CCO DR02' \]

The Output Program Counter now remains in Count 5, which is the Load Keyboard count, and is unable to advance until the Output Row Counter reaches its Count zero.

The first character of the output message segment, which is the Window Machine Select Position, immediately follows the Request to Output character in transmission from the central data processing station. Let it be assumed that the first character represents Window Machine Select Position No. 15.

When the Window Machine Select Position character has been shifted into the Receive Shift Register, Parity is checked, and a Character Present (also termed Clock Data) signal JCA107 is generated. The Window Machine Select Character No. 15 contains a Flag Bit, a Data Bit, a Parity Bit, a 2's Bit, a 2's Bit, and a 2's Bit. It is thus seen that all seven of the flip-flops in the Receive Shift Register are set in this case.

The character is checked for proper parity, and causes generation of a true Odd Parity Clock signal DPC when parity is correct, in accordance with the equation for DPC given in FIG. 58, and shown in block diagram form in FIG. 68.
A Receiver Clock signal CR is generated in accordance with the equation \( CR = TRN + FR0 \) TRS, given in FIG. 59. This signal is combined with FR0 and FR1 signals to produce a Character Present signal JCA107 in accordance with the equation JCA107 = FR0 FR1 CR, found in FIG. 59.

The Character Present signal JCA107 is used to gate the Output Select Register, the Output Data Register, the Output Longitudinal Bit Check Register, the Blow-Out SCR signal, and various time delays.

The output lines from the Receive Shift Register flip-flops are designated FR0, FR1, FR2, FR3, FR4, FR5, and FR6. Of these, the lines FR3 to FR6 inclusive provide signals for the Data Bit 29, 21, 25, and 23 lines JCA104 to JCA104, respectively, according to the equations JCA101 = FR3, JCA102 = FR4, JCA103 = FR5, and JCA104 = FR6, given in FIG. 59. The block diagrams relating to these equations are found in FIGS. 67 and 71. The lines JCA101 to JCA104 inclusive form inputs to the Output Select Register latches ASO1 to ASO4 inclusive, according with the equations for ASO1, ASO2, ASO3, and ASO4 found in FIG. 46.

The outputs of the Output Select Register latches are fed to a Binary to Decimal Decoder network, where one of sixteen output lines will be at a true signal level. This line is connected to the associated Delay Driver, which provides a ground on one of the Window Machine Select lines, in this case line JWM115, in accordance with the equations for the Window Machine Select lines given in FIGS. 50 and 51 and the block diagram of FIGS. 86 and 86A.

The zero-volt signal on the line JWM115 energizes the output select relays in the window machine controller associated with window machine No. 15 through the appropriate connection in the program board TBC1 of the window machine controller, as has been previously described.

The line JWM115 also provides ground to the Window Machine Output Interrogate line JM100, which is coupled to the Window Machine Output Answer Ready line JM101 over Output Flag Circuit contacts in the window machine, as shown in FIGS. 15, 17A, and 17B. The line JM101 returns to the remote controller as the Window Machine Ready line JWM101, and the signal thereon provides an indication to the remote controller that the window machine is ready to receive an output message segment.

In addition, the line JWM115 is connected over contacts K309A1C1 in the window machine controller to the Window Machine On line JWM102, as shown in FIGS. 17A and 17B, and the signal on this line indicates to the remote controller that the window machine is in an online condition.

The Data Register flip-flops AD01 to AD04 inclusive are also set to the same configuration as the Output Select Register latches by the same JCA107 signal inverted, in accordance with the Output Data Register equations given in FIG. 45.

All of the four Output Data Register flip-flops are used as inputs to the Output Longitudinal Bit Check Register in accordance with the equations of FIGS. 45 and 46, and as inputs to the Binary to Decimal Decoder network for the Output Data Register.

The Output Longitudinal Bit Check Register signal CLO is generated by the fall of the JCA107 signal, which occurs 55 microseconds after the fall of the inverse signal JCA107', in accordance with the equation CLO = JCA107 FPO(5) FCO(0)' + CFO FPO(3), given in FIG. 46. This 55-microsecond delay is necessary to provide time to allow the Output Data Register flip-flops to change states prior to the clocking of the Output Longitudinal Bit Check Register.

The inputs to the Output Longitudinal Bit Check Register from the Output Data Register flip-flops cause the Output Longitudinal Bit Check Register flip-flops to change state to conform to the configuration of the inputs thereto as of the time of the fall of the signal JCA107.

The first signal JCA107 also generates a Blow-Out SCR signal DBO in accordance with the expression JCA107 FPO(5) which is included in the equation for DBO given in FIG. 47. In addition, this signal JCA107 triggers the Deionization (500 microseconds) Time Delay TD04 and the Inhibit (1 millisecond trigger for TD01) Time Delay TD06 according to the equations

\[
\begin{align*}
\text{TD04} & = \text{FPO(5)}(\text{JCA107 \ FCO(0)' + CFO}) \\
\text{TD06} & = \text{FPO(5)}(\text{JCA107 \ FCO(0)' + CFO})
\end{align*}
\]

both found in FIG. 52.

The Inhibit Time Delay signal TD06 triggers the Clock Detector (60 millisecond retig). Time Delay TD01 according to the expression FPO(5) TD06 (when there are no errors) included in the equation for \( \text{dDO1} \) found in FIG. 52.

Timing out of the Time Delay TD04 causes the FIRing Pulse (55 microseconds) Time Delay TD05 to be triggered in accordance with the equation \( \text{dDO5} = \text{TD04} \). The Time Delay TD05 is a 55-microsecond One Shot which generates a signal that affects the FIRing Pulse SCR signal DFO and the Output Row Counter Clock signal CCO.

The FIRing Pulse SCR signal DFO is generated in accordance with the equation for DFO given in FIG. 47. This signal gates the output of the Binary to Decimal Decoder associated with the Output Data Register, in accordance with the "Digit Lines" equations given in FIG. 50. These nine output lines drive the Solenoid Matrix Grounders. In this case, a Ground circuit is not fired because the Window Machine Select Position number is fifteen and the decoding network has only nine output lines. Of course, even when the Window Machine Select Position number is nine or less, no Solenoid Matrix Driver is fired, and no key of the window machine keyboard is depressed.

The Output Row Counter is advanced to Count 2 at the fall of the Time Delay signal TD05. A Row Counter Clock signal CCO is generated in accordance with the expression FPO(5) FCO(0)' TD05 included in the equation for CCO found in FIG. 45. This clock signal is effective to reset the Output Row Counter flip-flop FC01 and set the flip-flop FC02 in accordance with the equations \( \text{FC01} = \text{CCO} \) and \( \text{FC02} = \text{CCO} \text{FC01 DRO2} \).

The second character of the output message segment is always zero. This zero causes a signal JCA107 to be generated, and causes the Time Delay TD05 to be advanced. The time Delay TD05 then advances the Output Row Counter to Count 3 by generating a clock signal CCO in accordance with the equation in FIG. 46, which is effective to change the state of the flip-flop of the Output Row Counter in accordance with the equations for those flip-flops given in FIG. 48.

There are no "NOD" Characters ("no data" characters inserted for timing synchronization purposes) following any zero in the output message segment, since no delay is required following a zero to pull down a key on the window machine keyboard. Therefore the next character in the output message segment follows the zero in seven milliseconds.

Let it be assumed that the next significant digit in the output message segment is a digit 6 in Count 9 of the Output Row Counter, corresponding to row 7 of the window machine keyboard, which is the dollar row. When this digit 6 is shifted into the Receive Shift Register, parity is checked, and a Character Present signal JCA107 is again sent to the output section of the remote controller.

As the fall of the inverse signal JCA107, the Output Data Register flip-flops are set to the binary configuration representing the decimal number 6. The Time Delay signal TD04 is generated by the signals FPO(5) JCA107 and FCO(0)', as given in the equation in FIG. 52.
At the fall of the signal JCA107, a Longitudinal Bit Register Clock signal CLO is generated in accordance with the equation given in FIG. 46. It should be noted that the Output Longitudinal Bit Check Register is a four flip-flop register which is loaded in parallel, digit by digit, with the digit strain character. On each operation of each flip-flop is therefore similar to that of a one-bit adder with no carry. Flip-flop ALO1 is loaded with the low order data bit from the flip-flop AD01; flip-flop ALO2 is loaded with the higher order data bit from the flip-flop AD02, and so on. Each flip-flop AD01 to AD04 inclusive receives a data bit simultaneously at both the "set" and the "reset" inputs. Receiving a "one" bit, or true signal, always causes the flip-flop to change from its previous state, regardless of whether it was previously set or reset. Flip-flop switching occurs on the fall of the clock signal CLO.

At the fall of the signal JCA107, the Output Longitudinal Bit Check Register flip-flops therefore change states as per the configuration of the digit set into the Output Data Register flip-flops AD01 to AD04 inclusive at the preceding fall of the inverse signal JCA107. In this example, the flip-flops AD02 and AD03 are set, and the Output Longitudinal Bit Check Register flip-flops ALO1 to AD04 inclusive are all true, in accordance with the Window Machine Select number fifteen. Since the flip-flops AD02 and AD03 are set, or true, the flip-flops ALO2 and ALO3 will change state to a reset, or false, condition at the fall of the signal JCA107, while the flip-flops ALO1 and AD04 remain set, or true.

The Denoization Time Delay signal TD04 follows the signal JCA107, as in the preceding description. Also, the signal JCA107 gates the SCR Blow-Out Pulse DBO to blow out any silicon controlled rectifiers in the Soleonoid Matrix Driver and Ground circuits which may have been fired, although in this example, none has been fired up to this time.

The SCR Firing Pulse DFO goes true when the Time Delay TD05 goes true, in accordance with the equation found in FIG. 47. As previously described, the signal DFO gates the output of the Binary Decimal Decoder associated with the Data Register, in accordance with the "Digit Lines" equations given in FIG. 50. In this example, an output signal is generated for the No. 6 output line JW146', in accordance with the equation

\[
JW146" = AD0(6) DFO FCO(0)'
\]

The line JW146' will switch to a minus 8-volt level for 55 microseconds, and will trigger the Soleonoid Matrix Ground circuit for the digit six output.

During the previous Row Counts 3 to 8 inclusive, a Soleonoid Matrix Driver circuit was fired for each row. This was not effective to energize a solenoid to pull down a key of the window machine keyboard, however, because no Soleonoid Matrix Grounder circuit was fired in any of these cases, since there were zeros in these row count positions of the output message segment. The same SCR Blow-Out Pulse DBO referred to above serves to deenergize the silicon controlled rectifier for row 8.

The same SCR Firing Pulse DFO referred to above also gates the output signals for the Row Select lines JW121' to JW133' inclusive. The equations for these lines are found in FIGS. 49 and 50, and the corresponding block diagram is shown in FIGS. 85A, and 85B. The line JW127' is the line corresponding to row 7 of the window machine keyboard, and a signal thereon is effective to fire the row 7 Soleonoid Matrix Driver circuit.

A plus 50-volt D.C. potential is now available to the solenoids for the No. 7, or dollar, row of the window machine keyboard, and ground potential is now connected to the number six digit line associated with the solenoids for the digit 6 keys in the various rows of the window machine keyboard. Accordingly, a current path is completed from a source of plus 50-volt potential over the row 7 solenoid driver circuit, the No. 6 solenoid of row 7, and the No. 6 solenoid grounder circuit, to a ground connection. This is effective to energize the No. 6 solenoid in row 7, thus causing the corresponding key to be depressed on the window machine keyboard.

At the fall of the inverse signal JCA107, the Output Row Counter is advanced to Count 10. The next Clock Data signal JCA107 is generated after the six "NOD" (no data) characters which follow a character greater than zero to allow the Driver and Grounder circuits to remain energized for 49 milliseconds to assure sufficient time for the window machine key to be depressed, and after the next data character has been received from the central data processing station.

The output data character to be received in Count 10 of the Output Row Counter is zero, in the example. When the zero for Count 10 has been shifted into the Receive Shift Register, it causes a signal JCA107 to be generated, causes the set Output Data Register flip-flops AD01 to AD04 to be reset, and causes the Time Delay TD04 to be set, and to begin a 500-microsecond time-out.

The signal JCA107 gates the SCR Blow-Out Pulse DBO in accordance with the expression JCA107 FPO(5) included in the equation for DBO given in FIG. 47. This causes the row 7 silicon controlled rectifier and the digit 6 silicon controlled rectifier, both previously fired as described above, to be extinguished. The fall of the Time Delay signal TD05, which in turn was triggered by the timing out of the expression TD04, as previously described, generates a Row Counter Clock signal CCO, which advances the Output Row Counter to Count 11.

The same sequence of operations as described above for Count 10 is followed in Count 11, in which a zero is also received, in the illustrated example. When the Time Delay signal TD05 again falls, another signal CCO is generated, which advances the Output Row Counter to Count 12.

The character received from the central data processing station in this count represents a Lamp Digit, and for the purpose of this example, it will be assumed that a digit 12 representing a particular "hold" condition to be designated by the system user, is received in the Receive Shift Register, and is set into the flip-flops of the Output Data Register at the fall of the inverse signal JCA107, so that the flip-flops AD03 and AD04 are set.

The signal JCA107 triggers the Time Delay TD04 in the manner previously described. At the fall of the signal JCA107, the Output Longitudinal Bit Check Register flip-flops ALO1 to AD04 inclusive change states in accordance with the states of the Output Data Register flip-flops, as previously described.

Triggering of the Time Delay TD04 causes the Lamp Reset (25 milliseconds) Time Delay TD03 to be triggered, in accordance with the equation \( iD03 = FCO(12) TD04 \), given in FIG. 52.

The signal JCA107 also triggers the Inhibit (1 millisecond trigger for TD01) Time Delay TD06 in accordance with the equation

\[ TD06 = FPO(5) JCA107FCO(0)' + CPO \]

found in FIG. 52.

Timing out of the Time Delay signal TD06 causes a true Lamp Reset signal to be generated and maintained on the line JWM175 as the output of a latch in the event that one or more of the Lamp Digit Control lines JWM171 to JWM174 inclusive had previously been true, in accordance with the equation

\[ JWM175 = TD01 \]

\[ TD06(JWM171 + JWM172 + JWM173 + JWM174), \]
given in FIG. 51, and the corresponding block diagram shown in FIG. 93. The signal on the line JWM175 is transmitted to the window machine controller for the selected window machine, where it is effective to energize the relay K205 (FIG. 16A), thereby opening the contacts.
A digit character is transmitted to the Receive Shift Register from the central data processing station during Row Count 15. The output Data Register flip-flops AD04 inclusive are set to this configuration, and the Output Longitudinal Bit Check Register flip-flops ALO1 to ALO4 inclusive change state as per the settings of the flip-flops AD01 to AD04 inclusive, in the manner previously described. At the subsequent fall of the Time Delay signal TDO5, the solenoid driver for digit 8 and the solenoid gronder for the digit 8 are fired, thus causing the "Receive" key in control row 1 of the window machine keyboard to be pulled down by its solenoid. The Output Row Counter Clock Signal CCO follows the signal TDO5 and advances the Output Row Counter to Count 16 at the same time as the pulling down of the "Receive" key by its solenoid is initiated.

In the illustrated example, the character shifted into the Receive Shift Register from the central data processing station during Count 16, relating to the control row 2 of the window machine keyboard, is a zero. Accordingly, no key is pulled down in control row 2, but the window machine keyboard, and the Output Row Counter is advanced to Count 17.

With the Output Row Counter in Count 17, a digit 9 character is transmitted to the Receive Shift Register from the central data processing station. The Output Data Register flip-flops AD01 to AD04 inclusive are set to this configuration, and the Output Longitudinal Bit Check Register flip-flops ALO1 to ALO4 inclusive change state as per the settings of the flip-flops AD01 to AD04 inclusive, as has been previously explained. At the subsequent fall of the Time Delay signal TDO5, the solenoid driver for row 3, and the solenoid gronder for the digit 9, are fired, thus causing the A Deposit key in control row 3 of the window machine keyboard to be pulled down by its solenoid. The Output Row Counter Clock signal CCO follows the signal TDO5 and advances the Output Row Counter to Count 18 at the same time as the pulling down of the A Deposit key by its solenoid is initiated.

After the customer six "NOD" characters have been received by the Receive Shift Register following the seventeenth character, the Sum Check character is received in Count 18. This character represents the Longitudinal Bit Sum of the seventeen data characters transmitted to the branch from the central data processing station during the output message segment. Assuming that there are no errors, the digit value of the Sum Check character received by the Receive Shift Register in Count 18 is the same as the digit value of the character stored in the Output Longitudinal Bit Check Register at this time. Therefore the flip-flops of the Output Data Register which are set from the Receive Shift Register in accordance with the value of the Sum Check Character correspond in their settings to the flip-flops of the Output Longitudinal Bit Check Register which have been set according to the Sum Check character accumulated in that register. Accordingly, at the fall of the signal JCA107 in Count 18, those flip-flops of the Output Longitudinal Bit Check Register which are set by virtue of the inputs from the corresponding flip-flops of the Output Data Register, and the Output Longitudinal Bit Check Register is therefore reset to zero, assuming no error, so that a signal ALO(0), representing the logical product of the inverted output of each of the flip-flops ALO1 to ALO4 inclusive of the Output Longitudinal Bit Check Register, is true, in accordance with the equation $ALO(0) = ALO' 1 \cdot ALO' 2 \cdot ALO' 3 \cdot ALO' 4$, which is shown in block form in FIGS. 91 and 91A.

The Time Delay TDO5 is triggered, in the manner previously described, when Time Delay TD05 and falls out in Row Count 18. This produces true signal for the Output Row Counter Clock CCO, which follows the Time Delay signal TDO5 in accordance with the expression $FPO(5) \cdot FCO(0)' \cdot TDO5$ included in the equation for CCO given in FIG. 46.
Also the Reset Drive signal DRO2 is true at this time in accordance with the expression FPO(5) FCO(18) included in the equation for DRO2 given in FIG. 48.

A true Reset Drive signal DRO2, in combination with a true Output Row Counter Clock signal CCC, is effective on the setting of the flip-flops FPOL according to the equation oPO1 = CPO, and by the setting of the flip-flops FPOL according to the equation FPO1 = CPO FPO1 DRO1'. It will be seen that, to reset the flip-flop FPOL and to set the flip-flop FPOL, an Output Program Counter Clock signal CPO is required. This signal is generated in accordance with the expression CTO GCO1 included in the equation for CPO given in FIG. 46.

The Main Timing Clock signal CTO is generated in accordance with the expression TRS FPO(5) included in the equation for CTO given in FIG. 47.

The Sync Memory flip-flop GCO1 is set to provide a true signal in accordance with the expression FPO(5) FCO(0) TDO1 included in the equation for GCO1 given in FIG. 49.

The Clock Detector Time delay TDO1 is a 65-millisecond time delay which times out when not retriggered by the inhibit Time Delay TDO6, which in turn, is triggered by the Character Present signal JCA107. The time delay TDO1 is not retriggered after the eighteenth character of the output message segment is received, and consequently will time out.

Timing out of the Time Delay TDO1 is effective to set the Sync Memory flip-flop GCO1 in accordance with the expression for GCO1 given above. This, in turn, is effective to generate an Output Program Counter Clock pulse CPO, which resets the flip-flop FPOL and sets the flip-flop FPOL to advance the Output Program Counter to Count 6.

Program Count 6 is a Delay count in which provision is made for an Automatic Override operation of the system in the event that an output error has been detected. The Time Delay TDO1 is retriggered and held true in Count 6, as shown by the equation for TDO1 given in FIG. 52.

The Error Override (49 milliseconds) Time Delay TDO2 was not triggered in accordance with the equation for TDO2 given in FIG. 52 when the Output Row Counter returned to zero in the illustrated example, due to the fact that there was no error. It may be noted that the terms (AE01 + AE02 + AE03 + AE04) in the equation for TDO2 relate to various types of errors. The Time Delay signal TDO2 is therefore false during Count 6 in the illustrated example.

A Main Timing Clock signal CTO is generated in accordance with TRS FPO(6) included in the equation for CTO given in FIG. 47.

The Sync Memory flip-flop GCO1 is set in accordance with the expression CTO FPO(6) TDO2', which is included in the equation for GCO1 given in FIG. 49. Setting of this flip-flop produces a true signal GCO1, which is effective to generate a true Output Program Counter Clock signal CPO in accordance with the expression GCO1 CTO included in the equation for CPO given in FIG. 46. This advances the Output Program Counter to Count 7 by setting the flip-flop FPOL according to the equation fPO1 = CPO DRO1', while the flip-flops FPOL and FPO3 remain set.

With the Output Program Counter in Count 7, a Window Machine Trip signal JWM190 is sent from the remote controller to the selected window machine (in this case, the No. 15) to trip said window machine for operation. This signal is generated and maintained by a latch, as shown diagrammatically in FIG. 49, the input for the latch being given by the equation JWM(190) = ASOS FPO(7) TD01.

The signal ASOS was set true by a latch (see FIG. 86) in accordance with the equation oSO5 = FPO(5) FCO(1) JCA107 by the first signal JCA107 in Row Count 5, and has remained true during the intervening period, since it is not reset until the Output Program Counter returns to Count zero, as shown by the equation oSO5 = FPO(0).

The Time Delay TDO1 is no longer held true when the Output Program Counter advances to Program Count 7. Therefore, 65 milliseconds after the advance of the Program Counter to Count 7, the Time Delay TDO1 times out, and its output signal goes false. This limits the Window Machine Trip signal to 65 milliseconds duration.

Timing out of the Time Delay TDO1 also causes the Output Program Counter to advance to Count zero. The Sync Memory flip-flop GCO1 is set by the signal TDO1 going false, in accordance with the expression CTO FPO(7) TDO1 included in the equation for GCO1 given in FIG. 49. It may be noted that a true Main Timing Clock signal CTO is provided by the expression TRS FPO(7) included in the equation for CTO given in FIG. 47.

The true signals GCO1 and CTO are effective to generate an Output Program Counter Clock signal CPO in accordance with the equation given in FIG. 46. This is effective to reset all three of the Output Program Counter flip-flops FPOL, FP02, and FPO3, as shown by the equations of FIG. 48, and thus advance the Output Program Counter to Count zero. This is a Delay count in which the latch ASOS is reset in accordance with the equation oSO5 = FPO(0).

When the Transmit Shift Register is empty, a Request for Character signal JCA5 is generated in accordance with the equation JCA5 = DTE DRI DRE. This signal is provided to maintain proper timing synchronization between the Transmit Shift Register and the Output Program Counter, and generates a Main Timing Clock signal CTO in accordance with the expression JCA5 FPO(0) included in the equation for CTO given in FIG. 47. The Sync Memory flip-flop rC01 is set in accordance with the expression CTO FPO(0) FCO(0) JCA4 included in the equation for GCO1 given in FIG. 49.

An Output Program Counter Clock pulse is then generated according to the expression GCO1 CTO, and this advances the Output Program Counter to Count 1, which is the Answer Count. In this Count, the remote controller generates an Answer Output O.K. signal JCA102 in response to true signals FPO(1) and JCA106, and the assumed absence of errors, as given in the equation for JCA102 in FIG. 49.

The signal JCA102 is used to generate an Output O.K. signal DOK in accordance with the equation DOK = DRI' JCA5 JCA102. When there has been no Request to Input signal, and the Transmit Shift Register is empty, the Output O.K. control character is loaded into the Transmit Shift Register by setting the flip-flops FT2, FT5, and FT7 of that Register, in accordance with the equations given in FIG. 56, and said control character is shifted out of said register for transmission to the central data processing station.

The Request to Output Memory latch gro, shown in FIG. 65, is reset according to the equation ogRo = CT(DER DTE + DOK DTE + DMI1) given in FIG. 58, when the Output O.K. control character is loaded into the Transmit Shift Register.

When the signal GRO goes false, the Request to Output signal JCA106 goes false, according to the equation JCA106 = GRO, and this sets the Sync Memory flip-flop GCO1 in accordance with the expression FPO(1) JCA106 included in the equation for GCO1 given in FIG. 49.
A true signal is generated for the Main Timing Clock CTO in accordance with the expression TRS FPO(1) included in the equivalent described for CTO given in FIG. 47.

The true signals GCO1 and CTO combine to produce a true Output Program Counter Clock signal CPO, which advances the Output Program Counter to Count 2, which is used to send the Type of Output Error. However, it is assumed in the present example that all transmissions have been completed and CTO cannot go true.

When the Transmit Shift Register is again empty, the Output Program Counter is advanced to Count 3 by the Output Program Counter Clock CPO in accordance with the equations CTO = JCA5 FPO(2); gC01 = CTO FPO(2)

and CPO = CTO GCO1. Program Count 3 is used for reset purposes, and the Output Select Register is reset at this time in accordance with the equations oasD01 to oasD04 inclusive = FPO(3), given in FIG. 46.

The Error Ready line IWM20 advances from Count 3 to Count 4 by the next Output Program Counter Clock signal CPO in accordance with the equations CTO = TRS FPO(3); gC01 = CTO FPO(3)

and CPO = GCO1 CTO. The Counter remains in Count 4 until another Request to Output character is received from the central data processing station.

INPUT ERROR DESCRIPTION

Input errors which may occur during input operations of the system may be divided into two general groups. In the event that an input error in the first group takes place, an Error Latch AEI1 is set, and in the event that an input error in the second group takes place, an Error latch AEI2 is set.

An Error signal AEI1 is generated by setting of that latch in response to a Request to Input signal ICA6 if no answer is received from the central data processing station within 350 milliseconds.

An Error signal AEI2 is generated by setting of that latch in response to one of several categories of errors or machine malfunctions. A first category of error may occur in Program Count 5, if the central data processing station fails to send an Input O.K. signal JCA2 within 350 milliseconds after an input message segment has been transmitted. A second category of error will occur if the Answer Ready signal IWM20 fails to go false within 350 milliseconds after the Input Program Counter has advanced to Count 7. A third category of error involves a transmission error, such as wrong parity or wrong sum check, for example, which may be detected in Program Count 4 or 5 and has caused the central data processing station to return an Input Error signal JCA3. A fourth category of error occurs when an illegal character is generated or when the connection between the window machine and the remote controller is lost in Program Count 4 by the Answer Ready line IWM20 being broken in one of the Row Counts 2 to 17 inclusive.

A detailed description will now be given of the operating sequence of the system in the event that an Error signal AEI1 is generated. During the normal input sequence of operation of the system, after the window machine has been selected, the Request to Input signal ICA6 goes true in accordance with the equation

\[ \text{IC}6 = \text{GC}13 \text{ AEI1'} \text{ AEI2'} \]

a Request to Input character is transmitted in Program Count 2, and the signal ICA6' going false starts the Time Delay TD12' which causes the Time Delay TD12' to go false and sets the Error latch AEI1 in accordance with the equation

\[ \text{aE}11 = \text{FP}1(2) \text{ TD}12' (5E + 5') \]

given in FIG. 30, and shown diagrammatically in FIG. 77. This causes the signal AEI1' to go false, which in turn causes the Request to Input signal ICA6 to go false in accordance with the equation

\[ \text{IC}6 = \text{GC}13 \text{ AEI1'} \text{ AEI2'} \]

The signal ICA6' thus goes true and re-triggers the Time Delay TD12 in accordance with the equation

\[ \text{ID}12 = \text{IC}65' \text{ FP}1(5) \text{ F}11(7') + \text{FP}1(4) + \text{FP}1(6) \]

In addition, the true signal ICA6' resets the Request to Input Memory latch GRI in accordance with the equation

\[ \text{opRI} = \text{I} \text{CA6}\text{' + DM}11 \]

In FIG. 57.

The signal GRI' goes true and is applied to the gate for the Request to Input signal DRI. However, the fact that the signal ICA6 is false at this time prevents the signal DRI from going true, as may be seen from the equation

\[ \text{DI}12 = \text{IC}65' \text{ GR}1 \text{ ICA6} \]

The false level of the signal AEI1 inhibits the flip-flop GCI1 to prevent it from being set in accordance with the expression CTI FP1(2) AEI1 included in the equation for gC11 given in FIG. 34. The true signal AEI1 sets the Sync Memory flip-flop GCI2 in accordance with its equation given in FIG. 34.

Setting of the flip-flop GCI2 generates a Program Counter Reset Drive signal DRI2 in accordance with the expression

\[ \text{GCI2} = \text{FEA9(9') FE}1(3') \text{ AEI1' + AEI2} \]

included in the equation for DR12 given in FIG. 31. Also, the true signal GCI2 generates a Program Counter Clock signal according to the equation

\[ \text{P}1 = \text{CTI(GCI1 + GCI2)} \]

The true signal DRI2 is effective to reset the flip-flop FP12 in accordance with the equation

\[ \text{opDR}2 = \text{FP}1(1 + \text{DR}12) \]

This resets the Input Program Counter to Count zero at the fall of the signal CPI.

The true signal AEI1 is also applied to a gate for the Reset Error Counter "A" signal DR13, which gate is defined by the equation

\[ \text{DRI}3 = \text{DR}1 + \text{SR} + \text{AEI1(9')} \text{ + FE}1(3') + \text{AEI2 + AEI1'} \text{ AEI2'} \]

However, the signal FEA9 is false at this time and prevents the signal DR13 from going true.

Since the inverse signal DR13' is true, the Error Counter "A" flip-flops FEA1 to FEA4 inclusive can be set, in accordance with the equations in FIG. 32, thus permitting Error Counter "A" to tally the number of retrieves which are made.

With the Input Program Counter reset to Count zero, an Error Counter Clock pulse CE is generated at the fall of the next Program Counter Clock signal CPI in accordance with the equation

\[ \text{CE} = \text{FP}1(0) \text{ CPI} \]

This sets the flip-flop FEA1 to represent the first error retry in accordance with the equation

\[ \text{FE}1 = \text{CE DR}13' \]

It should be noted that the Scan Counter Clock is not permitted to run during error retries, due to the fact that the selected window machine has not been dropped, and the signals IWM20 and GC13 remain true. Therefore the Scan Counter remains in the Count which corresponds to the number of the window machine which was originally selected. The Sync Memory flip-flop GCI2 is reset in Program Count zero at the fall of the Special Transmitter one shot TTS, and the signal GC12 controlling the Program Counter Reset Drive signal DR12 thus goes false, causing the signal DRI2 to go false, and its inverse signal DR12' to go true. As may be seen in the Program Counter equations in FIGS. 32 and 33, the term DR12' is included in the setting equations for the Input Program Counter flip-flops. The Sync Memory flip-flop GCI1 goes true at

lay signal TD12 then goes true and sets the Error latch AEI1 in accordance with the equation

\[ \text{aE}11 = \text{FP}1(2) \text{ TD}12' (5E + 5') \]
the fall of the next signal CTI when the signal GC12' is true.

The next Program Counter Clock signal CPI advances the Input Program Counter to Count 1, and the Error Register latch AEII is reset at the fall of the following signal CPI, in accordance with the equation

\[ oe_{EI} = FPI(1) \cdot CPI + 5R \cdot ST + DRW \]

The signal AEII' goes true and causes a Request to Input signal ICA6 to be generated in accordance with the equation \[ ICA6 = GC13 \cdot AEIV' \cdot AEII' \]. This results in the inverse signal ICA6' going false, which starts the Time Delay TD12 for 350 milliseconds time delay, in accordance with the equation

\[ td_{II} = IC5' \cdot FPI(5') \cdot FPI(7') + FPI(4) + FPI(6) \]

The true signal ICA6 generates a Request to Input Drive signal DRI in accordance with the equation

\[ DRI = IC5' \cdot GRI' \cdot ICA6 \]

given in FIG. 57.

The false signal ICA6', applied to the resetting input of the latch GRI, in the DRJ 4, which includes the terms \[ ICA6' + DM1 \], permits the latch GRI to be set when the signal DRI goes true and the Transmit Shift Register is empty, in accordance with the equation \[ gRI = CT \cdot DTE \cdot DRI \].

Setting of the latch GRI causes the inverse signal GRI' to go false, which, in turn, causes the signal DRI to go false in accordance with the equation

\[ DRI = IC5' \cdot GRI' \cdot ICA6 \]

The Request to Input character is again transmitted to the central data processing station in Program 2, and the Input Program Counter waits in that Count for a Start Input signal JCA1 from central. Should transmission line conditions, or other problems, prevent the central data processing station either from receiving the Request to Input character or from sending the Start Input signal JCA1 within 350 milliseconds, the Time Delay TD12 will time out, and the Error Register latch AEII will be set again.

The preceding sequence is repeated until the “A” Error Register has failed nine retries. Should another error, setting the latch AEII, occur during the ninth retry, the Input Program Counter will advance through the remaining program counts, and the Input Row Counter will remain in Count zero.

When the signal AEII goes true, this is effective to set the Sync Memory flip-flop GC11, in accordance with the equation \[ FC1 = CX + GRI + CRI \cdot DRI \]. The true output signal GC12 then causes the generation of a Program Counter Clock pulse CPI in accordance with the equation

\[ CPI = CTI(CCT1 + GC12) \]

The true signals GC12 and AEII are also applied to the gate for the signal DRJ, but the signal FEA(9') is false at this time and prevents the signal DRJ from going true, in accordance with the equation for DRJ in FIG. 31. Therefore the Input Program Counter is not reset, but instead is advanced to Count 3 at the fall of the signal CPI.

The Sync Memory flip-flop output signal GC12 remains true, as applied to the gate for the Program Counter Clock CPI, until Program Count 6, due to the signal FES(9') being false in the reset input to the flip-flop GC12, and the signal AEII being true on the input for setting said flip-flop.

The signal AEII', being false, causes the signal ICA6' to go true, in accordance with the equation

\[ ICA6 = GC13 \cdot AEIV' \cdot AEII' \]

This retriggered the Time Delay TD12, which causes the output signal TD12 to remain true through the ninth retry, in accordance with the equation for td12 given in FIG. 37.

The true signal ICA6' also resets the Request to Input Memory latch GRI in accordance with the equation \[ oe_{EI} = ICA6' + DM1 \]. The resulting true output signal GRI' prepares the gate for the signal DRJ.

The true signal GC12 generates a true signal DRJ in accordance with the equation for DRJ given in FIG. 31. This causes the signal DRJ' to go false, and, since this signal is applied to the inputs for setting the Row Counter flip-flops FC1 to FC15 inclusive, as may be seen in FIGS. 31 and 32, the Row Counter is prevented from advancing.

Each succeeding Program Counter Clock Signal CPI advances the Input Program Counter by one Count. In Count 6, the Sync Memory flip-flop GC12 is reset in accordance with the expression TTS FPI(6), included in the equation for oeCI2 given in FIG. 34. On the next Main Timing Clock signal CTI, the Sync Memory flip-flop GC11 is set in accordance with the expression \[ FC1 = FPI(6) \cdot GC12 \] included in the equation for gc11 given in FIG. 34. When the output signal GC12 goes false, the signal DRJ goes false.

With the next Program Counter Clock Signal CPI, the Input Program Counter advances to Count 7. In this Count, the Sync Memory flip-flop GC13 is reset in accordance with the expression CTI FPI(7) GC12 included in the equation for ogCI2 given in FIG. 34.

The Input Error line JWM38 goes true when the Input Program Counter is in Count 7, in accordance with the expression FPI(8) AEIV included in the equation for JWM38 given in FIG. 36. The true signal JWM38 is effective to energize the input error relay \[ K104 (FIG. 16B) \] in the Error lamp circuit in the selected window machine, which causes the holding contacts \[ K104AC1 (FIG. 16B) \] to close to maintain the relay K104 in energized condition. In addition, the contacts \[ K104AC4 (FIG. 19) \] close, applying a true signal to the Lamp Digit 1 line JMI71, which turns on the Send Error lamp in the selected window machine. The contacts \[ K104BC2 (FIG. 16B) \] open in the Ready Interrogate line JMI9, which breaks the Input Flag circuit and drops the window machine from communication with the remote controller, causing the Answer Ready line JWM20 to go false. A true inverse signal JWM20 completes the gate to set the Sync Memory flip-flop GC11 in accordance with the expression FPI(7) JWM20 TD11 included in the equation for gCI1 given in FIG. 34. This generates another Program Counter Clock signal CPI to advance the Input Program Counter to Count zero.

In Program Count zero, an Error Counter Clock signal CF is generated, in accordance with the equation \[ CF = FPI(0) \cdot CPI \], which resets the “A” Error Counter in accordance with the equations for resetting the flip-flops FEA1 to FEA4 inclusive, given in FIG. 32.

The Reset Drive signal DRJ goes false when the signal FEA(9') goes false in accordance with the expression AEII FEA(9) included in the equation for DRJ given in FIG. 31.

The Sync Memory flip-flop GC11 is set on the fall of the next Main Timing Clock signal CTI, in accordance with the expression

\[ CTI FPI(0) FC1(0) ICA4 ICA1' GC5' \]

included in the equation for GC11 given in FIG. 34. The following signal CTI advances the Input Program Counter to Count 1. In this Count, the Error Register latch AEII is reset in accordance with the equation

\[ oe_{EI} = FPI(1) \cdot CPI + 5R \cdot ST + DRW \]

Also, the Scan Counter Clock CSI commences pulsing when the signal FPI(1) goes true, in accordance with the expression TTN FPI(1) JWM20, thereby causing the
Scan Counter to resume counting and thus scanning the various window machines of the branch.

Detailed descriptions will now be given of the operating sequence of the system when various types of errors occur which result in the generation of an Error signal AEI2.

A first type of error resulting in the generation of a signal AEI2 may occur in Program Count 5 if the central data processing station fails to transmit to the branch an Input O.K. signal JCA2 within 350 milliseconds after an input error signal has been received from the branch to the central data processing station.

When the Input Program Counter advances to Count 5, after having transmitted the eighteen characters of the input message segment, the signal FP1(5) goes false, and the Time Delay TD12 commences its 350-millisecond timing-out period, in accordance with the equation

\[ TD12 = ICAG6 \cdot FP1(5) \cdot FP1(7) \cdot ER11 \cdot FP1(4) \cdot FP1(6) \]

The inverse Time Delay signal TD12' goes true after 350 milliseconds have elapsed, and the Error latch AEI2 is set in accordance with the expression TD12' = ICAG6 \cdot FP1(5) \cdot FP1(7). The inverse signal AEI2' goes false, which causes the Request to Input signal ICA6 to go false in accordance with the equation ICA6 = GC13 AEI1 AEI2'.

The inverse signal ICA6' accordingly goes true and retriggers the Time Delay TD12, as well as being applied to the reset trigger gate of the Control Memory latch GR, and the inverse signal GR1' goes true in the gate for the Request to Input Signal DRI, but since the signal ICA6 is false, a true signal DRI is not generated at this time.

Another output of the latch AEI2 is applied to the gate for the Reset Error Counter "B" signal DR15, but since the signals FE(9) and FE(3) are false, a true signal DR15 is not generated at this time. The signal DR15' therefore remains true in the set trigger gates of the Error Counter "B" flip-flops FEB1 and FEB2, so that the number of retries can be tallied.

The signal AEI2' going false prevents the Sync Memory flip-flop GCI1 from being set, and the signal AEI2 being true sets the Sync Memory flip-flop GCI2. The signal GCI2 being true in conjunction with the true signal AEI2 causes a signal DR12 to be generated in accordance with the equation given in FIG. 31. The signal GCI2 also causes the generation of Program Counter Clock and Main Timing Clock signals CP1 and CT1. The signal DR12 causes the flip-flop FP13 to be reset at the fall of the clock signal CP1, at which time the flip-flop FP11 is also reset, in accordance with the equations for those flip-flops given in FIG. 3. The Input Program Counter is thereby reset to Count zero.

In Count zero, the Sync Memory flip-flop GCI2 is reset at the fall of the signal TTS, and the Sync Memory flip-flop GCI1 is set on the next signal CT1. Going false of the signal GCI2 causes the signal DR12 to go false, which results in the inverse signal DR12' going true in the gates for setting the flip-flops of the Input Program Counter.

The Input Program Counter advances to Count 1 at the fall of the next signal CPI. An error Counter Clock signal CE is generated at the fall of the signal CPI which advanced the Input Program Counter to Count 1, in accordance with the equation CE = FP1(0) CPI. The Error Counter "B" flip-flop FEB1 is set at the fall of the signal CE, which represents the first error retry, in accordance with the equation FE1 = CE AEI2 DR13'.

The Error latch AEI2 is reset in Program Count 1 at the fall of the next signal CPI in accordance with the equation

\[ onAEI2 = FP1(1) CPI + DRW + SR ST \]

The signal AEI2' therefore goes true, which causes the Request to Input signal ICA6 to go true in accordance with the equation ICA6 = GC13 AEI1 AEI2', as a consequence, the inverse signal ICA6' goes false and causes the Time Delay TD12 to commence timing out, in accordance with the equation given in FIG. 31.

37. The false signal ICA6' is also applied to the reset gate of the Control Memory latch GR1, while the true signal ICA6 is applied to the gate for the Request to Input signal DRI, and produces a true signal DRI in accordance with the equation DR1 - ICAG6 ICAG6' ICAG6. The true signal DRI is applied to the gate for setting the Control Memory latch GR1, to set said latch. As a consequence, the inverse signal GR1' going false then turns the signal DRI false.

The request to Input character is again transmitted to the central data processing station in Program Count 2, and the Input Program Counter advances to Program Count 5 after again transmitting the eighteen characters of the input message segment. With the Input Program Counter in Count 5, the signal FP1(5) is false, which causes the Time Delay TD12 to commence timing out. If the central data processing station again fails to return an Answer Input O.K. signal JCA2 in 350 milliseconds, the signal TD12' goes true and sets the Error latch AEI2.

The preceding sequence is repeated until the "B" Error Counter tallies three retries. If the central data processing station returns an Answer Input O.K. signal before the retry limit is reached, the operation of the remote controller will function normally. However, let it be assumed that with the Input Program Counter in Count 5, the Error latch AEI2 is set on the third retry. The Input Program Counter then advances through the remaining counts, and the window machine is dropped from communication with the remote controller.

When the Error latch AEI2 is set on the third retry, the signal AEI2' goes false and causes the signal ICA6 to go false in accordance with the equation

\[ ICA6 = GC13 AEI1 AEI2' \]

The inverse signal ICA6' accordingly goes true and resets the Control Memory latch GR1 in accordance with the equation ogRI = ICAG6 + DM1. The signal GR1 prepares the gate for the signal DRI.

The true signal AEI2' causes the generation of a true signal DR15 in accordance with the expression AEI2' + FE(9) + FE(3), and the operation of the remote controller will function normally. However, let it be assumed that with the Input Program Counter in Count 5, the Error latch AEI2 is set on the third retry. The Input Program Counter then advances through the remaining counts, and the window machine is dropped from communication with the remote controller.

In Count zero, the Sync Memory flip-flop GCI2 is reset at the fall of the signal TTS, and the Sync Memory flip-flop GCI1 is set on the next signal CT1. Going false of the signal GCI2 causes the signal DR12 to go false, which results in the inverse signal DR12' going true in the gates for setting the flip-flops of the Input Program Counter.

The Input Program Counter advances to Count 1 at the fall of the next signal CPI. An error Counter Clock signal CE is generated at the fall of the signal CPI which advanced the Input Program Counter to Count 1, in accordance with the equation CE = FP1(0) CPI. The Error Counter "B" flip-flop FEB1 is set at the fall of the signal CE, which represents the first error retry, in accordance with the equation FE1 = CE AEI2 DR13'.

The Error latch AEI2 is reset in Program Count 1 at the fall of the next signal CPI in accordance with the equation

\[ onAEI2 = FP1(1) CPI + DRW + SR ST \]

The signal AEI2' therefore goes true, which causes the Request to Input signal ICA6 to go true in accordance with the equation ICA6 = GC13 AEI1 AEI2'. As a consequence, the inverse signal ICA6' goes false and causes the Time Delay TD12 to commence timing out, in accordance with the equation given in FIG. 31.

37. The false signal ICA6' is also applied to the reset gate of the Control Memory latch GR1, while the true signal ICA6 is applied to the gate for the Request to Input signal DRI, and produces a true signal DRI in accordance with the equation DR1 = ICAG6 ICAG6' ICAG6. The true signal DRI is applied to the gate for setting the Control Memory latch GR1, to set said latch. As a consequence, the inverse signal GR1' going false then turns the signal DRI false.

The request to Input character is again transmitted to the central data processing station in Program Count 2, and the Input Program Counter advances to Program Count 5 after again transmitting the eighteen characters of the input message segment. With the Input Program Counter in Count 5, the signal FP1(5) is false, which causes the Time Delay TD12 to commence timing out. If the central data processing station again fails to return an Answer Input O.K. signal JCA2 in 350 milliseconds, the signal TD12' goes true and sets the Error latch AEI2.

The preceding sequence is repeated until the "B" Error Counter tallies three retries. If the central data processing station returns an Answer Input O.K. signal before the retry limit is reached, the operation of the remote controller will function normally. However, let it be assumed that with the Input Program Counter in Count 5, the Error latch AEI2 is set on the third retry. The Input Program Counter then advances through the remaining counts, and the window machine is dropped from communication with the remote controller.

When the Error latch AEI2 is set on the third retry, the signal AEI2' goes false and causes the signal ICA6 to go false in accordance with the equation

\[ ICA6 = GC13 AEI1 AEI2' \]

The inverse signal ICA6' accordingly goes true and resets the Control Memory latch GR1 in accordance with the equation ogRI = ICAG6 + DM1. The signal GR1 prepares the gate for the signal DRI.

The true signal AEI2' causes the generation of a true signal DR15 in accordance with the expression AEI2' + FE(9) + FE(3), and the operation of the remote controller will function normally. However, let it be assumed that with the Input Program Counter in Count 5, the Error latch AEI2 is set on the third retry. The Input Program Counter then advances through the remaining counts, and the window machine is dropped from communication with the remote controller.

In Count zero, the Sync Memory flip-flop GCI2 is reset at the fall of the signal TTS, and the Sync Memory flip-flop GCI1 is set on the next signal CT1. Going false of the signal GCI2 causes the signal DR12 to go false, which results in the inverse signal DR12' going true in the gates for setting the flip-flops of the Input Program Counter.

The Input Program Counter advances to Count 1 at the fall of the next signal CPI. An error Counter Clock signal CE is generated at the fall of the signal CPI which advanced the Input Program Counter to Count 1, in accordance with the equation CE = FP1(0) CPI. The Error Counter "B" flip-flop FEB1 is set at the fall of the signal CE, which represents the first error retry, in accordance with the equation FE1 = CE AEI2 DR13'.

The Error latch AEI2 is reset in Program Count 1 at the fall of the next signal CPI in accordance with the equation

\[ onAEI2 = FP1(1) CPI + DRW + SR ST \]
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In the equation for GCI1 given in Fig. 34, this generates another Program Counter Clock pulse CPI to advance the Program Counter to Count zero. The true signal IWM20' also prepares the gate for the Scan Counter Clock CSI. The Sync Memory flip-flop GCI1 is reset at the fall of the Main Timing Clock signal CT1 that advanced the Program Counter to Count zero.

In Program Count zero, an Error Counter Clock pulse CE is generated, according to the equation CE=FPI(0) CPI, which resets the "B" Error Counter in accordance with the equation for flip-flops FEB1 and FEB2 given in Fig. 32. The signal DR15 goes false when the signal FEB(3) goes false.

The Signal Memory flip-flop GCI1 is set at the fall of the next signal CT1, and the Input Program Counter advances to Count 1 on the fall of the following signal CT1 by virtue of the generation of a Program Counter Clock signal CPI.

In Program Count 1, the Error latch AE12 is reset at the fall of the signal CPI. The gate for the Scan Counter Clock CSI is completed when the signal FPI(1) goes true, causing the Scan Counter to resume scanning.

A result of error resulting in the generation of a signal AE12 will occur only if the Answer Ready signal IWM20 fails to go false within 330 milliseconds after the Input Program Counter has advanced to Count 7. No retries are made when this error situation arises, due to the input section of the input controller having functioned correctly up to Program Count 7. Therefore it is necessary to drop the window machine from communication with the remote controller by a true signal on the Input Error line JWM38.

When the Input Program Counter advances to Program Count 7, the signal FPI(7') goes false and starts the Time Delay TD12 on its 350-millisecond time delay period. In order to advance the Input Program Counter to Count zero, the Sync Memory flip-flop GCI1 must be set.

Let it be assumed that the Answer Ready signal IWM20 does not go false. In this case, the inverse signal IWM20' remains false in the setting gate for the Sync Memory flip-flop GCI1, which prevents the Input Program Counter from advancing to Count zero. Thus the signal FPI(7') remains false in the gate for the Time Delay TD12, and in 350 milliseconds, the signal TD12 will be true and will set the Error latch AE12 in accordance with the expression TD12' FPI(7) included in the equation for AE12 given in Fig. 30. The true signal AE12 generates a true signal on the Input Error line JWM38 in accordance with the equation JWM38=FPI(7) ST(AE11+AE12).

The error signal error relay K104(Fig. 45) follows as a consequence of the true signal on the line JWM38. The holding contacts K104AC1 (Fig. 16B) close to maintain the relay K104 energized. Also a true signal is applied to the Lamp Digit 1 line J1711 by closing of the contacts K104AC4, and this turns on the Send Error lamp in the selected window machine. In addition, the contacts K104BC2 open in the Ready Interrogate line J119, which breaks the Input Flag circuit and stops the window machine from communication with the remote controller, causing the Answer Ready line IWM20 to go false. A true inverse signal IWM20' completes the gate to set the Sync Memory flip-flop GCI1 in accordance with the expression FPI(7) IWM20 TD11 included in the equation for GCI1 given in Fig. 34. A true signal GCI1 is effective to generate a Program Counter Clock signal CPI at the fall of the next Main Timing Clock signal CT1. The fall of the signal CPI advances the Input Program Counter to Count zero.

The Sync Memory flip-flop GCI1 is reset at the fall of the Main Timing Clock signal that advanced the Program Counter to zero, but is set again on the next signal CT1 by coincidence with the false signal for setting GCI1 given in Fig. 34. The true signal GCI1 is effective to generate another Program Counter Clock signal CPI which advances the Input Program Counter to Count 1.

An Error Counter Clock signal CE is generated at the fall of the signal CPI that advanced the Input Program Counter to Count 1, in accordance with the equation CE=FPI(0) CPI.

The Error Counter "B" flip-flop FEB1 will be set at the fall of the Error Counter Clock signal CE, in accordance with the equation FEB1=CE AE12 DR15. It may be noted that the signal DR15 is inhibited by the false signals FEA9(1) and FEB(2). The setting of the flip-flop FEB1, in this case, does not mean that a retry will occur. The flip-flop FEB1 is reset in Program Count zero following the successful transmission of the next input segment, in accordance with the equation of FEB1=CE(AE12+DR15)

The signal CE is derived according to the equation CE=FPI(0) CPI, and the signal DR15 is derived according to the expression AE11 AE12 included in the equation for DR15 given in Fig. 30.

A third type of error resulting in the generation of a signal AE12 may occur in Program Count 4 or 5 in the form of a transmission error such as wrong parity or the wrong sum check. This causes the central data processing station to return an Input Error character JCA3, which is effective to set the Error latch AE12 in accordance with the expression CT JCA3FPI(4)+FPI(5) included in the equation for AE12 given in Fig. 30.

This type of error causes the Input Program Counter to be reset to Count zero, the retries to be tallied in the "B" Error Counter, and the selected window machine to be dropped from communication with the remote controller in Program Count 7 after the third retry. The sequence of operation for this type of AE12 error is the same as described previously, except that the signal JCA3 controls the gate for setting the latch AE12 instead of the Time Delay TD12.

A fourth type of error resulting in the generation of a signal AE12 may occur when an illegal character is generated or when the connection between the window machine and the remote controller is lost in Program Count 4 by the Answer Ready line IWM20 being broken in one of the Row Counts 2 to 17 inclusive.

The Error Combination signal DE11 will go true if a short exists between adjacent contacts, or if there is an open circuit, in the storage switch being sensed of the selected window machine. The signal DE11 is generated by the Exclusive OR circuit which checks the logical sum of odd and event digits, in accordance with the equations for DE11, DDH1A, and DDHl given in Fig. 31, and shown diagrammatically in Figs. 77 and 80.

When this type of AE12 error occurs, the Input Row Counter is reset to Count zero, the retries are tallied in the "B" Error Counter, and the selected window machine is dropped from communication with the remote controller in Program Count 7 after the third retry, as described previously.

**Output error description**

Output errors which may occur during output operations of the system may be divided into four general groups, which correspond to four specific conditions which may exist in the window machine. These conditions, together with their related signal designations, are as follows:

**AE01**—Window Machine Busy

**AE02**—Window Machine Not There

**AE03**—Error Before Window Machine Key Select

**AE04**—Error After Window Machine Key Select.

It will be realized that the central data processing station can only transmit an output message to a window machine which has requested information via input message segments, and which is in an output mode of operation.
The Window Machine Busy condition mentioned above occurs when the central data processing station is outputting more than one segment of information to the selected window machine. An example of this might include a first segment containing interest information in an automatic updating operation with an AC2 digit to cause an automatic sub-balance operation, followed by a second segment containing current transaction information with an AC1 digit to cause an automatic balance operation.

The keys of the window machine keyboard are depressed by the key solventoid corresponding to the information contained in the first message segment, and the window machine is tripped for operation. During the relatively slow operation of the window machine, the central data processing station will attempt to output the second message segment.

Tripping of the window machine for operation causes the contacts SC503A1 (Fig. 15) to open in the Output Flag circuit. Thus, in turn, causes the signal to go false in the Window Machine Red Line IM100 in the remote controller, said line being connected to the Window Machine Ready Line IM101 in the window machine controller.

Should the central data processing station attempt to output to this window machine, the Request to Output message from central will set the Request to Output Memory latch GRO, shown in Fig. 65, in accordance with the window machine "busy" and the Time Delay TDO5 goes true in Output Row Count 1, which is the Select position, in accordance with the equation $EIO1 = IWM101^1 IWM102^1 TDO5^1$.

The true signal AEIO1 turns on a test panel indicator lamp to which it is directly connected (see Fig. 89), resets the Output Program Counter, resets the Output Row Counter, and causes the Transmit Shift Register to send an Output Error character followed by a digit 1.

The Output Program Counter and the Output Row Counter are reset by the Reset Drive signals DRO1 and DRO2, respectively. True signals DRO1 and DRO2 are generated in accordance with the expression AEIO1 FPO(5) contained in the equations for DRO1 and DRO2 given in Fig. 48. The Output Program Counter flip-flops are reset by a true Program Counter Clock signal CPO and a true signal DRO1 in accordance with the equations given in Fig. 48, and the Output Row Counter flip-flops are reset by a true Row Counter Clock signal CCO and a true signal DRO2 in accordance with the equations given in Fig. 48.

The next Request for Character signal JCA5 generates a Main Timing Clock signal CTO in accordance with the expression JCA5 FPO(0) included in the equation for CTO given in Fig. 41. The true signal CTO sets the Sync Memory latch in accordance with the expression CTO DRW' (SR' 'ST') FPO(0) FCO(0) JCA4 included in the equation for GC01 given in Fig. 49. The following signal JCA5 generates another CTO signal which is combined with the signal GC01 to produce a Program Counter Clock signal CPO to advance the Output Program Counter from Count zero to Count 1.

In Program Count 1, the Output Error signal ICA103 is made true in accordance with the equation $ICA103 = FPO(1) ICA106 GC03(1) AEIO1 + AEIO2 + AEIO3 + AEIO4$.

This signal, in combination with the inverse signals DRI' and JCA5', generates an Output Error Drive signal DER in accordance with the equation $DER = DRI' ICA5' ICA106 ICA103$.

On the next Transmitter Register Empty signal DTE, flip-flops FT2 and FT6 of the Transmit Shift Register are set in accordance with the equations given in Figs. 56 and 57 to load the Transmit Shift Register with the Output Error character.

The signals CT, DER, and DTE reset the Request to Output Memory latch GRO in accordance with the equation $opRO = CT(DER DTE + DOK DTE + DM11)$. This causes the signal JCA106 to go false in accordance with the equation $ICA106 = GRO$.

When the inverse signal JCA106' goes true, the Sync Memory flip-flop GC01 is again set in accordance with the expression $FPO(1) JCA106' CTO DRW' (SR' + ST')$ included in the equation given in Fig. 49. A true signal GC01 generates a Program Counter Clock signal CPO in accordance with the expression GC01 CTO included in the equation for CP0 given in Fig. 46, and the Output Program Counter is advanced to Count 2.

The signal FPO(2), in conjunction with the signal AEIO1, causes the Error Encode 2 Bit signal DEO1 to go true in accordance with the equation $DEO1 = FPO(2) GC03' AEIO4'(AEIO1 AEIO2 + AEIO3)$. The true signal DEO1 produces a true signal on the Input Data 2 Bit line ICA1, in accordance with the equation for ICA1 given in Fig. 33.

The Data On Line signal ICA7 goes true in Program Count 2 in accordance with the equation given in Fig. 34. This signal, in combination with the signal JCA5, generates a Load Data signal DLD in accordance with the equation $DLD = JCA5 ICA7$. This signal DLD will load the flip-flops of the Transmit Shift Register in accordance with Data Bit signals ICA1, ICA2, ICA3, ICA4, which, when received by the central data processing station, will provide the information that the error which occurred was an AEIO1 type of error.

The Output Program Counter is advanced to Count 3 by the same signal JCA5, which generates a Main Timing Clock signal CTO in accordance with the expression $JCA5 FPO(2)$ included in the equation for CTO given in Fig. 47. The signal CTO, in turn, is effective to set the Sync Memory flip-flop GC01 in accordance with the expression CTO FPO(2), and then to generate a Program Counter Clock signal CPO in accordance with the expression CTO GC0.

In Program Count 3, the Error latch AEIO1 is reset in accordance with the equation $opAEIO1 = FPO(3)$, and the AEIO1 indicator lamp is thereby extinguished. The Select Register flip-flops AS01 to AS04 inclusive are also reset, in accordance with the equations $opAE1 = opAO4 inclusive = FPO(3)$.

The next two signals TRS advance the Output Program Counter from Count 3 to Count 4. A signal CTO is generated in accordance with the expression TRS FPO(3); the Sync Memory flip-flop GC01 is set again in accordance with the expression CTO FPO(3); and a Program Counter pulse CPO is subsequently generated in accordance with the expression CTO GC0 when the next signal CTO comes true, thereby advancing the Output Program Counter to Count 4, in which Count it remains until a Request to Output signal is received from the central data processing station.

The Window Machine Not There condition mentioned above occurs when a given window machine has lost power or is in an off-line mode, and the central data processing station attempts to output to this machine.
Let it be assumed that the 115-volt D.C. power supply from the window machine to its associated window machine controller has been lost. This causes the window machine on line relay K309 (FIG. 17B) to be de-energized. The Character signal DCR (FIG. 17B) accordingly opens and causes the signal on the Character Machine On-Line in 161002 to go false.

When the remote controller receives the Request to Output message from the central data processing station, the Request to Output Memory latch GRO is set in accordance with the equation JCA106 = GRO. The Output Program Counter advances to Program Count 5, and the Output Row Counter advances to Row Count 1.

The Error latch AE02 is now set when the Time Delay signal TD05 comes true, in accordance with the equation AE02 = IWMI102. TD05 FCO(1) (5ST' + 5ST'). The true signal AE02 turns on a test panel indicator lamp to which it is directly connected (see FIG. 89), resets the Output Program Counter, sets the Output Row Counter, resets the Request to Output Memory, and causes the Transmit Shift Register to send an Output Error character followed by a digit 2.

The Output Program Counter and the Output Row Counter are reset by the Reset Drive signals DRO1 and DRO2, respectively. True signals DRO1 and DRO2 are generated in accordance with the expression AE02 FPO(5) contained in the equations for DRO1 and DRO2 given in FIG. 48. The Output Program Counter flip-flops are reset by a true Program Clock Counter Signal CP0 and a true signal DRO1 in accordance with the equations in FIG. 48, and the Output Row Counter flip-flops are reset by a true Counter Clock signal CCO and a true signal DRO2 in accordance with the equations given in FIG. 48.

The remainder of the operating sequence in the case of a Window Machine Not Error is the same as that previously described for a Window Machine Busy error, except that the Error latch AEO2, rather than the Error latch AE01, is set, and a digit 2, rather than a digit 1, is sent to the central data processing station following the transmission of the Output Error character. Sending of the digit 2 is controlled by generation of an Error Encode 02 Bit signal DEO2 in accordance with the equation

$DEO2 = FPO(2) GCO3' AEO4'(AEO2 + AEO3)$

The true signal DEO2 generates a true Data Bit 2 signal ICA2, which causes the Transmit Shift Register flip-flops to be set to transmit a digit 2 to the central data processing station.

At the close of the Window Machine Not Error sequence of operation, the Output Program Counter is in Count 4, and remains there until a Request to Output signal is received.

The Error Before Window Machine Key Select condition mentioned above occurs when any one of several given situations exists in the output message segment before a key could have been pulled down in the window machine. A first such situation would be a transmission parity error (such as a parity error or a loss of data indication in a data character). A second such situation would be a loss of clock signal in Row Count 1, 2, or 3. A third such situation would be the existence of a character greater than 9 in Row Count 3.

In the event of a transmission parity error, it should be noted that the Odd Parity Check signal DPC is generated by an Exclusive OR parity checking network, and is true when a character received has proper parity. If the parity is not correct when the character is in the Receive Shift Register, the signal DPC false and generates an Error in Transmission signal JCA108 in accordance with the expression DPC' FRO included in the equation for JCA108 given in FIG. 59.

In the case of a loss of data indication type of transmission error, it should be noted that the flip-flop FR1 in the Receive Shift Register indicates a data character when true and a control character when false. The output signal of the flip-flop FR1 is combined with a Nod Character signal DNR and output signals for the four control characters to determine whether or not the signal FR1' (the inverse of FR1) is correct.

Let it be assumed that during the transmission of a data character, a condition exists which caused that bit to be lost when it designates whether the transmitted character is a control character or a data character. When the character is received in the Receive Shift Register, the signal FR1' is true, even though there is actually not a control character in the Receive Shift Register. This causes the Error in Transmission signal JCA108 to be made true in accordance with the expression FR0 FR1' DRN' DRO' DDS' JCA2' JCA3 included in the equation for JCA108 given in FIG. 59.

A true signal JAC108, caused by either of the above-described transmission errors, when the Output Program Counter is in Count 5, and the Output Row Counter is in Count 1, 2, or 3, will set the Error latch AE03 in accordance with the equation for AE03 given in FIG. 45.

Another type of error, mentioned above, is a loss of clock error in Row Count 1, 2, or 3. It should be noted that the term "clock" as used here refers to the Character Present signal JCA107, which is generated in accordance with the equation JCA107 = FRO FRI CR. The signal JCA107 is used to generate the clock signals for the Output Data Register and the Output Longitudinal Bit Check Register.

The 1-millisecond Time Delay one shot TD06 is also triggered by the signal JCA107, in accordance with the equation $DO6 = FPO(5) [JCA107 FCO(0)'+CP0]$ and, in turn, is used to trigger the Clock Detector Time Delay one shot TD01 in accordance with the equation for TD01 given in FIG. 52. The signal TD06 will not register the Time Delay TD01 should a condition exist that would cause the loss of a character or an interruption between characters of the output segment, and in such a case, the Time Delay TD01 will time out. The signal TD01 going false in Row Count 1, 2, or 3 will set the Error latch AE03 in accordance with the equation for AE03 given in FIG. 45.

Another type of error, mentioned above, is the presence of a character greater than nine in Row Count 3. Characters greater than nine are illegal characters in all Row Counts other than 1, 12, and 18. The Error latch AE03 will therefore be set if an illegal character nine is received in Row Count 3, in accordance with the expression JCA107 JCA104 FCO(3) FCO(12) FCO(18') [JCA102 + JCA103] included in the equation for AE03 given in FIG. 45.

The Error latch AE03, upon being set by any of the above-described error conditions, turns on a test panel indicator lamp to which it is directly connected (see FIG. 89), resets the Output Program Counter, resets the Output Row Counter, resets the Request to Output Memory, and causes the Transmit Shift Register to send an Output Error character followed by a digit 3.

The Output Program Counter and the Output Row Counter are reset by the Reset Drive signals DRO1 and DRO2, respectively. True signals DRO1 and DRO2 are generated in accordance with the expression AE03 FPO(5) contained in the equation for DRO2 given in FIG. 48. The Output Program Counter flip-flops are reset by a true Program Clock Counter Signal CP0 and a true signal DRO1 in accordance with the equations given in FIG. 48, and the Output Row Counter flip-flops are reset by a true Counter Clock signal CCO and a true signal DRO2 in accordance with the equations given in FIG. 48.

The remainder of the operating sequence in the case of an AE03 error is the same as that previously de-
scribed for AFO1 and AFO2 errors, except that the Error latch AFO3, rather than the latch AEO1 or the latch AFO2, is set, and a digit 3, rather than a digit 1 or 2, is set in the central data processing station following the transmission of the Output Error character. Sending of the digit 3 is controlled by generation of an Error Encode 2\textsuperscript{a} Bit signal DEO1 and an Error Encode 2\textsuperscript{b} Bit signal DEO2, in accordance with the equations for DEO1 and DEO2 given in FIG. 42. The true signals DEO1 and DEO2 generate true Data Bit 2\textsuperscript{a} and Data Bit 2\textsuperscript{b} signals IC\textsubscript{A1} and IC\textsubscript{A2}, which cause the Transmit Shift Register flip-flops to be set to transmit a digit 3 to the central data processing station.

At the close of the AEO3 error sequence of operation, the Output Program Counter is in Count 4, and remains there until a Request to Output signal is received.

The Error After Window Machine Key Select condition mentioned previously will be set by any one of the following seven types of errors after the Output Program Counter has been advanced to Count 5, and the Output Error signal has been advanced to Count 3:

- Loss of “Clock,”
- Window Machine Busy,
- Loss of Window Machine,
- Transmission Error (Parity),
- Transmission Error (Loss of Data Indication Bit),
- Character Greater Than Nine,
- Incorrect Sum Check.

In the case of the Loss of “Clock” condition mentioned above, it is observed that “clock” here refers to the Character Present signal JCA\textsubscript{107} which is generated in accordance with the equation JCA\textsubscript{107} = FRO FRI CR. As has been mentioned, the signal JCA\textsubscript{107} is used to generate the clock signal for the Output Data Register and the Output Longitudinal Bit Check Register.

The 1-millisecond Time Delay one shot TD\textsubscript{0} is also triggered by the signal JCA\textsubscript{107}, in accordance with the equation for TD\textsubscript{0} given in FIG. 52, and, in turn, is used to trigger the Clock Detector Time Delay one shot TD\textsubscript{1} in accordance with the equation for TD\textsubscript{1} given in FIG. 52. The signal TD\textsubscript{0} will not trigger the Time Delay TD\textsubscript{1} should a condition exist that would cause the loss of a character or an interruption between characters of the output segment, and in such a case, the Time Delay TD\textsubscript{1} will time out. The signal TD\textsubscript{1} going false in any Row Count after Row Count 3 sets the Error latch AEO4 in accordance with the equation for AEO4 given in FIG. 45.

The second condition mentioned above is the Window Machine Busy condition. Should the Output Flag circuit be broken after the Output Program Counter has advanced to Count 5 and the Window Machine Busy condition is present, the Window Machine Ready line JWM\textsubscript{101} will go false. The inverse signal JWM\textsubscript{101}\textsuperscript{*} thus goes true, and the Error latch AEO4 is set in accordance with the expression FPO\textsubscript{5} TRS FCO\textsubscript{0} TRS FCO\textsubscript{2} TRS FCO\textsubscript{3} JWM\textsubscript{101} in the equation for AEO4 given in FIG. 45.

The third condition mentioned above is the Loss of Window Machine condition. Should the window machine be off-line or lose power after the Output Program Counter has advanced to Count 5 and the Output Error signal has been advanced past Count 3, the Window Machine On-line signal JWM\textsubscript{102} will go false, and its inverse signal JWM\textsubscript{102}\textsuperscript{*} will go true. This sets the Error latch AEO4 in accordance with the expression FPO\textsubscript{5} TRS FCO\textsubscript{0} TRS FCO\textsubscript{1} TRS FCO\textsubscript{2} JWM\textsubscript{102} in the equation for AEO4 given in FIG. 45.

The fourth condition mentioned above is the Transmission Error (Parity) condition. The Odd Parity Check term DPC results from an Exclusive OR parity network, and is true when a character received has proper parity. If parity is not correct when the character is in the Receive Shift Register, the signal DPC goes false, and generates an Error in Transmission signal JCA\textsubscript{108} in accordance with the expression DPC\textsuperscript{*} FRO in the equation for JCA\textsubscript{108} given in FIG. 59. A true signal JCA\textsubscript{108} after the Output Program Counter has advanced to Program Count 5 and the Output Error signal has been advanced past Count 3, causes the Error latch AFO4 to be set in accordance with the expression FPO\textsubscript{5} TRS FCO\textsubscript{0} TRS FCO\textsubscript{1} TRS FCO\textsubscript{2} JCA\textsubscript{108} included in the equation for AFO4 given in FIG. 45.

The fifth condition mentioned above is the Transmission Error (Loss of Data Indication Bit) condition. As has been previously described, the flip-flop FRI in the Receive Shift Register indicates a data character when true and a control character when false. The output signal of the flip-flop FRI is combined with a Odd Character signal DNR and output signals for the four control characters to determine whether or not the signal FRI\textsuperscript{*} (the inverse of FRI) is correct.

Let it be assumed that during the transmission of a data character, a condition exists that caused bit to be lost which designates whether the transmitted character is a control character or a data character. When the character is received in the Receive Shift Register the signal FRI\textsuperscript{*} is true, even though there is actually not a control character in the Receive Shift Register. This causes the Error in Transmission signal JCA\textsubscript{108} to be made true in accordance with the expression FPO\textsubscript{5} FRI\textsuperscript{*} DRO\textsuperscript{*} DSI JCA\textsubscript{2} JCA\textsubscript{3} in the equation for JCA\textsubscript{108} given in FIG. 59. A true signal JCA\textsubscript{108}, after the Output Program Counter has advanced a Count 5 and the Output Row Counter has advanced past Count 3, causes the Error latch AFO4 to be set, as previously described, in accordance with the expression FPO\textsubscript{5} TRS FCO\textsubscript{0} TRS FCO\textsubscript{1} TRS FCO\textsubscript{2} JCA\textsubscript{108} included in the equation for AFO4 given in FIG. 45.

The sixth condition mentioned above is the Character Greater Than Nine condition. Characters greater than nine are illegal in all Row Counts other than 1, 12, and 18. The Error latch AFO4 will be set if a character greater than nine is received in any Row Count after Count 3, other than 12 and 18, in accordance with the expression FPO\textsubscript{5} TRS FCO\textsubscript{0} TRS FCO\textsubscript{1} TRS FCO\textsubscript{2} JCA\textsubscript{108} JCA\textsubscript{104} FCO\textsubscript{12} FCO\textsubscript{18} JCA\textsubscript{102} JCA\textsubscript{103} in the equation for AFO4 given in FIG. 45.

The seventh condition mentioned above is the Incorrect Sum Check condition. As has been previously described, the eighteenth character of the equivalent segment is a character representing the longitudinal bit sum accumulated by a buffer in the central data processing station as it transmitted this segment. As has also been described, the Output Longitudinal Bit Check Register accumulates a character representing the bit sum of the characters received in this segment. In Row Count 18, the sum check character from the central data processing station is added into the Output Longitudinal Bit Check Register, as has been described. If the two bit sums agree, the flip-flops ALO1, ALO2, ALO3, and ALO4 will be reset, and the term ALO\textsuperscript{*} will be true, in accordance with the equation ALO\textsuperscript{*} = ALO1 ALO2 ALO3 ALO4. This causes the Error latch AFO4 to be set in accordance with the expression FPO\textsubscript{5} TRS FCO\textsubscript{0} TRS FCO\textsubscript{1} TRS FCO\textsubscript{2} JCA\textsubscript{108} FCO\textsubscript{12} FCO\textsubscript{18} TD\textsubscript{0} ALO\textsuperscript{*} included in the equation for AFO4 given in FIG. 45.

The Error latch AFO4, upon being set as a result of detection of any of the above-mentioned seven types of errors, turns on a test panel and indicator lamp to which it is directly connected (see FIG. 89), advances the Output Program Counter to Counter 6, resets the Output Row Counter, pulls down the Over Ride key of the window machine keyboard, drops the window machine from communication with the remote controller, and causes the Transmit Shift Register to transmit to the central data processing station.
processing station an Output Error character, followed by a digit 4.

Let it be assumed that an AEO4 type of error is detected, and Error latch AEO4 is set accordingly. The Select latch ASOS will have been set true when the window machine was selected. The output of this flip-flop, in conjunction with the output of the latch AEO4, will set the Lamp Control Digit 2 latch JWM171 and the Lamp Control Digit 2 latch JWM172 in accordance with the equations JWM171 = ADO2 FC01(13) + AEO4 ASOS and JWM172 = ADO2 FC01(13) + AEO4 ASOS, as shown diagrammatically in Figs. 92 and 93.

The signal AEO4 in combination with the signal FPO(5) causes a true Reset Row Counter Drive signal DR02 in accordance with the expression AEO4 FPO(5) included in the equation for DR02 given in Fig. 48.

The Output Row Counter is now in Count zero, and the Output Program Counter is now in Count 5. The signal FC0(0), in conjunction with the signal AEO4, prepares the gates for generating a true Output Digit 5 signal JWI45 and a true Output Control Row 1 signal JWI21 for causing the Over Ride key of the window machine keyboard to be pulled down.

The true signal AEO4 prevents retriggering of the Time Delay TDO1 in accordance with the equation for TDO1 given in Fig. 52, and the inverse signal TDO1 therefore comes true. This sets the Sync Memory flip-flop GC01 in accordance with the expression FPO(5) FC0(0) TDO1 included in the equation for GC01 given in Fig. 49. Since the signal CT0 is also true in accordance with the equation CT0 = FPO(5), a Program Counter Clock signal CPO is generated in accordance with the expression CT0 GC01 included in the equation for CPO given in Fig. 46. This advances the Output Program Counter from Count 5 to Count 6.

As the Output Program Counter advances from Count 5 to Count 6, the Time Delay one shot TDO2 is triggered in accordance with the equation DR02 = FPO(5) FC0(0) GC01 (AEO1 + ADO2 + AEO3 + AEO4). The Firing Pulse SCR signal DFO is generated by the true signal TDO2 in accordance with the equation for DFO given in Fig. 47.

The true signal DFO completes the gates for the Row 1 Select signal JWI21 and the Digit 5 Select signal JWI45, in accordance with the equations

\[ JWI21 = DFO(FCO(15) + AEO4 FC0(0)) \]

\[ JWI45 = DFO(ADO(5) FC0(9) + FC0(0) AEO4) \]

causing the Solenoid Driver and Grouter circuits to be fired, in the manner previously described, to energize the Over Ride key solenoid for the depression of said key.

The Time Delay signal TDO2 remains true for 49 milliseconds to allow sufficient time for the Over Ride key to be pulled down.

During the time that the Output Program Counter remains in Count 6, the Time Delay signal TDO1 is held true. When the Time Delay TDO2 times out, the inverse signal TDO2 comes true, and the Output Program Counter is able to advance. The Sync Memory flip-flop GC01 is set according to the expression FPO(6) TDO2 included in the equation for GC01 given in Fig. 49. The Main Timing Clock signal CTO is true during Program Count 6, in accordance with the equation CTO = FPO(6). A Program Counter Clock pulse is thus generated in accordance with the equation

\[ CPO = CTO(GC01 + DR01 FPO(0))' \]

and advances the Output Program Counter to Count 7.

The Time Delay one shot TDO1 is no longer held true, and will time out in 65 milliseconds, after which the inverse signal TDO1 will be true. In Program Count 7, the Window Machine Trip signal JWM190 goes true in accordance with the equation

\[ JWM190 = ASOS FPO(7) TDO1 \]

and trips the window machine for operation. The signal JWM190 remains true until the Time Delay TDO1 times out. At such time, the Sync Memory flip-flop GC01 is set in accordance with the expression FPO(7) TDO1 included in the equation for GC01 given in Fig. 49. The Main Timing Signal CTO is true during Program Count 7, in accordance with the equation CTO = FPO(7). A Program Counter Check signal CPO is thus generated in accordance with the equation

\[ CPO = CTO(GC01 + DR01 FPO(0))' \]

which advances the Output Program Counter to Count zero, in which Count the Select flip-flop ASOS is reset in accordance with the equation \( asos = fpo(0) \).

The Output Program Counter will now advance to Program Count 1 with the next two Request for Character signals JCAS. A Main Timing Clock signal CTO is first generated in accordance with the expression JCAS FPO(0). This sets the Sync Memory flip-flop GC01 in accordance with the expression CTO FPO(0) FC0(0) JCA4. The next signal JCAS generates another Main Timing Clock signal CTO, which is effective to generate a Program Counter Clock signal CPO in accordance with the expression CTO GC01. This advances the Output Program Counter to Count 1.

In Program Count 1, the Answer Output Error line ICA103 is made true in accordance with the equation ICA103 = FPO(1) JCA106 GC03(4) AE01 + AEO2 + AEO3 + AEO4)

The true signal ICA103, in conjunction with true signals JCA5 and DR1, generates an Output Error Drive signal DER in accordance with the equation

\[ DER = JCA5 DR1 ICA103 \]

On the next Transmitter Register Empty signal DTE, the Transmit Shift Register is loaded with an Output Error Character by setting of the flip-flops F12 and F16 in accordance with the equations for these flip-flops given in Figs. 56 and 57. The same signals DER, DTE, and CT used in setting these flip-flops also reset the Request to Output Memory latch GRO in accordance with the equation

\[ gro = ct(der dte + dko dte + dm1) \]

Going false of the signal GRO causes the signal ICA106 to go false in accordance with the equation

\[ ICA106 = GRO \]

When the inverse signal ICA106' goes true, the Sync Memory flip-flop GC01 is set in accordance with the expression FPO(1) JCA106' CTO included in the equation for GC01 given in Fig. 49, and a Program Counter Clock signal CPO is generated in accordance with the equation

\[ CPO = CTO(GC01 + DR01 FPO(0))' \]

This causes the Output Program Counter to advance to Program Count 2.

The signal FPO(2), in conjunction with the signal AEO4, causes the Error Encode 2 Bit signal DEO3 to go true in accordance with the equation

\[ DEO3 = FPO(2) GC03 AEO4 \]

The true signal DEO3 produces a true signal on the Input Data 2 Bit line ICA3, in accordance with the equation for ICA3 given in Fig. 34.

The Data On line signal ICA7 goes true in Program Count 2 in accordance with the equation given in Fig. 34. This signal, in combination with the signal ICA5, generates a Load Data signal DLD in accordance with the equation \( dld = jcas ica7 \). This signal DLD will load the flip-flops of the Transmit Shift Register in accordance with Data Bit signals ICA1, ICA2, ICA3, ICA4, which,
when received by the central data processing station, will provide the information that the error which occurred was an AE04 type of error.

The Output Program Counter is advanced to Count 3 by the same signal ICAS5, which generates a Main Timing Clock signal CTO in accordance with the expression ICAS5 FPO(2) included in the equation for CTO given in FIG. 47. The signal CTO, in turn, is effective to set the Sync Memory flip-flop GCOI in accordance with the expression CTO FPO(2), and then to generate a Program Counter Clock signal CPO in accordance with the expression CTO GCOI.

In Program Count 3, the Error latch AE04 is reset in accordance with the equation ouE04 = FPO(3), and the AE04 indicator lamp is thereby extinguished. The Select Register flip-flops ASO1 to ASO4 inclusive are also reset, in accordance with the equations ouSO1 to ouSO4 inclusive = FPO(3).

The next two signals TRS advance the Output Program Counter from Count 3 to Count 4. A signal CTO is generated in accordance with the expression TRS FPO(3), and this is effective to set the Sync Memory flip-flop GCO1 in accordance with the expression CTO GCO1. A Program Counter Clock pulse CPO is then generated by the next signal CTO in accordance with the expression CTO GCO1. This advances the Output Program Counter from Count 3 to Count 4, in which Count it remains until another request to Output signal is received from the central data processing station. As a consequence of this type of Error operating sequence, the window machine will have been operated with the Over Ride key depressed, and the Receive Error lamp on the keyboard of the window machine will have been illuminated.

Power supply and sequencing

The remote controller power supply and sequencing circuitry is shown in FIGS. 97 and 97A, and will now be described.

Let it be assumed that the remote controller is connected over a plug 280 to a 115-volt, 60-cycle A.C. power source, and that the power is turned off in the remote controller. In such a case, the Power Off lamp 1804 on the remote controller control panel is illuminated, over a circuit which includes the lamp 1804 (filaments A and C) in series with the contacts PK202B C3 and extends between the terminals 281, 282, which are connected to a 12.6-volt A.C. supply in the solenoid driver power supply 283. This power supply is of conventional design and is used to provide power at various voltages for the remote controller circuitry.

Now let it be assumed that the Power On button SP081 is momentarily depressed to initiate the power-up sequence. This sequence occurs in two stages of Warm Up and Power On, requiring ten seconds each.

During the first ten seconds of the Warm Up period, the Power Off lamp 1804 is extinguished, the Warm Up lamp 1803 is turned on, the various logic voltages are developed, the cooling fans are turned on, and 115-volt A.C. power is supplied to the data sub-set power receptacle in the remote controller. This manner in which this is accomplished will now be described.

The relay PK202 is energized over a circuit which extends from the 12.6-volt A.C. terminal 281 over a half wave rectifier 284A, closed contacts SP080B controlled by the Power Off button SP082, closed contacts SP080B controlled by the Power On button SP081, closed contacts PK303BC1, PK303BC1, PK303BC2, and the relay PK202, to the other 12.6-volt A.C. terminal 282.

Energization of the relay PK202 causes the contacts PK202BC3 to open in the circuit for the Power Off lamp 1804 (filaments A and C), and that lamp is extinguished. The contacts PK202AC3 close in the circuit for the Warm Up lamp 1803 (filaments B and D), which also includes the normally closed contacts PK203BC1, and that lamp is turned on. The contacts PK202A1 close to complete a holding circuit for maintaining the relay PK202 in energized condition. The contacts PK202A2 close and complete an energizing circuit for the relay PK201, extending from one terminal of the 115-volt A.C. plug 280 over the fuse F201, the contacts PK201A2, the relay PK201, and back to a second terminal of the plug 280.

Energization of the relay PK201 closes the contacts PK201A1, which completes a path over the 5-ampere fuse F201 and the contacts PK201A1 to apply 115-volt A.C. power to the logic power supply 284, which is of conventional design and which is used to supply power at various voltages for the remote controller circuitry.

The contacts PK201A3 are also closed by energization of the relay PK201, and complete a path including two terminals of the 115-volt A.C. supply plug 280, the fuse F202, the contacts PK201A3, the normally closed contacts PK203BC2, and the time delay TD201. This initiates operation of the time delay TD201 and starts it on the first of two ten-second time periods. Closing of the contacts PK201A3 also completes a path for applying power to a data sub-set power receptacle 285.

In addition, energization of the relay PK201 closes the contacts PK201A4, to complete a circuit path for applying 115-volt A.C. power to the motors of two cooling fans 286 and 287.

During the ten-second warm-up period initiated by operating the time delay TD201, the logic voltages of plus 12 volts D.C., minus 8 volts D.C., and minus 20 volts D.C. are developed by the logic power supply 284 in a conventional manner.

At the end of the first ten-second time period, the time delay contacts TD201A1 close, completing a path to energize the relay PK204 over a path which extends from one terminal of the plug 280 over the fuse F201, the closed contacts PK202A2, the contacts TD201A1, and the relay PK204, back to another terminal of the plug 280. Energization of the relay PK204 closes the contacts PK204A1, to complete a holding circuit for maintaining the relay PK204 energized, and also closes the contacts PK204A2 to complete a path for supply 115-volt A.C. power from the plug 280 to the solenoid driver power supply 283.

The time delay TD201 continues on its second ten-second time period, and during this period, the solenoid driver voltages of plus 50 volts D.C., plus 75 volts D.C., 12.6 volts A.C., and one volt A.C. are developed by the solenoid driver power supply 283 in a conventional manner. It may be noted that the plus 75-volt supply is applied to two terminals 276 and 277 in two paths over two resistors 278 and 279, which terminals are connected to the blow-out card circuits of FIG. 98.

At the end of the second ten-second period, the contacts TD201A2, controlled by the time delay TD201, close. This completes a path for energizing the relay PK203, said path extending from one terminal of the plug 280 over the 5-ampere fuse F202, the contacts PK201A3, the contacts TD201A2, and the relay PK203, back to another terminal of the plug 280.

Energization of the relay PK203 closes the contacts PK203A2 to complete a holding circuit for maintaining the relay PK203 in energized condition. The contacts PK203BC2 open, breaking the circuit for the time relay TD201, which permits said time delay to reset to its home position, opening the contacts TD201A1 and TD201A2. The contacts PK203BC1 open, turning off the Warm Up lamp 1803, filaments B and D. The contact PK203A1 closes, completing a circuit to illuminate the Power On lamp 1803, filaments A and C, said circuit extending from the 12.6-volt A.C. terminal 282 over the contacts PK202A3, the contacts PK203A1, the lamp 1803, filaments A and C, and back to the other 12.6-volt A.C. terminal 281. The contacts PK203BC12 (FIG. 83) open, and the contacts K203AC12 (FIG. 83) close to
complete a circuit to initiate the Logic Reset signal DRW. This completes the Power Up sequence.

**Overload protection**

An overload condition of the branch sub-system which is severe enough to blow any of the fuses protecting the D.C. voltage supplies will result in down-sequencing the power distribution. Also, should an SCR driver for the 150-volt solenoid fail to blow out in the prescribed time, a sense circuit has been provided that will detect this failure and will down-sequence the power distribution.

A sense relay PK302 is connected across the terminals of a 2.5-ampere fuse F302 in the minus 8-volt power supply line, and will remain relaxed as long as the fuse is intact. If blown, the fuse causes current to flow through the coil of the relay PK302, thereby energizing said relay. This causes the contacts PK302BC1 to open in the holding circuit for the relay PK202, deenergizing said relay.

Deenergization of the relay PK202 causes the contacts PK202A4 to open to stop the clocking circuit for the relay PK202. The contacts PK202A2 also open, deenergizing the relays PK201 and PK204; and the contacts PK202AC3 open, turning off the Power On lamp 1803, filaments A and C, and B and D. In addition, the contacts PK202BC3 close to turn on the Power Off lamp 1804, filaments A and C.

Deenergization of the relay PK201 causes the contacts PK201A4 to open, turning off the fans 286 and 287. The contacts PK201A1 also open, interrupting the 115-volt A.C. circuits to the logic power supply 284. In addition, the contacts PK201A3 open, interrupting the 115-volt A.C. circuit to the data sub-set receptacle 285, and deenergizing the relay PK203. The previously-mentioned contacts of the relay PK203 transfer in the logic reset circuit and in the indicator lamp circuits.

Deenergization of the relay PK204 causes the contacts PK204A1 to open in the holding circuit for said relay. Also the contacts PK204A2 open to interrupt the 115-volt A.C. power line to the solenoid driver power supply 283.

The sense relay PK303 has two coils, one of which is connected across the terminals of the 5-ampere fuse F301 in the plus 12-volt circuit, and the other of which is connected across the terminals of the 12-ampere fuse F303 in the minus 20-volt circuit. When either of these fuses is blown, the coil associated with it will energize the relay PK303. The contacts PK303BC1 are in series with the contacts PK303BC2 in the energizing circuit for the relay PK202, so that the relay PK202 is deenergized when the contacts PK303BC1 are opened by energization of the relay PK303. This causes the relay PK202 to be deenergized, which, in turn, causes down-sequencing of the power supplies, in the manner previously described.

An SCR Sense circuit has been provided to detect the failure of an SCR driver to "blow out" within a prescribed time limit. This time limit is determined by the SCR Detector term DMO13, in accordance with the equation DMO13 = SW TD02’ [FPO(5') + TD01'], shown in diagrammatic form in FIG. 95. In this equation, SW is the logic term assigned to the contacts PK206A4 (FIG. 95) controlled by the relay PK206 (FIG. 99A), which is energized as long as an output cable of the remote controller is connected through a window machine controller to a window machine. Therefore the contacts PK206A4 will be closed under the above conditions, supplying a ground to this leg of the AND gate shown in FIG. 95. The inverse output TDO2 of the Error Override Time Delay TD02 will always be true under non-error conditions, supplying zero potential to this leg of the AND gate shown in FIG. 95. So, when the signal FGPO(5') is true, the time limit mentioned above will be extended by the 49-millisecond time delay of TD02. In this manner the SCR driver causing energization of the Over Ride key sensor can be sensed.

Under normal conditions, the inverse output TDO1 of the Clock Detector Time Delay TDO1 is false in Output Program Count 5 until the inverse signal FCO(18) goes false. The signal TDO1 goes true in 65 milliseconds, at which time this leg of the AND gate shown in FIG. 95 will be at zero volts potential. Should the signal TDO1 go true in Output Program Count 5 due to loss of clock, the signal DNO13 goes true, so that any SCR's which have been fired can be sensed.

The sense circuit is connected to one side of, and controls, the sense relay PK301 (FIG. 98D). Under normal conditions, the output of the sense circuit zero volts. Since the relay PK301 is connected at its other side to ground over the closed contacts PK203A4, it remains deenergized. However, should an SCR fail to "blow out," the 50-volt potential from the SCR, in conjunction with a true signal DMO13, will apply sufficient potential to the connection with the relay PK301 to cause said relay to be energized. This causes the contacts PK301BC2 (FIG. 97) to open in the energizing circuit for the relay PK202, thereby deenergizing said relay, and causing a down-sequencing of the power supplies. Also the contacts PK301BC1 (FIG. 98D) open, to isolate the energized relay K301 from a portion of the sense circuit. A detailed description of the SCR sense circuit will be given subsequently.

An additional OR input is incorporated in the SCR sense circuit, which detects the loss of either the plus 50-volt supply or the plus 75-volt supply. A relay PK401 (FIG. 97A) is connected between ground and a fuse F402 via a resistor 288 and three zener diodes 289, while a relay PK205 (FIG. 97A) is connected between ground and the fuse F204 via a resistor 290 and two zener diodes 291. The relay PK401 controls normally open contacts PK401BC1 (FIG. 98D) and the relay PK205 controls normally open contacts PK205BC1 (FIG. 98D). These contacts are connected in parallel between ground and a portion of the sense circuit.

Should either the plus 50-volt power supply or the plus 75-volt power supply be lost, its associated relay PK205 or PK401 will be deenergized, causing the corresponding relay contacts PK205BC1 or PK401BC1 to close. This causes the sense circuit to apply sufficient potential to the connection with the relay PK301 to cause said relay to be energized, which results in down-sequencing of the power supplies, as previously described.

**Testing and simulation means**

A number of different testing and simulation means are provided in the present system in order to enable a system user to determine whether or not all parts of the system are functioning properly. FIGS. 99, 99A, 100, 101, 102, and 103 of the drawings are particularly directed to certain portions of the branch sub-system circuitry which provide testing and simulation means.

A first group of tests may be performed when the branch sub-system, including the selected window machine, is in an on-line mode of operation. This, of course, is advantageous, since it eliminates the need for interrupting the regular functioning of the system. A window machine check-out test may be performed with the selected window machine in an on-line mode. This test is controlled by the central data processing station, and serves to check the operability and accuracy of the window machine components and functions. In addition, several types of diagnostic tests are available to give a service man at a given branch the ability to determine the output segment or segments to be transmitted continuously from the central data processing station. These diagnostic tests require the use of special routines which are put into memory at the central data processing station. It should be noted that all of the on-line tests may be controlled by the central data processing station, and do not utilize the special test circuitry of FIGS. 99, 99A, 100, 101, 102, and 103.
A number of additional tests for determining the proper functioning of the various branch components of equipment may be made when these units are off line. Certain of these are performed by operating a "turn-around" switch (not shown) in the branch data sub-set, connecting the data input and data output lines of the data sub-set, so that one window machine can serve as input means for the remote controller, with the input information being transmitted from the window machine through its associated window machine controller to the remote controller, through the data sub-set with "turn-around" switch actuated, and back to the remote controller to illuminate the indicator lights shown in FIG. 98D, as output means to indicate whether or not the branch sub-system equipment is functioning properly in transmitting the input message. Similarly, using the "turn-around" switch of the data sub-set, the test switches SR701 to SR708 inclusive (FIGS. 99 and 99A) of the remote controller may be employed to simulate an output message which is transmitted from the remote controller, through the test sub-set, such as a "turn-around" switch actuated, back to the remote controller, and through a selected window machine controller, to a selected window machine, the keys of which will be operated in accordance with the simulated output message.

It is also possible to operate the sub-system components in off-line tests when these components are disconnected from the branch data sub-set by using a data sub-set simulator, the circuitry for which is shown in FIGS. 101, 102, and 103. This device is partially connected to the remainder of the remote controller circuitry at all times, and the connections are completed, by substituting an electrical plug connection of the data sub-set simulator for the plug connection normally used to connect the data sub-set to the remote controller.

Since the data sub-set simulator does not form a part of the present invention, its structure will not be described in detail. However, it may be pointed out that it includes manually-operable clock and data signal generating means, as well as a 1-kc, signal generating means, in addition to various control switches, all shown in FIG. 103, by means of which clock and data signals may be manually generated for application to the branch sub-system apparatus. The data sub-set simulator also includes indicator lights for various signals, as shown in FIG. 102, and further includes Error Memory latches AE13, AE14, AE15, AE05, AE06, and AE07, shown in FIGS. 100 and 101, for controlling certain of the indicator lights of FIG. 102, and maintaining said certain lights illuminated after completion of an operation, to aid service personnel in diagnosing error conditions.

The data sub-set simulator includes a "turn-around" switch and may be used in place of the data sub-set in performing the types of off-line tests described above. The manual clocking feature of the data sub-set simulator makes it possible to proceed through an operating sequence step by step at a rate determined by the service man switch, and thus greatly facilitates the tracing of error conditions.

In addition to the test apparatus described above, a system simulator (not shown) may be provided to test a window machine separately from the remainder of the branch sub-system, thus enabling the remainder of the sub-system to be utilized in a normal on-line mode, while operation of the window machine is being tested separately.

It is to be understood that the various testing and simulating means described above, and specifically those included in the branch sub-system circuitry, do not form a part of the present invention. However, drawings showing the circuitry involved, as well as a brief description, have been included herein for convenience, since in the branch sub-system forming the illustrated embodiment of the invention, the testing and simulation circuitry is integrally connected to the remainder of the branch sub-system circuitry.

**COMPONENT CIRCUITRY**

In this section, descriptions are provided of the construction and operation of the various components, such as flip-flops, level converters, one-shots, gates, etc., shown in block form in the logic block diagrams of Figs. 91 to 103 inclusive. In the drawings, the circuit diagram for each component accompanied by a block showing the way in which that component is depicted in the logic block diagrams of the drawings. It will, of course, be realized that the invention is not limited to the use of the specific types of circuits shown and described herein for the various components, which are included only for purposes of illustration, since any suitable and well-known types of circuits may be used for the various components.

**Branch to data sub-set level converter**

A circuit for this type of level converter is shown in FIG. 115, together with the block used to represent it in the logic diagrams. Conventionally, the data sub-sets of the illustrated embodiment of the invention employ logic levels of minus 5 volts and plus 5 volts, while the remote controller employs logic levels of minus 8 volts and zero volts. It is therefore necessary to convert the signals which pass between the units from one level to the other. As shown in FIG. 115, an input terminal 301 for the branch to data sub-set level converter is connected over a 2000-ohm resistor 302 to a point 303 in the base circuit of an NPN-type transistor 306. From the point 303 a circuit branch extends over a 5100-ohm resistor 304 to a terminal 305, to which is applied a source of plus 12-volt D.C. potential. The emitter of the transistor 306 is connected to ground, while the collector of said transistor is connected through a 510-ohm resistor 307 in the base circuit of a PNP-type transistor 314. From the point 308, a branch of the circuit extends over a 2400-ohm resistor 309 to a terminal 310, to which is applied a plus 12-volt D.C. source of potential. Also, from a point 311 in the base circuit of the transistor 314, a path extends over a 1000-pico farad capacitor 312 to a point 313 in the collector circuit of the transistor 314. The emitter of the transistor 314 is connected to a terminal 315, to which is applied a plus 5-volt D.C. source of potential.

The point 313 in the collector circuit of the transistor 314 is connected over a point 316 to an output terminal 321 for the level converter circuit. A first branch extends from the point 316 over a 910-ohm resistor 317 to a terminal 318, to which is applied a minus 20-volt D.C. source of potential. A second circuit branch extends from the point 316 over a diode 319 to a terminal 320, to which is applied a minus 5-volt D.C. source of potential.

It will be noted that the level converter is represented diagrammatically by the block 322, having an input terminal 301 and an output terminal 321.

The operation of the circuit of FIG. 115 will now be described. Let it be assumed that the signal level at the input terminal 301 is minus 8 volts. In such a case, the base of the transistor 306 is at approximately minus 1.4 volts, which causes said transistor to be reverse-biased. The base of the transistor 314 in such a case is at approximately plus 12 volts, which causes the transistor also to be reverse-biased. With the transistor 314 reverse-biased, current flows from the minus 5-volt terminal 320 through the forward-biased diode 319 and the resistor 317 to the minus 20-volt terminal 318, causing the output terminal 321 to be at a minus 5-volt potential.

Now let it be assumed that the signal level at the input terminal 301 is switched to zero volts. This causes the potential at the base of the transistor 306 to go to approximately plus 0.4 volt, forward-biasing the transistor 306 into conduction, which causes the base potential of the transistor 314 to go to approximately plus 2.2 volts.

Since the emitter of this transistor is connected to the
plus 5-volt terminal 315, the transistor 314 is now forward-biased and conducting. The clamping diode 319 is reverse-biased in such a case, and the output terminal 321 is at a level of plus 5 volts.

**Data sub-set to branch level converter**

A circuit for this type of level converter is shown in FIG. 116, together with the block used to represent it in the logic diagrams. This converter serves to convert the voltage level of signals passing from the data sub-set to the remote controller from logic levels of minus and plus 5 volts to logic levels of zero and minus 8 volts. As shown in FIG. 116, an input terminal 328 for the data sub-set to branch level converter is connected over a 12,000-ohm resistor 329 to a point 330 in the basic circuit for a PNP-type transistor 333. From the point 330, a branch extends over a 16,000-ohm resistor 331 to a terminal 332, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 333 is connected to ground, and the collector of said transistor is connected to the base of a second PNP-type transistor 341 over a point 334, a 1800-ohm resistor 337, and a point 338. From the point 334 a circuit branch extends over a 2000-ohm resistor 335 to a terminal 336, to which is applied a minus 20-volt D.C. source of potential. From the point 338, a branch circuit extends over a 16,000-ohm resistor 339 to a terminal 340, to which is connected a plus 12-volt D.C. source of potential.

The emitter of the transistor 341 is connected to ground, and the collector of said transistor is connected over a point 342 to an output terminal 345. From the point 342 a first circuit branch extends over a diode to a terminal 347, to which is applied a minus 8-volt D.C. source of potential, and a second branch extends from the point 342 over a 910-ohm resistor 343 to a terminal 344, to which is applied a minus 20-volt D.C. source of potential.

Also included in FIG. 116 is a block representation of the data sub-set to branch level converter as it appears in the logic diagram. In this representation, the block is designated by the reference character 348, while the input terminal and the output terminal are designated by the reference characters 328 and 345, respectively, as they are in the circuit diagram.

Operation of the circuit of FIG. 116 will now be described. Let it be assumed that the level of the signal applied to the input terminal 328 is plus 5 volts. In this case, the base of the transistor 333 is at approximately plus 3 volts, which causes the transistor to be reverse-biased, and which causes the base of the transistor 341 to be at approximately 0.2 volt. In such a case, the transistor 341 conducts, causing the output terminal 345 to be at a signal level of zero volts.

Now let it be assumed that the input signal level at the terminal 328 is switched to minus 5 volts. The base of the transistor 333 is now at approximately 0.2 volt, which forward-biases the transistor 333 into conduction. Conduction of the transistor 333 causes the base of the transistor 341 to go to approximately 1.4 volts, thereby reverse-biasing the transistor 341 and cutting it off. With the transistor 341 non-conducting, the clamp diode 346 is forward-biased and current flows from the minus 8-volt terminal 347 through the diode 346 and the resistor 343 to the minus 20-volt terminal 344, which causes the output terminal 345 to be at a level of minus 8 volts.

**Input level converter**

A circuit for this type of level converter is shown in FIG. 117, together with the block used to represent it in the logic diagrams. In general, voltage levels of zero volts and minus 20 volts are used in the window machine controller and in the window machine, because these voltage levels are suitable for use with relay contacts. On the other hand, as previously indicated, the voltage levels of the remote controller are zero volts and minus 8 volts. As a consequence, it is necessary to provide level converters for converting the level of signals passing between the remote controller and the various window machine controllers. The input level converter converts signal levels of zero and minus 20 volts to signal levels of zero and minus 8 volts.

In FIG. 117, an input terminal 360 is connected over a point 361, a 1500-ohm resistor 364, a point 365, a diode 366, and a point 367, all in series, to the base of an NPN-type transistor 368.

A first branch extends from the point 361 over a 2700-ohm resistor 362 to a terminal 363, to which is applied a minus 20-volt D.C. source of potential. A second branch extends from the point 361 over a diode 371, a point 372, and a 0.047-microfarad capacitor 373, all in series, to a point 374 in the emitter circuit of the transistor 368, said emitter circuit terminating in a terminal 375, to which is connected a minus 8-volt D.C. source of potential. The points 365 and 372 are connected together. A circuit branch extends from the point 367 over a 51,000-ohm resistor 369 to a terminal 370, to which is applied a plus 12-volt D.C. source of potential.

The collector of the transistor 368 is connected over a 3600-ohm resistor 376 and a point 377, in series, to the base of a PNP-type transistor 380. A first branch extends from the point 377 over a 20,000-ohm resistor 378 to a terminal 379, to which is applied a plus 12-volt D.C. source of potential. A second branch extends from the point 377 over a diode 381 to a point 382 in the emitter circuit of the transistor 380, said emitter circuit being connected to ground.

The collector of the transistor 380 is connected over a 1200-ohm resistor 383 and a point 384, in series, to the base of an NPN-type transistor 385. A first circuit branch extends from the point 384 over a 12,000-ohm resistor 386 to a terminal 387, to which is applied a minus 20-volt D.C. source of potential. A second circuit branch extends from the point 384 over a diode 389 to a point 388 in the emitter circuit of the transistor 385, said emitter circuit terminating in a terminal 397, to which is applied a minus 8-volt D.C. source of potential.

The collector of the transistor 385 is connected over a 359 to an output terminal 390. A first circuit branch extends from the point 359 over a diode 391 to ground, and a second circuit branch extends from the point 359 over a point 396, an 820-ohm resistor 392, and a point 393, all in series, to a terminal 394, to which is applied a plus 12-volt D.C. source of potential. Between the points 359 and 393, a second 820-ohm resistor 395 is connected in parallel with the 820-ohm resistor 392.

Also shown in FIG. 117 is a block representation of the input level converter, represented by a block 398, to which are applied the input terminal 360 and the output terminal 390.

The operation of the circuit of FIG. 117 will now be described. Let it be assumed that an input signal of minus 20 volts is applied to the input terminal 360. Current flows, in this case, from the plus 12-volt D.C. terminal 370 over the resistor 369, the diode 366, and the diode 371, to the terminal 360. The base of the transistor 368 is then at a level of approximately minus 17.5 volts, reverse-biasing said transistor.

With the transistor 368 non-conducting, current flows from the plus 12-volt terminal 370 through the diode 378 and the diode 381 to ground. The base of the transistor 380 is at approximately plus 0.4 volt potential, thereby reverse-biased said transistor, to prevent conduction therethrough. With the transistor 380 non-conducting, current flows from the minus 8-volt terminal 397 through the diode 389 and the resistor 386 to the minus 20-volt terminal 387, thereby reverse-biasing the transistor 385 and preventing conduction therethrough. Since the transistor 385 is non-conducting, it is applied forward a plus 12-volt terminal 394 through the parallel resistors 392 and 395, and through the diode 391 to ground. Since the
diode 391 is conducting, the output terminal 390 is at ground potential or zero volt.

Now let it be assumed that the signal on the input terminal 360 is switched to zero volts. Current now flows from the plus 12-volt terminal 370 over the resistor 369 and the diodes 366 and 371 to the terminal 360, which is at zero volts. In this case, the potential at the base of the transistor 368 is approximately minus 7.8 volts, forward-biasing said transistor and causing it to conduct. Current thus flows from the plus 12-volt terminal 379 through the resistors 378 and 376, and through the transistor 368, to the minus 8-volt terminal 375. This causes the diode 381 to be reverse-biased. The base of the transistor 386 and output terminal 411 applied thereto, which forward-biases said transistor, causing it to conduct. Current flows from ground through the transistor 380, the resistor 363, and the resistor 386 to the minus 20-volt terminal 387. The diode 389 is reverse-biased, and the base of the transistor 386 is at approximately minus 7.4 volts potential, forward-biasing the transistor 386 and causing current to flow from the plus 12-volt D.C. terminal 394 through the parallel resistors 392 and 395, and through the transistor 385 to the minus 8-volt terminal 397. The clamping diode 391 is reverse-biased, and the potential at the terminal 390 is minus 8 volts D.C.

**Output level converter**

A circuit for this type of level converter is shown in FIG. 118, together with the block used to represent it in the logic diagram. The output level converter is used to convert the logic levels of zero and minus 8 volts used in the remote controller to the logic levels of zero and minus 20 volts used in the window machine controller and the window machine.

In FIG. 118, an input terminal 401 is connected over a 1800-ohm resistor 402 and a point 403 to the base of a PNP-type transistor 404. From the point 403, a first circuit branch extends over an 18,000-ohm resistor 405 to a terminal 406, to which is applied a plus 12-volt D.C. source of potential. A second branch extends from the point 403 over a diode 407 to a point 408 in the collector circuit of the transistor 404.

The emitter of the transistor 404 is connected to ground. The collector of the transistor 404 is connected to ground, the output terminal 408 to an output terminal 411, and is also connected over the point 406 and a 5100-ohm resistor 409 to a point 410, to which is applied a minus 20-volt D.C. source of potential. Also shown in FIG. 118 is a block 412, representing the showing of the output level converter in the logic block diagrams. The block 412 has the input terminal 401 and the output terminal 411 applied thereto.

The operation of the circuit of FIG. 118 will now be described. Let it be assumed that a signal having a potential of zero volts is applied to the input terminal 401. In this case, the voltage drop between the plus 12-volt D.C. terminal 406 and the input terminal 401, through the resistors 405 and 402, will cause the base of the transistor 404 to be at approximately plus 1.2 volts potential. The transistor 404 is therefore reverse-biased and cut off. The potential at the output terminal 411 will accordingly be minus 20 volts.

Now let it be assumed that the input signal potential at the terminal 401 is switched to minus 8 volts. In this case, the voltage at the base of the transistor 404 is changed to approximately minus 0.2 volt, which forward-biases the transistor 404 and causes it to conduct. In such a case the potential at the output terminal 411 is at zero volts. It may be noted that a negative feedback circuit is formed by the capacitor 407, which is connected between the collector and the base of the transistor 404. Changes on the collector are coupled back to the base and cause the base potential to cause the base potential to change more slowly. This feed-back causes the rise time of the output signal to be between two and 7.5 microseconds. The fall time of the output signal is less than 20 microseconds.

**Logic inverter**

A circuit for the logic inverter is shown in FIG. 119, together with the block used to represent it in the logic diagrams.

The various inverters described herein, including logic, power, drive, NPN, and special NPN inverters, having the symbols I2, I3, I4, I5, and IC, respectively, are effective to invert a signal from one logic level to the other, and differ in accordance with the varying circuit requirements of the other logical elements with which they are used.

An input terminal 418 is provided for the logic inverter of FIG. 119, and is connected over a point 419, a 3900-ohm resistor 420, a point 421, and a point 422 to the base circuit of a PNP-type transistor 423. A 240-microfarad capacitor 424 is connected between the points 419 and 421 in parallel with the resistor 420. A circuit branch extends from the point 422 over a 33,000-ohm resistor 425 to a terminal 426, to which is applied a source of +12-volt D.C. potential.

The emitter of the transistor 423 is connected to ground, while the collector of said transistor is connected over points 427 and 428 to an output terminal 429. From the point 427, a branch extends over a 2200-ohm resistor 430 to a terminal 431, to which is connected a source of minus 20-volt D.C. potential, and from the point 428 a branch extends over a diode 432 to a terminal 433, to which is connected a minus 8-volt D.C. source of potential.

Also shown in FIG. 119 is a block 434, to which the input and output terminals 418 and 429 are applied, representing the manner in which the logic inverter is shown in the logic block diagrams.

The operation of the logic inverter of FIG. 119 will now be described. Let it be assumed that the input at the terminal 418 is at a true level of zero volts. In such a case, the voltage at the base of the transistor 423 is at approximately plus 0.2 volt, which prevents said transistor from conducting. With the transistor 423 non-conducting the output at the terminal 429 is clamped at minus 8 volts by the diode 432 conducting through the resistor 430 to the minus 20-volt supply at the terminal 431. Now let it be assumed that the signal at the input terminal 418 is switched to a false level of minus 8 volts. The voltage at the base of the transistor 423 is now minus 0.2 volt, which causes said transistor to conduct. The potential of the collector now rises toward ground, reverse-biassing the diode 432. With collector potential at ground, the potential at the output terminal 429 is also at ground.

**Power inverter**

A circuit for the power inverter is shown in FIG. 120, together with the block used to represent it in the logic diagrams.

An input terminal 438 is provided for the power inverter of FIG. 120, and is connected over a point 439, a 1800-ohm resistor 440, a point 441, and a point 442 to the base circuit of a PNP-type transistor 443. A 350-microfarad capacitor 444 is connected between the points 439 and 441 in parallel with the resistor 440. A circuit branch extends from the point 442 over a 16,000-ohm resistor 445 to a terminal 446, to which is applied a plus 12-volt D.C. source of potential.

The emitter of the transistor 443 is connected to ground, while the collector of said transistor is connected over points 447 and 448 to an output terminal. From the point 447, a branch extends over a 1100-ohm resistor 450 to a terminal 451, to which is connected a source of minus 20-volt D.C. potential, and from the point 448, a branch extends over a diode 452 to a terminal 453, to which is connected a minus 8-volt D.C. source of potential.
Also shown in FIG. 120 is a block 454, to which the input and output terminals 438 and 449 are applied, representing the manner in which the power inverter is shown in the logic diagrams.

The operation of the power inverter is identical to the operation of the logic inverter. The only difference between the two inverters is the component size, which enables the power inverter to deliver approximately double the output current that the logic inverter can deliver.

**Drive inverter**

A circuit for the drive inverter is shown in FIG. 121, together with the block used to represent it in the logic diagrams.

An input terminal 458 is provided for the drive inverter of FIG. 121, and is connected over a point 459, a 650-ohm resistor 460, a point 461, and a point 462 to the base circuit of a PNP-type transistor 463. A 1500-microfarad capacitor 464 is connected between the points 459 and 461 in parallel with the resistor 460. A circuit branch extends from the point 462 over a 10,000-ohm resistor 465 to a terminal 466, to which is applied a source of plus 12-volt D.C. potential.

The emitter of the transistor 463 is connected to ground, while the collector of said transistor is connected over points 467 and 468 to an output terminal 469. From the point 467, a branch extends over a 2200-ohm resistor 470 to a terminal 471, to which is applied a source of minus 20-volt D.C. potential, and from the point 468 a branch extends over a diode 472 to a terminal 473, to which is applied a minus 8-volt D.C. source of potential.

Also shown in FIG. 121 is a block 474, to which the input and output terminals 458 and 469 are applied, representing the manner in which the drive inverters are shown in the logic diagrams.

The operation of the drive inverter is identical to that of the logic inverter. The only difference between the two inverters is the component size, which enables the drive inverter to deliver approximately five times the output current that the logic inverter delivers.

**NPN inverter**

A circuit for the NPN inverter is shown in FIG. 122, together with the block used to represent it in the logic diagrams.

An input terminal 478 is provided for the NPN inverter of FIG. 122, and is connected over a point 479, a 750-ohm resistor 480, a point 481, and a point 482 to the base circuit of an NPN-type transistor 483. A 1000-microfarad capacitor 484 is connected between the points 479 and 481 in parallel with the resistor 480. A circuit branch extends from the point 482 over a 3,600-ohm resistor 485 to a terminal 486, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 483 is connected to a terminal 487, to which is applied a minus 8-volt D.C. source of potential. The collector of said transistor is connected over points 488 and 489 to an output terminal 490. From the point 488, a branch extends over a 2200-ohm resistor 491 to a terminal 492, to which is applied a plus 12-volt D.C. source of potential, and from the point 489, a branch extends over a diode 493 to ground.

Also shown in FIG. 122 is a block 494, to which the input and output terminals 478 and 490 are applied, representing the manner in which the NPN inverters are shown in the logic block diagrams.

The operation of the NPN inverter of FIG. 122 will now be described. First let it be assumed that the input at the terminal 478 is at a true level of zero volt. In such a case, the potential at the base of the transistor 483 is minus 7.8 volts. Since the emitter of the transistor 483 is connected to a minus 8-volt potential source, said transistor conducts, and current flows from the plus 12-volt terminal 492 through the resistor 491 and the transistor 483 to the minus 8-volt terminal 487. The diode 493 is reverse-biased by the collector of the transistor 483 going to minus 8 volts, and the output at the terminal 490 is accordingly minus 8 volts.

Now let it be assumed that the input signal at the terminal 478 is switched to a minus 8-volt level. The potential at the base of the transistor 483 is now minus 10 volts, and said transistor is cut off. In this case, the diode 493 is forward-biased, and current flows from the plus 12-volt terminal 492 through the resistor 491 and the diode 493 to ground, so that the potential at the output terminal 490 is switched to a zero volt level.

**Special NPN inverter**

A circuit for the special NPN inverter is shown in FIG. 123, together with the block used to represent it in the logic diagram.

An input terminal 498 is provided for the special NPN inverter of FIG. 123, and is connected over a point 499, a 2200-ohm resistor 500, a point 501, and a point 502 to the base circuit of an NPN-type transistor 503. A 330-microfarad capacitor 504 is connected between the points 499 and 501 in parallel with the resistor 500. A circuit branch extends from the point 502 over a 33,000-ohm resistor 505 to a terminal 506, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 503 is connected to a terminal 507, to which is applied a minus 8-volt D.C. source of potential. The collector of said transistor is connected over points 508 and 509 to an output terminal 510. From the point 508, a branch extends over a 4700-ohm resistor 511 to a terminal 512, to which is applied a plus 12-volt D.C. source of potential. From the point 509, a branch extends over a diode 513 to ground.

Also shown in FIG. 123 is a block 514, to which the input and output terminals 498 and 510 are applied, representing the manner in which the special NPN inverters are shown in the logic diagrams.

The operation of the special NPN inverter is the same as that described for the NPN inverter. The two inverters are the same in circuit configuration, and differ in that the special NPN inverter has output capabilities which exceed those of the NPN inverter.

**OR gate**

Shown in FIG. 124 is a typical OR gate configuration having three inputs, together with the block which is used to represent an OR gate in the logic block diagrams. OR gates may have any desired number of inputs from two on, but the one shown in FIG. 124, having three inputs, will be described as illustrative.

The three input terminals 518, 519, and 520 are each connected over diodes 521, 522, and 523, respectively, to points 524, 525, and 526, respectively, which are also connected to a conductor extending over a 3000-ohm resistor 527 to a terminal 528, to which is applied a minus 20-volt D.C. source of potential. At its other end, said conductor terminates in an output terminal 529.

The block 530, having inputs 518, 519, and 520 and an output 529, shows the OR gate as represented in the logic block diagrams.

Operation of the OR gate is as follows. Logic level input voltages at the input terminals 518 to 520 inclusive are switched between the false level of minus 8 volts and the true level of zero volt. When the input voltages are all at the false level of minus 8 volts, a current of 4 milliamperes per diode flows from the terminals 518, 519, and 520, through the diodes 521, 522, and 523, and the 3000-ohm resistor 527 to the minus 20-volt terminal 528.

The output voltage in this case is at the false level of minus 8 volts, less the diode voltage drop, which amounts to 0.4 volt per diode. When any input voltage at any one of the terminals 518 to 520 inclusive is switched to the true level of zero volts, the current increases to 7 milliamperes per diode, over a circuit extending from the zero-volt terminal, through the diode (or diodes) and the...
resistor 527 to the minus 20-volt terminal 528. The output voltage at the terminal 529 is then switched to zero volts, less the diode voltage drop. When one input voltage is switched to a false level of minus 8 volts, the output voltage remains at zero volts, because the diode connected to the input terminal to which the minus 8-volt signal level is applied is reverse-biased. When all of the input terminals 518 to 520 inclusive have minus 8-volt signals applied thereto, the output terminal 529 is switched to minus 8 volts.

**AND gate**

Shown in Fig. 125 is a typical AND gate configuration having three inputs, together with a block showing the manner in which an AND gate is represented in the logic block diagrams. It will be realized that an AND gate can have any number of inputs from two on, and that the three-input AND gate shown in Fig. 125 is merely illustrative of AND gates having other numbers of inputs.

The AND gate of Fig. 125 is provided with three input terminals 534, 535, and 536, which are connected over diodes 537, 538, resistors 541, and 542 on a conductor which extends over a 24,000-ohm resistor 543 to a terminal 544 at one end, to which is applied a plus 12-volt D.C. source of potential. At its other end, the conductor extends to an output terminal 545.

Also included in Fig. 125 is a block 546 representing the manner in which AND gates are shown in the logic block diagrams. The block 546 is provided with input terminals 534, 535, and 536, and with an output terminal 545.

In operation of the AND gate, logic level input voltages are switched between the false level of minus 8 volts and the true level of zero volts. When all of the input voltages applied to the terminals 534 to 536 inclusive are at the false level of minus 8 volts, a current of 0.8 milliampere per diode flows from the plus 12-volt supply terminal 544 through the resistor 543 and the diode 537 to 539 inclusive to the terminals 534 to 536 inclusive. At this time, the output at the output terminal 545 is minus 8 volts. When the input voltage at any of the terminals 534 to 536 inclusive is switched to a true level of zero volts, the output voltage of the terminal 545 remains at a minus 8-volt level because the diode connected to the terminal to which the zero-volt signal level is applied is reverse-biased. When the signal levels at all of the input terminals 534 to 536 inclusive are switched to zero volts, the current flow decreases to 0.5 milliampere per diode from the plus 12-volt terminal 544 through the resistor 543 and the diodes 537 to 539 inclusive to the input terminals 534 to 536 inclusive. The output voltage at the terminal 545 is then switched to a true level of zero volts plus the voltage drop across the diodes, which amounts to 0.2 volt per diode. When inverted logic signals are applied to the AND circuit and all of the inputs are at the true level of zero volts, then the output at the terminal 545 is zero volts. When any single input voltage at any of the terminals 534 to 536 inclusive is switched to a false level of minus 8 volts, then the output voltage at the terminal 545 is switched to a minus 8-volt level.

**Flip-flop**

A two-transistor NPN flip-flop circuit is used in the illustrated embodiment of the remote controller and is shown in Fig. 126, together with a block representation of the manner in which the flip-flop appears in the logic block diagrams. The flip-flop has multiple inputs, so that it can be operated by either positive-going or negative-going logic input signals. A positive-going clock input is used to internally gate the selected input signal. As is customary in flip-flop circuits, the circuit configuration allows only one transistor to be conducting at a given time. The output of the two transistors are used to describe the “state” of the flip-flop. When one of the transistors is conducting, the flip-flop is said to be “on,” or in the “set” state. The reverse condition, in which the other flip-flop is conducting and the first transistor is cut off, is said to be the “off,” or “reset,” state.

Four input terminals 550 to 555 inclusive are provided in the flip-flop circuit shown in Fig. 126, and two output terminals 554 and 555, designated F and F’, are provided. Of the input terminals, the terminals 550 and 551 are “set” terminals, designated f and f’, respectively, and terminals 552 and 553 are “reset” terminals, designated of and of’, respectively. Two voltage levels can be used to trigger the set and reset sides of the flip-flop. A true level of zero volt is used to trigger the circuit when applied to the f or of input terminals 550 and 552, while a false level of minus 8 volts is used to trigger the circuit when applied to the f’ and of’ input terminals 551 and 553. Additional input terminals 556 and 557 are provided, and are connected to the input terminals 551 and 553 over diodes 558 and 559 to permit the “ANDing” of true inputs when desired.

When the true-level input terminals 550 and 552 are used, the false-level input terminals 551 and 553 must be connected to a minus 8-volt supply or a minus 8-volt potential on the input terminals 554 and 555, and a diode is connected in a series with each of these terminals in the appropriate direction. When the false-level input terminals 551 and 553 are used, the true-level input terminals 550, 552, 556, and 557 may be left “floating” when not otherwise connected to an input circuit. The selected input signals must be present in conjunction with the fall of a clock signal which is applied at clock terminal 560 in order to cause the flip-flop to change states.

The construction of the circuit of Fig. 126 will now be described. Included in said circuit are two NPN-type transistors 561 and 562, the emitters of which are connected to a source of minus 8-volt D.C. potential at terminals 563 and 564. The collector of the transistor 561 is connected over points 565, 566, and 567, and over a 2200-ohm resistor 568, to a terminal 569, to which is applied a source of plus 12-volt D.C. potential. The point 565 is connected over a point 570 to the output terminal 554. From the point 570 a path extends over a diode 571 to a base reference potential, shown here as ground. The collector of the transistor 562 is connected over points 572, 573, and 574 and a 2200-ohm resistor 575 to a terminal 576, to which is applied a source of plus 12-volt D.C. potential. The point 572 is connected over a point 577 to the output terminal 555. From the point 577 a path extends over a diode 578 to ground.

From the point 572 in the collector circuit of the transistor 561, a path extends over a 3300-ohm resistor 579, a point 580, a point 581, a diode 582, a point 583, and a point 584 to the base of the transistor 562. A 500-microfarad capacitor 585 is connected between the points 567 and 580 in parallel with the resistor 579. From the point 581 a path extends over a diode 586 and a point 587 to a point 572 in the collector circuit of the transistor 562.

In a similar manner, the point 573 in the collector circuit of the transistor 562 is connected over a 3300-ohm resistor 588, a point 589, a point 590, a diode 591, a point 592, and a point 593 to the base of the transistor 561. A 500-microfarad capacitor 594 is connected between the points 574 and 589 in parallel with the resistor 588. From the point 590 a path extends over a diode 595 and a point 596 to the point 565 in the collector circuit of the transistor 561.

The points 583 and 592 are connected over resistors 597 and 598, of 15,000 ohms each, to a terminal 599, to which is applied a minus 20-volt D.C. source of potential.

From the point 593 in the base circuit of the transistor 561 a path extends over a diode 600, points 601 and 602, a diode 603, a point 604, a 7500-ohm resistor 605, a point
606, an 8200-ohm resistor 607, and a point 608 to the input terminal 550. A 22,000-ohm resistor 609 is connected between the points 601 and 604 in parallel with the diode 603. A 560-microfarad capacitor 610 is connected between the point 602 and a point 611 in parallel with the points 605 and 607. From the point 604 a path extends over an 820-ohm resistor 612 to the input terminal 551. From the point 606 a path extends to a terminal 613, to which is applied a plus 12-volt D.C. source of potential. From the point 611 a path extends over the diode 558 to the input terminal 556. The base of the capacitor 584 in the base circuit of the transistor 562, a path extends over a diode 616, a point 617, a diode 618, a diode 619, a point 620, a 7500-ohm resistor 621, a point 622, an 8200-ohm resistor 623, and a point 624 to the input terminal 552. A 22,000-ohm resistor 625 is connected between the points 617 and 620 in parallel with the diode 619. A 560-microfarad capacitor 626 is connected between the points 618 and a point 627 in parallel with the resistor 621 and 623. From the point 620 a path extends over an 820-ohm resistor 628 to the input terminal 553. From the point 622 a path extends to a terminal 629, to which is applied a plus 12-volt D.C. source of potential. From the point 627 a path extends over the diode 559 to the input terminal 557.

From the point 611, a path extends over a point 630 and a diode 631 to the point 597, which is connected to the collector circuit of the transistor 562. Similarly, from the point 627 a path extends over a point 632 and a diode 633 to the point 596, which is connected to the collector circuit of the transistor 561. From the point 630 a path also extends over a diode 634 to a point 635, which is connected to the clock input terminal 560. Likewise, a path extends from the point 632 over a diode 636 to the point 635 and thence to the clock input terminal 560.

Also shown in FIG. 126 is a block 637, representing the flip-flop as shown in the logic block diagrams. Applied to the block 637 are the input terminals 550 to 553, the output terminals 554 and 555, and the clock terminal 560.

Operation of the flip-flop of FIG. 126 will now be described. Let it be assumed that the flip-flop is in the reset state, with the transistor 561 conducting, the transistor 562 cut off, and the input terminal 550, together with the terminal 556, disconnected and "floating." The base of the transistor 562 is at a potential of approximately minus 7 volts, and the base of the transistor 562 is at a potential of approximately minus 10 volts, causing the output terminal 554 to be at a minus 8-volt signal level and the output terminal 555 to be at a zero volt signal level. Also it be assumed that the signal input level at the terminal 556 is minus 8 volts. Current flows from the plus 12-volt terminal 613 through the resistor 605 and the resistor 612 to the terminal 551, causing the point 604 to be at minus 6.2 volts. The diodes 600 and 603 are reverse-biased, and with no current flow through the resistor 609, the potential at the points 601 and 602 is approximately 6.2 volts.

With the potential at the clock terminal 560 to minus 8 volts, the diode 634 is forward-biased, and the side of the capacitor 610 adjacent the point 611 is at a potential of minus 8 volts. As the clock pulse goes true, the potential at the side of the capacitor 610 adjacent to the point 611 goes to zero volts, so that the capacitor is charged. At the fall of the clock pulse, the side of the capacitor 610 adjacent to the point 611 again assumes a potential of minus 8 volts. The charge of the capacitor 610 adjacent to the negative-going clock signal. As the other side of the capacitor 610 adjacent to the point 602 goes toward a potential of approximately minus 14 volts, the diode 600 becomes forward-biased, providing a discharge path for the capacitor 610. Current then flows from the base circuit of the transistor 561 through the diode 600 to the capacitor 610. This current reduces the current flow in the base-emitter junction of the transistor 561, causing said transistor to go toward cut-off. Less current flow in the emitter-collector circuit of the transistor 561 causes less voltage drop across the collector resistor 568. This positive-going change is coupled via the capacitor 585 and the resistor 579 to the base of the transistor 562, and changes the base of said transistor 562 to a less negative potential, thus causing the transistor 562 to begin to conduct.

The collector of the transistor 562 then goes toward a potential of minus 8 volts, which negative-going change is coupled via the capacitor 594 and the resistor 588 to the base of the transistor 561, driving the transistor 561 into a cut-off condition, while the transistor 562 is, in turn, driving the transistor 562 toward a saturated condition. The diodes 582 and 586 form an "anti-saturation" network which prevents the transistor 562 from being driven into saturation. This is necessary in order to keep said transistor at a more sensitive level for faster switching.

With the transistor 561 cut off, current flows from the plus 12-volt terminal 569 over the resistor 568 and the diode 571 to ground, clamping the signal level at the output terminal 554 at zero volt, which is the "true" level of the output signal, indicating that the flip-flop is in its "set" state.

Let it now be assumed that the flip-flop is in the "set" state, and that the input terminal 553 is connected to a minus 8-volt supply and that the input terminal 552 is connected to a logic term through an external node (not shown). Let it now be assumed that the signal level at the clock input terminal 556 is at minus 8 volts, and that the signal level at the terminal 552 is at minus 8 volts. Current flows from the plus 12-volt D.C. terminal 629 through the resistor 623 to the minus 8-volt clock terminal 560 and the minus 8-volt input terminal 552, causing one side of the capacitor 626 to be at a minus 8-volt level. Current also flows from the plus 12-volt D.C. terminal 629 through the resistor 621 and the resistor 628 to the minus 8-volt signal level at the terminal 553, causing the other side of the capacitor 626 to be at minus 6.2 volts.

Now let it be assumed that the input signal at the terminal 552 is switched to zero volt, while the clock is still at minus 8 volts. Current will then flow from the plus 12-volt level at the terminal 629 through the resistor 623 to the minus 8-volt level at the clock terminal 560, which will keep one side of the capacitor 626 at a minus 8-volt signal level. Now let it be assumed that the signal level at the input terminal 552 remains true and the clock signal at the terminal 556 goes true. Current now flows from the plus 12-volt terminal 629 to zero volts at the input terminal 552 and at the clock terminal 560, which causes the side of the capacitor 626 adjacent to the point 627 to go to a zero volt level, thereby causing the other side of the capacitor 626 adjacent to the point 627 to be switched to minus 6.2 volts. At the fall of the clock signal from zero to minus 8 volts at the terminal 560, the side of the capacitor 626 adjacent to the point 627 is switched to a minus 8-volt signal level, which voltage change causes the capacitor to charge in the opposite direction, drawing current from the base circuit of the transistor 562, as previously described, and causing the flip-flop to begin to switch following the same principle as has previously described in setting of the flip-flop. It is believed that further explanation of the operation of the flip-flop is not necessary, since the above description will provide an adequate explanation to one skilled in the art.

**Exclusive OR**

Shown in FIG. 127 is a circuit which may be employed in the present invention to perform the exclusive OR logical function, together with a block representing the manner in which said circuit is shown in the logic block diagrams. The illustrated exclusive OR circuit uses two PNPs-type transistors connected in a circuit configuration which provides a true output level of zero volt when either one of its two inputs is at a true level of zero volt and the other one of said inputs is at a false level of minus 8 volts. The
circuit provides a false output at a level of minus 8 volts when both inputs are at the same level (either both true or both false).

The circuit of FIG. 127 is provided with two input terminals 645, 646 and an output terminal 647. A path connects the input terminal 645 to the base of a PNP-type transistor 649 over a point 649, an 820-ohm resistor 650, and a point 651. A 240-microfarad capacitor 652 is connected in parallel with the resistor 650 between the points 649 and 651. A path extends from the point 651 over a 56,000-ohm resistor 653 to a terminal 654, to which is applied a source of plus 12-volt D.C. potential. A path connects the input terminal 646 to a second PNP-type transistor 635 over a point 655, an 820-ohm resistor 657, and a point 658. A 240-microfarad capacitor 659 is connected in parallel with the resistor 657 between the points 656 and 658. A path extends from the point 658 over a 56,000-ohm resistor 660 to a terminal 661, to which is applied a source of plus 12-volt D.C. potential.

The two transistors 648 and 655 are cross-coupled, the emitter of the transistor 648 being connected to the point 656 in the base circuit of the transistor 655, while the emitter of the transistor 655 is connected to the point 649 in the base circuit of the transistor 648. The collectors of the transistors 648 and 655 are connected to a common point 662, from which a path extends over a 5600-ohm resistor 663 to a terminal 664, to which is applied a minus 20-volt D.C. source of potential. From the point 662 a second path extends over a diode 665 to a terminal 666, to which is applied a source of minus 8-volt D.C. potential. A third path extends from the point 662 to the output terminal 647.

Also shown in FIG. 127 is a block 667, to which the input terminals 645 and 646 and the output terminal 647 have been applied. This block represents the manner in which the exclusive OR circuit of FIG. 127 is shown in the logic block diagrams.

The operation of the exclusive OR circuit of FIG. 127 will now be described. First let it be assumed that a signal level of zero volt is present at both of the input terminals 645 and 646. Under these conditions, the emitters of the transistors 648 and 655 will be at zero volts, and the bases of these transistors will be at approximately 1.8 volts. The two transistors 648 and 655 are thus reverse-biased and cut off. With no current through the transistors, their collectors will be clamped at minus 8 volts, by the conduction of a minus 8-volt potential through the diode 665 and the resistor 663 to the minus 20 volts supply at the terminal 664. Now let it be assumed that the signal level at the input terminal 646 is switched to minus 8 volts while the input at the input terminal 645 remains at zero volt. The transistor 655 now has zero volts at the emitter and approximately minus 5 volts at the base, which forward-biases said transistor and causes it to conduct. In this case, the transistor 648 remains reverse-biased, with minus 8 volts on the emitter and plus 1.8 volts on the base. The collector of the transistor 655 goes toward ground, reverse-biasing the diode 665 and causing the potential level at the output terminals 647 to rise toward the true level of zero volt. Since the circuit is symmetrical, the discussion above also applies to the case where the input at the terminal 645 is switched to minus 8 volts and the input at the terminal 646 remains at zero volt. The output signal at the terminal 647 in such a case also is then at a zero-volt level.

Finally, let it be assumed that the signal levels at both of the input terminals 645 and 646 are at minus 8 volts. The emitters of both the transistors 648 and 655 are then at minus 8 volts, while the bases of said transistors are at a potential level of approximately minus 5 volts. Both transistors are thus reverse-biased and cut off. In such a case, the potential level at the output terminal 647 is clamped at minus 8 volts through the diode 665. The capacitors 652 and 659 are used to give a faster fall time at the output of the circuit.

OR-inverter
Shown in FIG. 128 is an OR-inverter circuit used in the present invention to provide a combined logical OR and signal inverting function. Also shown in FIG. 128 is a representation of the manner in which this circuit is shown in block form in the logic block diagrams.

The circuit shown in FIG. 128 actually consists of a group of four OR gates, each coupled to an inverter, with each OR gate having one of its inputs common to all four in the group. Since the four individual OR-inverter circuits are identical, only one such individual circuit will be described in detail.

Five input terminals 671 to 675 inclusive are provided for the circuit of FIG. 128, together with four output terminals 676 to 679 inclusive. It will be noted that the input signal applied to the terminal 675 is applied to all of the four OR gates of the circuit together with a signal from one of the other input terminals 671 to 674 inclusive.

Taking the uppermost individual circuit of FIG. 128 as illustrative, the input signals on the terminals 671 and 675 are applied over diodes 680 and 681 to a point 682 connected over a 3000-ohm resistor 683 to a terminal 684, to which is applied a source of minus 20-volt D.C. potential. From the point 682 a path also extends over a point 685, an 8100-ohm resistor 686, and points 687 and 688 to the base of a PNP-type transistor 689. A 330-microfarad capacitor 690 is connected between the points 685 and 687 in parallel with the transistor 688. From the point 688 a path extends over a 16,000-ohm resistor 691 to a terminal 692, to which is applied a plus 12-volt D.C. source of potential.

The emitter of the transistor 689 is connected to ground, and the collector of said transistor is connected over points 693 and 694 to the output terminal 676. From the point 693 a path extends over a 1100-ohm resistor 695 to a terminal 696, to which is applied a minus 20-volt D.C. source of potential. From the point 694 a path extends over a diode 697 to a terminal 698, to which is applied a minus 8-volt D.C. source of potential.

Also shown in FIG. 128 is a block 699 representing the manner in which the OR-inverter circuit is shown in the logic block diagrams. The input terminals 671 to 675 inclusive and the output terminals 676 to 679 inclusive are shown as applied to the block 699.

The mode of operation of the circuit of FIG. 128 is believed to be obvious to one skilled in the art, since the OR gate comprising the two input terminals such as 671 and 675 together with the diodes such as 680 and 681 operates in the same manner as the OR gate previously described. Similarly, the inverter portion of the circuitry of FIG. 128 operates in the same manner as the inverters previously described.
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Taking the uppermost individual circuit of FIG. 129 as illustrative, the input signals on the terminals 704 and 708 are applied over diodes 713 and 714, functioning as an AND gate, to a 24,000-ohm resistor 716 to a terminal 717, to which is applied a source of plus 12-volt D.C. potential. From the point 715, a path also extends over a point 718, a 3900-ohm resistor 719, and points 720 and 721 to the base of a PNP-type transistor 722. A 240-microfarad capacitor 723 is placed in parallel between the points 718 and 720. From the point 721, a path extends over a 33,000-ohm resistor 724 to a terminal 725, to which is applied a plus 12-volt D.C. source of potential.

The emitter of the transistor 722 is connected to ground, and the collector of said transistor is connected over points 726 and 727 to the output terminal 709. From the point 726, a path extends over a 2200-ohm resistor 728 to a terminal 729, to which is applied a minus 20-volt D.C. source of potential. From the point 727, a path extends over a point 730 to a terminal 731, to which is applied a minus 8-volt D.C. source of potential.

Also present in FIG. 129 is a block 732 representing the manner in which the circuit of FIG. 129 is shown in the logic block diagram. Applied to the block 732 are input terminals 704 to 708 inclusive and output terminals 709 to 712 inclusive.

The mode of operation of the circuit of FIG. 129 is believed to be obvious to one skilled in the art, since the AND gate comprising the two input terminals such as 704 and 708 and the diodes 713 and 714 operates in the same manner as the AND gate previously described. Similarly, the inverter portion of the circuitry of FIG. 129 operates in the same manner as the inverters previously described.

Logic latch

A logic latch element used in the illustrated embodiment of the present invention is shown in FIG. 130, together with a block representation of said latch as it appears in the logic block diagrams. It will be noted that a block representing an OR gate is associated with a block representing the latch, and that an OR gate circuit is associated with the latch circuit in FIG. 130.

Two output terminals 734 and 735 and four input terminals 736 to 739 inclusive are provided for the circuit of FIG. 130. Of these, the input terminals 737, 738, and 739 are connected to diodes 742 and 743. The collector point 743 to form the OR gate mentioned above. The input terminal 736 is connected over a diode 744, a point 745, an 1800-ohm resistor 746, and a point 747 to the base of a PNP-type transistor 748. The diode 744, together with a diode 749, forms an AND gate for applying input signals to the base of the transistor 748. The diode 749 is adapted to receive a signal from another portion of the circuit not yet described, and is also connected over a point 750 to the point 745. From the point 750, a second path extends over a 24,000-ohm resistor 751 to a terminal 752, to which is applied a plus 12-volt D.C. source of potential. Also from the point 750, a branch extends over a 330-microfarad capacitor 753 and a point 754 to the point 747. A further path extends from the point 754 over a 16,000-ohm resistor 755 to a terminal 756, to which is applied a plus 12-volt D.C. source of potential. The emitter of the transistor 748 is connected to ground, and its collector is connected over points 757 and 758 to a diode 759. From the point 757 a path extends over a 1100-ohm resistor 760 to a terminal 761, to which is applied a source of minus 20-volt D.C. potential. From the point 758, a path extends over a point 762 and a diode 763 to a terminal 764, to which is applied a source of minus 8-volt D.C. potential. From the point 762 a path extends to the output terminal 734.

The point 743 is connected over a point 765 to a diode 766. From the point 765, a path also extends over a 3000-ohm resistor 767 to a terminal 768, to which is applied a minus 20-volt D.C. source of potential.

The diodes 759 and 766 together constitute a second AND gate in FIG. 130. The collector of the diode 759 is connected in a common circuit with the diode 766 over points 769 and 770. From these points a parallel combination of a 1800-ohm resistor 771 and a 330-microfarad capacitor 772 extends over additional points 773 and 774 to the base of a second PNP-type transistor 775.

In FIG. 130 an additional path extends over a 24,000-ohm resistor 776 to a terminal 777, to which is applied a source of plus 12-volt D.C. potential. Also from the point 773, an additional path extends over a 10,000-ohm resistor 778 to a terminal 779, to which is applied a source of plus 12-volt D.C. potential.

The emitter of the transistor 775 is connected to ground, while its collector is connected over points 780, 781, and 782 to the output terminal 735. From the point 780, an additional path extends over an 1100-ohm resistor 783 to a terminal 784, to which is applied a source of minus 20-volt D.C. potential. From the point 782, a path extends over a diode 785 to a terminal 786, to which is applied a source of minus 8-volt D.C. potential. From the point 784, a path extends back to the diode 749 to provide one of the inputs for the AND gate comprising that diode and the diode 748.

Also shown in FIG. 130 is the block 788 representing the manner in which the associated logical latch and OR gate are shown in the logic block diagrams. The output terminals 734 and 735, and the input terminals 736 to 739 inclusive, are applied to the blocks 787 and 788.

The operation of the logic latch will now be described. Let it be assumed that the latch is in a reset state, in which the signal at the output terminal 734 is at zero volt and the signal at the terminal 735 is at minus eight volts. The transistor 748 is conducting while the transistor 775 is cut off. Let it also be assumed that the input signal at terminal 736 is at zero volt, while the input signal through the OR gate is at minus 8 volts at the point 743. This negative input to the AND gate made up of the diodes 759 and 766 causes the base of the transistor 775 to go negative, so that said transistor conducts, and the output signal at the terminal 735 goes to zero volt.

It will be recalled that the collector of the transistor 775 is connected over the point 782 to the diode 749. Therefore the collector of diode 749, and consequently the collector of the transistor 775 is "ANDed" with the zero-volt signal input of the terminal 736 through the diodes 749 and 744, respectively. The base of the transistor 748 thus goes to a positive potential, which reverse-biases said transistor and turns it off. Current now flows from the minus-8-volt terminal 764 through the diode 763 and the resistor 760 to the minus 20-volt terminal 761 and causes the output terminal 734 to go to a minus 8-volt signal level. This minus 8-volt signal is also applied to the diode 759, which keeps the transistor 775 in conduction regardless of any further changes in the signal at point 743, and thus maintains the OR gate terminals 737 to 739 inclusive. The latch is now in the set state and will remain in that state until it is reset.

With the latch in the set state described above, and with the input signal level at point 743 at zero volt, let it be assumed that the input signal at the terminal 736 is switched to a signal level of minus 8 volts. This causes the output of the AND gate made up of the diodes 744 and 749 to go toward a minus 8-volt level. The base potential of the transistor 748 consequently goes negative and forward-biases said transistor into conduction. With the transistor 748 conducting, the signal level at the output terminal 734 goes to zero volt. The zero-volt input to the diode 759 is combined with the zero-volt input to the diode 766 in the AND gate made up of these two diodes and causes the base of the transistor 775 to go to a positive potential, which cuts off said transistor. Current now flows from the minus 8-volt terminal 786
through the diode 785 and the resistor 783 to the minus 20-volt supply at the terminal 784. The output terminal 735 is thus clamped at the minus 8-volt signal level. With the output signal levels described above, the latch is in the reset state.

It is possible for both the output terminals 734 and 735 to be at zero volt at the same time if both of the input signal levels—namely, the signal level at the terminal 736 and the signal level at the point 743—are at a minus 8-volt level, regardless of the previous state of the signal latch. However, the inputs to this type of latch are logically controlled to prevent this condition from occurring.

**Five-volt power supply**

Shown in FIG. 131 is a circuit for providing plus and minus five-volt power supplies, together with a block showing the manner in which this circuit is represented in the logic block diagrams.

A minus five-volt power supply is provided by the circuit of FIG. 131 at the terminal 794, and a plus five-volt power supply is provided at the terminal 795. The terminal 794 is connected over points 796 and 797 to the emitter of a PNP-type transistor 798. The collector of said transistor is connected over a 16-ohm resistor 799 to a terminal 800, to which is applied a minus 8-volt D.C. source of potential. The base of said transistor is connected over a point 801 and an 82-ohm resistor 802 to a terminal 803, to which is applied a minus 8-volt D.C. source of potential. From the point 801 a circuit path also extends over a zener-type diode 804 and points 805 and 806 to a connection to a base reference potential shown here as ground. Between the points 805 and the emitter circuit of the transistor 798 are connected in parallel a 50-ohm resistor 807 and a 0.68-microfarad capacitor 808.

The plus five-volt D.C. terminal 795 is connected over points 809 and 810 to the emitter of a PNP-type transistor 811. The collector of the transistor 811 is connected over a 12-ohm resistor 812 and points 813 and 814 to the point 806, which, it will be recalled, is connected to ground. A 1.5-microfarad capacitor 815 is connected between the points 809 and 814. A second path extends from the point 809 over a 120-ohm resistor 816 to a terminal 817, to which is applied a plus 12-volt D.C. source of potential. A second path extends from the point 810 over a 40-ohm resistor 818 to a terminal 819, to which is applied a plus 12-volt D.C. source of potential. The base of the transistor 811 is connected over a point 820 and a zener-type diode 821 to a second path extending from the point 820 over a 270-ohm resistor 822 to a terminal 823, to which is applied a plus 12-volt D.C. source of potential.

Also shown in FIG. 131 is a block representation of the manner in which the circuit is illustrated in the logic block diagrams. This includes interconnected blocks 824 and 825 representing the minus five-volt power supply and a plus five-volt power supply, respectively, with the appropriate output power supply terminals 794 and 795 connected thereto.

Operation of the circuit of FIG. 131 will now be described. It may be noted that the minus 8-volt and the plus 12-volt regulated power supply outputs of the remote control are used as input voltages for the minus five-volt and plus five-volt supplies, respectively.

With respect to the plus five-volt power supply, let it be assumed that the plus 12-volt power supply is on. With plus 12-volt power to the circuit, current flows from the plus 12-volt terminal 823 through the resistor 822 and the zener-type diode 821 to ground at the connection associated with point 806. The zener-type diode 821 causes the base of the transistor 811 to remain at approximately plus 5 volts. The plus 5 volts is also supplied to the emitter of the transistor 811, and said transistor is forward-biased into conduction. With said transistor conducting, current flows from the plus 12-volt terminals 817 and 819 over the parallel resistors 816 and 818 in series with the transistor 811 and the resistor 812 to ground. The voltage divider network formed by these four components mentioned above causes the emitter of the transistor 811 to be at a voltage level of plus five volts.

The regulation is accomplished by the current dividing principle. With no load connected to the output terminal 795, all current flows through the transistor 811 and the resistor 812. With a load connected to the terminal 795, the current divides between the load and the transistor 811, resistor 812 circuit. Should the load increase, the voltage at the terminal 795 goes toward the value of plus four volts, causing the emitter of the transistor 811 to be less positive. The transistor accordingly reduces its conduction. Less current flowing through the transistor and through the resistor 812 results in having more current available to the load. This increase in current to the load results in restoring the terminal 795 to the desired plus five-volt operating level. The capacitor 815 is used to filter minor fluctuations of the load.

With respect to the operation of the minus five-volt supply portion of the circuitry of FIG. 131, let it be assumed that the minus 8-volt power supply is on. With minus 8 volts available to the minus 5-volt supply circuit, current flows from ground through the zener-type diode 804 and the resistor 802 to the minus 8-volt terminal 803. The zener-type diode 804 causes the base of the transistor 798 to remain at a level of approximately minus 4.7 volts, so that it is forward-biased and conducting. With no load at the terminal 794, all current flows through the transistor 798 to the minus 8-volt terminal 803, causing the voltage at the terminal 794 to be minus 4.4 volts. As the load increases, the voltage drop across the resistor 807 increases, causing the emitter of the transistor 798 to become more negative. The transistor accordingly decreases its conduction and thereby makes more current available to the load. The output of the minus 5-volt power supply accordingly will be seen to be approximately minus 4.4 volts.

**Special relay driver**

Shown in FIG. 132 is a special relay driver circuit employed in the illustrated embodiment of the present invention, together with a block diagram representing the manner in which said circuit is shown in the logic block diagrams.

An input terminal 829 in the circuit of FIG. 132 is connected over a 12,000-ohm resistor 830 and a point 831 to the base of an NPN-type transistor 832. From the point 831 a second path extends over a 20,000-ohm resistor 833 to a terminal 834, to which is applied a source of minus 20-volt D.C. potential.

The emitter of the transistor 832 is connected to a terminal 835, to which is applied a source of minus 8-volt D.C. potential, while the collector of said transistor is connected over points 836, 837, a 150-ohm resistor 838, and a point 839 to the base of a PNP-type transistor 840. From the point 836, a path extends over a 80-ohm resistor 841 to a terminal 842. From the point 837 a path extends over a diode 843 to ground. From the point 839, a first path extends over a 1,500-ohm resistor 844 to a terminal 845, to which is applied a source of plus 12-volt D.C. potential, while a second path extends to a terminal 846. The emitter of the transistor 840 is connected to ground, while its collector is connected to an output terminal 847 for the circuit of FIG. 132.

For certain uses of the circuit, the terminals 842 and 846 may be connected by a jumper wire 848, shown in dashed lines, or by other suitable means, as will subsequently be described in detail.

Also shown in FIG. 132 is a block 849 illustrating the manner in which the voltage at the output of FIG. 132 is represented in the logic block diagrams. Applied to the block 849 are the input and output terminals 829 and 847, as well as the dashed line 848 representing a jumper wire between the terminals 842 and 846. Where the jumper wire is not
used in the logic block diagrams, no line appears therein, and the wire used is a solid line appears.

Operation of the circuit of FIG. 132 will now be described. The circuit is used in the drive and decoder portion of up to eight relays. It is arranged so that the current output capabilities can be increased by placing the jumper wire 848 between the terminals 842 and 846, which increases the base drive to the output transistor 840. Input levels between zero and minus 0.3 volt are effective to turn on the driving circuit, and levels between minus 7.66 volts and minus 8.49 volts are effective to turn off said circuit. Without the jumper connection, the maximum output current that the circuit can drive is 370 milliamperes. With the jumper connection, maximum deliverable output current increases to 1.32 amperes.

Let it be assumed that the input signal level at the terminal 829 is minus 8 volts. The junction of the resistors 830 and 833, and the base of the transistor 832, at the point 831, is at approximately 8.6 volts, which reverse-biases the transistor 832. Current flows from the plus 12-volt supply through the transistors 844 and 838, and the diode 843 to ground. The potential at the base of the transistor 840 is plus 2 volts, which reverse-biases said transistor. With the transistor 840 cut off, the output terminal 847 has no path to ground, and consequently a circuit connected to it is interrupted.

Now it is to be assumed that the input terminal 829 is switched to zero volt. The potential at the base of the transistor 832 is now minus 7.2 volts, which forward-biases the transistor into conduction. Current now flows from the plus 12-volt terminal 845 through the resistor 844, the resistor 838, and the transistor 832 to the minus 12-volt terminal 835. The clamping diode 843 is now reverse-biased, and the base of the transistor 840 is now at minus 0.2 volt. Accordingly, the transistor 840 now conducts and provides ground potential for the output terminal 847. The current flows from the ground connection through the transistor 840 to the terminal 847 and through the connected relay or lamp circuit to a minus 20-volt source of potential elsewhere.

**AND diodes**

Shown in FIGS. 133, 134, and 135 are sub-circuits containing one or more diodes connected between terminals to enable the diodes to be connected as desired into other portions of the circuitry of the logic block diagrams. This type of arrangement increases the flexibility of circuit design and assembly, and permits increased manufacturing economy. Also shown in association with the various sub-circuits in FIGS. 133, 134, and 135 are blocks 850, 851, and 852, respectively, illustrating the manner in which the various AND diode circuits, having different numbers of terminals, are represented in the logic block diagrams. Reference characters have not been applied to the individual diodes and terminals of FIGS. 133, 134, and 135, since the arrangement of these sub-circuits is believed to be obvious from the drawings without further explanation. It may be noted that a complete AND circuit may be obtained by connecting an AND diode sub-circuit in an appropriate manner to a "resistor AND" sub-circuit (to be described subsequently). Also the AND diode sub-circuits may be used in other circuit relationships in accordance with the function which it is desired to perform utilizing that particular portion of the logic block diagrams.

**Decimal-to-binary encoder**

Shown in FIG. 136 is a circuit which is used for decimal-to-binary encoding purposes in the illustrated embodiment of the present invention. As included in FIG. 136 is a block which illustrates the manner in which the decimal-to-binary encoder is represented in the logic block diagrams.

The circuit of FIG. 136 has ten input terminals 854 representing the ten decimal digit values, and has six output terminals 855, representing binary digit values 1, 2, 4, and 8 plus special outputs X and P. The input and output terminals are interconnected in a network according to a predetermined pattern in order to produce the desired encoding function. Diodes 856 are placed in the lines associated with each of the input terminals in order to prevent any undesired "sneak" paths from being available to cause erroneous encoding.

The block 857 included in FIG. 136, to which input terminals 854 and output terminals 855 are applied, illustrates how the decimal-to-binary encoder is represented in the logic block diagrams.

The operation of the circuit of FIG. 136 will now be described. Only one of the ten digit lines connected to the terminals 854 will be at a true level of zero volt at any one time, while the one time, while the other nine lines are at a level of minus 20 volts. Let it be assumed that the input terminal 854 representing the digit "6" is at a true level of zero volt. In such a case, the four diodes in the lines connected to the digit 6 are all forward-biased, and the output terminals 855 associated with the values P, 2, 4, and X are true. A true-level signal on the output terminal having value P indicates that an additional bit is required to satisfy the "parity" requirements. The output terminals 2 and 4 being true and the output terminals 1 and 8 being false set up the binary configuration for the decimal digit 6. The output terminal X being true indicates that the digit being encoded is an even number. It will be noted that the output terminal 855 having value X will be true when a zero, 2, 4, 6, or 8 is encoded.

**Clamping diodes**

Shown in FIG. 137 is a circuit used to provide clamping diodes for a number of lines in the logic block diagrams. This circuit includes a plurality of input terminals 858, each having a line connected thereto with a diode 860 in said line. All of the lines are connected to a common which in turn is connected to a terminal 859, to which is applied a source of minus 20-volt D.C. potential.

Also shown in FIG. 137 is a block 861, having the terminals 858 applied thereto, which is representative of the manner in which the clamping diode block is illustrated in the logic block diagrams.

**Binary-to-decimal encoder No. 1**

Shown in FIGS. 138A and 138B, taken together, is a binary-to-decimal encoding circuit which is used in the illustrated embodiment of the present invention, together with a block representing the same circuit as shown in the logic block diagrams.

This circuit includes nine output terminals 865 comprising eight terminals for receiving binary information as to the state of the output and inverse output lines from other circuit components of the system, plus one terminal connected to ground. Thus the input terminals represent binary values 1, 2, 4, and 8, plus the inverse of each of these values.

A total of ten output terminals 866 for the circuit of FIGS. 138A, 138B are provided, each corresponding to one of the decimal values zero to nine inclusive. Each output terminal is connected over a logic inverter circuit to selected ones of the input terminals 865 over a five-legged AND gate, as may readily be seen in FIGS. 138A and 138B.

Since all of the output portions of the binary-to-decimal encoder are generally similar except for the particular input terminals with which the various AND gates are connected, only one such circuit will be described; namely, the circuit in FIG. 138A for producing a decimal digit five output. In that circuit, the output terminal 866 is connected over points 867 and 868 to the collector of a PNP-type transistor 869. From the point 867, an additional circuit branch extends over a diode 870 to a terminal 871, to which is applied a source of minus 8-volt
D.C. potential. From the point 868, an additional circuit path extends over a 2200-ohm resistor 872 to a terminal 873, to which is applied a source of minus 20-volt D.C. potential.

The emitter of the transistor 869 is connected to ground, and the base of said transistor is connected over points 874 and 875, and a parallel combination of a 3900-ohm resistor 876 and a 240-microfarad capacitor 877 to a point 878 of an AND gate which includes five diodes 879 connected at points such as 880 to common conductors associated with each of the input terminals 865. From the point 874 an additional path extends over a 3300-ohm resistor 881 to a terminal 882, to which is applied a source of plus 12-volt D.C. potential. From the point 878 of the AND gate, a circuit branch also extends over a 24,000-ohm resistor 883 to a terminal 884, to which is applied a source of plus 12-volt D.C. potential.

Also shown in FIGS. 138A, 138B is a block 885 illustrating the manner in which the binary-to-decimal encoding circuit is represented in the logic block diagrams. This block shows input terminals 865 and output terminals 866 associated therewith.

The operation of the binary-to-decimal encoding circuit will now be described. The input terminals 865 designated B1, B2, B4, B8, B1', B2', B4', and B8' represent the two possible states of the four binary bits of a binary-coded decimal term, while the input terminal designated G is connected to ground or to a logic term which will gate the encoding circuit.

Let it be assumed that the terminal G is connected to ground and the binary configuration for the decimal digit five is present at the input terminals 865. Voltage levels of the various input terminals are then as follows:

<table>
<thead>
<tr>
<th>Terminal</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>0</td>
</tr>
<tr>
<td>B2</td>
<td>-8</td>
</tr>
<tr>
<td>B4</td>
<td>-8</td>
</tr>
<tr>
<td>B8</td>
<td>-8</td>
</tr>
<tr>
<td>B1'</td>
<td>-8</td>
</tr>
<tr>
<td>B2'</td>
<td>0</td>
</tr>
<tr>
<td>B4'</td>
<td>0</td>
</tr>
<tr>
<td>B8'</td>
<td>0</td>
</tr>
</tbody>
</table>

It will be seen from FIG. 138A that the only AND gate to have all five inputs is the AND gate associated with the decimal digit five output terminal 866. The zero-volt output from the AND gate at the point 878 causes the transistor 869 to be cut off and the output terminal 866 for the decimal digit five to be clamped at a minus 8-volt level. The outputs of all of the other AND gates of the encoder will be at a minus 8-volt level, so that their associated transistors are conducting, and their associated output terminals are accordingly at a zero-volt level. The minus 8-volt signal at the decimal digit five output terminal 866 thus indicates that five was the binary-coded decimal number received.

Binary-to-decimal encoder No. 2

Shown in FIGS. 139A and 139B, taken together, is a second type of binary-to-decimal encoding circuit, which is similar to the circuit shown in FIGS. 138A and 138B, except that a plurality of OR gates are employed in place of the AND gates employed in the former circuit. Also shown in FIG. 139B is a block representing the subject circuit as shown in the logic block diagrams. This circuit includes nine input terminals 890 comprising eight terminals for receiving binary information as to the state of the output and inverse output lines from other circuit components of the system, plus one terminal connected to ground. Thus the input terminals represent binary values 1, 2, 4, and 8, plus the inverse of each of these values.

A total of ten output terminals 891 for the circuit of FIGS. 139A, 139B are provided, each corresponding to one of the decimal values zero to nine inclusive. Each output terminal is connected over a logic inverter circuit to selected ones of the input terminals over a five-lead OR gate, as may readily be seen in FIGS. 139A, 139B.

Since all of the output terminals of the binary-to-decimal encoder of FIGS. 139A and 139B are generally similar except for the particular input terminals which the various OR gates are connected, only one such circuit will be described; namely, the circuit in FIG. 139A for producing a decimal digit five output. In that circuit, the output terminal 891 is connected over points 892 and 893 to the collector of a PNP-type transistor 894. From the point 892 an additional circuit branch extends over a diode 895 to a terminal 896, to which is applied a source of minus 8-volt D.C. potential. From the point 893, an additional circuit path extends over an 1100-ohm resistor 897 to a terminal 898, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 894 is connected to ground, and the base of said transistor is connected over points 899 and 900, and a parallel combination of an 1800-ohm resistor 901 and a 330-ohm-microfarad capacitor 902 to a point 903 of an OR gate which includes five diodes 904 connected at points such as 905 to common conductors associated with each of the input terminals 890. From the point 899 an additional path extends over a 16,000-ohm resistor 906 to a terminal 907, to which is applied a plus 12-volt D.C. source of potential. From the point 903 of the OR gate, a circuit branch also extends over a 3000-ohm resistor 908 to a terminal 909, to which is applied a minus 20-volt source of potential.

Also shown in FIGS. 139A and 139B is a block 910 illustrating the manner in which the binary-to-decimal encoding circuit of FIGS. 139A, 139B is represented in the logic block diagrams. This block shows input terminals 890 and output terminals 891 associated therewith.

The operation of the binary-to-decimal encoding circuit No. 2 will now be described. The input terminals 890 designated B1, B2, B4, B8, B1', B2', B4', and B8' represent the two possible states of the four binary bits of a binary-coded decimal term, while the input terminal designated G is connected to a logic term which will gate the encoding circuit.

Let it be assumed that the input terminal 890 designated G is connected to a gate term that is at a minus 8-volt level, and that the binary configuration for the decimal digit five is present at the input terminals 890. The voltage levels of the various input terminals are then as follows:

<table>
<thead>
<tr>
<th>Terminal</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>0</td>
</tr>
<tr>
<td>B1'</td>
<td>-8</td>
</tr>
<tr>
<td>B2</td>
<td>-8</td>
</tr>
<tr>
<td>B2'</td>
<td>0</td>
</tr>
<tr>
<td>B4</td>
<td>-8</td>
</tr>
<tr>
<td>B4'</td>
<td>0</td>
</tr>
<tr>
<td>B8</td>
<td>-8</td>
</tr>
<tr>
<td>B8'</td>
<td>0</td>
</tr>
</tbody>
</table>

It will be seen from FIG. 139A that the only OR gate to have all five inputs false is the OR gate associated with the decimal digit five output terminal 891. The resulting minus 8-volt output from the OR gate causes the transistor 894 to conduct, which provides a true zero-volt output at the output terminal 891 associated with the decimal output. The outputs of all of the other OR gates of the encoder will be at zero-volt level, so that their associated transistors will be cut off and their associated output terminals 891 will be clamped at a minus 8-volt level. The zero-volt output at the decimal digit five output terminal 891 thus indicates that five was the binary-coded decimal number received.

60 and 350 millisecond retriggerable one-shots

Shown in FIG. 140 is a circuit for a retriggerable one-shot device which may be employed in the present invention, together with two blocks showing the circuit, with different component values to provide two different delay times, as represented in the logic block diagrams. In the illustrated embodiment, the circuit of FIG. 140 is used for two different one-shots, one having a duration of 60
milliseconds, and the other having a duration of 350 milliseconds. The 60-millisecond one-shot will be described herein, and it will be understood that the same circuit may be used to provide a 350-millisecond one-shot by appropriate changes in component values.

As shown in FIG. 140, the circuit is provided with an input terminal 914 and an output terminal 915. The terminal 914 is connected over a parallel combination of a 3900-ohm resistor 916 and a 240-microfarad capacitor 917 to the base of a PNP-type transistor 918. Between the parallel combination of resistor and capacitor and the base of the transistor, a circuit branch extends over a 33,000-ohm resistor 919 to a terminal 920, to which is applied a plus 12-volt source of D.C. potential. The emitter of the transistor 918 is connected to ground, and the collector of said transistor is connected over points 922 and 923, and a parallel combination of a 1500-ohm resistor 924 and a 470-microfarad capacitor 925 to the base of a PNP-type transistor 926. From the point 922, a branch extends over a 1600-ohm resistor 927 to a terminal 928, to which is applied a source of minus 20-volt D.C. potential. From the point 923, a circuit branch extends over a diode 929 to a terminal 930, to which is applied a minus 8-volt D.C. source of potential. Between the parallel combination of the resistor 924 and the capacitor 925 and the base of the transistor 926, a circuit branch extends over a 16,000-ohm resistor 931 to a terminal 923, to which is applied a plus 12-volt D.C. source of potential.

The emitter of the transistor 926 is connected to ground, while the collector is connected over a point 933, a diode 934, a point 935, a parallel combination of a 2700-ohm resistor 936 and a 330-microfarad capacitor 937, and a point 938 to the collector of an NPN-type transistor 939.

From the point 935 a circuit branch extends over a 2400-ohm resistor 940 to a terminal 941, to which is applied a minus 20-volt D.C. source of potential. From the point 938 a circuit branch extends over a 6200-ohm resistor 942 to a terminal 943, to which is applied a plus 12-volt D.C. source of potential.

The emitter of the transistor 939 is connected over points 944 and 945, a diode 946, points 947 and 948, a diode 949, a point 950, and a 560-microfarad capacitor 951 to the previously-described point 923 in the circuit of the transistor 918. The collector of the transistor 939 is connected over a 3000-ohm resistor 952 to a terminal 953, to which is applied a plus 12-volt D.C. source of potential.

From the point 944, a circuit branch extends over a 10,000-ohm resistor 954 to ground. From the point 945, a circuit branch extends over a 150,000-ohm resistor 955 to a terminal 956, to which is applied a minus 20-volt D.C. source of potential. From the point 944, a circuit branch extends over a 430,000-ohm resistor 957 to a terminal 958, to which is applied a plus 12-volt D.C. source of potential. From the point 950, a first path extends over a 6800-ohm resistor 959 to ground, while a second path extends over a 100,000-ohm resistor 960 to a terminal 961, to which is applied a minus 20-volt D.C. source of potential.

From the point 948, a path extends to a point 962 in the base circuit of a PNP-type transistor 963. The emitter of said transistor is connected over a point 964 and a 430,000-ohm resistor 965 to a terminal 966, to which is applied a plus 12-volt D.C. source of potential. From the point 964, an additional path extends to the base of a PNP-type transistor 967, the emitter of which is connected to ground. The collectors of the transistors 963 and 967 are connected together over points 968, 969, and 970. From the point 968, a path extends over a 2200-ohm resistor 971 to a terminal 972, to which is applied a minus 20-volt D.C. source of potential.

From the point 968, an additional circuit path extends over a parallel combination of a 1500-ohm resistor 973 and a 330-microfarad capacitor 974 to the base of a PNP-type transistor 975. Between said parallel combination and the base of said transistor a path extends over a 16,000-ohm resistor 976 to a point 977, to which is applied a plus 12-volt D.C. source of potential. The emitter of the transistor 975 is connected to ground, and the collector is connected over a point 978 to the output terminal 915. From the point 978, a first circuit path extends over a diode 979 to a terminal 980, to which is applied a minus 8-volt D.C. source of potential. A second path extends from the point 978 over a 1000-ohm resistor 981 to a terminal 982, to which is applied a minus 20-volt D.C. source of potential.

Returning now to the point 933, a path extends therefrom over a point 983, a diode 984, a point 985, a parallel combination of a 1600-ohm resistor 986 and a 470-microfarad capacitor 987, and a point 988 to the base of a PNP-type transistor 989. The emitter of said transistor is connected to ground. From the point 988 an additional branch extends over an 11,000-ohm resistor 990 to a point 991, to which is applied a plus 12-volt D.C. source of potential. From the point 985, an additional path extends over a point 992 and a 2200-ohm resistor 993 to a terminal 994, to which is applied a minus 20-volt D.C. source of potential.

The previously-mentioned point 990 is connected over a point 995 and a diode 996 to the point 992. From the point 995 an additional path extends over a diode 997 to a terminal 998, to which is applied a minus 8-volt D.C. source of potential.

The previously-mentioned point 962 is connected over a point 999 and a diode 1000 to ground, and is also connected from the point 999 over a diode 1001, a 620-ohm resistor 1002, a point 1003, a point 1004, parallel capacitors 1005 and 1006, each of 0.39-microfarad capacitance; and a point 1007, to the collector of the transistor 989. The point 983 is connected to the point 1003 over a diode 1008. The point 1007 is connected over two parallel 500-ohm resistors 1009 and 1010 to terminals 1011 and 1012, to each of which is applied a minus 20-volt D.C. source of potential.

A terminal 1013, to which is applied a minus 20-volt D.C. source of potential, is also connected to the point 1007 over an 1800-ohm resistor 1014, a point 1015, and a diode 1016. From the point 1015 a path extends over a zener-type diode 1017 to ground. An additional path also extends from the point 1015 over another zener-type diode 1018 to a point 1019, which is connected over a 430-ohm resistor 1020 to a terminal 1021, to which is applied a minus 20-volt D.C. source of potential.

The point 1019 is connected over a 50,000-ohm variable resistor 1022 and a 140,000-ohm resistor 1023, in series, to the point 1004.

Also shown in FIG. 140 is a first block 1027, which illustrates the manner in which the 60-millisecond one-shot described above in FIG. 140 is depicted in the logic block diagram. The input terminal 914 and the output terminal 915 are shown as applied to the block 1027. In addition, FIG. 140 also shows a block 1028, having the input terminal 914 and the output terminal 915 applied thereto, which depicts the manner in which a 350-millisecond one-shot is represented in the logic block diagrams. As has been previously stated, the circuit for the 350-millisecond one-shot is substantially identical to the circuit for the 60-millisecond one-shot, with the component values being altered to produce the longer delay. It is believed that it would be obvious for one skilled in the art to develop the necessary component values to produce the desired 350-millisecond delay, and consequently that circuit will not be described in detail herein.

Operation of the circuit of FIG. 140 will now be described. This one-shot is triggered by a zero-volt input, having a duration of 200 microseconds or more, applied to the input terminal 914. This produces a change in the voltage level of the output signal from minus 8 volts to
zero volt. The output signal returns to a minus 8-volt level 65 milliseconds after the fall of the last input trigger signal. Input trigger signals occurring after a first trigger signal 8 volts below this 65-millisecond time-out of the one-shot cause the output signal level to remain at a true level of zero volts, reset the timing circuit, and, at the fall of the last such input trigger signal, begin the timing out of the one-shot circuitry. Let it first be assumed that the input at the terminal 914 is at a level of minus 8 volts. The transistors 967, 963, and 918 are conducting, while the transistors 926, 939, 989, and 975 are cut off. The output at the terminal 915 is clamped by the diode 979 at minus 8 volts.

Now let it be assumed that the signal on the input terminal 914 is switched to zero volts. This positive-going 8-volt change causes the potential at the base of the transistor 918 to go to plus one volt, reverse-biasing said transistor and cutting it off. This causes the collector of said transistor to be clamped at minus 8 volts, through the diode 929 and the resistor 927 to the minus 20-volt supply and the change is coupled to the base of the transistor 926 through the capacitor 925 and the resistor 924, causing the base of the transistor 926 to go to a level of minus 0.4 volt, thereby forward-biasing said transistor and causing it to conduct. As a result, the collector of the transistor 926 is pulled to the minus 0.4-volt reference by the diode 9008 to conduct from zero volt through the resistor 1023, the resistor 1022, and the resistor 1020, to the minus 20-volt potential applied to the terminal 1021. The point 1003 is then at a minus 0.4-volt potential. The diode 904 is forward-biased at this time, causing the base of the transistor 999 to be at a plus 0.5-volt potential, which will keep said transistor reverse-biased.

The junction of the collector of the transistor 989, the capacitors 1005 and 1006, the resistors 1009 and 1010, and the diode 1016, namely point 1007, will be at minus 8.5 volts due to conduction of the diode 1016 from the minus 8.5-volt reference at the point 1015 through the resistors 1009 and 1010 to the minus 20-volt potential source.

A zero-volt potential on the collector of the transistor 926 causes the base of the transistor 939 to go to a plus 1.5-volt potential, thereby forward-biasing said transistor, which is of the NPN type, so that the emitter of the transistor 939 assumes a level of plus 1.5 volts. The zero-volt potential on the collector of the transistor 926 also causes the base of the transistor 963 to go to plus 0.2 volt potential, the transistor 963 and cutting it off. The base of the transistor 967 is switched to plus 0.2 volt, reverse-biasing that transistor. The collectors of the transistors 963 and 967 go to a level of minus 8 volts, due to the conduction of minus 8 volts, through the diode 997 and the resistor 971 to the minus 20-volt supply at the terminal 972. This 8-volt negative-going change is coupled through the capacitor 974 and the resistor 973 to the base of the transistor 975. The base of said transistor is now at a level of minus 0.4 volt, so that said transistor conducts, which results in a signal level of minus 20 volts at the input terminal 915.

Now let it be assumed that the input at the terminal 914 switches back to a minus 8-volt level. The base of the transistor 918 is accordingly switched to a level of minus 4 volts, thereby forward-biasing said transistor and causing it to conduct. The collector of said transistor then goes to a zero-volt level, causing the base of the transistor 926 to switch to plus 1-volt signal level. The collector of the transistor 926 accordingly goes to a level of approximately minus 12 volts, causing the base of the transistor 939 to go to a level of minus 5 volts, thereby reverse-biasing the transistor 939, which is thereby rendered incapable of holding the transistor 963 in an off condition.

As the transistor 926 was turned off, the negative-going change on the collector of the transistor 926 is "QRed" with the collectors of the transistors 963 and 967 through the diodes 984 and 996 to the base of the transistor 989, which is now switched to a level of minus 0.5 volt. The transistor 989 is now forward-biased, which causes the point 1007 to go toward a zero-volt level. This 8-volt change causes the capacitors 1005 and 1006 to be charged over a circuit which extends through the resistors 1023, 1022, and 1020 to the minus 20-volt terminal 1021. The capacitors 1005 and 1006 will charge exponentially, causing the junction of the resistor 1023 and the capacitors 1005 and 1006, at the point 1004, to change from a level of plus 3 volts to a level of minus 0.4 volt. This charging of the capacitors 1005 and 1006 takes 65 milliseconds. Charging of the capacitors causes the base of the transistor 963 to remain at a level of plus 0.2 volt for the additional 65 milliseconds. The holding in a non-conducting condition of the transistors 963 and 967 keeps the transistor 975 turned on for the 65-millisecond time interval.

At the conclusion of this period, the transistors 963 and 967 commence conducting and cut off the transistor 975. If, during the unstable state of the one-shot, another positive-going trigger signal is received at the input terminal 914, the time period of 65 milliseconds will restart. Such action occurs because the transistor 939 turns on again, holding the one-shot output true for the duration of the retrigger pulse signal. Since the transistor 989 is off during this period, the capacitors 1005 and 1006 recharge, and repeat their function when the transistor 939 turns off and the transistor 989 turns on again.

55-microsecond one-shot

Shown in FIG. 141 is another type of one-shot circuit which may be employed in the present invention. In the illustrated embodiment, this one-shot has a delay time of 55 microseconds. Also shown in FIG. 141 is a block depicting the manner in which this one-shot is represented in the logic block diagrams. As shown in FIG. 141, the circuit is provided with an input terminal 1035 and an output terminal 1036. The input terminal 1035 is connected over a 680-microfarad capacitor 1037, over a point 1038, a diode 1039, and a point 1040 to the base of a PNP-type transistor 1041. From the point 1038, a first circuit path extends over a 4700-ohm resistor 1042 to ground, and a second path extends over a 100,000-ohm resistor 1043 to a terminal 1044, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 1041 is connected to ground, and the collector of said transistor is connected to a point 1045, from which two branches extend. The first branch extends from the point 1045 over a parallel combination of a 240-microfarad capacitor 1046 and a 3900-ohm resistor 1047, and a point 1048 to the base of a PNP-type transistor 1049. A second path extends from the point 1045 over a point 1050, a parallel combination of a 330-microfarad capacitor 1051 and a 3900-ohm resistor 1052, and a point 1053, to the base of a PNP-type transistor 1054.

The emitter of the transistor 1049 is connected to ground, while the collector is connected over points 1055 and 1056 to the output terminal 1036. From the point 1055 a circuit branch extends over a 2000-ohm resistor 1057 to a terminal 1058, to which is applied a minus 20-volt D.C. source of potential. From the point 1056, a circuit branch extends over a diode 1059 to a terminal 1060, to which is applied a minus 8-volt D.C. source of potential.

From the previously-mentioned point 1053 in the base circuit of the transistor 1054, a path extends over a 33,000-ohm resistor 1061 and a point 1062 to a terminal 1063, to which is applied a plus 12-volt D.C. source of potential. The point 1062 is connected over a 33,000-ohm resistor 1064 to the previously-mentioned point 1048 in the base circuit of the transistor 1049.
The emitter of the transistor 1054 is connected to ground, while the collector of said transistor is connected over a point 1065 and a 1000-ohm resistor 1066 to a terminal 1067, to which is applied a minus 20-volt D.C. source of potential. The point 1065 is connected to a 0.022-microfarad capacitor 1068, a point 1069, and a 100-ohm resistor 1070 to the point 1040 in the base circuit of the transistor 1041.

From the point 1069, a further circuit path extends over a diode 1071, a 8-point 1072, a 3600-ohm resistor 1073, a point 1074, a point 1075, and a 1800-ohm resistor 1076 to a terminal 1077, to which is applied a minus 20-volt D.C. source of potential. The point 1075 is connected to the point 1065 over a diode 1078.

The point 1050 in the collector circuit of the transistor 1041 is connected over a point 1079 and a 1000-ohm resistor 1080 to a terminal 1081, to which is applied a minus 20-volt D.C. source of potential. From the point 1079, a circuit path also extends over a diode 1082, a point 1083 (which is connected to the point 1072), and a 22,000-ohm resistor 1084, to a point 1085, which is connected to the previously-mentioned point 1074. The point 1085 is connected over a point 1086 and a diode 1087 to the point 1079. From the point 1086 an additional path extends over a zener-type diode 1088 to ground.

Also shown in FIG. 141 is a block 1089, to which the input terminal 1035 and the output terminal 1036 are shown applied. This block represents the manner in which the one-shot circuit of FIG. 141 is represented in the logic block diagrams.

The operation of the one-shot shown in FIG. 141 will now be described. In the stable state of this device, the base of the transistor 1041 is at a minus 0.2-volt level, with said transistor being forward-biased. The transistors 1069 and 1054 are reverse-biased, with their bases at a level of plus 0.8 volt. The output signal level at the terminal 1036 is clamped to a minus 8-volt level by the diode 1059 conducting from the minus 8-volt supply at the terminal 1060 through the resistor 1057 to the minus 20-volt supply at the terminal 1058. The diode 1088 is an 8-volt zener-type diode, and current flows from ground through said diode and the resistor 1076 to the minus 20-volt supply at the terminal 1077. With the transistor 1041 conducting, current flows from ground, through the transistor 1041, emitter to collector, through the resistor 1080 to the minus 20-volt supply. The diode 1087 is reverse-biased.

The collector of the transistor 1041 is coupled to the base of the transistor 1054 through the capacitor 1051 and the resistor 1052, causing the base of the transistor 1054 to be at a level of plus 0.8 volt, which reverse-biases said transistor. Current flows from the minus 8-volt level at the point 1075 through the diode 1078 and the resistor 1066 to the minus 20-volt supply at the terminal 1067. The capacitor 1068 charges to a minus 8-volt potential. The potential at the junction of the resistor 1064, the resistor 1047, and the base of the transistor 1049 at the point 1048, is at plus 0.8 volt, which also reverse-biases the transistor 1049. The clamping diode 1059, in the collector circuit of the transistor 1049, is forward-biased and conducts from the minus 8-volt supply at the terminal 1060 through said diode and the resistor 1057 to the minus 20-volt supply. The output at the terminal 1036 is accordingly at a minus 8-volt signal level.

Now let it be assumed that the input at the terminal 1035 is switched to a zero-volt level. The capacitor 1037 and the resistor 1042 differentiate this signal into a positive-going spike. The plus 6-volt spike forward-biases the diode 1039, which causes the base of the transistor 1053 to be at a level of 8 volts, thereby reverse-biases said transistor and cutting it off, so that the collector circuit is no longer grounded. The diode 1087 is now forward-biased and will conduct from the minus 8-volt level at one side of the zener-type diode 1088 through the diode 1087 and the resistor 1080 to the minus 20-volt supply at the terminal 1081, causing the collector of the transistor 1041 to go to a minus 8-volt signal level. This negative-going change is blocked through the capacitor 1052 to the base of the transistor 1054. The potential on the base of the transistor 1054 now goes to minus 0.4 volt, forward-biases said transistor, the collector of which goes toward ground. This causes the capacitor 1068 to discharge through the diode 1071, and the parallel resistors 1084 and 1073. The capacitor 1068 takes 55 microseconds to discharge. This causes the base of the transistor 1041 to remain positive until the capacitor 1068 is discharged.

The negative-going signal on the collector of the transistor 1041 is coupled to the base of the transistor 1049, causing the potential on said base to go to a level of minus 0.4 volt. This causes the transistor 1049 to conduct, and the output at the terminal 1036 accordingly goes to zero volts. When the capacitor 1068 is discharged, the base of the transistor 1041 again goes negative, causing said transistor to commence conducting once more and to cut off conduction in the transistors 1049 and 1041, to the output terminal 1036. The output signal from the circuit of FIG. 141 is accordingly a pulse going from minus 8 volts to zero volts, remaining at a zero-volt level for 55 microseconds, and then returning to minus 8 volts.

500 and 1000 microsecond one-shots

Shown in FIG. 142 is a circuit for a one-shoe device which may be employed in the present invention, and two blocks representing the circuit, with different component values, to provide two different delay times, of 200 and 1000 microseconds, as depicted in the logic block diagrams. In the illustrated embodiment of the invention, the circuit of FIG. 142 is used for two different one-shots, one having a duration of 500 microseconds, and the other having a duration of 1000 microseconds. The 500-microsecond one-shot will be described herein, and it will be understood that the 1000-microsecond one-shot is the same as the 500-microsecond one-shot with the exception of the timing capacitors. The 500-microsecond one-shot uses a 0.22-microfarad capacitor, while the 1000-microsecond one-shot uses a 0.47-microfarad capacitor.

In FIG. 142, the circuit is shown as provided with an input terminal 1092 and an output terminal 1093. The input terminal 1092 is connected over a 680-microfarad capacitor 1094 to a point 1095, from which a plurality of circuit paths extend, a first such path extending over a 27,000-ohm resistor 1096 to a terminal 1097, to which is applied a source of minus 20-volt D.C. potential. A second path extends over a 4700-ohm resistor 1098 and points 1099, 1100, 1101, and 1102, and a 1800-ohm resistor 1103, to a terminal 1104, to which is applied a source of minus 20-volt D.C. potential. From the point 1099 a path extends over a zener diode 1105 to ground.

An additional path extends from the point 1095 over a diode 1106, a point 1107, a 0.22-microfarad capacitor 1108, and a point 1109 to the base of a PNP-type transistor 1110. The emitter of the transistor 1110 is connected to ground, while the collector of said transistor is connected over a point 1111, a point 1112, a point 1113, and a 1000-ohm resistor 1114 to a terminal 1115, to which is applied a minus 20-volt D.C. source of potential.

The point 1110 is connected to the point 1113 over a diode 1116. The point 1113 is also connected over a diode 1117, a point 1118, a 2400-ohm resistor 1119, and a variable 1000-ohm potentiometer 1120 to the point 1101. From the point 1111, an additional circuit path extends over a parallel combination of a 240-microfarad capacitor 1121 and a 4300-ohm resistor 1122, in series with a point 1123, to the base of a PNP-type transistor 1124. The emitter of the transistor 1124 is connected to ground, while the collector of said transistor is connected over points 1125 and 1126 to the output terminal 1093. From the point 1125, a path extends over a 2000-ohm resistor 1127 to a terminal 1128, to which is applied a minus
20-volt D.C. source of potential. From the point 1126, a path extends over a diode 1129 to a terminal 1130, to which is applied a minus 8-volt D.C. source of potential. From the point 1123 in the base circuit of the transistor 1124, the path extends over a 30,000-ohm resistor 1131 and a point 1132 to a terminal 1133, to which is applied a plus 12-volt D.C. source of potential. From the point 1112 in the collector of the transistor 1110, there extends a parallel path over a 330-microfarad capacitor 1134 and a 3900-ohm resistor 1135, and a point 1136 to the base of a PNP-type transistor 1137. The point 1136 is connected to the point 1132 over a 27,000-ohm resistor 1138.

The emitter of the transistor 1137 is connected to ground, while the collector is connected over a point 1139 and a 1100-ohm resistor 1140 to a terminal 1141, to which is applied a minus 20-volt D.C. source of potential. The point 1139 is connected over points 1142 and 1143 and a 220-ohm resistor 1144 to the base of a PNP-type transistor 1145.

The emitter of the transistor 1145 is connected over a point 1146 to the previously-mentioned point 1107. An additional path extends from the point 1142 over a diode 1147 to the point 1146. The collector of the transistor 1145 is connected over a point 1148 and a 560-ohm resistor 1149 to a point 1150, which is a minus 20-volt D.C. source of potential. From the point 1148, an additional path extends over a 100-ohm resistor 1151 and a diode 1152 to a terminal 1153, to which is applied a minus 8-volt D.C. source of potential.

In further reference to the circuit of FIG. 142, it may be noted that the point 1109 is connected to the point 1118 over a diode 1154, and that the point 1102 is connected to the point 1143 over a diode 1155.

Also shown in FIG. 142 is a block 1156 having the input terminal 1092 and the output terminal 1093 applied thereto, representing the manner in which the circuit of FIG. 142 is depicted in the logic block diagrams, when used in the form of a 500-microsecond one-shot. Similarly, the block 1157 with the input terminal 1092, and the output terminal 1093 affixed thereto, represents the manner in which the circuit of FIG. 142 is depicted in the logic block diagrams when used with a different capacitor as a 1000-microsecond one-shot.

The operation of the circuit of FIG. 142, when constructed to function as a 500-microsecond one-shot, will now be described. First, let it be assumed that the input at the terminal 1092 is at a signal level of minus 8 volts. The base of the transistor 1110 is then at minus 0.2 volts, and said transistor is conducting. The collector of the transistor 1110 is connected through the resistor 1135 and the capacitor 1134 to the base of the transistor 1137. The base potential of the transistor 1137 is plus one volt, which maintains said transistor in a reverse-biased condition. The collector of this transistor is then at minus 8 volts. The emitter and base of the transistor 1145 are at minus 8 volts potential, and that transistor is cut off. The collector of the transistor 1110 is also connected to the base of the transistor 1124, which is at a plus one volt signal level, and that transistor is cut off. The output at the terminal 1093 is accordingly clamped at a minus 8-volt signal level by the diode 1129.

Now let it be assumed that the input at the terminal 1092 changes from a minus 8-volt signal level to a zero-volt signal level. The transistor 1110 is reverse-biased and the transistor 1109 is cut off. The output of the capacitor 1109 differentiates the input signal, and the resulting 8-volt positive-going spike is applied to the base of the transistor 1110 through the capacitor 1108. This plus 8-volt spike reverse-biases the transistor 1110, and the collector thereof goes toward a potential of minus 8 volts. This negative-going change is coupled through the capacitor 1134 and the resistor 1135 to the base of the transistor 1137, causing said base to go to a signal level of minus 0.2 volt, which causes said transistor to commence conducting. The collector of the transistor 1137 then goes toward zero volts, which in turn causes the base of the transistor 1145 to go to plus 0.2 volt, thereby cutting off said transistor and causing the capacitor 1108 to commence charging.

Charging of the capacitor 1108 causes the base of the transistor 1110 to assume a plus 8-volt signal level, which then decays exponentially, holding said transistor cut off for a period of 500 microseconds. The capacitor 1108 charges mainly through the diode 1114, the resistor 1119, and the potentiometer 1120, to the minus 8-volt signal level from one side of the zener-type diode 1105. The RC time constant of the above-described network can be adjusted by changing the resistance of the potentiometer 1120 to obtain a 500-microsecond wave-form at the output terminal 1093. As the current for charging of the capacitor 1108 decays, the transistor 1110 again begins to conduct. During the time of 500 microseconds that the transistor 1110 was cut off, the base potential of the transistor 1124 was lowered to minus one volt. This causes the transistor 1124 to conduct, and the output terminal 1093 accordingly goes to a zero-volt signal level as a result of the conduction of the transistor 1124. This transistor remains in conduction until the transistor 1110 begins to conduct once again.

As the transistor 1110 commences conduction once again, the transistor 1110 is reverse-biased. The base of the transistor 1145 is now at a level of minus 8.2 volts, and the collector is at a potential near minus 0.2 volt due to the charge on the capacitor 1108. The transistor 1145 accordingly conducts and discharges the capacitor 1108. When the capacitor is discharged, the transistor 1145 is again cut off.

25 and 50 millisecond one-shots

Shown in FIG. 143 is a circuit for a one-shot device which may be employed in the present invention, and two blocks representing the circuit, with different component values, to provide two different delay times, as depicted in the logic block diagrams. In the illustrated embodiment, the circuit of FIG. 143 is used for two different one-shots, one having a duration of 25 milliseconds, and the other having a duration of 50 milliseconds. The circuits for these two one-shots are identical except for the amount of capacitance employed in the RC circuit which controls the length of the delay. Therefore only the 25-millisecond one-shot circuit will be described herein specifically, it being understood that the 50-millisecond one-shot is substantially identical.

As shown in FIG. 143, the circuit is provided with an input terminal 1162 and an output terminal 1163. The input terminal 1162 is connected over a 1000-microfarad capacitor 1164 to a point 1165. From this point a plurality of circuit paths extend, one of said paths extending over a diode 1166, a 1000-ohm resistor 1167, and points 1168, 1169, and 1170 to the base of a PNP-type transistor 171. From the point 1168, a path extends over a diode 1172 to ground, and from the point 1169, a path extends over a 240,000-ohm resistor 1173 to a terminal 1174, to which is applied a source of plus 12-volt D.C. potential.

From the point 1165, an additional path extends over a 16,000-ohm resistor 1175, points 1167, 1177, 1178, and 1179, and a 1800-ohm resistor 1180 to a terminal 1181, to which is applied a minus 20-volt D.C. source of potential. The point 1176 is connected to ground over a zener-type diode 1182 having an 8-volt potential difference thereacross.

A further path extends from the point 1165 over a 5100-ohm resistor 1183 and a point 1184 to a point 1185 on the collector circuit of the transistor 1171. From the point 1185, an additional path extends over a 2000-ohm resistor 1186 to a terminal 1187, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 1171 is connected over a point 1188 and a 100,000-ohm resistor 1189 to a ter-
minal 1190, to which is applied a plus 12-volt D.C. source of potential. The point 1188 in the emitter circuit of the transistor 1171 is connected to the base of an NPN-type transistor 1191, the emitter of which is connected to ground, and the collector of which is connected to the previously mentioned point 1184.

The collector circuit of the transistor 1171 is connected over a parallel combination of a 3900-ohm resistor 1192 and a 680-microfarad capacitor 1193 to a point 1194, which in turn is connected to the base of a PNP-type transistor 1195. The point 1194 is connected over a 43,000-ohm resistor 1196 to a terminal 1197, to which is applied a plus 12-volt D.C. source of potential.

The emitter of the transistor 1195 is connected to ground, while the collector of said transistor is connected over points 1198, 1199, and 1200 to the previously-mentioned output terminal 1163. From the point 1199, a path extends over a 1200-ohm resistor 1201 to a terminal 1202, to which is applied a minus 12-volt D.C. source of potential. The previously-mentioned point 1179 is connected over a diode 1203 to the point 1200.

From the point 1199 another path extends over a 1800-ohm resistor 1204 to the base of a PNP-type transistor 1205. The collector of said transistor is connected over a point 1206 and a 240-ohm resistor 1207 to a terminal 1208, to which is applied a minus 20-volt D.C. source of potential. The emitter of said transistor is connected over a point 1209 and parallel capacitors 1210 and 1211 of 0.47-microfarad capacitance each to a point 1212, which in turn is connected to the previously-described point 1170 over a diode 1213. The points 1198 and 1209 are connected over a diode 1214. A further path extends from the point 1206 over a 270-ohm resistor 1215, a point 1216 connected to ground, and a 12,000-ohm resistor 1217 to the point 1209. From the point 1212, an additional path extends over a 20,000-ohm resistor 1218, a point 1219, and a 30,100-ohm resistor 1220 to the point 1178. In parallel with the resistor 1220 between the points 1178 and 1121 is a 100,000-ohm variable resistor 1221.

Also included in FIG. 143 is a first block 1222, to which the input terminal 1162 and the output terminal 1163 are applied. This block represents the manner in which the 25-millisecond one-shot circuit of FIG. 143 is represented in the logic block diagrams. Similarly, a second block 1223 is included in FIG. 143 having the input terminal 1164 and the output terminal 1163 applied there to. This manner in which a 50-millisecond one-shot circuit is represented in the logic block diagrams.

The operation of the circuit of FIG. 143 will now be described. This one-shot is triggered by the rise of an input signal switching from a minus 8-volt level to a zero-volt level at the input terminal 1162. The output at the terminal 1163 will be at zero volts for 25 milliseconds following receipt of the input signal and will then return to its original level of minus 8 volts.

First let it be assumed that the signal level at the input terminal is at minus 8 volts. In this case, the base of the transistor 1171 is at a minus 0.8-volt level, forward-biasing said transistor. The emitter of the transistor 1171 begins to go negative due to the voltage drop across the resistor 1189. As the emitter of the transistor 1171 begins to go negative, the transistor 1191 becomes forward-biased in the collector circuit of the transistor 1171. In the collector circuit of the transistor 1171 a potential of minus 0.2 volt. The conduction of the transistors 1171 and 1191 maintains the base of the transistor 1195 at a level of plus one volt. This transistor is cut off, and the output terminal 1163 is clamped by the diode 1203 and the resistor 1201 at the reference voltage of minus 8 volts. The transistor 1205 has a minus 8-volt potential on its base and a minus 7.8-volt potential on its emitter and conducts. The timing capacitors 1210 and 1211 have minus one volt potential on the left side at the point 1212. The junction of the capacitor 1211, the capacitor 1210, and the resistor 1217 at point 1209 is at a potential level of minus 8.2 volts.

Let it now be assumed that the input signal at the terminal 1162 is switched to a zero-volt level. The capacitor 1216 and the diode 1217 differentiate the input signal and forward-bias the diode 1166 and the diode 1172. Conduction of these diodes causes the base of the transistor 1171 to go to a potential of plus 0.8 volt. This cuts off the conduction in the transistor 1171 and causes the transistor 1191 to start to cut off. The collectors of the transistors 1171 and 1191 begin to go negative. This negative-going change is coupled through the capacitor 1193 and the resistor 1192 to the base of the transistor 1195, causing the said base to go to a voltage level of minus 0.4 volt. The transistor 1195 is now forward-biased and conducting, and its collector accordingly goes toward a zero-volt potential level. This causes the output signal at the terminal 1163 to switch to a minus 8-volt level to a zero-volt level. The diode 1214 is now forward-biased, causing the point 1209 to be switched to zero volts. This positive-going voltage change causes the capacitors 1210 and 1211 to commence to charge. The potential of the point 1212 at this time is plus 7.5 volts, which decreases to a minus one-volt potential level as the capacitors 1210 and 1211 charge through the resistors 1218, 1220, and 1221. The capacitors 1210 and 1211 will take 25 milliseconds to charge, and during this charge time the base of the transistor 1171 is held at a level of plus 0.8 volt, which keeps said transistor from conducting. When the potential of the point 1212 reaches a minus one-volt level, the transistor 1171 commences conducting, which causes the transistor 1191 also to commence conducting and the transistor 1195 to be cut off. The potential at the output terminal 1163 has been zero volts for 25 milliseconds, and is now switched back to the minus 8-volt level. As the transistor 1195 is cut off, the clamping diode 1203 becomes forward-biased, and the diode 1214 is reverse-biased. The potential at the base of the transistor 1205 goes to a minus 8-volt level. This forward-biases the transistor 1205, and it conducts, rapidly discharging the capacitors 1210 and 1211 to minus 8 volts. The rapid discharge of the capacitors 1210 and 1211 by the transistor 1205 has now prepared the one-shot of FIG. 143 to operate once again.

Latch

A circuit for a latch which may be employed in the illustrated embodiment of the present invention is shown in FIG. 144, together with the block used to represent the latch in the logic diagrams. Generally speaking, the latch shown in FIG. 144 is a clocked latch consisting of an NPN-type transistor and a PNP-type transistor connected in a feed-back loop. The latch is a bistable device, in that both transistors are either conducting or cut off. The circuit has two outputs, one from the collector of each transistor. In the "reset" state, which is also known as the "closed" or "latched" state, the PNP-type transistor output is approximately minus eight volts, and the NPN-type transistor output is approximately zero volts. These outputs reverse in the "set" state of the latch, which is also known as the "open" or "unlatched" state. There is one set input to the latch which requires a negative signal for operation. To set the signal, the negative signal is applied to the reset input terminal of the latch. The "set" signal will operate the latch, irrespective of the clock signal. There are two "reset" signals for the latch, a positive-level signal and a negative-level signal. A signal of the indicated polarity, wider than the clock input, and coincident with the clock input signal, applied to either reset input terminal, will reset the latch.

Referring now to the circuit of FIG. 144, a set input terminal 1227 is provided, together with reset input terminals 1228 and 1229, and a clock input terminal 1230.
Let it now be assumed that the latch of FIG. 44 is in an off or reset state. A negative signal of minus 8 volts is applied at the terminal 1227. The base of the transistor 1240 then has a negative potential of about 0.2 volt, and that transistor accordingly conducts, causing its collector voltage to rise from the clamped minus 8-volt level to a zero level. The positive-going change on the collector of the transistor 1240 is coupled through the resistor 1249, the capacitor 1248, and the diode 1251 to the base of the transistor 1254, thereby forward-biasing that transistor and holding it in conduction. This causes the collector of the transistor 1254 to go to a minus 8-volt level. This negative-going change on the collector is coupled to the base of the transistor 1240 over the capacitor 1265 and the resistor 1256, and is effective to drive the transistor 1240 into saturation, which in turn causes the transistor 1254 to approach saturation. The diodes 1263 and 1251 in the base-collector circuit of the transistor 1254 keep that transistor from going into saturation, however. The latch of FIG. 144 will now remain set, regardless of the signal changes on the input terminal 1227. In this condition, the output at the terminal 1231 is at zero volts, and the output at the terminal 1232 is at minus 8 volts.

Now let it be assumed that the latch of FIG. 144 in the set state with input terminals 1227 and 1228 disconnected. Let it also be assumed that the input at the terminal 1228 is switched to minus 8 volts. Current flow from the plus 12-volt supply at the terminal 1282 through the resistor 1278 and the resistor 1277 causes the potential at the point 1270 at one side of the capacitor 1271 to drop to a minus 6.5-volt level. When the clock signal applied to the terminal 1230 goes to a true level of zero volts, the potential at the point 1272 at the other side of the capacitor 1271 will have a zero volt level, and the capacitor is accordingly charged to approximately six volts. At the fall of the clock signal on the terminal 1230 from the zero-volt level to the minus 8-volt level, the capacitor 1271 is charged to approximately 14 volts. The top plate of the capacitor 1271 at this time is at a minus 14-volt potential, forward-biasing the diode 1269 and causing the base of the transistor 1254 to go toward minus 14 volts. As this base goes more negative than the emitter, which is at minus 8 volts, the transistor 1254 begins to cut off, and its collector begins to go toward zero volts. This positive-going change on the collector of the transistor 1254 is coupled over the combination of the capacitor 1265 and the resistor 1266 to the base of the transistor 1240, and causes that transistor to begin to cut off, so that its collector begins to go toward a minus 8-volt signal level. The negative-going signal on the collector of the transistor 1240 in turn is coupled to the base of the transistor 1254, which further drives the transistor 1254 toward cut-off. This complementary action continues until both of the transistors 1240 and 1254 are cut off. The output signal at the terminal 1231 is now clamped at a minus 8-volt signal level, and the output voltage at the terminal 1232 is now clamped at a zero-volt level. In consequence, the latch is said to be in the reset state.

When the true-level reset trigger signal at the input terminal 1229 is used for resetting the latch, the terminal 1228 must be tied to a minus 8-volt supply. With minus 8 volts on the terminal 1229, the diode 1273 is reverse-biased, and the clock signal applied to the terminal 1230 cannot affect the latch. When the signal at terminal 1229 is switched to zero volt, the capacitor 1271 will charge to approximately six volts. The rise of the clock signal will not affect the latch, but as the clock falls, the latch will be reset in the manner described above.

**Blow-out circuit**

Shown in FIG. 145 is a circuit which may be used in the illustrated embodiment of the present invention for "blowing out" the solenoid driver and grounder circuits, together with a block depicting the manner in which this
circuit is represented in the logic block diagrams, particularly in FIG. 98.

The circuit of FIG. 145 includes an input terminal 1287 and output terminals 1288 to 1291 inclusive. A block 1292, showing the representation of this circuit in the logic block diagrams, is also provided with these terminals. The circuit and its operation are fully described in the copending United States patent application Ser No. 362,854, filed Apr. 27, 1964, inventors Lowery K. Jones and James D. Turner. Reference may be had thereto for a complete explanation of this circuit.

Sense circuit

Shown in FIG. 146 is a circuit which may be used in the illustrated embodiment of the present invention to detect the failure of a solenoid driver circuit to "blow out" within a prescribed time limit, together with a block depicting the manner in which this circuit is represented in the logic block diagrams, particularly in FIG. 98D. It will be recalled that an explanation has been previously made in the specification of the relays and other components associated with this sense circuit.

As shown in FIG. 146, four terminals, 1295 to 1298 inclusive, are provided for connecting this circuit to the remainder of the circuit (FIG. 98D). The terminal 1295 is connected over a zener-type diode 1299 and a 2000-ohm resistor 1300 to a point 1301. From the point 1301, a first branch extends over a diode 1302 to ground; a second branch extends over a 24,000-ohm resistor 1303 to a terminal 1304, to which is applied a source of minus 20-volt D.C. potential; and a third path extends to a point 1305. From the point 1305, a first path extends over a diode 1306 to a terminal 1307, to which is applied a minus 8-volt D.C. source of potential, and a second path extends over a diode 1308 to a point 1309. From the point 1309, a first path extends to the terminal 1297, and a second path extends over a 3900-ohm resistor 1310 and a point 1311 to the base of the PNP-type transistor 1312. From the point 1311, an additional path extends over a 33,000-ohm resistor 1313 to a terminal 1314, to which is applied a plus 12-volt source of D.C. potential.

The emitter 1316 of the transistor 1312 is connected to ground, while the collector of said transistor is connected over a point 1315, a 3900-ohm resistor 1316, and a point 1317 to the base of a PNP-type transistor 1318. From the point 1315, a first circuit extends over a 2200-ohm resistor 1319 to a terminal 1320, to which is applied a source of minus 20-volt D.C. potential, and a second path extends over a diode 1321 to a terminal 1322, to which is applied a minus 8-volt D.C. source of potential. From the point 1317, a path extends over a 33,000-ohm resistor 1323 to a terminal 1324, to which is applied a plus 12-volt D.C. source of potential.

The emitter of the transistor 1318 is connected to ground, while the collector of said transistor is connected over a point 1325, a diode 1326, a point 1327, a 1800-ohm resistor 1328, and a point 1329, to the base of a PNP-type transistor 1330. From the point 1325, a first path extends over a 2200-ohm resistor 1331 to a terminal 1332, to which is applied a minus 20-volt D.C. source of potential, while a second path extends from the point 1325 over a diode 1333 to a terminal 1334, to which is applied a minus 8-volt D.C. source of potential. From the point 1327, a first path extends over a 3900-ohm resistor 1335 to a terminal 1336, to which is applied a minus 8-volt D.C. source of potential, while a second path extends over a point 1337 and a diode 1338 to a terminal 1339, to which is applied a minus 8-volt D.C. source of potential. The previously-mentioned terminal 1296 is connected to the point 1337. From the point 1329, a path extends over a 15,000-ohm resistor 1340 to a terminal 1341, to which is applied a minus 12-volt D.C. source of potential.

The emitter of the previously-mentioned transistor 1330 is connected to ground, while the collector of said transistor is connected to the previously-mentioned terminal 1298.

Also shown in FIG. 146 is a block 1342, representing the manner in which the sense circuit is depicted in FIG. 98D. The terminals 1295 to 1298 inclusive are shown as applied to this block.

The operation of the sense circuit will now be described. As shown in FIGS. 146 and 98D, the input terminal 1295 receives the positive 50-volt pulses from the row select coil drivers; the input terminal 1296 is connected to the contacts PK205BC1 and PK401BC1, which have previously been described; the terminal 1297 is connected to the line which carries the signal DMO13; and the output terminal 1298 is connected to one side of the relay contacts PK301BC1.

Before any positive pulses are present on the input terminal 1295, current flow from the terminal 1307 over the diode 1306, and the resistor 1303 to the terminal 1304, which is at minus 20 volt level, is effective to clamp the cathode of the diode 1308 at a minus 8-volt level, which forward-biases this diode. Current flow in the base circuit of the transistor 1312 from plus 12 volts at the terminal 1314 over the resistors 1313, the resistor 1310, and the diode 1308 to the minus 8-volt clamp at the point 1305 causes the base of the transistor 1312 to go to a voltage level of minus 0.4 volt, thereby forward-biasing said transistor and causing it to conduct.

With the transistor 1312 conducting, current flow from ground at the emitter, through the collector resistor 1319 to the minus 20-volt terminal 1320, causes the collector to go to ground potential. Current flow from the plus 12-volt terminal 1324 through the resistors 1323 and 1316 to zero volts causes the base of the transistor 1318 to go to a plus 1.2 volt level, therefore reverse-biasing the transistor 1318 and preventing it from conducting. With the transistor 1318 turned off, current flow from the minus 8-volt terminal 1334 through the diode 1333 and the collector resistor 1331 to the minus 20-volt terminal 1332 clamps the collector of the transistor 1318 at a potential level of minus 8 volts and reverse-biases the diode 1326. Current flow from the plus 12-volt terminal 1341 through the resistors 1340, 1328, and 1335 to the minus 20-volt terminal 1336 causes the base of the transistor 1330 to go to a potential level of minus 0.4 volt, thereby forward-biasing said transistor.

With the transistor 1330 conducting, current flow from the ground connection at the emitter, through the transistor, and through the closed contacts PK301BC1 (FIG. 98D) in the collector circuit and over a serial combination of a 180-ohm resistor 1343 and a 180-ohm resistor 1344 to a terminal 1345, to which is connected a minus 20-volt D.C. source of potential, causes the collector of the transistor 1330 to go to a ground potential. The relay PK301 (FIG. 98D) now has ground potential on both of its coil terminals, and is therefore maintained in a relaxed or deenergized condition.

When a positive 50-volt pulse from a coil driver silicon controlled rectifier is present at the terminal 1295, current flows through the zener-type diode 1299, the resistor 1300, and the diode 1302 to ground, which clamps the cathode of the diode 1308 at ground potential.

The signal DMO13 applied to the terminal 1297 is false at this time, and therefore current flow from the plus 12-volt terminal 1314 through the resistor 1313 and the resistor 1310 to a minus 8-volt level at the terminal 1297 maintains the base of the transistor 1312 at a minus 0.4-volt level, holding that transistor in a conducting condition.

Under normal conditions, the silicon controlled rectifiers are "blown out" before the signal DMO13 goes true. When the plus 50 volt signal level is removed from the input terminal 1295, the minus 8-volt clamp is again in effect at the cathode of the diode 1308, thus producing the previously mentioned path from the plus 12 volt terminal 1314 to the minus 8-volt terminal 1307. In such a case,
the base of the transistor 1312 is maintained at a minus 0.4-volt level when the signal DMO13 goes true and presents a ground potential to the 1297.

Should one of the cell driver silicon controlled rectifiers fail to "blow out," a plus 50-volt signal level will still be present at the input terminal 1295 at the time that the signal DMO13 goes true and applies a zero-volt signal level to the terminal 1296. With the signal DMO13 true, the transistor 1308 is also at zero volt potential. Therefore, current flow from the plus 12-volt terminal 1314 through the resistors 1313 and 1310 to zero volt causes the base of the transistor 1312 to go more positive than ground, thereby reverse-biasing said transistor and turning it off. In such a case, current flows from the minus 8-volt supply 1322 through the clamping diode 1321 to the minus 20-volt terminal 1320 via the resistor 1319, thereby clamping the collector potential of the transistor 1312, at point 1315, at a minus 8-volt signal level.

Current flow from the plus 12-volt terminal 1324 through the resistors 1323 and 1316 to the minus 8-volt terminal 1322 causes the base of the transistor 1318 to go to minus 0.4 volt, thereby causing the transistor 1318 to commence conducting. Current then flows from ground at the emitter of said transistor through the resistor 1331 to the terminal 1332, to which is applied a minus 20-volt B. C. source of potential, as previously mentioned, thereby causing the collector of the transistor 1318 to go to a zero-volt potential. The diode 1326 in such a case is forward-biased, causing current flow from zero volt at the diode 1326 to minus 20 volts at the terminal 1336, via the resistor 1335. Current flow from the plus 12-volt terminal 1341 via the resistors 1340 and 1328 to zero volt causes the base of the transistor 1330 to go positive with respect to ground. As a consequence, the transistor 1330 stops conducting, which removes the collector of said transistor from a ground potential level. With ground removed from this side of the relay PK301 (FIG. 98D), current flows from ground at one side of the contacts PK303A3 (FIG. 98D), which contacts are closed at this time, through the relay PK301 to the minus 20-volt terminal 1345 via the resistors 1343 and 1344, thereby causing the relay PK301 to energize, opening the contacts PK301B1 (FIG. 98D). Opening of these contacts isolates the relay PK301 from the transistor 1330, so that said relay will not be deenergized when the transistor 1330 commences conducting once more.

As previously described, the contacts PK301B2C (FIG. 97) now open in the energizing circuit for the relay PK202, deenergizing said relay, which results in down-sequencing of the power supply.

Solenoid driver circuit

Shown in FIG. 147 is a circuit which may be used in the illustrated embodiment of the present invention for driving the solenoids of the solenoid keyboard matrix of the window machine, together with a block depicting the manner in which this circuit is represented in the logic block diagrams, particularly Figs. 98, 98A, 98B, 98C, and 98E.

The circuit of FIG. 147 includes an input terminal 1349 and output terminals 1350 and 1351. A block 1352, showing the representation of this circuit in the logic block diagrams, is also provided with these terminals. This circuit and its operation are fully described in the co-pending United States patent application Ser. No. 362, 854, filed Apr. 27, 1964, inventors Lowery K. Jones and James D. Turner. Reference may be had thereto for a complete explanation of this circuit.

OR diodes

Shown in FIGS. 148 and 149 are partial circuits including multiple and single diodes which are used in the illustrated embodiment of the present invention, together with blocks which depict the manner in which these diodes are represented in the logic block diagrams. The separate diodes are provided for flexibility in assembling circuits having a number of input connections. The diodes in FIG. 148 are called OR diodes because their cathodes are connected together in the same manner as diodes are connected in OR circuits, while the diode of FIG. 149 is also called an OR diode for convenience because it is shown as oriented in the same direction as the diodes of FIG. 148.

The partial circuit of FIG. 148 includes two input terminals 1356 and 1357, together with an output terminal 1358. The terminals 1356 and 1357 are connected over diodes 1359 and 1360 to a common point 1361, to which the terminal 1358 is also connected. A block 1362, representing this partial circuit, also has the terminals 1356 to 1358 inclusive applied thereto.

Similarly, the partial circuit of FIG. 149 includes an input terminal 1363 and an output terminal 1364 connected by a diode 1365. A block 1366, representing this partial circuit, also has the terminals 1363 and 1364 applied thereto.

AND resistors

Shown in FIG. 150 is a partial circuit including a resistor connected to a terminal at either end, which is used in the illustrated embodiment of the present invention, together with a block depicting the manner in which this resistor is represented in the logic block diagrams. This resistor is called an AND resistor because it is of the same resistance (namely, 24,000 ohms) which is used in AND circuits in the present invention, and because one end of the said resistor is adapted to be connected over its terminal to a source of plus 12-volt D.C. potential.

The circuit of FIG. 150 includes a 24,000-ohm resistor 1369, which is connected at one end to a terminal 1370 and at the other end to a terminal 1371. Conventionally, a source of 12-volt D.C. potential will be applied to one of these terminals; namely, terminal 1371 in the illustrated embodiment. A block 1372, representing this partial circuit, as it appears in the logical block diagrams, also has the terminal 1370 applied thereto. The terminal 1371 is not shown in connection with the block 1372, because it represents a power terminal in the illustrated embodiment.

OR resistors

Shown in FIGS. 151 and 152 are two versions of partial circuits including resistors, which are used in the illustrated embodiment of the present invention, together with blocks depicting the manner in which these partial circuits are represented in the logic block diagrams. The separate resistors are provided for flexibility in assembling various types of circuits. The resistor of FIG. 151 is called an OR resistor (having a symbol designation of RO) because of its 3000-ohm resistance which is used in OR circuits, and because one of its terminals is connected to a minus 20-volt D.C. power supply. The resistor of FIG. 152 is also called an OR resistor (having a symbol designation of 2RO) because it has a resistance of 1500 ohms and because one of its terminals is connected to the minus 20-volt D.C. power supply.

The partial circuit of FIG. 151 includes a 3000-ohm resistor 1373, an input terminal 1374 connected to one end thereof, and a terminal 1375 connected to the other end of said resistor. A source of minus 20-volt D.C. potential may be applied to the terminal 1375. A block 1376, representing the partial circuit including the resistor 1373, is also shown in FIG. 151 and has the terminal 1374 applied thereto.

In FIG. 152, a 1500-ohm resistor 1377 has an input terminal 1378 applied to one end thereof, and a terminal 1379 applied to the other end thereof. A source of minus 20-volt D.C. potential may be applied to the terminal 1379. A block 1380, representing this partial circuit, also has the terminal 1378 applied thereto.
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Latch

Shown in FIG. 153 is a circuit which may be used in a testing device, termed a data sub-set simulator, incorporated in the illustrated embodiment of the present invention, together with a block depicting the manner in which this circuit is represented in the logic block diagrams, specifically in FIG. 103.

The circuit of FIG. 153 includes two input terminals 1384, 1385, and an output terminal 1386. As shown in FIG. 103, the input terminals 1384 and 1385 are connected to two contact positions of the manual clock switch 5901A, while the output terminal 1386 provides a signal reflecting the condition of that switch.

The terminal 1384 is connected over a point 1387, a parallel combination of a 240-microfarad capacitor 1388 and a 2200-ohm resistor 1389, and a point 1390, to the base of an NPN-type transistor 1391. From the point 1390, an additional circuit path extends over a 33,000-ohm resistor 1392 to a terminal 1393, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 1391 is connected to a terminal 1394, to which is applied a minus 5-volt D.C. source of potential. The collector of said transistor is connected over points 1395, 1396, and 1397 to the output terminal 1386. From the point 1395, an additional circuit branch extends over a 500-ohm resistor 1398 to a terminal 1399, to which is applied a plus 12-volt D.C. source of potential. From the point 1396, an additional circuit branch extends over a diode 1400 to a terminal 1401, to which is applied a plus 5-volt D.C. source of potential.

From the input terminal 1385, a circuit path extends over a point 1402, a parallel combination of a 240-microfarad capacitor 1403 and a 2200-ohm resistor 1404, and a point 1405, to the base of an NPN-type transistor 1406. The point 1402 is connected to the point 1397 in the collector circuit of the transistor 1391. The point 1405 is connected over a 33,000-ohm resistor 1407 to a terminal 1408, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 1406 is connected to a terminal 1409, to which is applied a minus 5-volt D.C. source of potential. The collector of said transistor is connected over points 1410 and 1411 to the point 1387, which, it will be recalled, is also connected to the input terminal 1384. From the point 1406, an additional circuit path extends over a 600-ohm resistor 1412 to a terminal 1413, to which is applied a plus 12-volt D.C. source of potential. From the point 1411, an additional circuit path extends over a diode 1414 to a terminal 1415, to which is applied a plus 5-volt D.C. source of potential.

Also included in FIG. 153 is a block 1416, depicting the manner in which the circuit of FIG. 153 is shown in the logic block diagram of FIG. 103. The input terminals 1384, 1385, and the output terminal 1386, are applied to the block 1416.

Operation of the latch circuit of FIG. 153 will now be described. Essentially this latch consists of two NPN inverters connected to a cross-coupled configuration, with the inputs to the inverter circuits coming from the manual clock switch 5901A. The latch is used to provide absolute switching when the stable states at the input terminals 1384 and 1385 are switched from one level to the other by manual depression of said switch. The function of the latch circuit of FIG. 153 is to prevent possible contact bounce of the switch contacts from affecting the circuits which are connected to the output terminal 1386 of the circuit of FIG. 153. It will be seen that at any given time, with the switch in either of its stable states, one of the transistors 1391 or 1406 will be conducting, while the other will be cut off. Changing the condition of the switch, as by depressing the switch, or by releasing it if already depressed, causes that transistor which is conducting to be cut off, while the transistor which has been cut off is rendered conducting. It will be seen from the circuit that when either of the two transistors 1391 or 1406 is rendered conducting, the cross-coupling effect causes the other transistor to be driven to a cut-off condition. If the latch of FIG. 153 were not used in conjunction with the switch 5901A, possible contact bounce as a switch is operated might result in multiple clock pulses which would provide undesired results.

Minus five-volt supply

Shown in FIG. 154 is a power supply circuit which may be used in the data sub-set simulator mentioned in connection with FIG. 153, incorporated in the illustrated embodiment of the present invention. Also included in FIG. 153 is a block depicting the manner in which this power supply circuit is represented in the logic block diagrams, specifically FIG. 103. The circuit of FIG. 154 includes a terminal 1420, to which a minus 8-volt source of potential is applied, and a terminal 1421, from which the desired supply of approximately minus 5 volts D.C. potential may be taken. The terminal 1420 is connected over a point 1422, an 82-ohm resistor 1423, and a point 1424 to the base of a PNP-type transistor 1425. The point 1424 is connected over a zener-type diode 1426 to the ground. The point 1422 is connected over a 16-ohm resistor 1427 to the collector of the transistor 1425.

The emitter of said transistor is connected over a point 1428 to the output terminal 1421, from which the supply potential of approximately minus five volts D.C. is taken. From the point 1428, an additional circuit path extends over a parallel combination of a 0.68-microfarad capacitor 1429 and a 30-ohm resistor 1430 to ground.

A block 1431 is also included in FIG. 154 and represents the manner in which the circuit of FIG. 154 is depicted in the logic block diagram of FIG. 103.

Operation of the circuit of FIG. 154 will now be briefly described. With the power on, current will flow from ground through the resistor 1423 and the diode 1426 to the minus 8-volt supply at terminal 1420. The transistor 1425 is forward-biased, and current accordingly flows from ground through the resistor 1430, the transistor 1425, and the resistor 1427 to the minus 8-volt supply. The output of this supply circuit is actually about minus 4.2 volts. The capacitor 1429 serves as a filter capacitor.

Plus five-volt supply

Shown in FIG. 155 is a circuit which may be used in the data sub-set simulator, mentioned in the description of FIG. 153 above, incorporated in the illustrated embodiment of the present invention. Also included in FIG. 155 is a block depicting the manner in which this power supply circuit is represented in the logic block diagrams, specifically FIG. 103. The circuit of FIG. 155 includes a first terminal 1434, which is connected to a source of plus 12-volt D.C. potential, in order to enable the desired power supply to be delivered by this circuit. The desired power supply is delivered from a second terminal 1435. The terminal 1434 is connected over a point 1436, a 270-ohm resistor 1437, and a point 1438 to the base of a PNP-type transistor 1439.

The collector of said transistor is connected over a 12-ohm resistor 1440 to ground, while the emitter of said transistor is connected over points 1441 and 1442, and a 5-microfarad capacitor 1443, to ground. The point 1438 in the base circuit of the transistor 1439 is connected over a zener-type diode 1444 to ground. A first path extends from the point 1436 over a 40-ohm resistor 1445 to the point 1441 in the emitter circuit of the transistor 1439, while a second path extends from the point 1436 over a 120-ohm resistor 1446 to the point 1442 in the emitter circuit of the transistor 1439.

A block 1447 is also included in FIG. 155, representing the manner in which plus 5-volt power supply circuit is shown in FIG. 103, and the terminal 1435, from which
the plus 5-volt supply is delivered, is applied to the block 1447.

Operation of the plus 5-volt supply circuit will now be
described. With the power to the system on, current flows
from the plus 12-volt supply at the terminal 1434 through the
resistor 1437 and the zener-type diode 1444 to ground. The
transistor 1439 is forward-biased and will conduct current
from the plus 12-volt supply through the parallel resistors 1445 and 1446, through the transistor 1439, and
through the resistor 1440 to ground. The output of this
supply circuit is actually about plus 4.6 volts. The capaci-
tor 1443 performs a filtering function in the circuit.

**Power source**

Shown in FIG. 156 is a partial circuit which serves a
power transmission function, used in the data sub-set
simulator incorporated in the illustrated embodiment of
the present invention, together with a block depicting the
manner in which this partial circuit is represented in the
logic block diagrams, specifically FIG. 103.

Actually the partial circuit of FIG. 156 simply repre-

sents a convenient means by which potential is applied
at a central point for distribution therefrom to a number
of points in various circuits, all of which require specific
potential levels. For example, in FIG. 156, the terminal
1450 is connected to a central source of plus 12-volt D.C. potential, and this terminal is in turn connected to a
terminal 1453, which is connected to all of the termi-

nals in the associated circuitry which require a source
of plus 12-volt D.C. potential. In a similar manner, the
terminal 1454 is connected to ground, so that a ground
connection may be supplied where needed by connection
to the terminal 1454. In a similar manner, the terminal
1451 is connected to a source of minus 8-volt D.C.

potential and to a terminal 1455, from which connections
may be made to other portions of the circuitry which
require a minus 8-volt potential. It will be noted that a 40-

microfarad capacitor 1457 is connected between the ter-

minals 1454 and 1455 for power supply filtering purposes.
A terminal 1452, to which a source of minus 20-volt D.C.
potential is applied, is connected to a terminal 1456, from
which minus 20-volt D.C. potential may be supplied to
other portions of the circuitry where needed.

Also included in FIG. 156 is a block 1458, represen-
ting the power source partial circuit, with terminals 1453
to 1456 applied thereto, representing the potential source
which may be connected to other portions of the data
sub-set simulator circuitry where required.

**Data sub-set simulator circuit**

Shown in FIG. 157 is a circuit which includes a num-
er of interconnected logical components used in the
data sub-set simulator. Also shown in FIG. 157 is a block

diagram depicting the manner in which this circuit is
represented in the logic block diagrams, specifically FIG. 103.

As may be noted from the block diagram of FIG. 157,
the circuit includes a "data sub-set to branch" level con-
verter, a logic inverter, an AND inverter, a one-kilocycle
multivibrator, and two "branch to data sub-set" level con-
verters. In operation, a one-kilocycle square wave from the
multivibrator is converted to the desired signal level and
used to provide an output signal in one instance, and is
ANDed with the input to the AND inverter from the logic
inverter to produce an output signal of square wave
configuration for the other output.

Three input terminals 1462, 1463, and 1464 are pro-
vided for the circuit, as are two output terminals 1465 and
1466. The output signal of the circuit over a point 1467, a parallel combination of a 1600-ohm resistor 1468
and a 240-microfarad capacitor 1469, and a point 1470, to the base of a PNP-type transistor 1471.

The emitter of the transistor 1471 is connected to
ground, while the collector of said transistor is connected
over a point 1472, a parallel combination of a 3900-

ohm resistor 1473 and a 240-microfarad capacitor
1474, and a point 1475, to the base of a PNP-type tran-

sistor 1476.

From the point 1467, a circuit path extends over a 5100-

ohm resistor 1477 to ground, and from the point 1470,

an additional path extends over a 33,000-ohm resistor
1478 to a terminal 1479, to which is applied a plus 12-

volt D.C. source of potential. From the point 1472, an

additional circuit path extends over a 2200-ohm resistor
1480 to a terminal 1481, to which is applied a minus 20-

volt D.C. source of potential. From the point 1472, an

additional circuit path extends over a diode 1482 to a

terminal 1483, to which is applied a minus 8-volt D.C.

source of potential. From the point 1475, an additional

circuit path extends over a 2200-ohm resistor 1484 to a

terminal 1485, to which is applied a plus 12-volt D.C.

source of potential.

The emitter of the transistor 1476 is connected
to ground, while the collector of said transistor is connected
over a point 1486, a point 1487, a diode 1488, a point
1489, a parallel combination of a 330-microfarad capa-

citor 1490 and a 1800-ohm resistor 1491, and a point
1492, to the base of a PNP-type transistor 1493. From

the point 1486, an additional circuit path extends over a

2200-ohm resistor 1494 to a terminal 1495, to which is

applied a minus 20-volt D.C. source of potential. From

the point 1487, an additional path extends over a diode

1496 to a terminal 1497, to which is applied a minus 8-

volt D.C. source of potential. From the point 1489, an

additional circuit path extends over a 24,000-ohm resis-

tor 1498 to a terminal 1499, to which is applied a plus 12-

volt D.C. source of potential. An additional path extends

from the point 1497 to the one-kilocycle multivibrator

mentioned above, and this path will again be referred to

subsequently. From the point 1492, an additional path
extends over a 16,000-ohm resistor 1500 to a terminal
1501, to which is applied a plus 12-volt D.C. source of

potential.

The emitter of the transistor 1493 is connected
to ground, while the base of said transistor is connected
over a point 1502, a point 1503, a parallel combination of a

240-microfarad capacitor 1504 and a 2200-ohm resis-
tor 1505, and a point 1506 to the base of an NPN-
type transistor 1507. From the point 1502, an additional
circuit path extends over a 2200-ohm resistor 1508 to a

terminal 1509, to which is applied a minus 20-volt D.C.

source of potential. From the point 1503, an additional
circuit path extends over a diode 1510 to a terminal
1511, to which is applied a minus 8-volt D.C. source of

potential. From the point 1506, an additional circuit path
extends over a 33,000-ohm resistor 1512 to a terminal
1513, to which is applied a minus 20-volt D.C. source of

potential.

The emitter of the transistor 1507 is connected to

a terminal 1514, to which is applied a minus 5-volt D.C.

source of potential, and the collector of said transistor

is connected over points 1515 and 1516 to the output

terminal 1465. From the point 1515, an additional circuit
path extends over a 600-ohm resistor 1517 to a terminal
1518, to which is applied a plus 12-volt D.C. source of

potential. From the point 1516 an additional circuit path
extends over a diode 1519 to a terminal 1520, to which

is applied a source of plus 5-volt D.C. potential.

As previously mentioned, an additional circuit path
extends from the point 1589 to the multivibrator circuit
included in FIG. 157. This path extends over a diode
1524 and points 1525, 1526, and 1527 to the collector
of a PNP-type transistor 1528.

A path also extends from the point 1527 over a pair
of parallel capacitors 1529 and 1530, the capacitor 1529
being of 0.082-microfarad capacitance, and the capacitor
1530 being of 0.0047-microfarad capacitance, and over a
point 1531 to the base of a PNP-type transistor 1532,

which is cross-coupled with the transistor 1589.

The emitters of both of the transistors 1528 and 1532
are connected to ground. The base of the transistor 1528
1532.
is connected over a point 1533 and parallel capacitors 1534 and 1535, of 0.082-microfarad capacitance and 0.0047-microfarad capacitance, respectively, and over points 1536 and 1537 to collector of the transistor 1532.

From the point 1525, an additional circuit path extends over a point 1538, a diode 1539, a point 1540, a point 1541, a point 1542, a diode 1543, a point 1544, and a point 1545 to the previously-mentioned point 1537. From the point 1538, an additional circuit path extends over a 1000-ohm resistor 1546 to a terminal 1547, to which is applied a minus 20-volt D.C. source of potential. From the point 1541, a first circuit path extends over a zener-type diode 1548 to ground, and a second path extends over a 1800-ohm resistor 1549 to a terminal 1550, to which is applied a minus 20-volt D.C. source of potential. From the point 1544 an additional circuit path extends over a 1000-ohm resistor 1551 to a terminal 1552, to which is applied a minus 20-volt D.C. source of potential. From the point 1540, an additional circuit path extends over an 8200-ohm resistor 1553, a point 1554, and a diode 1555 to the previously-mentioned point 1533 in the base circuit of the transistor 1528. A diode 1556 is connected between the points 1526 and 1555.

As previously mentioned, from the multivibrator circuit a path extends over the level converter circuit to the output terminal 1466. In FIG. 157, this path extends from the point 1536 over a parallel combination of a 240-microfarad capacitance 1561 and a 2200-ohm resistor 1562, and over a point 1563, to the base of an npn-type transistor 1564. From the point 1563, an additional circuit path extends over a 33,000-ohm resistor 1565 to a terminal 1566, to which is applied a minus 20-volt D.C. source of potential.

The emitter of the transistor 1564 is connected to a terminal 1567, to which is applied a minus 5-volt D.C. source of potential, and the collector of said transistor is connected over points 1568 and 1569 to the input terminal 1466. From the point 1568, an additional circuit path extends over a 600-ohm resistor 1570 to a terminal 1571, to which is applied a plus 12-volt D.C. source of potential, and from the point 1569, an additional circuit path extends over a diode 1572 to a terminal 1573, to which is applied a plus 5-volt D.C. source of potential.

Also included in FIG. 157 is the block representation of the circuit, to which the input terminals 1462, 1463, and 1464 are applied as well as the output terminals 1465 and 1466. The block representation includes a block 1577 representing a "data-used-set-branch" level converter, a block 1578 representing a logic inverter, a block 1579 representing an AND inverter, a block 1580 representing a one-kilocycle multivibrator, and blocks 1581 and 1582 representing two "branch to data sub-set" level converters. The various blocks are interconnected in a manner corresponding to the showing in the circuit, and this corresponding configuration is found in FIG. 103 of the logic block diagrams.

With reference to the operation of the circuit shown in FIG. 157, it may be noted that the various blocks, such as the level converters and the inverters, function in the manner previously explained in the description of these blocks elsewhere in this specification. With respect to the multivibrator 1580, it may be noted that the circuit for this multivibrator is symmetrical in design, and the multivibrator is of the free-running type. No trigger input pulse is required to start the circuit operation, which commences as soon as power is applied. This results from tolerance and variation in the physical construction of the components, so that one of the two transistors 1528 and 1532 begins to conduct faster or harder than the other.

A minus 8-volt reference is developed when current flows from ground through the 8-volt zener-type diode 1548 and the resistor 1549 to the minus 20-volt terminal 1550. Let it be assumed that the transistor 1532 is conducting and the transistor 1528 is cut off. In this case, the collector of the transistor 1532 will go to ground potential. This positive-going 8-volt change causes the capacitors 1534 and 1535 to discharge exponentially through the diode 1555 and the resistor 1553 to the minus 8-volt reference. This in turn causes the base of the transistor 1528 to remain positive. The diode 1539 is forward-biased, and the capacitors 1529 and 1530 will charge. When the capacitors 1534 and 1535 are discharged, the diode 1555 becomes reverse-biased, and the base of the transistor 1528 will begin to go to a negative potential, which forward-biases said transistor into a conducting state. The positive-going 8-volt change causes the capacitors 1529 and 1530 to discharge and cut off the transistor 1532. When the capacitors 1529 and 1530 are discharged, the transistor 1532 again begins conducting, cutting off the transistor 1528.

The discharge time of the capacitors determines the frequency of the output that is taken from the collector of the transistors 1528 and 1532. These outputs are in the form of an 8-volt square wave, changing at the rate of 1000 cycles per second. The output of the transistor 1532 is used as an input to the level converter 1582 to provide a desired signal on the output terminal 1466, while the output of the transistor 1528 is used as one input to the AND inverter circuit 1579, the output of which is converted by the level converter 1581 to provide the desired signal at the output terminal 1465.

**Indicator lamps**

Shown in FIG. 158 is a circuit for indicator lamps used in the illustrated embodiment of the present invention, together with a block representation of the manner in which the indicator lamp circuitry is represented in the logic block diagrams.

In the system, a visual indication of the state of certain logic propositions is accomplished through use of indicator tubes, which may be of the type 6977 indicator diode tube. As shown in FIG. 158, the tubes 1586 are connected in two rows of twelve tubes each. A one-volt a.c. source of potential is provided at terminals 1587 and 1588 for the filaments of the tubes, and a plus 50-volt supply is connected at the plates of the tubes. The control signal for each tube is provided at the grid from a terminals such as 1590 over a 100,000-ohm resistor 1591. With a minus 8-volt false signal level at the input grid resistor of the tube, indicator tube conduction is cut off, and no illumination is present. Switching the input grid to a zero-volt true signal level allows the tube to conduct.

The block 1592 to which the various input terminals 1590 are applied represents the manner in which this circuit is depicted in the logic block diagrams.

While the form of the embodiment shown and described herein is admirably adapted to fulfill the objects primarily stated, it is to be understood that it is not intended to confine the invention to the one form or embodiment disclosed herein, for it is susceptible of embodiment in various other forms.

**What is claimed:**

1. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising (a) a plurality of multiple-row keyboard-operated input-output devices capable of having the keyboard set either remotely in response to electrical signals applied thereto or manually;
information transmitting means for transmitting input and output messages in serial form between the central data processing station and a selected input-output device;
scan counter means for sequentially scanning all of the input-output devices in a branch and operable to select a given input-output device by halting in the event that said given input-output device is conditioned to transmit an input message to the central data processing station, to enable communication to take place between the given input-output device and the central data processing station;
output select means for selecting one of the input-output devices of the branch in accordance with the information contained in an output message; gating means associated with each input-output device and operable to cause a selected input-output device to be coupled to the central data processing station over the information transmitting means for transmission of input and output information therebetween;
multiple-row storage means associated with each input-output device for storage of information manually input into a selected input-output device by means of its keyboard;
input row counter means for controlling the sequential read-out of information from the storage means of a selected input-output device to cause this information to be transmitted to the central data processing station via the information transmitting means; input program counter means for controlling the operation of the input row counter means during an input operation in which information is transmitted to the central data processing station from the selected input-output device;
output data register means operable to determine the digital values of keys to be set in a selected input-output device in accordance with information transmitted from the central data processing station by means of an output message;
output row counter means cooperating with the output data register means and operable to control the row-by-row sequence of setting of the keys of a selected input-output device to cause said keys to be set in accordance with information contained in an output message; and
output program counter means for controlling the operation of the output row counter means during an output operation in which information is transmitted to the selected input-output device from the central data processing station.

2. The combination of claim 1, also including checking means for the correctness of information contained in input and output messages transmitted by the information transmitting means.

3. The combination of claim 1, also including checking means for the correctness of information contained in input and output messages transmitted by the information transmitting means.

4. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising a plurality of multiple-row keyboard-operated input-output devices capable of having the keyboard set either remotely in response to electrical signals applied thereto or manually;
information transmitting means for transmitting input and output messages in serial form between the central data processing station and a selected input-output device;
scan counter means for sequentially scanning all of the input-output devices in a branch and operable to select a given input-output device by halting in the event that said given input-output device is conditioned to transmit an input message to the central data processing station, to enable communication to take place between the given input-output device and the central data processing station;
input operating means operable to cause information entered manually into a selected input-output device to be transmitted to the central data processing station via the information transmitting means during an input operation in which information is transmitted to the central data processing station from the selected input-output device;
output data register means operable to determine the digital values of keys to be set in a selected input-output device in accordance with information transmitted from the central data processing station by means of an output message;
output row counter means cooperating with the output data register means and operable to control the row-by-row sequence of setting of the keys of a selected input-output device to cause said keys to be set in accordance with information contained in an output message; and
output program counter means for controlling the operation of the output row counter means during an output operation in which information is transmitted to the selected input-output device from the central data processing station.

6. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising
a plurality of multiple-row keyboard-operated input-output devices capable of having a keyboard set either remotely in response to electrical signals applied thereto or manually;
information transmitting means for transmitting input and output messages in serial form between the central data processing station and a selected input-output device;
scan counter means for sequentially scanning all of the input-output devices in a branch and operable to select a given input-output device by halting the event that said given input-output device is conditioned to transmit an input message to the central data processing station, to enable communication to take place between the given input-output device and the central data processing station;
output select means for selecting one of the input-output devices of the branch in accordance with the information contained in an output message;
gating means associated with each input-output device and operable to cause a selected input-output device to be coupled to the central data processing station over the information transmitting means for transmission of input and output information therebetween;
input operating means operable to cause information entered manually into a selected input-output device to be transmitted to the central data processing station via the information transmitting means during an input operation in which information is transmitted to the central data processing station from the selected input-output device and output operating means operable in accordance with information transmitted from the central data processing station via the information transmitting means for remotely setting a selected input-output device during an output operation in which information is transmitted to the selected input-output device from the central data processing station.

8. The combination of claim 7, also including input error means for the detection and indication of input message errors.

9. The combination of claim 7, also including output error means for the detection and indication of output message errors.

10. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising
a plurality of multiple-row keyboard-operated input-output devices capable of having a keyboard set either remotely in response to electrical signals applied thereto or manually;
information transmitting means for transmitting input and output messages in serial form between the central data processing station and a selected input-output device;
scan counter means for sequentially scanning all of the input-output devices in a branch and operable to select a given input-output device by halting in the event that said given input-output device is conditioned to transmit an input message to the central data processing station, to enable communication to take place between the given input-output device and the central data processing station;
gating means associated with each input-output device and operable to cause an input-output device selected by the scan counter to be coupled to the central data processing station over the information transmitting means for transmission of an input message thereto; multiple-row storage means associated with each input-output device for storage of information manually input into a selected input-output device via the keyboard;
input row counter means for controlling a sequential read-out of information from the storage means of a selected input-output device to cause this information to be transmitted to the central data processing station via the information transmitting means;
input program counter means for controlling the operation of the input row counter means during an input operation in which information is transmitted to the central data processing station from the selected input-output device; and
output operating means operable in accordance with information transmitted from the central data processing station via the information transmitting means for remotely setting a selected input-output device during an output operation in which information is transmitted to the selected input-output device from the central data processing station.

7. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising
a plurality of multiple-row keyboard-operated input-output devices capable of having the keyboard set either remotely in response to electrical signals applied thereto or manually;
information transmitting means for transmitting input and output messages in serial form between the central data processing station and a selected input-output device;
input program counter means for controlling the operation of the scan counter means and of the input row counter means during an input operation in which information is transmitted to the central data processing station from the selected input-output device; error latch means effective in the event of a failure to receive a proper answering signal from the central data processing station in reply to an input message to cause a specified number of retry transmissions of the input message to the central data processing station; error counter means to count the number of retries made and to limit said retries to a predetermined number; error control means energized when a specified number of retries of an input message have been made without receiving a proper answering signal from the central data processing station; error indication means operable by the energization of the error control means to provide an indication of an input error at the selected input-output device; and error interrupt means operable by the energization of the error control means to interrupt the coupling of the selected input-output device with the central data processing station.

11. The combination of claim 10, also including encoding means for translating the messages transmitted by the information transmitting means from one form to another.

12. The combination of claim 10, also including checking means for checking the correctness of information contained in input messages transmitted by the information transmitting means from the selected input-output device to the central data processing station.

13. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising a plurality of multiple-row keyboard-operated input-output devices capable of having the keyboard set either remotely in response to electrical signals applied thereto or manually; information transmitting means for transmitting input and output messages in serial form between the central data processing station and the selected input-output device; scan counter means for sequentially scanning all of the input-output devices in a branch and operable to select a given input-output device by halting in the event that said given input-output device is conditioned to transmit an input message to the central data processing station, to enable communication to take place between the given input-output device and the central data processing station; gating means associated with each input-output device and operable to cause an input-output device selected by the scan counter means to be coupled to the central data processing station over the information transmitting means for transmission of an input message thereto; multiple-row storage means associated with each input-output device for storage of information manually input into the input-output device via the keyboard; read-out means for causing the information stored in the multiple-row storage means associated with a selected input-output device to be transmitted to the central data processing station via the information transmitting means; and error responsive means energized in the event of failure to receive a proper answering signal from the central data processing station in reply to an input message transmitted to the central data processing station from the selected input-output device.

14. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising a plurality of multiple-row keyboard-operated input-output devices capable of having the keyboard set either remotely in response to electrical signals applied thereto or manually; information transmitting means for transmitting input and output messages in serial form between the central data processing station and the selected input-output device; scan counter means for sequentially scanning all of the input-output devices in a branch and operable to select a given input-output device by halting in the event that said given input-output device is conditioned to transmit an input message to the central data processing station, to enable communication to take place between the given input-output device and the central data processing station; gating means associated with each input-output device and operable to cause an input-output device selected by the scan counter means to be coupled to the central data processing station over the information transmitting means for the transmission of an input message thereto; multiple-row storage means associated with each input-output device for storage of information manually input into the input-output device via the keyboard; read-out means for causing the information stored in the multiple-row storage means associated with a selected input-output device to be transmitted to the central data processing station via the information transmitting means; and error responsive means energized in the event of failure to receive a proper answering signal from the central data processing station in reply to an input message transmitted to the central data processing station from the selected input-output device.

15. The combination of claim 14, also including error indication means operable by the energization of the error responsive means to provide an indication of an input error at the selected input-output device.

16. The combination of claim 14, also including error interrupt means operable by the energization of the error responsive means to interrupt the coupling of the selected input-output device with the central data processing station.

17. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising a plurality of multiple-row keyboard-operated input-output devices capable of having the keyboard set
either remotely in response to electrical signals applied thereto or manually;
information transmitting means for transmitting input and output messages in serial form between the central data processing station and a selected input-output device;
scan counter means for sequentially scanning all of the input-output devices in a branch and operable to select a given input-output device by halting in the event that said given input-output device is conditioned to transmit an input message to the central data processing station, to enable communication to take place between the given input-output device and the central data processing station;
gating means associated with each input-output device and operable to cause an input-output device selected by the scan counter means to be coupled to the central data processing station over the information transmitting means for transmission of an input message thereto;
multiple-row storage means associated with each input-output device for storage of information manually input into the input-output device via the keyboard; Input row counter means for controlling the sequential read-out of the information contained in the multiple-row storage means associated with a selected input-output device to cause this information to be transmitted to the central data processing station via the information transmitting means; and input program counter means for controlling the operation of the scan counter means and of the input row counter means during an input operation in which information is transmitted to the central data processing station from the selected input-output device.
In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising:
a plurality of multiple-row keyboard-operated input-output devices capable of having the keyboard set either remotely in response to electrical signals applied thereto or manually;
information transmitting means for transmitting input and output messages in serial form between the central data processing station and a selected input-output device;
scan counter means for sequentially scanning all of the input-output devices in a branch and operable to select a given input-output device by halting in the event that said given input-output device is conditioned to transmit an input message to the central data processing station to enable communication to take place between the given input-output device and the central data processing station;
gating means associated with each input-output device and operable to cause an input-output device selected by the scan counter means to be coupled to the central data processing station over the information transmitting means for transmission of an input message thereto;
multiple-row storage means associated with each input-output device for storage of information manually input into the input-output device via the keyboard; and
readout means for causing the information stored in the multiple-row storage means associated with a selected input-output device to be transmitted to the central data processing station via the information transmitting means;
a plurality of multiple-row keyboard-controlled input-output devices, each provided with a plurality of solenoids for operating individual keys on the keyboard when energized by electrical signals applied thereto;
totalizer means associated with each of said input-output devices to enable amounts to be added and subtracted for the deriving of totals;
printing means associated with each of said input-output devices to enable amounts and other information to be recorded in connection with the processing of records;
balance means associated with each input-output device and operable in accordance with information contained in an output message from the central data processing station to cause a balance operation of a selected input-output device following an item operation of said device to cause the printing means to record a balance accumulated by the totalizer means;
information transmitting means for transmitting messages in serial form between the central data processing station and a selected input-output device; output select means for selecting one of the input-output devices of the branch in accordance with the information contained in an input message; gating means associated with each input-output device and operable to cause a selected input-output device to be coupled over the information transmitting means to the central data processing station for transmission of information from the central data processing station to the selected input-output device; output row counter means operable to provide a partial energizing circuit for all of the solenoids in each row of the keyboard of a selected input-output device in row-by-row sequence; output program counter means for controlling the operation of the output row counter means during an output operation in which information is transmitted to the selected input-output device from the central data processing station; and
output data register means operable in accordance with information transmitted from the central data processing station via the information transmitting means, and encoded into a form compatible with the digital system employed in the keyboards of the input-output devices, to provide a partial energizing circuit for all of the solenoids of a given row of the keyboard of a selected input-output device, so that only the solenoid for which partial energizing circuits are completed by both the output row counter means and the output data register means at a given time will be energized to operate the corresponding key of a selected input-output device.
In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, in a branch, comprising:
a plurality of multiple-row keyboard-controlled input-output devices, each provided with a plurality of solenoids for operating individual keys on the keyboard when energized by electrical signals applied thereto;
totalizer means associated with each of said input-output devices to enable amounts to be added and subtracted for the deriving of totals;
printing means associated with each of said input-output devices to enable amounts and other information to be recorded in connection with the processing of records;
balance means associated with each input-output device and operable in accordance with information contained in an output message from the central data processing station to cause a balance operation of a
selected input-output device following an item operation of said device to cause the printing means to record a balance accumulated by the totalizer means; information transmitting means for transmitting messages in serial form between the central data processing station and a selected input-output device; output select means for selecting one of the input-output devices of the branch in accordance with the information contained in an output message; gating means associated with each input-output device and operable to cause a selected input-output device to be coupled over the information transmitting means to the central data processing station for transmission of information from the central data processing station to the selected input-output device; and solenoid energizing means responsive to information contained in output messages transmitted from the central data processing station to the selected input-output device for sequential energization of solenoids for selected keys in the various rows of the multiple-row keyboard of the selected input-output device.

21. In a branch sub-system of an on-line system in which records maintained at a central data processing station may have additional entries made to any record at any one of a plurality of branch locations, the combination, with a branch comprising:

a plurality of multiple-row keyboard-controlled input-output devices, each provided with a plurality of solenoids for operating individual keys on the keyboard when energized by electrical signals applied thereto; information transmitting means for transmitting messages in serial form between the central data processing station and a selected input-output device; output select means for selecting one of the input-output devices of the branch in accordance with the information contained in an output message; gating means associated with each input-output device and operable to cause a selected input-output device to be coupled over the information transmitting means to the central data processing station for transmission of information from the central data processing station to the selected input-output device; output row counter means operable to provide a partial energizing circuit for all of the solenoids in each row of the keyboard of a selected input-output device in row-by-row sequence; output program counter means for controlling the operation of the output row counter means during an output operation in which information is transmitted to the selected input-output device from the central data processing station; and output data register means operable in accordance with information transmitted from the central data processing station via the information transmitting means, and encoded into a form compatible with the digital system employed in the keyboards of the input-output devices, to provide a partial energizing circuit for all of the solenoids of a given digit value of the keyboard of a selected input-output device, so that only the solenoid for which partial energizing circuits are completed by both the output row counter means and the output data register means at a given time will be energized to operate the corresponding key of a selected input-output device.

22. The combination of claim 21 also including totalizer means associated with each of said input-output devices to enable amounts to be added and subtracted for the deriving of totals.

23. The combination of claim 22, also including printing means associated with each of said input-output devices to enable item amounts, balance amounts, and other information to be recorded in connection with processing of records.

24. The combination of claim 23 also including balance means associated with each input-output device and operable in accordance with information contained in an output message from the central data processing station to cause a balance operation of a selected input-output device following an item operation of said device to cause the printing means to record a balance accumulated by the totalizer means.

25. The combination of claim 21, also including encoding means for translating the messages transmitted by the information transmitting means from one form to another.

26. The combination of claim 21 also including checking means for checking the correctness of information contained in output messages transmitted by the information transmitting means from the central data processing station to the selected input-output device.

27. The combination of claim 21, also including error latch means operable to be set, in the event of an error occurring during an output operation from the central data processing station to the selected input-output device, to establish the existence of an error condition.

28. The combination of claim 27, also including error indication means responsive to the error latch means to provide an indication of an error condition at the selected input-output device.

29. The combination of claim 27, also including error message means responsive to the error latch means to cause an error message to be transmitted over the information transmitting means to the central data processing station in the event of an error occurring during an output operation.

30. The combination of claim 21 also including hold means responsive to the information contained in an output message from the central data processing station to provide an indication at the selected input-output device of a hold condition existing in connection with the record being processed.

31. The combination of claim 30, also including override means associated with the selected input-output device and operable to initiate an input message to override the existing hold condition.

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