

[54]
DIGITAL SPEED CONTROL

[75]
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[22]
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180/105 E; 317/5; 123/102

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Int. Cl.
B60k 31/00

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Field of Search
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[56]
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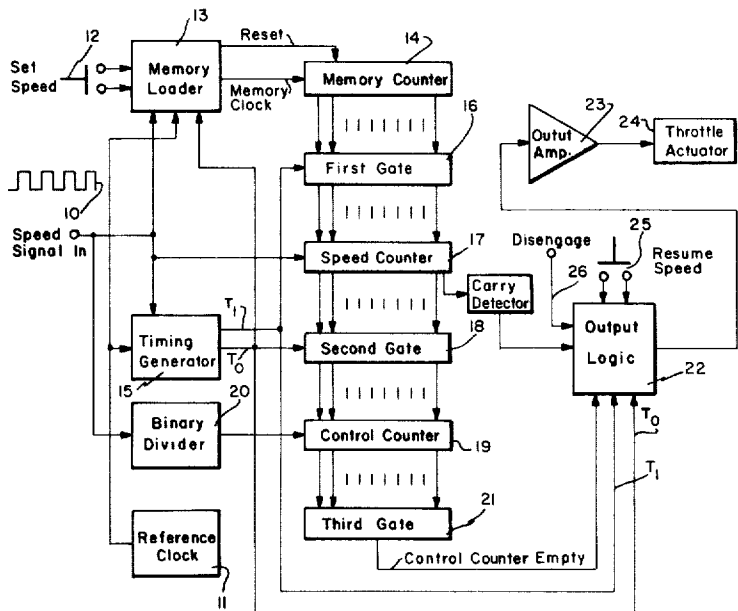
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ABSTRACT

A digital system for maintaining the speed of a motor vehicle at a preselected speed is disclosed wherein a desired vehicle speed is set into a digital memory bank. The instantaneous actual speed of the vehicle is determined by a digital readout. The desired vehicle speed and the actual speed of the vehicle are compared to produce a digital error signal which is used to control the throttle setting of the vehicle so that the actual speed of the vehicle equals the desired speed.

7 Claims, 4 Drawing Figures



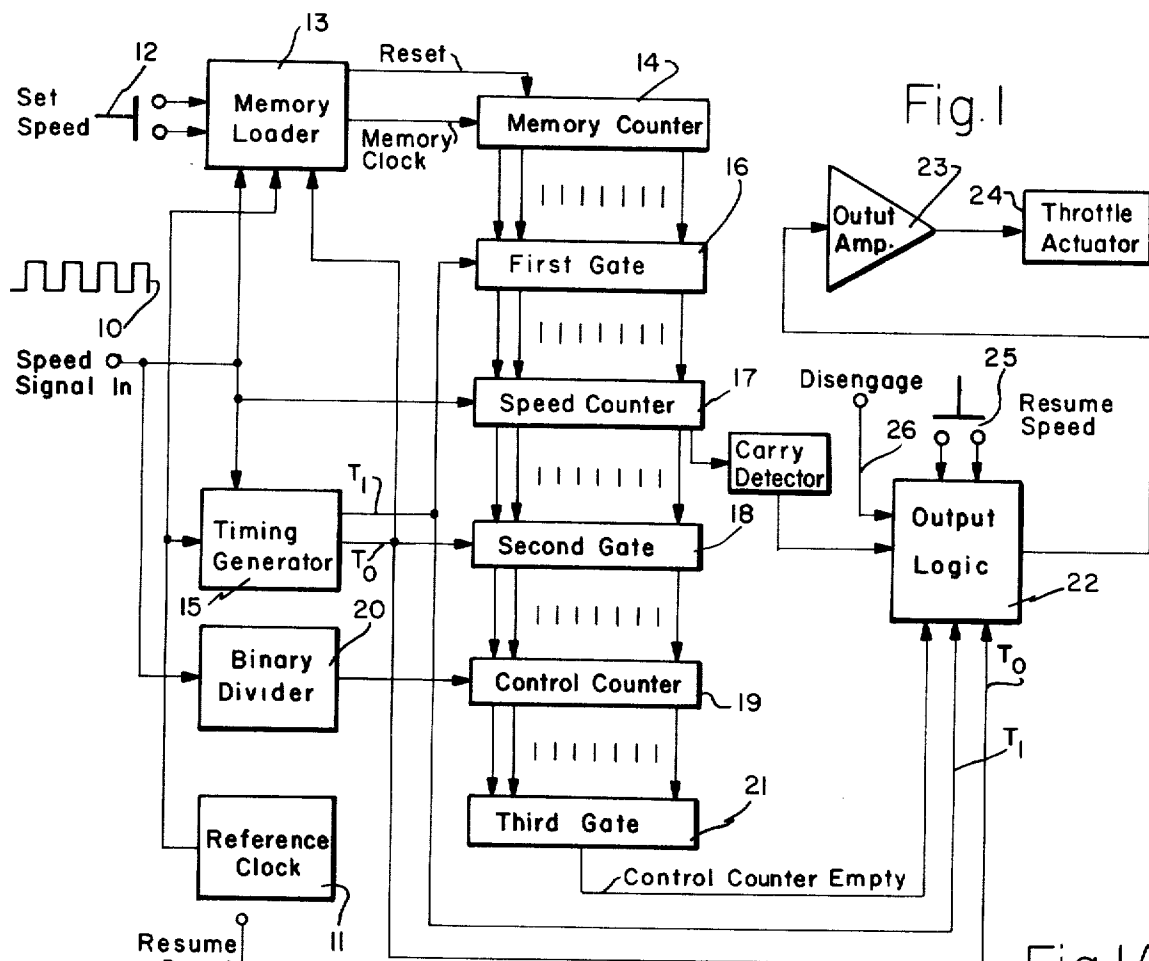


Fig. 1

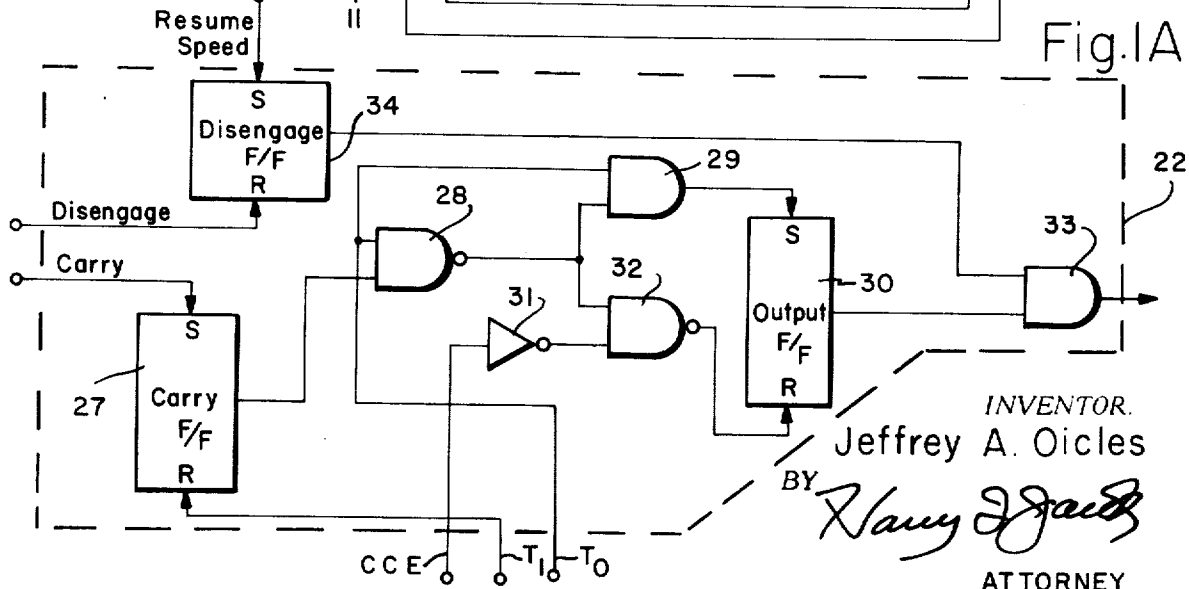


Fig. 1A

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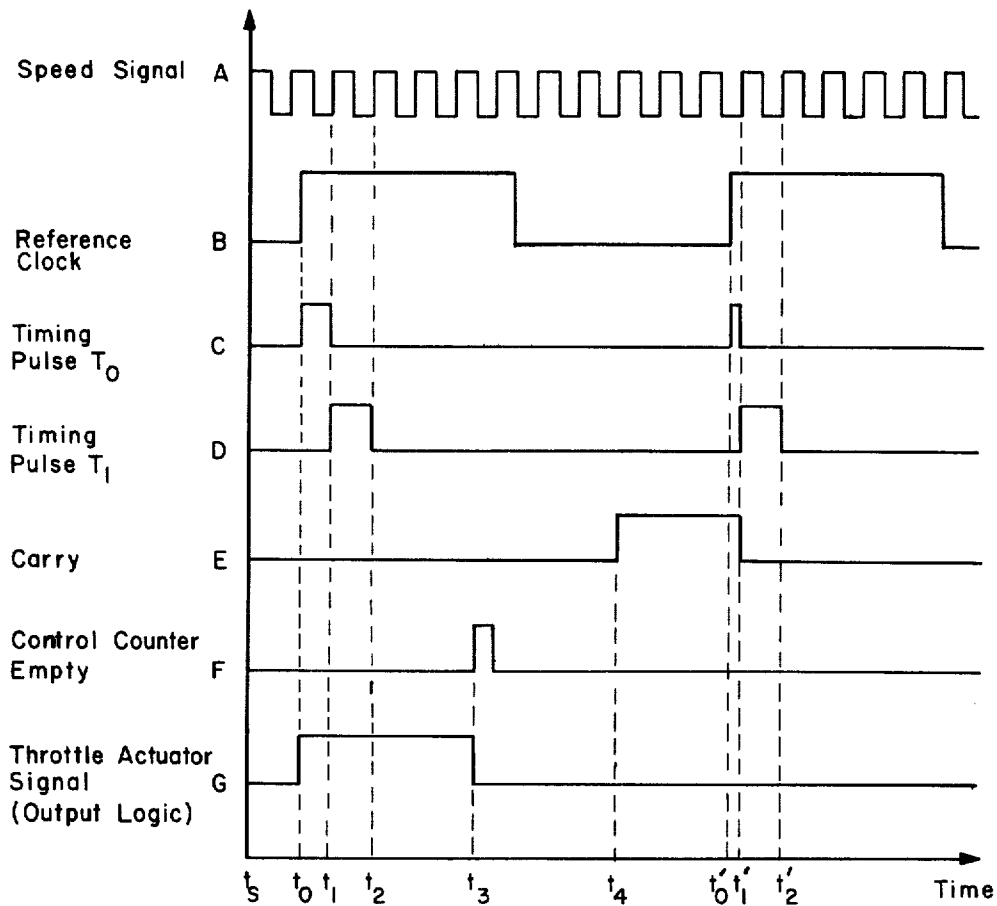


Fig.2

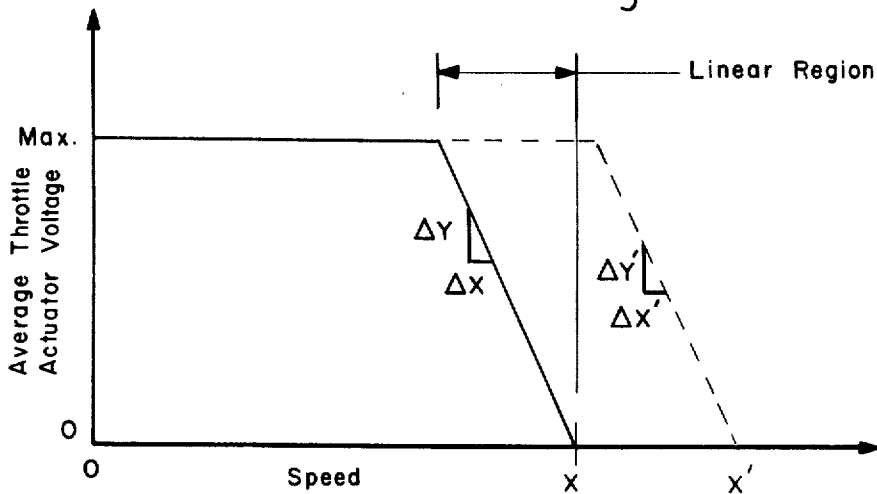


Fig.3

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DIGITAL SPEED CONTROL**CROSS REFERENCE TO RELATED APPLICATION**

This is a continuation of application Ser. No. 1,448 filed Jan. 8, 1970 now abandoned.

BACKGROUND OF THE INVENTION

Automatic speed control devices are highly advantageous in driving great distances on limited access highways in order to help a driver maintain a desired speed for a long period of time.

The earliest automatic speed control was an elementary dashboard throttle control positioned to hold the throttle at a fixed setting. This type of control, however, is unable to compensate for the various changes in driving conditions, such as wind, terrain, and road surface characteristics.

Electronic automobile speed controls have been developed using two analog electrical signals, one proportional to the actual vehicle speed and the other proportional to the desired vehicle speed. These analog signals are compared to generate an error signal which is applied to position the throttle to make the actual speed of the vehicle to the desired speed.

Further improvements to these prior art devices have been disclosed which utilize analog memory systems for recording the desired vehicle speed. A typical analog memory comprises a high quality capacitor which is charged to a preselected voltage. The amount of voltage stored in the capacitor is proportional to the desired speed. A very high input impedance amplifier is used to read out the preselected voltage and compare it to the voltage representative of actual vehicle speed. These high quality capacitors must be able to maintain their charge within one percent for five hours. To accomplish this, the capacitors must be of an expensive variety and be hermetically sealed to prevent leakage. The high cost of these capacitors is therefore highly disadvantageous.

Another example of an analog memory is disclosed in U.S. Pat. No. 3,340,950 by Albert Hopengarten. Hopengarten discloses an analog memory for a speed control wherein a tone having a frequency proportional to vehicle speed is generated. When the desired speed is reduced, the corresponding tone is recorded on a magnetic track. Means are provided for controlling the speed of the vehicle in response to the recorded frequency.

Analog memories such as those described above are expensive in comparison to a digital memory. However, using a digital memory in an analog system would require digital-to-analog converters which would destroy the inherent economy of a digital memory.

It would be desirable, therefore, to construct an all digital speed maintaining system to take full advantage of the economy of a digital memory. In addition, the emerging technology of metal oxide semiconductor large scale integration (MOS LSI) circuits makes the digital approach economically attractive for programs involving large quantities, such as automobile production. Furthermore, the nature of digital electronics results in a speed maintaining system that is largely unaffected by temperature variations, power supply noise, aging and production tolerances.

SUMMARY

In accordance with a preferred embodiment of the

present invention, the speed of a motor vehicle is sensed by a digital sensor to produce digital speed pulses. A reference clock generates a series of reference clock pulses. A digital counter counts and stores the number of digital speed pulses occurring in one period of the reference clock thus producing a digital number proportional to the desired speed of the vehicle. The number of speed pulses occurring in one reference clock period is digitally compared to the stored number of speed pulses to produce a digital error signal. The speed of the vehicle is controlled by an electromechanical throttle valve solenoid. In response to the digital error signal, the throttle valve solenoid adjusts the speed of the vehicle to be the desired speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an example of a preferred embodiment of the speed maintaining system according to the invention;

FIG. 1A is a logic diagram of the output logic shown in FIG. 1;

FIG. 2 is a system timing diagram displaying wave forms of the various system components; and

FIG. 3 is a plot of the average throttle actuator voltage versus the actual speed of the vehicle.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the digital speed control shown in FIG. 1, a digital speed signal 10 is received from the vehicle at the "speed signal in" terminal. The speed signal is in the form of a series of pulses as illustrated in FIG. 2A. As the speed of the vehicle increases, the number of pulses per unit of time increases proportionately. Thus, speed signal 10 represents the actual speed of the vehicle at any instant of time.

The speed signal 10 may be derived in any of the number of ways known for generating a series of pulses responsive to the speed of a moving vehicle. For example, speed signal 10 may be generated by a rotating gear operatively connected to the drive train, rotating at a speed proportional to the speed of the vehicle and inducing pulses into a detector as each gear tooth passes by the detector. The number of pulses per unit of time would therefore be proportional to the speed of the vehicle. In other words, the frequency of the speed signal is proportional to the speed of the vehicle.

A reference clock 11 produces a series of pulses as shown in FIG. 2B. The frequency of reference clock 11 is much lower than the frequency of the speed signal 10 shown in FIG. 2A. It is within the scope of the invention, however, to provide reference timing having a much higher frequency than the speed signal. Choice of timing schemes may be dictated by digital equipment limitations and not theory. Therefore, for purposes of the following discussion, reference will be made only to a timing scheme employing a reference clock frequency that is lower than the frequency of speed signal 10.

To engage the speed maintaining system, the vehicle operator adjusts the vehicle speed to the desired value and depresses a "set speed" button 12. Depressing button 12 triggers a memory loader 13 which causes a memory counter 14 to count and store the number of speed signal pulses for one period of the reference clock. The number of speed signal pulses stored in any one reference clock period is a binary digital number

proportional to the speed of the vehicle during that reference clock period. The desired speed of the vehicle is hereinafter referred to as the set speed.

To understand more fully how memory loader 13 and memory counter 14 operate, reference is made to timing generator 15. Timing generator 15 produces output pulses T_0 and T_1 shown in FIGS. 2C and 2D respectively. Timing pulse T_0 rises to a preselected potential at the initiation of the first reference clock pulse occurring at time t_0 shown in FIG. 3. At the initiation of the next speed signal timing pulse, occurring at time t_1 and shown in FIG. 2A, timing pulse T_0 returns to zero, at which time timing pulse T_1 rises to some preselected voltage. At the initiation of a second speed signal timing pulse, occurring at time t_2 , timing pulse T_1 returns to zero. At the initiation of a second reference clock pulse, timing pulse T_1 rises up at time t_0' and falls at time t_1' . Similarly, timing pulse T_2 rises up at time t_1' and falls at time t_2' .

Memory loader 13 receives speed signal pulses, reference clock pulses and T_0 timing pulses. When set speed button 12 is depressed, memory loader 13 is enabled to search for the beginning of the next reference clock period. Referring to FIG. 2B, assume that set speed button 12 is depressed at time t_0 . The next reference clock period will thus begin at time t_0 . At time t_0 , a T_0 timing pulse resets memory counter 14 to zero via the reset line and speed signal 10 is directed by memory loader 13, via the memory clock line, to memory counter 14. Memory counter 14 is a digital up counter clocked by speed signal 10 which counts up for one reference clock period. At time t_0' , memory counter 14 ceases counting, and memory loader 13 completes its function until set speed button 12 is depressed to enter a new speed into memory counter 14.

Since memory counter 14 has counted the number of speed signal pulses in a known period of time, i.e., one reference clock period, the digital number stored therein is proportional to the set speed of the vehicle during that reference clock period which immediately follows the depression of set speed button 12.

A first gate 16, which is an AND gate, receives timing pulse T_1 , and the digital number representative of the set speed stored in memory counter 14. The output of first gate 16 is fed to a speed counter 17. At times t_1 , t_1' , . . . t_n , timing pulse T_1 enables first gate 16 to gate the digital number representative of the set speed stored in memory counter 14 to speed counter 17.

Speed counter 17 is a digital down counter which is clocked by speed signal 10. Speed counter 17 therefore will counter down the digital number previously stored in memory counter 14 for one reference clock period. If the instantaneous vehicle speed is the same as the set speed, speed counter 17 will count down to zero at the end of one reference clock period because the number of speed pulses counted by speed counter 17 during one reference clock period is the same number of speed pulses counted by memory counter 14 during a like reference clock period.

If the actual speed of the vehicle is greater than the set speed, speed counter 17 will count down through zero before the end of one reference clock period because the number of speed pulses counted by speed counter 17 during one reference clock period is greater than the number of speed pulses counted by memory counter 14 during a like reference period. Whenever speed counter 17 counts down through zero, a carry

detector 17a outputs a "carry" pulse. Carry detector 17a may be an AND gate which detects binary zeros at the output of speed counter 17.

The "carry" pulse is used by an output logic 22 to command a decrease in speed. The operation of output logic 22 will be explained in detail below.

If the actual speed of the vehicle is less than the set speed, speed counter 17 will count less speed pulses during one reference clock period than memory counter 14 will count during a like reference period. Thus a discrete digital number will remain stored on speed counter 17 at the end of the reference clock period. This remaining digital number is proportional to the difference in speed between the set speed and the actual vehicle speed.

A second gate 18, which is also an AND gate, receives timing pulse T_0 and the digital number proportional to the difference in speed between the set speed and the actual vehicle speed remaining in speed counter 17. The output of second gate 18 is fed to a control counter 19 which is a digital down counter. At times t_0 , t_0' , . . . t_n , timing pulse T_0 enables second gate 18 to gate the digital number proportional to the difference in speed between the set speed and the actual vehicle speed remaining in speed counter 17 to control counter 19.

Speed signal 10 is divided by some whole number by a binary divider 20. The output of binary divider 20 is used to clock control counter 19. The output of control counter 19 is fed to third gate 21. Third gate 21 is an AND gate which produces a pulse output called the "control counter empty," shown in FIG. 2F and occurring at time t_3 , whenever control counter 19 counts down through zero. Since control counter 19 counts down the digital number proportional to the difference in speed between the set speed and the actual speed of the vehicle, the length of time from t_0 , when control counter 19 begins counting, until t_3 , when control counter 19 empties, is likewise proportional to that difference in speed. Therefore the control counter empty signal is used in conjunction with output logic 22 to command an increase in speed.

Output logic 22 controls the speed of the vehicle as follows. Output logic 22 receives timing pulses T_0 and T_1 from timing generator 15, the carry signal from carry generator 17a and the control counter empty signal from third gate 21. The output of logic 22 is amplified by an output amplifier 23 which in turn drives a throttle actuator 24. Throttle actuator 24 directly controls the speed of the vehicle.

The operation of output logic 22 can be explained with reference to the logic diagram of FIG. 1A. A carry flip-flop 27 is set upon receipt of a carry pulse generated by carry generator 17a whenever speed counter 17 counter down through zero. Carry flip-flop 27 is reset upon receipt of a T_1 pulse. At T_0 pulse and the output of carry flip-flop 27 are fed into a first NAND gate 28. A NAND gate will output a logical zero only when logical ones appear at both input terminals. The output of first NAND gate 28 and the T_0 pulse line are fed to the input of a first AND gate 29. The output of first AND gate 29 sets an output flip-flop 30. The control counter empty pulse line is inverted by an inverter 31. The output of inverter 31, which is the inverted control counter empty pulse, and the output of first NAND gate 28 are fed to a second NAND gate 32. The output of second NAND gate 32 resets output flip-flop

30. The output of output flip-flop 30 is fed to output amplifier 23 via a second AND gate 33.

The system may be disengaged or engaged by means of a disengage flip-flop 34. Output flip-flop 30 is gated to drive the throttle actuator by a second AND gate 33. Second AND gate 33 is enabled and disabled by the output of disengage flip-flop 34. When the disengage flip-flop is set, the logical one output enables AND gate 33. Thus the output from flip-flop 30 is able to drive throttle actuator 24. When the disengage flip-flop is reset, the logical zero output disables AND gate 33 to cut off the output of flip-flop 30 from throttle actuator 24. A disengage pulse to reset flip-flop 34 may be generated by applying the brakes of the vehicle, or by moving the transmission to a neutral position. To reengage the system, a resume speed button 25 is depressed to generate a pulse to set flip-flop 34 to enable second AND gate 33 to gate the output of flip-flop 30 to throttle actuator 24.

The generation of the throttle actuator signal may be explained with reference to FIGS. 1A and 2. If there is no carry pulse at time t_0 , carry flip-flop 27 will be in the reset position outputting a logical zero to one input of first NAND gate 28. First NAND gate 28 will therefore output a logical one to enable first AND gate 29. A T_0 pulse occurring at time t_0 passes through enabled first AND gate 29 to set output flip-flop 30. A second NAND gate 32 insures that output flip-flop 30 is not accidentally reset by outputting a logical zero. The inputs to NAND gate 32 are a logical one from NAND gate 28 and the output of inverter 31. Inverter 31 inverts the control counter empty line to produce a logical one so long as there is no control counter empty pulse.

A carry pulse from the output of carry detector 17a prevents the setting of output flip-flop 30 and insures that it is reset. The carry pulse sets, and a T_1 pulse resets, a carry flip-flop 27. When set, carry flip-flop 27 outputs a logical one to one input of NAND gate 28. A T_0 pulse into the other input of NAND gate 28 produces a logical zero at the output of NAND gate 28. The logical zero output of NAND gate 28 disables AND gate 29 so the T_0 pulse cannot set output flip-flop 30. The logical zero output of NAND gate 28 insures that NAND gate 32 produces a logical one to reset output flip-flop 30. The T_1 pulse always resets carry flip-flop 27 to permit a T_0 pulse to set output flip-flop 30 unless another carry pulse again sets carry flip-flop 27.

Recall that the length of time from t_0 until t_3 is proportional to the difference in speed between the set speed and the actual speed of the vehicle. To produce a square wave having a pulse width proportional to the difference in speed between the set speed and the actual vehicle speed, the control counter empty pulse is used to reset output flip-flop 30. Assume that a T_0 pulse has set output flip-flop 30, and there is no carry pulse, so the output of NAND gate 28 is a logical one. Thus one input to NAND gate 32 is a logical one. A control counter empty pulse inverted by inverter 31 will produce a momentary logical zero at the other input to NAND gate 32. The control counter empty pulse will therefore pass through NAND gate 32 to reset output flip-flop 30 to produce the wave form shown in FIG. 2G.

The output of output logic 22 is therefore a pulse width modulated square wave having a pulse width proportional to the difference in speed between the set speed and the actual speed of the vehicle, so long as the

set speed is greater than the actual vehicle speed. If the actual vehicle speed is greater than the set speed, there will be a constant carry signal produced which results in a zero throttle actuator signal.

Throttle actuator 24 directly controls the throttle, and thus the speed of the vehicle. Throttle actuator 24 may be an electro-pneumatic device responsive to a pulse width modulated signal. Typically, actuator 24 overrides the normal throttle control of the vehicle when the speed maintaining system is engaged. The vehicle operator would normally apply zero throttle, therefore, when there is no input to actuator 24 there is zero throttle applied to the vehicle. As the pulse width of the input voltage to actuator 24 increases, the average voltage increases proportionately. As the average input voltage increases, the speed of the vehicle increases as shown in FIG. 3.

Referring to FIG. 3, if the speed of the vehicle is equal to the set speed "X" there will be no carry pulse from carry generator 17a or a control counter empty pulse from third gate 21. The throttle actuator signal will be flat, thus yielding a zero throttle actuator voltage. At speeds above set speed X, there will be a carry pulse generated by carry generator 17a, thus insuring a zero average throttle actuator voltage. Zero throttle actuator voltage produces a zero throttle which would cause the vehicle to slow down until it reaches the set speed.

At speeds below set speed X, the average throttle actuator voltage increases linearly until it reaches a maximum value. The maximum value occurs when there is a continuous output from output logic 22 because speed counter 17 has transferred a binary digital number, proportional to the difference in speed between the set speed and the actual vehicle speed, to control counter 19 which is so large that control counter 19 cannot count down to zero within one reference clock period.

The maximum value of the average throttle actuator voltage is the maximum value of output amplifier 23. By adjusting the gain of amplifier 23, the maximum average throttle actuator voltage can be raised or lowered.

The gain of the speed maintaining system is the slope $\Delta Y/\Delta X$ of the plot of average throttle actuator voltage versus speed shown in FIG. 3. The slope can be adjusted by altering the divisor of binary divider 20. If the divisor is large, control counter 19 will be clocked at a slower rate. Thus control counter 19 will empty in a longer period of time for a given difference between the set speed and an actual vehicle speed. Since control counter 18 takes longer to empty, the pulse width of the output from logic 22 is increased and the average throttle actuator voltage is increased. Therefore the slope of the curve shown in FIG. 3 is steepened and the gain of the system is increased. Similarly, if the divisor of binary divider 20 is decreased, control counter 19 will count down faster, control counter 19 will empty in a shorter period of time for a given difference between the set speed and an actual vehicle speed, and the average throttle actuator voltage will be lower, thus the gain of the system will be decreased.

If a higher set speed, such as X is chosen, the gain of the system $\Delta Y'/\Delta X' = \Delta Y/\Delta X$ because, as explained above, the average throttle actuator voltage is proportional to the absolute difference in speed between the

set speed and the actual vehicle speed, not a percentage difference in speed.

It can therefore be seen that when the actual speed of the vehicle drops below the set speed, the average throttle actuator voltage increases until a maximum voltage is reached. Thus for actual vehicle speeds substantially below the set speed, the speed of the vehicle is quickly brought up to the set speed. As the speed of the vehicle nears the set speed, the average throttle actuator voltage decreases to zero at the set speed to prevent a jerky movement. At speeds above the set speed, the average throttle actuator voltage remains at zero until the vehicle speed falls below the set speed.

If the speed of the vehicle rises above the set speed, the throttle actuator voltage decreases to zero until the speed of the vehicle returns to the set speed as described above. It is within the scope of the invention, however, to provide means for applying the brakes of the vehicle to slow it down when the vehicle speed rises substantially above the set speed.

In addition, a sensor responsive to throttle pressure could be included to slow the vehicle to a stop in the event that the vehicle operator was suddenly incapacitated.

what is claimed is:

1. A digital speed control for maintaining a motor vehicle at a preselected constant speed comprising:

- a. means for generating a first digital signal responsive to the actual speed of the vehicle comprising a series of speed signal pulses having a pulse repetition frequency proportional to the speed of the vehicle;
- b. means for generating a second digital signal responsive to a constant preselected vehicle speed comprising a digital reference clock, a first digital counter and means for clocking said first digital counter in response to said first digital signal during a first given reference clock period, thereby storing in said first digital counter a first digital number responsive to the preselected speed of the vehicle;
- c. means for digitally comparing the first digital signal responsive to the actual speed of the vehicle and the second digital signal responsive to the constant preselected vehicle speed to produce a digital error signal comprising;
- d. second digital down counter means clocked by said first signal responsive to the actual speed of the vehicle;
- e. means for generating a first and a second timing pulse at the beginning of each reference clock period;
- f. first AND gate means gating, upon receipt of a second timing pulse, the first digital number responsive to the speed of the vehicle stored in said first digital counter means to the second digital counter means, said second digital counter means being a down counter clocked by the first digital signal pulse train to count down for one reference clock period, so that if the actual speed of the vehicle is greater than the preselected speed of the vehicle the second counter will count down through zero, and if the actual speed of the vehicle is less than the preselected speed of the vehicle a second digital number will remain stored on the second digital counter;
- g. means for generating a "carry" signal when the second digital counter counts down through zero;

- h. binary means for dividing the first digital signal responsive to the actual speed of the vehicle;
 - i. third digital counter means clocked by the divided binary signal responsive to the actual speed of the vehicle;
 - j. second AND gate means gating, upon receipt of a first timing pulse, the second digital number stored in the second digital down counter to the third digital counter means, said third digital counter means being a down counter clocked by the divided binary signal responsive to the actual speed of the vehicle counting down during one reference clock period, so that if the actual speed of the vehicle is less than the preselected speed of the vehicle the third counter may count down through zero;
 - k. third AND gate means producing an output whenever the third counter counts down through zero;
 - l. means for producing a pulse width modulated error signal having a pulse width proportional to the difference in speed between the preselected constant speed and an actual vehicle speed lower than the preselected speed; and
 - m. means for adjusting the speed of the vehicle in response to said pulse width modulated error signal to maintain the preselected constant speed.
2. A digital speed control as claimed in claim 1 wherein the means for producing the pulse width modulated error signal comprises:
- means for producing a first voltage at times corresponding to one speed signal pulse after the beginning of the second reference clock period;
 - means for inhibiting the first voltage if a carry signal is produced; and
 - means for inhibiting the first voltage in response to an output from the third AND gate.
3. A digital speed control as claimed in claim 1 wherein the means for producing the pulse width modulated error signal comprises:
- a first resetable digital flip-flop having an output
 - times means for setting said first flip-flop at times corresponding to one speed signal pulse after the beginning of the second reference clock period;
 - means for inhibiting the setting of said first flip-flop if a carry signal is produced, and
 - means for resetting said first flip-flop in response to an output from said third AND gate.
4. A digital speed control as claimed in claim 3 and further including:
- a second resetable digital flip-flop;
 - a fourth AND gate, one input to said fourth AND gate being from the output of said first digital flip-flop, and
 - the other input to said fourth AND gate being from the output of said second digital flip-flop;
 - means for resetting said second flip-flop in response to a command to disengage the speed maintaining system; and
 - means for setting said second flip-flop to engage the speed maintaining system.
5. A digital speed control as claimed in claim 4 wherein the command to disengage the system is in response to a braking command.
6. A digital speed control as claimed in claim 5 wherein the means for adjusting the speed of the vehicle in response to the digital error signal comprises positioning a throttle to vary the speed of the motor of the vehicle.

7. A digital speed control for maintaining a motor vehicle at a preselected constant speed comprising:
means for generating a first digital signal comprising a series of speed signal pulses having a pulse repetition frequency proportional to the actual speed of the vehicle;
a digital reference clock;
a first digital counter counting the number of speed signal pulses in one reference clock period to produce a first digital number proportional to a preselected speed of the vehicle during a first particular reference clock period;
means for storing said first digital number responsive to the speed of the vehicle in said first digital counter;
a second digital counter clocked by the first digital signal pulse train;
means for generating a first timing pulse at the beginning of each reference clock period;
means for generating a second timing pulse after the beginning of each reference clock period;
a first AND gate gating, upon receipt of a second timing pulse, the first digital number responsive to the speed of the vehicle stored in said first digital counter to the second digital counter;
said second digital counter being a down counter clocked by the first digital signal pulse train counting down for one reference clock period, so that if the actual speed of the vehicle is greater than the preselected speed of the vehicle the second counter will count down through zero, and if the actual speed of the vehicle is less than the preselected speed of the vehicle a second digital number will be stored on the second digital counter;
means for generating a carry signal when said second

digital counter counts down through zero;
binary means for dividing the first digital signal responsive to the actual speed of the vehicle;
a third digital counter clocked by the divided binary signal responsive to the actual speed of the vehicle;
a second AND gate gating, upon receipt of a first timing pulse, the second digital number stored in the second digital down counter to the third digital counter;
said third digital counter being a down counter, clocked by the divided binary signal responsive to the actual speed of the vehicle, counting down during one reference clock period, so that if the actual speed of the vehicle is less than the preselected speed of the vehicle the third counter may count down through zero;
a third AND gate producing an output whenever the third counter counts down through zero;
means for producing a pulse width modulated error signal having a width proportional to the difference in speed between the preselected constant speed and an actual vehicle speed lower than the preselected speed comprising:
a first resetable digital flip-flop having an output;
means for setting the first flip-flop in response to a first timing pulse;
means for inhibiting the setting of the first flip-flop if a carry signal is produced, and
means for resetting the first flip-flop in response to an output from the third AND gate; and
means for adjusting the speed of the vehicle in response to the digital error signal, produced by the first flip-flop, to maintain the preselected constant speed.

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