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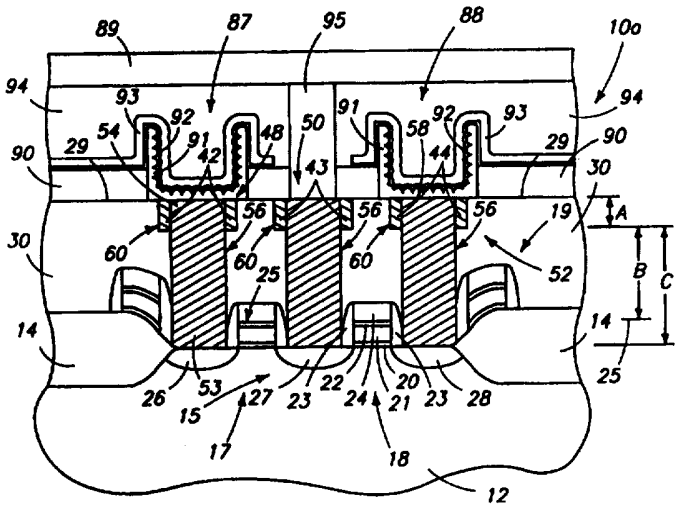

(57) Abstract

A semiconductor processing method of forming a contact pedestal includes: a) providing a node location (28) to which electrical connection is to be made; b) providing insulating dielectric material (30) over the node location; c) etching a contact opening into the insulating dielectric material over the node location to a sufficient degree but not to outwardly expose the node location, the contact opening having a base; d) providing a spacer layer over the insulating dielectric material within the contact opening to a thickness which less than completely fills the contact opening; e) anisotropically etching the spacer layer to form a sidewall spacer (44) within the opening; f) etching through the contact opening base to outwardly expose the node location; g) filling the contact opening with an electrically conductive material (56); h) rendering the sidewall spacer electrically conductive.

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DESCRIPTION

A SEMICONDUCTOR PROCESSING METHOD FOR FORMING A CONTACT PEDESTAL FOR A STORAGE NODE OF A CAPACITOR IN INTEGRATED CIRCUITRY

Technical Field

This invention relates to semiconductor processing methods of forming contact pedestals and to integrated circuitry employing contact pedestals. The invention also relates to methods of forming a storage node of a capacitor.

Background Art

As DRAMs increase in memory cell density, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing cell area. Additionally, there is a continuing goal to further decrease cell area. The principal way of increasing cell capacitance is through cell structure techniques. Such techniques include three-dimensional cell capacitors, such as trenched or stacked capacitors.

Conventional stacked capacitor DRAM arrays utilize either a buried bit line or a non-buried bit line construction. With buried bit line constructions, bit lines are provided in close vertical proximity to the bit line contacts of the memory cell field effect transistors (FETs), with the cell capacitors being formed horizontally over the top of the wordlines and bit lines. With non-buried bit line constructions, deep vertical contacts are made through a thick insulating layer to the cell FETs, with the capacitor constructions being provided over the word lines and beneath the bit lines. Such non-buried bit line constructions are also referred to as "capacitor-under-bit line" or "bit line-over-capacitor" constructions.

In DRAM and other integrated circuitry, ohmic electrical contact is typically made relative to an electrically conductive diffusion region in a semiconductor substrate between a pair of conductive lines provided over the substrate. In some instances, contact plugs or pedestals are utilized to facilitate making electrical connection to the substrate, and contend with adverse vertical topography. Such can provide the advantage of producing a larger targeting area for a subsequent conductive line contact to the diffusion region through the pedestal. My earlier U.S. Patent Nos. 5,338,700; 5,340,763; 5,362,666; and 5,401,681 are hereby incorporated by reference into this disclosure.

Brief Description of the Drawings

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 7.

Fig. 9 is a diagrammatic sectional view of an alternate embodiment semiconductor wafer fragment at one alternate processing step in accordance with the invention.

Fig. 10 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 9.

Fig. 11 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 10.

Fig. 12 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 11.

Fig. 13 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 12.

Fig. 14 is a diagrammatic sectional view of another alternate embodiment semiconductor wafer fragment at another alternate processing step in accordance with the invention.

Fig. 15 is a diagrammatic sectional view of still another alternate embodiment semiconductor wafer fragment at yet another alternate processing step in accordance with the invention.

Fig. 16 is a view of the Fig. 15 wafer fragment at a processing step subsequent to that depicted by Fig. 15.

Fig. 17 is a diagrammatic sectional view of yet another alternate embodiment semiconductor wafer fragment at yet another alternate processing step in accordance with the invention.

Fig. 18 is a view of the Fig. 17 wafer fragment at a processing step subsequent to that depicted by Fig. 17.

Fig. 19 is a diagrammatic sectional view of still yet another alternate embodiment semiconductor wafer fragment at still yet another alternate processing step in accordance with the invention.

Fig. 20 is a view of the Fig. 19 wafer fragment at a processing step subsequent to that depicted by Fig. 19.

Fig. 21 is a view of the Fig. 19 wafer fragment at a processing step subsequent to that depicted by Fig. 20.

Fig. 22 is a view of the Fig. 19 wafer fragment at a processing step subsequent to that depicted by Fig. 21.

Fig. 23 is a view of the Fig. 19 wafer fragment at a processing step subsequent to that depicted by Fig. 22.

Fig. 24 is a diagrammatic top view of a contact pedestal in accordance with the invention.

Best Modes for Carrying Out the Invention and Disclosure of Invention

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In accordance with one aspect of the invention, a semiconductor processing method of forming a contact pedestal comprises:

providing a node location to which electrical connection is to be made;

providing insulating dielectric material over the node location;

etching a contact opening into the insulating dielectric material over the node location to a degree insufficient to outwardly expose the node location, the contact opening having a base;

providing a spacer layer over the insulating dielectric material to within the contact opening to a thickness which less than completely fills the contact opening;

anisotropically etching the spacer layer to form a sidewall spacer within the contact opening;

after forming the sidewall spacer, etching through the contact opening base to outwardly expose the node location;

filling the contact opening to the node location with electrically conductive material;

rendering the sidewall spacer electrically conductive; and

etching the electrically conductive material to form an electrically conductive contact pedestal comprising the sidewall spacer, the pedestal having an outer surface which is substantially coplanar with opposing laterally adjacent electrically insulative surfaces.

In another aspect, integrated circuitry comprises:

a node location;

an electrically conductive longitudinal contact pedestal in electrical connection with the node location, the contact pedestal comprising:

an inner longitudinal portion in electrical connection with the node location and an outer longitudinal portion, the outer longitudinal portion comprising an anisotropically etched sidewall spacer and a radially inner electrically conductive pillar, the spacer being electrically conductive and in electrical connection with the pillar;

the pillar and spacer having a substantially coplanar common outer surface; and

insulating dielectric material having a substantially planar outer surface which is substantially coplanar with the contact pedestal common outer surface.

In accordance with yet another aspect, a semiconductor processing method of forming a storage node of a capacitor comprises:

providing an electrically conductive pillar within a mass of insulating material;

etching the pillar and mass of insulating material at substantially the same rate to form a capacitor container opening within the mass of insulating material, the pillar projecting from the capacitor container opening; and

providing a capacitor storage node within the capacitor container opening in electrical connection with the pillar.

A first embodiment is described with reference to Figs. 1-7. Fig. 1 illustrates a semiconductor wafer fragment 10 comprised of a bulk monocrystalline silicon substrate 12 and a spaced pair of field oxide regions 14. Regions 14 define active area 15 therebetween. A series of four wordline construction 16, 17, 18 and 19 are provided relative to substrate 12. In the depicted cross-sectional view of wafer fragment 10, wordlines 16 and 19 overlie the opposing field oxide regions 14, and wordlines 17 and 18 constitute a pair of

wordlines which overlie active area 15. Wordlines 16, 17, 18 and 19 respectively comprise a gate dielectric layer 20, an overlying conductively doped polysilicon layer 21, an associated silicide layer 22, electrically insulative sidewall spacers 23, and a cap 24. Such can be provided of conventional construction, with spacers 23 and cap 24 for example comprising an oxide, nitride or other electrically insulative material. For purposes of the continuing discussion, the subject wordlines respectively have an outermost conductive surface 25 which in the preferred embodiment is the topmost surface of refractory silicide layer 22. Conductively doped diffusions regions 26, 27 and 28 are provided within substrate 12 alternatingly adjacent wordlines 17 and 18 as shown, and constitute respective first, second and third active area node locations to which respective electrical connection will be made.

An insulating dielectric material layer 30, preferably borophosphosilicate glass (BPSG), is provide over the wordlines and node locations. In this embodiment, insulating dielectric layer 30 is planarized to have a planarized outer surface 29, and provided to have a preferred thickness above node locations 26, 27 and 28 of from about 8,000 Angstroms to about 12,000 Angstroms. An example thickness of layer 30 above the outermost portion of caps 24 of wordlines 16 and 19 is about 4,500 Angstroms. If desired, a thin barrier layer (not shown), such as undoped SiO_2 deposited by decomposition of tetraethylorthosilicate or a silicon nitride layer, can be provided over the substrate prior to deposition of layer 30 to serve as a shield to undesired boron or phosphorous diffusion from BPSG layer 30 into substrate 12.

A hard mask or etch stop layer 31 is provided outwardly of insulating dielectric layer 30. Such preferably comprises a material to which underlying insulating dielectric layer 30 can be substantially selectively etched, as will be apparent from the continuing description. Example and preferred materials for layer 31 include doped or undoped polysilicon, or Si_3N_4. An example thickness for layer 31 is 2500 Angstroms.

Referring to Fig. 2, contact openings 32, 33 and 34 are etched into hard mask layer 31 and insulating dielectric material layer 30. Contact opening 32 constitutes a first contact opening etched over first node location 26. Contact opening 33 constitutes a second contact opening etched over second node location 27. Contact opening 34 constitutes a third contact opening 34 etched over third node location 28. Each is etched into insulating dielectric layer 30 to a degree which is insufficient to outwardly expose the underlying respective

node locations. An example preferred etch depth into layer 30 is 3,500 Angstroms. Contact openings 32, 33 and 34 include first, second and third contact bases 35, 36 and 37, respectively, which are positioned elevationally outward of wordlines 16, 17, 18, 19 and their associated outermost conductive surfaces 25.

Referring to Fig. 3, a spacer layer 40 is provided over masking layer 31, and accordingly over insulating dielectric material 30, to a suitable thickness which less than completely fills the respective contact openings 32, 33 and 34. Such will be utilized to ultimately produce electrically conductive anisotropically etched sidewall spacers. Example and preferred materials for layer 40 at this point in the process include either doped or undoped polysilicon.

Referring to Fig. 4, spacer layer 40 is anisotropically etched to form a first sidewall spacer 42 within first contact opening 32, a second sidewall spacer 43 within second contact opening 33, and a third sidewall spacer 44 within third contact opening 34. Such sidewall spacers are ultimately rendered to be electrically conductive and constitute laterally outward portions of an electrically conductive contact pedestal. Accordingly, where spacer layer 40 is provided to be electrically conductive prior to the anisotropic etching to produce the construction of Fig. 4, spacers 42, 43 and 44 will be electrically conductive immediately upon their formation. Where spacer layer 40 is not provided to be electrically conductive prior to the Fig. 4 anisotropic etching, spacers 42, 43 and 44 can be rendered electrically conductive after their formation by diffusion doping, ion implant, or some other method.

Referring to Fig. 5, and after etching anisotropic spacer layer 40, etch chemistry is changed to etch through first, second and third contact opening bases 35, 36, and 37, respectively, to outwardly expose node locations 26, 27 and 28, respectively. During such etching, hard mask or etch stop layer 31 restricts etching of insulating dielectric material layer 30 thereunder. If sidewall spacers 23 of the subject wordline constructions constitute nitride, as in this example, such layers are preferably not appreciably etched during the etching of BPSG layer 30. If the material of spacers 23 comprises oxide, such material will more typically be etched during the etch of layer 30 to outwardly expose the node locations, but this should not be problematic. Provision of the illustrated spacers 42, 43 and 44 within contact openings 32, 33, and 34 desirably has the effect of moving the resultant narrowed contact etch to the node locations away from the conductive wordline edges such that exposure thereof will not occur during

the etch to expose the node locations. Accordingly, spacers 23 and cap 24 are not a preferred embodiment requirement.

Referring to Fig. 6, remaining first, second, and third contact openings 32, 33, 34, respectively, are filled with an electrically conductive material layer 46, such as *in situ* conductively doped polysilicon.

Referring to Fig. 7, electrically conductive material layer 46 is etched inwardly to insulating dielectric material layer 30 to form an electrically conductive first contact pedestal 48, an electrically conductive second contact pedestal 50, and an electrically conductive third contact pedestal 52. Each comprises an inner longitudinal portion 53 effectively in electrical connection with the associated node location, and an outer longitudinal portion 54. Outer longitudinal portion 54 for pedestals 48, 50 and 52 comprises anisotropically etched spacers 42, 43, and 44, respectively, and a radially inner electrically conductive pillar 56. Spacers 42, 43 and 44 are in respective ohmic electrical connection with their associated pillars 56, with pillars 56 comprising and extending between outer longitudinal portion 54 and inner longitudinal portion 53 of the respective contact pedestals. Example and preferred etching techniques include chemical-mechanical polishing (CMP) or blanket plasma etch.

Such produces respective pedestal outer surfaces 58 which are substantially coplanar with planar insulating dielectric layer surfaces 29, with individual outer surfaces 58 constituting a substantially coplanar common outer surface with respect to the individual pillars and spacers. Such a construction and method further produces pedestal caps 60 of radially wider construction than longitudinal inner portions 53 of the contact pedestals, with such caps 60 having a substantially common longitudinal thickness "A". In the depicted and preferred embodiment, the distance between the respective contact bases and their associated node locations is shown to be constant at dimension "C". The thickness of insulating material over outermost conductive surfaces 25 of wordlines 17 and 18 to the contact opening bases is depicted with dimension "B". Most preferably, "A" and "B" are each greater than or equal to 0.1 micron.

Fig. 8 illustrates subsequent wafer processing, whereby capacitor constructions 87 and 88 are provided in electrical connection with pedestals 48 and 52, and a bit line 89 is provided in electrical connection with pedestal 50. An insulating layer 90 is provided outwardly of layer 30 and pedestals 48, 50 and 52. Capacitor container openings are provided through layer 90 to pedestals 48 and 52. Capacitor storage nodes 91 are provided therein. Layer 90 is

etched to expose the outer lateral sidewalls of nodes 91. A cell dielectric layer 92 and a cell plate layer 93 are provided over the substrate. A subsequent insulating layer 94 is provided. A contact plug 95 is provided through layers 94 and 90 to pedestal 50. Bit line 89 is provided in electrical connection with plug 95 for DRAM circuitry fabrication.

An alternate embodiment is described with reference to Figs. 9-13. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "a" or with different numerals. Fig. 9 depicts an alternate embodiment wafer fragment 10a which is essentially the same as that depicted by Fig. 1, but for elimination of hard mask layer 31 and increased thickness of layer 30a. An example thickness for layer 30a is from about 20,000 Angstroms to about 25,000 Angstroms.

Referring to Fig. 10, such is similar to Fig. 4 of the first described embodiment, with there being no associated masking layer 31. Further, contact openings 32a, 33a and 34a are provided deeper relative to insulating dielectric layer 30a, with the associated spacers 42a, 43a and 44a being substantially thicker. Such is represented by dimension "F". Further, the anisotropic etching to produce such spacers effectively outwardly exposes insulating dielectric material of layer 30 over the wordlines, wherein such was capped from such exposure by layer 31 in the first described embodiment.

Referring to Fig. 11, the step of collectively etching through the respective first, second and third contact opening bases of the first described embodiment also etches insulating dielectric material 30a over the illustrated wordlines, but to a degree insufficient to outwardly expose conductive surfaces 25 of such wordlines. Further, "D" is less than "F" preferably by from 0.1 micron to 0.3 micron. The illustrated dimension "E" from the contact opening base of the highest contact opening to its associated node location will be less than the dimension "D" etch of layer 30a above the wordlines. A more preferred relationship is to have "D" greater than or equal to about 1.3E. Most preferred is for "D" to be equal to from about 1.3E to about 1.5E.

Referring to Fig. 12, an electrically conductive material layer 46a is once again deposited to fill the remaining first, second and third contact openings to the respective node locations.

Referring to Fig. 13, etching is conducted to produce the illustrated contact pedestals 48, 50 and 52.

Fig. 14 illustrates yet another modified embodiment. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "b" or with different numerals. Fig. 14 differs principally from the first described embodiment in that outer surface 29b of insulating dielectric layer 30b is initially provided to be unplanarized. Accordingly, masking layer 31b provided thereover is also unplanarized. With such example, a preferred deposited thickness for layer 30b is greater than or equal to 14,000 Angstroms. Processing of the Fig. 14 wafer fragment would then occur as above, with an etching step being conducted to produce the desired electrically conductive contact pillars.

Yet another alternate embodiment is described with reference to Figs. 15 and 16. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "c" or with different numerals. Fig. 15 is similar to the Fig. 14 depiction, but eliminates provision of the masking layer 31/31b and provides a thicker layer 30c. In such instance, the preferred deposited thickness of deposited layer 30c is greater than or equal to about 24,000 Angstroms.

Referring to Fig. 16, the etch of BPSG layer 30c is conducted preferably as a timed etch down to approximately 2000 to 3000 Angstroms above conductive outer surfaces 25 of the wordlines. Most preferably, the thickness of nitride caps 24 in such embodiment where provided is equal to about 2,000 Angstroms. Subsequently, layer 46c is deposited. An etch would then be constructed to produce the same essential construction of Fig. 7.

Yet another alternate embodiment is described with reference to Figs. 17 and 18. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "d" or with different numerals. Fig. 17 depicts an embodiment whereby insulating dielectric layer 30d is subjected to a planarizing etch, such as CMP, initially to stop atop the outer caps 24 of the outermost wordlines, with such effectively functioning as etch stop caps. Accordingly, such caps should be of a different material than layer 30d to facilitate or provide the desired planarizing etch stopping function. Insulating layer 31d is subsequently provided.

Fig. 18 illustrates subsequent processing in accordance with the above preferred embodiments, whereby conductive material is provided within the contact openings immediately prior to etching thereof, which will ultimately produce the desired conductive contact pedestals isolated from one another. Such etch can

again be an anisotropic dry etch, an isotropic wet etch, or chemical-mechanical polishing.

Yet another alternate embodiment is described with reference to Figs. 19-23. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "e" or with different numerals. In wafer fragment 10e, wordline 16e, 17e, 18e and 19e are provided without provision of any separate insulating material caps. Such caps could of course also be eliminated in the Figs. 1 - 16 described embodiments, with the invention only being limited by the accompanying claims. Elimination of the caps facilitates reduction in topology to be planarized, and facilitates reduction of what would otherwise be required for the thickness insulating layer 30 - 30e. Such layer in this described embodiment is preferably deposited to a thickness of from about 25,000 Angstroms to about 30,000 Angstroms. Contact openings 32e, 33e and 34e are etched as shown, with their depth penetration relative to insulating dielectric layer 30e preferably being between about 6,000 Angstroms and 12,000 Angstroms to provide a depth below the lowest topology of the outer portion of circuitry peripheral to the figure.

Fig. 20 shows wafer fragment 10e at the processing step substantially equivalent in sequence to that depicted by Fig. 6 in the first described embodiment.

Referring to Fig. 21, the electrically conductive pillar material within contact openings 32, 33, and 34, as well as their associated spacers and surrounding insulating material, is etched as shown. Such etching preferably uses an etch chemistry which etches all such materials at substantially the same rate to produce the illustrated capacitor container openings 70 and 72 over or relative to node locations 26 and 28. Such effectively provides conductive pillars 74 and 76 which project or extend respectively from the bases of contact openings 74 and 76 to the associated node locations 26 and 28, respectively. An example chemistry which will produce the illustrated anisotropic etch and etch polysilicon and BPSG at substantially the same rate would include NF_3, or a combination of CF_4 plus CHF_3. Alternately and by way of example only, polysilicon and BPSG can be etched sequentially using a first etch chemistry of SF_6 and Cl_2 followed by a second etch chemistry of CF_4, CHF_3 and Ar.

Referring to Fig. 22, a second layer 78 of electrically conductive material, preferably conductively doped polysilicon, is provided outwardly of etch stop layer 31e (and accordingly insulating dielectric layer 30e) and to within capacitor

container openings 70 and 72 to a thickness which less than completely fills such openings.

Then, referring to Fig. 23, etching is conducted relative to both second electrically conductive layer 78 and first electrically conductive layer 46e. This, effectively in the same step, defines contact pedestal 50 and an isolated capacitor storage node 80 within capacitor container opening 70 and an isolated capacitor storage node 82 with capacitor container opening 72. In accordance with preferred aspects of the invention, such can be utilized as a capacitor container storage node in fabrication of DRAM circuitry. The preferred etching by which the Fig. 23 construction is achieved is chemical-mechanical polishing.

The above described embodiments enable improvements in pedestal constructions over prior art constructions. For example with respect to my earlier 5,338,700 patent, the construction there disclosed if using 0.75 micron pitch technology would have an oval shaped base having a length of 0.5 microns and a width of 0.25 microns, and a substantially circular top of 0.5 micron diameter. This is in part due to the self-aligned contact etch which produces the illustrated plugs. Preferred pedestal constructions in accordance with the invention can have a pedestal base and a pedestal top which are both substantially circular, with the top having a diameter of 0.5 micron and the base having a diameter of 0.25 micron for 0.75 micron pitch technology. A self-aligned contact etch is not required.

For example, Fig. 24 depicts a diagrammatic top view of contact pedestal 99 having an outer longitudinal portion 54f and inner longitudinal portion 53f. As shown, both are substantially circular in radial cross section, with outer portion 54f being larger (twice as large) in radial cross section than inner portion 53f.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS

1. A semiconductor processing method of forming a contact pedestal comprising the following steps:

providing a node location to which electrical connection is to be made;

providing insulating dielectric material over the node location;

etching a contact opening into the insulating dielectric material over the node location to a degree insufficient to outwardly expose the node location, the contact opening having a base;

providing a spacer layer over the insulating dielectric material to within the contact opening to a thickness which less than completely fills the contact opening;

anisotropically etching the spacer layer to form a sidewall spacer within the contact opening;

after forming the sidewall spacer, etching through the contact opening base to outwardly expose the node location;

filling the contact opening to the node location with electrically conductive material;

rendering the sidewall spacer electrically conductive; and

etching the electrically conductive material to form an electrically conductive contact pedestal comprising the sidewall spacer, the pedestal having an outer surface which is substantially coplanar with opposing laterally adjacent electrically insulative surfaces.

2. The semiconductor processing method of forming a contact pedestal of claim 1 wherein the spacer layer is provided to be electrically conductive prior to the anisotropic etching thereby rendering the spacer to be electrically conductive immediately upon its formation.

3. The semiconductor processing method of forming a contact pedestal of claim 1 wherein the spacer layer is not provided to be electrically conductive prior to the anisotropic etching, the spacer being rendered electrically conductive after the anisotropic etching.

4. The semiconductor processing method of forming a contact pedestal of claim 1 wherein the insulating dielectric material includes an outermost surface, the outermost surface being substantially unplanarized prior to the etching step to form the pedestal.

5. The semiconductor processing method of forming a contact pedestal of claim 1 wherein the insulating dielectric material includes an outermost surface, the outermost surface being substantially planar prior to the etching step to form the pedestal.

6. The semiconductor processing method of forming a contact pedestal of claim 1 wherein the insulating dielectric material includes an outermost surface, the outermost surface being substantially unplanarized prior to the etching step to form the pedestal, an unplanarized masking layer being provided over the unplanarized insulating dielectric material outermost surface prior to the etching step to form the pedestal.

7. The semiconductor processing method of forming a contact pedestal of claim 1 further comprising:

providing a capacitor container opening and a second layer of electrically conductive material over the insulating dielectric layer and to within the capacitor container opening to a thickness which less than completely fills the capacitor container opening; and

the etching step to form the pedestal also including etching the second layer of conductive material to define an isolated capacitor storage node plate within the capacitor container opening.

8. The semiconductor processing method of forming a contact pedestal of claim 1 further comprising:

providing a second node location and a second contact opening into the insulating dielectric layer over the second node location, the second contact opening being insufficiently deep to outwardly expose the second node location, the second contact opening having a second base;

the spacer layer also being provided within the second contact opening and the anisotropic etching thereof providing a second spacer within the second contact opening;

after forming the second sidewall spacer, etching through the second contact opening base to outwardly expose the second node location;

filling the second contact opening to the second node location with the electrically conductive material;

before the etching step to form the pedestal, etching the insulating dielectric material and the conductive material filling the second contact opening to form a capacitor container opening over the second node location and a pillar of conductive material extending between the capacitor container opening and the second node location;

providing a second layer of electrically conductive material over the insulating dielectric layer and to within the capacitor container opening to a thickness which less than completely fills the capacitor container opening; and

the etching step to form the pedestal also including etching the second layer of conductive material to define an isolated capacitor storage node plate within the capacitor container opening.

9. The semiconductor processing method of forming a contact pedestal of claim 8 wherein the etching to form the capacitor container contact opening is conducted to etch the insulating dielectric material and the conductive material filling the second contact opening at substantially the same rate.

10. A semiconductor processing method of forming a contact pedestal comprising the following steps:

providing a pair of wordlines having a node location therebetween to which electrical connection is to be made;

providing insulating dielectric material over the pair of wordlines and the node location;

etching a contact opening into the insulating dielectric material over the node location to a degree insufficient to outwardly expose the node location between the pair of wordlines, the contact opening having a base positioned elevationally outward of conductive portions of the pair of wordlines;

providing a spacer layer over the insulating dielectric material to within the contact opening to a thickness which less than completely fills the contact opening;

anisotropically etching the spacer layer to form a sidewall spacer within the contact opening and to outwardly expose the insulating dielectric material over the pair of wordlines;

after forming the sidewall spacer, etching through the contact opening base to outwardly expose the node location between the pair of wordlines, the step of etching through the contact opening base also etching insulating dielectric material over the pair of wordlines but to a degree insufficient to outwardly expose the pair of wordlines;

filling the contact opening to the node location with electrically conductive material;

rendering the sidewall spacer electrically conductive; and

etching the electrically conductive material to form an electrically conductive contact pedestal comprising the sidewall spacer, the pedestal having an outer surface which is substantially coplanar with opposing laterally adjacent electrically insulative surfaces.

11. The semiconductor processing method of forming a contact pedestal of claim 10 wherein the spacer layer is provided to be electrically conductive prior to the anisotropic etching thereby rendering the spacer to be electrically conductive immediately upon its formation.

12. The semiconductor processing method of forming a contact pedestal of claim 10 wherein the spacer layer is not provided to be electrically conductive prior to the anisotropic etching, the spacer being rendered electrically conductive after the anisotropic etching.

13. The semiconductor processing method of forming a contact pedestal of claim 10 wherein the insulating dielectric material includes an outermost surface, the outermost surface being substantially unplanarized prior to the etching step to form the pedestal.

14. The semiconductor processing method of forming a contact pedestal of claim 10 wherein the quantity of insulating material etched over the pair of wordlines during the step of etching through the contact opening base is greater than or equal to at least about 1.3 times the distance between the contact base and the node location.

15. The semiconductor processing method of forming a contact pedestal of claim 10 wherein the quantity of insulating material etched over the pair of wordlines during the step of etching through the contact opening base is equal to from about 1.3 to 1.5 times the distance between the contact base and the node location.

16. A semiconductor processing method of forming a storage node of a capacitor comprising the following steps:

providing an electrically conductive pillar within a mass of insulating material;

etching the pillar and the mass of insulating material to form a capacitor container opening within the mass of insulating material, the pillar projecting from the capacitor container opening; and

providing a capacitor storage node within the capacitor container opening in electrical connection with the pillar.

17. The semiconductor processing method of claim 16 wherein the pillar and the mass of insulating material are etched at substantially the same rate.

18. Integrated circuitry comprising:

a node location;

an electrically conductive longitudinal contact pedestal in electrical connection with the node location, the contact pedestal comprising:

an inner longitudinal portion in electrical connection with the node location and an outer longitudinal portion, the outer longitudinal portion comprising an anisotropically etched sidewall spacer and a radially inner electrically conductive pillar, the spacer being electrically conductive and in electrical connection with the pillar;

the pillar and spacer having a substantially coplanar common outer surface; and

insulating dielectric material having a substantially planar outer surface which is substantially coplanar with the contact pedestal common outer surface.

19. Integrated circuitry comprising:

a pair of wordlines having a node location therebetween, the wordlines having respective conductive outermost surfaces;

an electrically conductive longitudinal contact pedestal in electrical connection with the node location, the contact pedestal comprising:

an inner longitudinal portion in electrical connection with the node location and an outer longitudinal portion, the outer longitudinal portion comprising an anisotropically etched sidewall spacer and a radially inner electrically conductive pillar, the spacer being electrically conductive and in electrical connection with the pillar, the inner portion comprising the pillar, the spacer comprising a base and having a longitudinal thickness;

the pillar and spacer having a substantially coplanar common outer surface; and

insulating dielectric material over the wordlines and having a substantially planar outer surface which is substantially coplanar with the contact pedestal common outer surface, the insulating dielectric material over the outermost conductive surfaces of the wordlines having respective thickness which is greater than or equal to a sum of, a) the distance between the spacer base and the node location, and b) the spacer longitudinal thickness.

20. Integrated circuitry comprising:

a node location;

an electrically conductive longitudinal contact pedestal in electrical connection with the node location, the contact pedestal comprising:

an inner longitudinal portion in electrical connection with the node location and an outer longitudinal portion, the outer longitudinal portion comprising an anisotropically etched sidewall spacer and a radially inner electrically conductive pillar, the spacer being electrically conductive and in electrical connection with the pillar, the inner longitudinal portion being substantially circular in radial cross section, the outer longitudinal portion being substantially circular in radial cross section and being larger in radial cross section than the inner longitudinal portion.

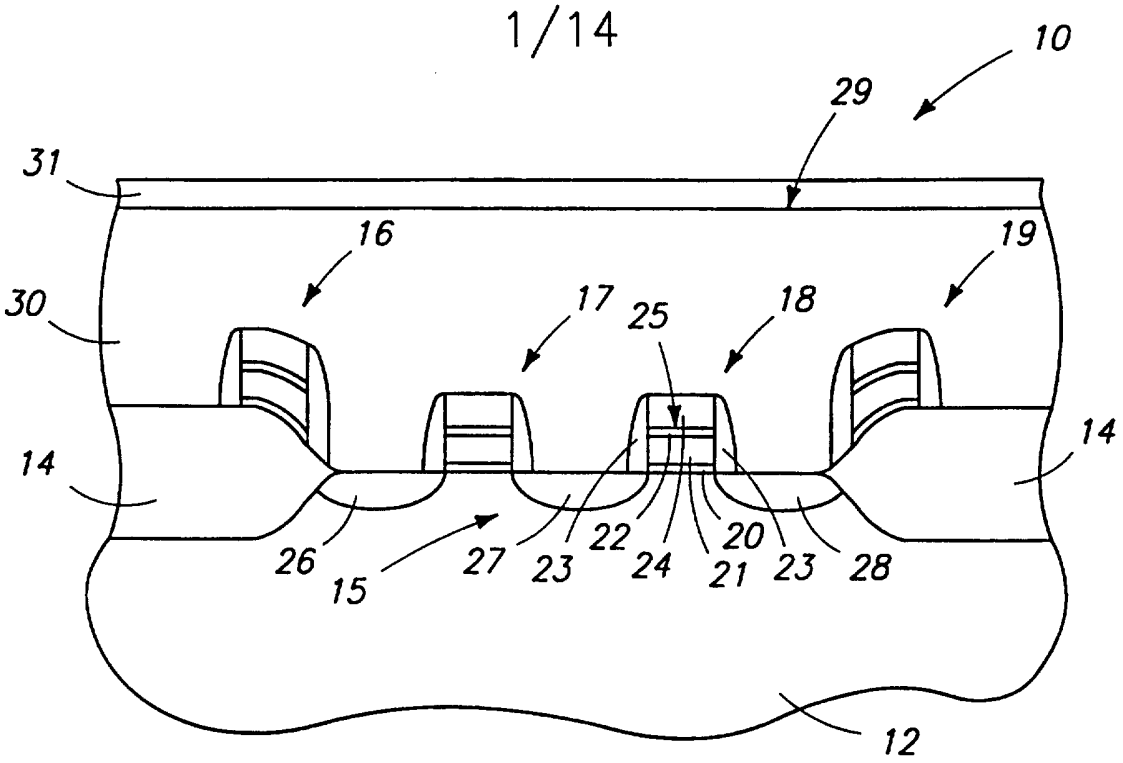
10
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Fig 1

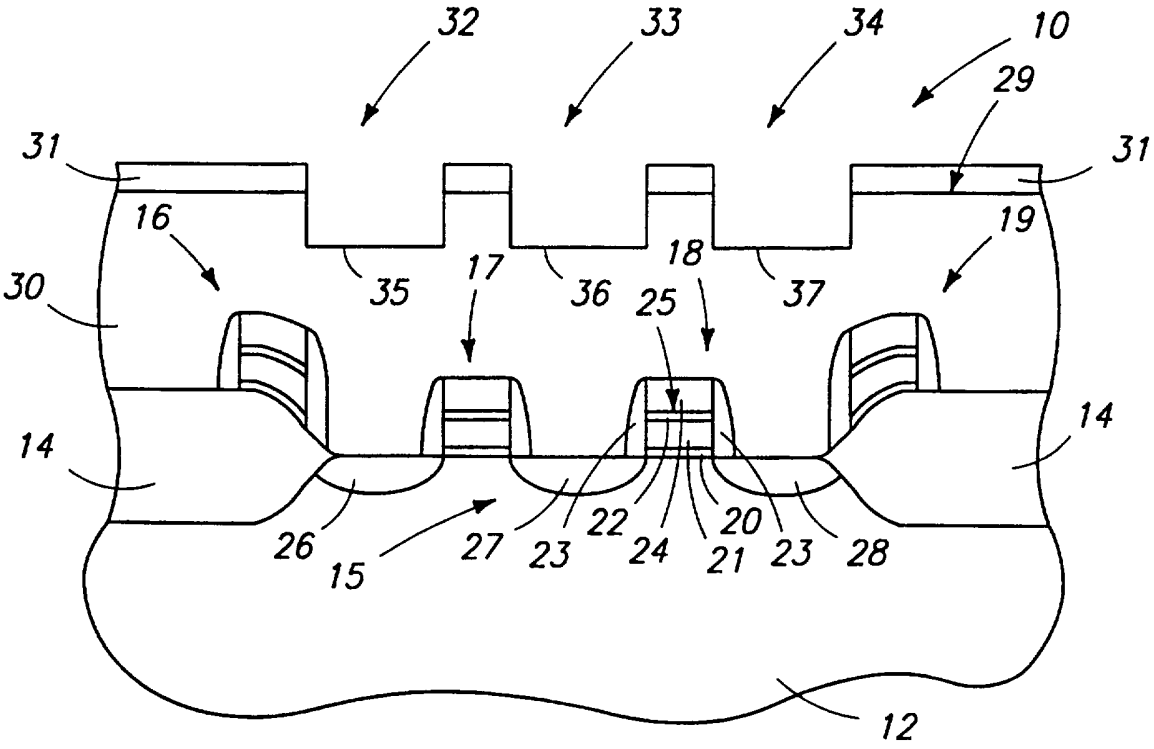
32
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Fig 2

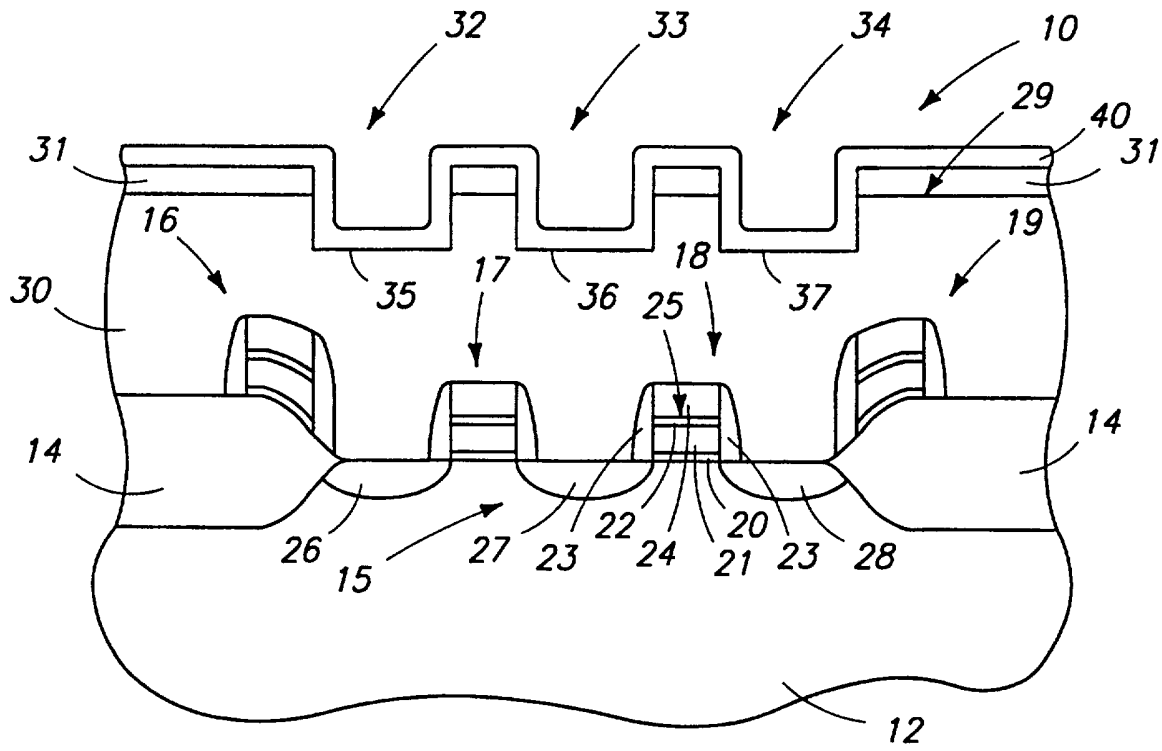
32
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Fig 3

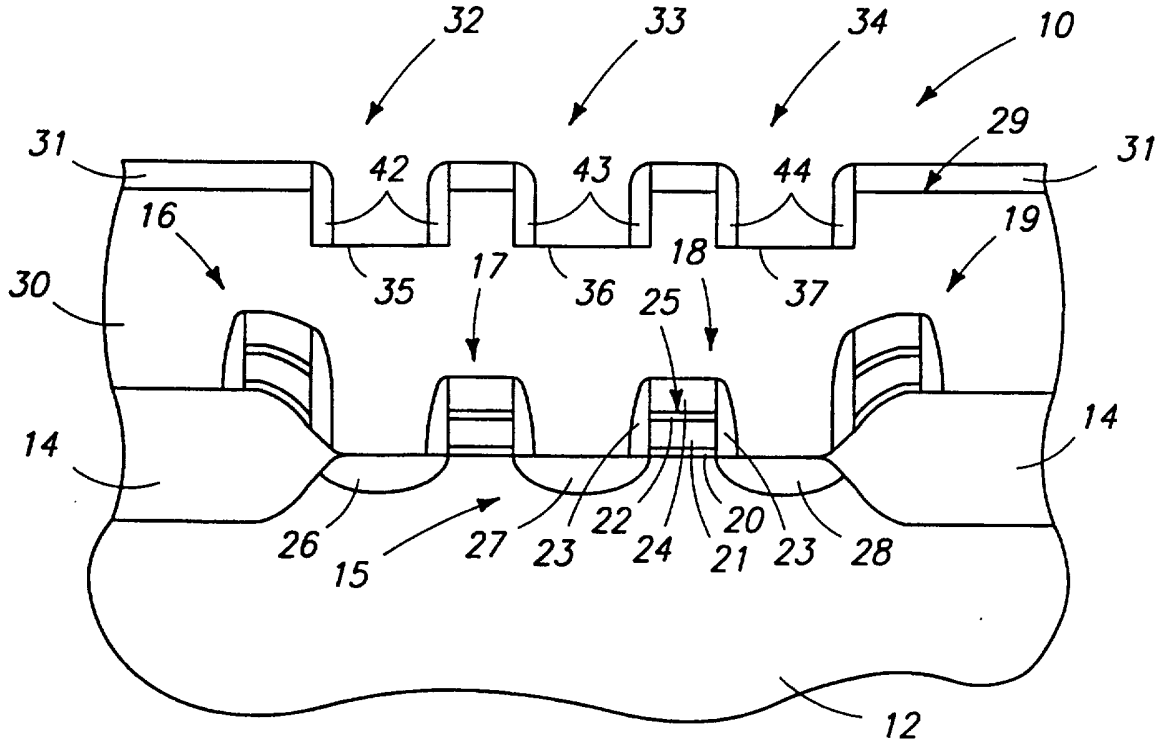
32
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Fig 4

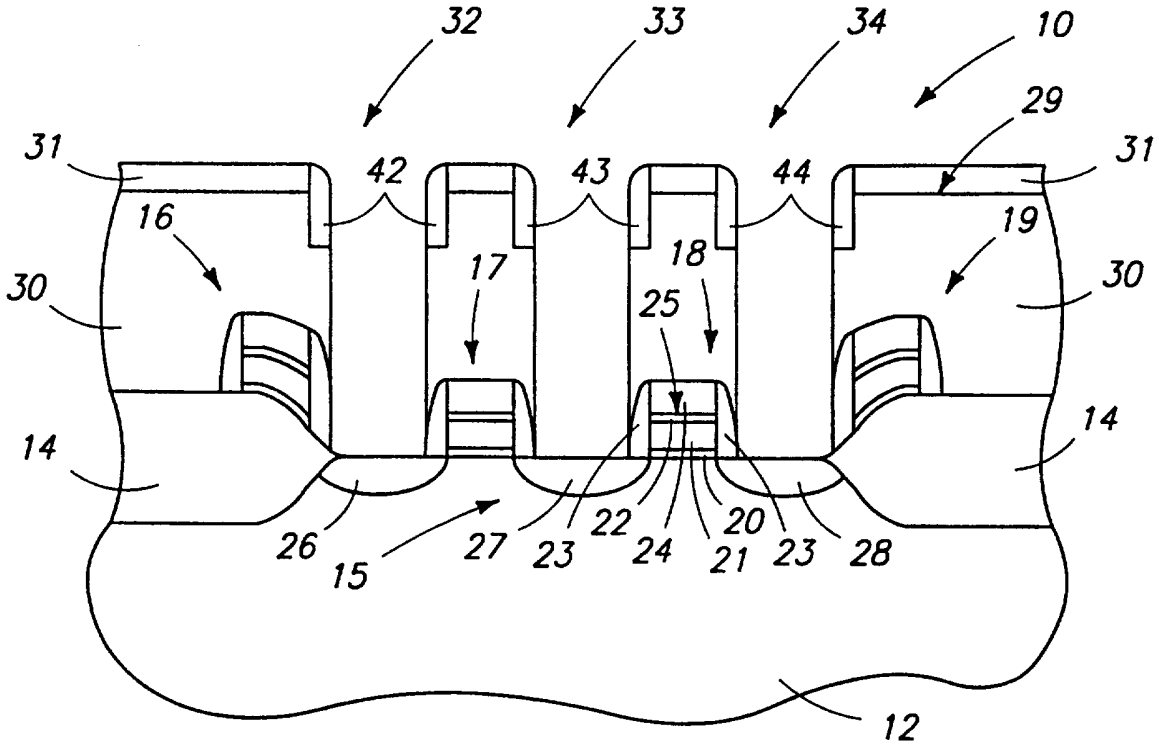
32
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Fig 5

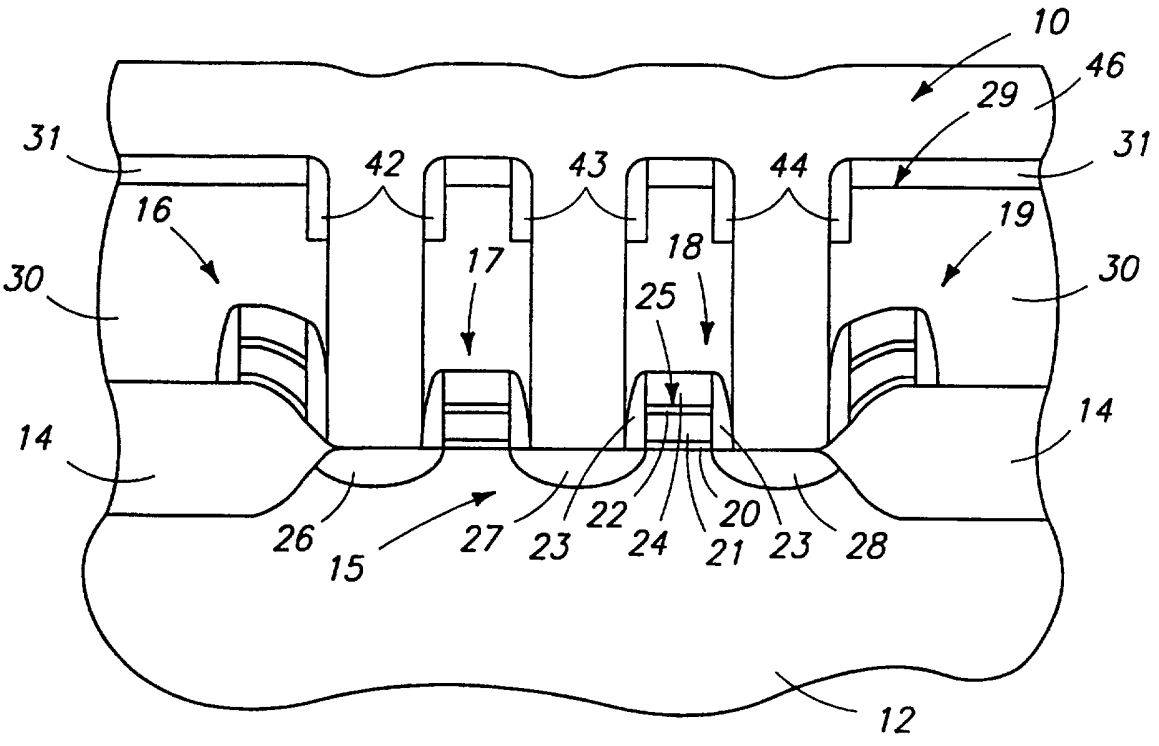
10
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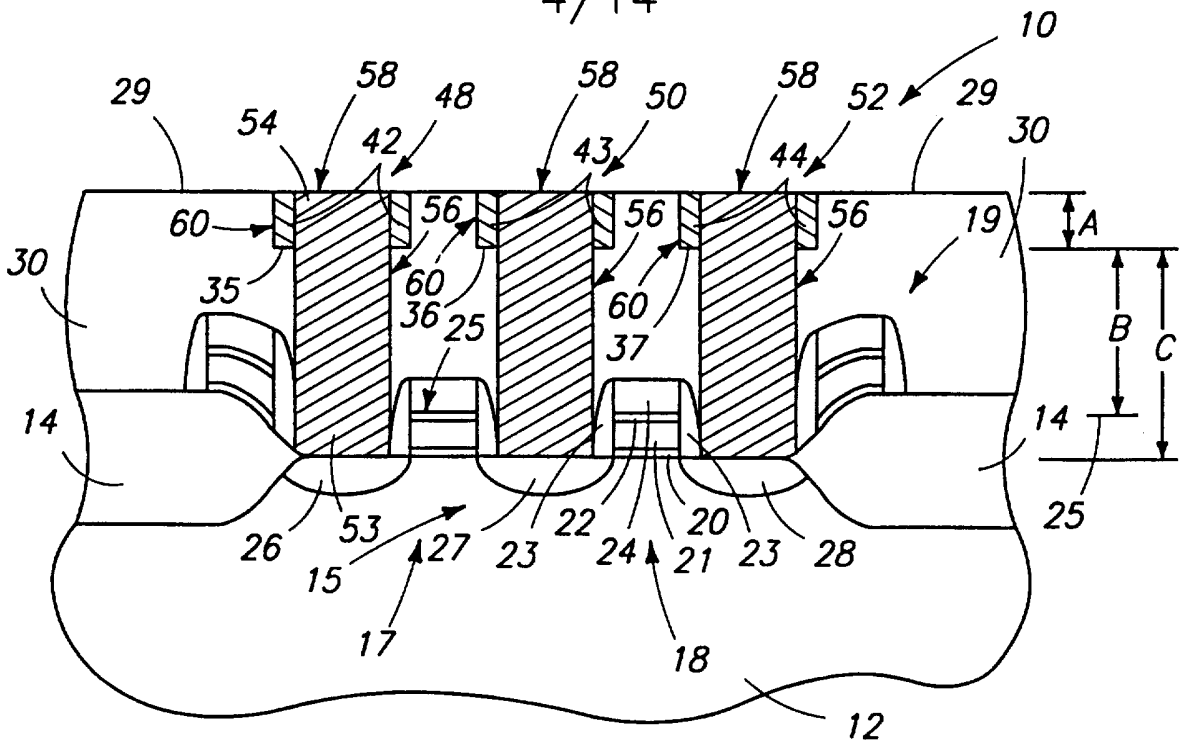
Fig 6


10
29
58
48
58
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58
52
29
54
42
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30
60
56
56
56
19
A
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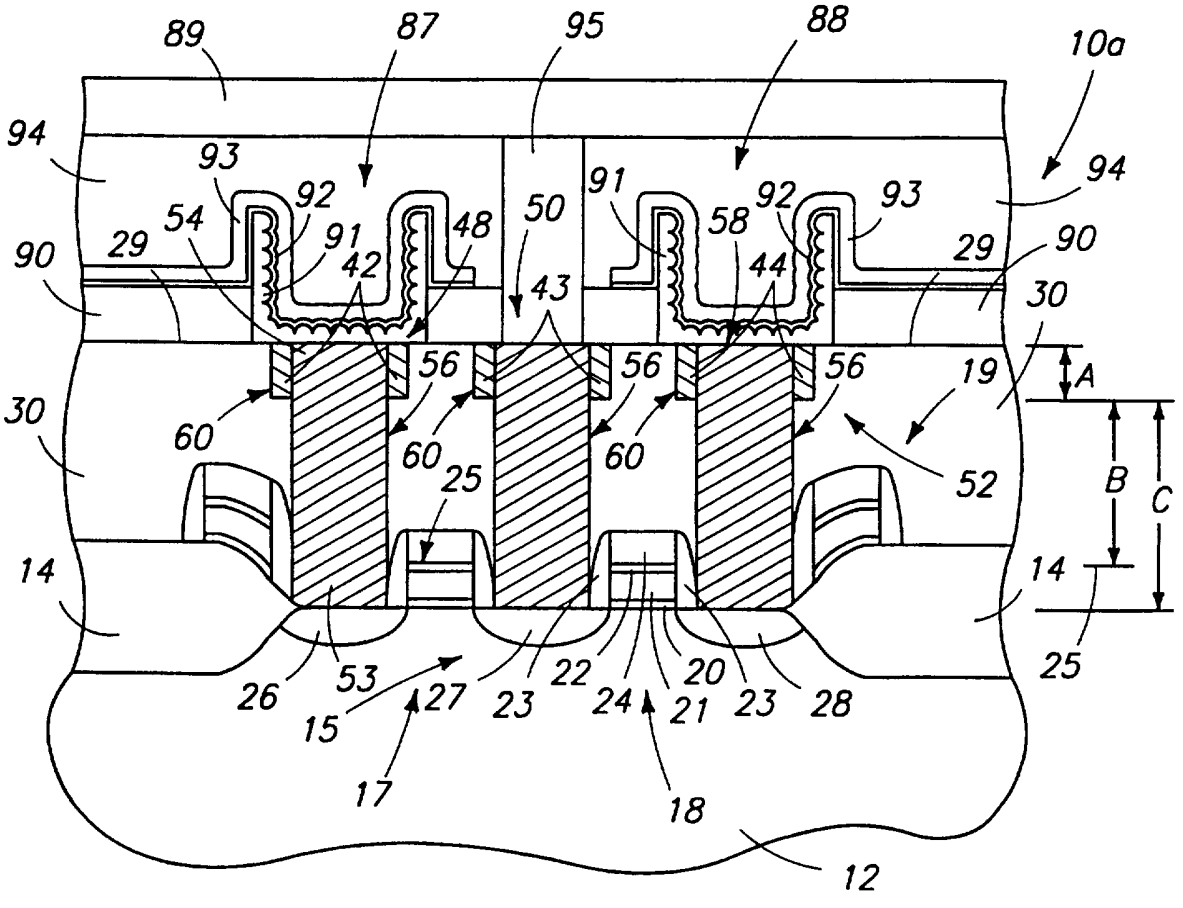
Fig 7


89
87
95
88
10a
94
93
92
91
92
93
94
54
48
50
58
90
29
91
42
43
44
29
90
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56
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A
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60
60
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B
C
14
14
25
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Fig 8

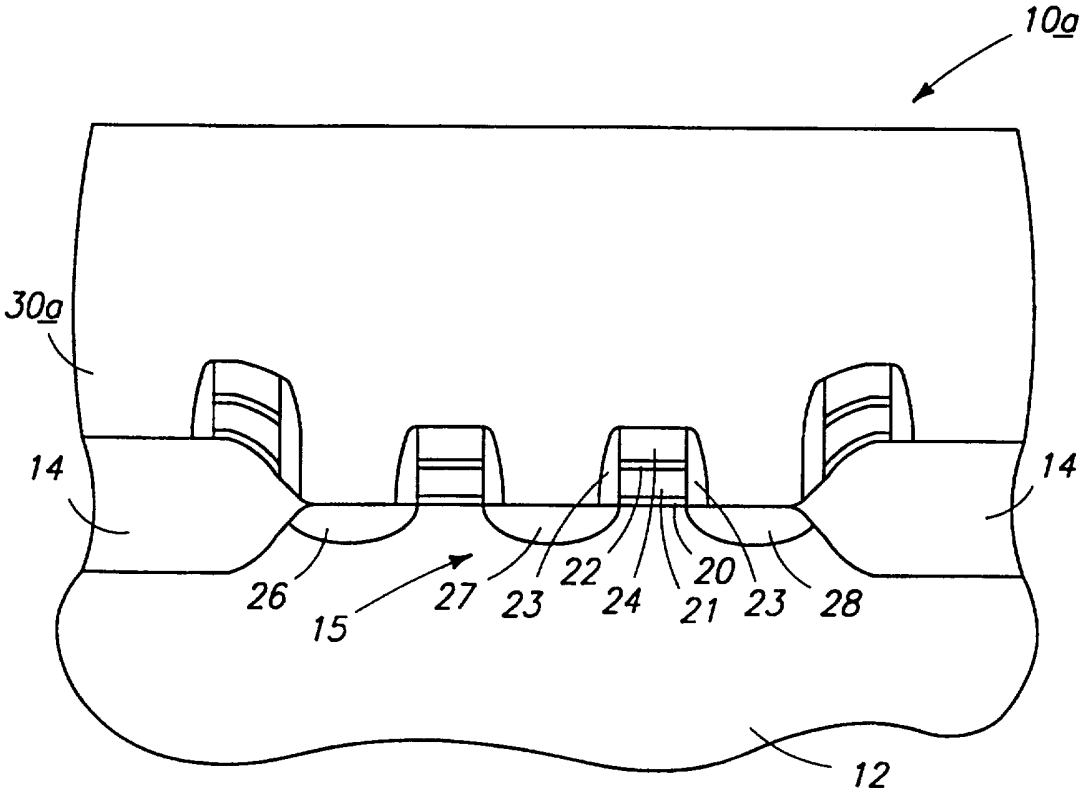

Fig 9

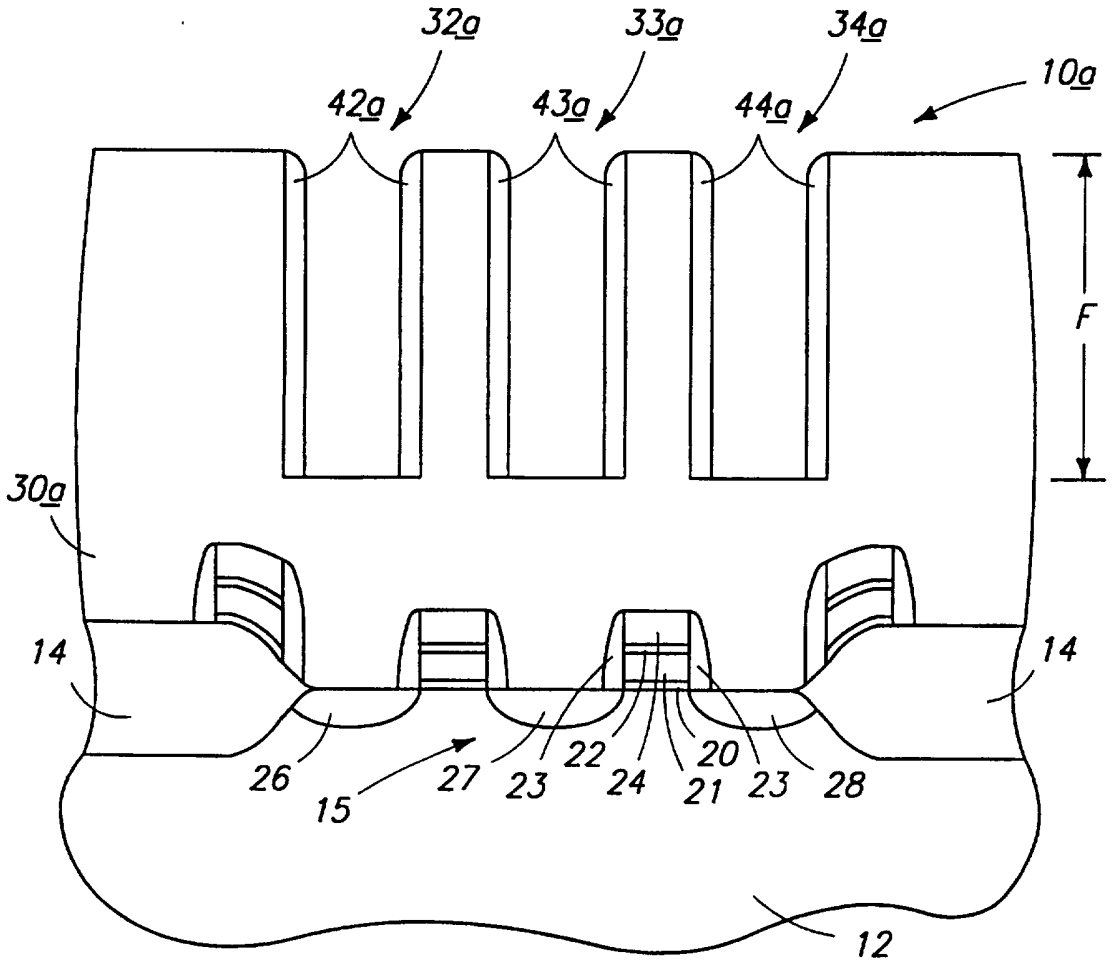
32a
33a
34a
10a
42a
43a
44a
F
30a
14
14
26
15
27
23
22
24
21
20
23
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Fig 1B

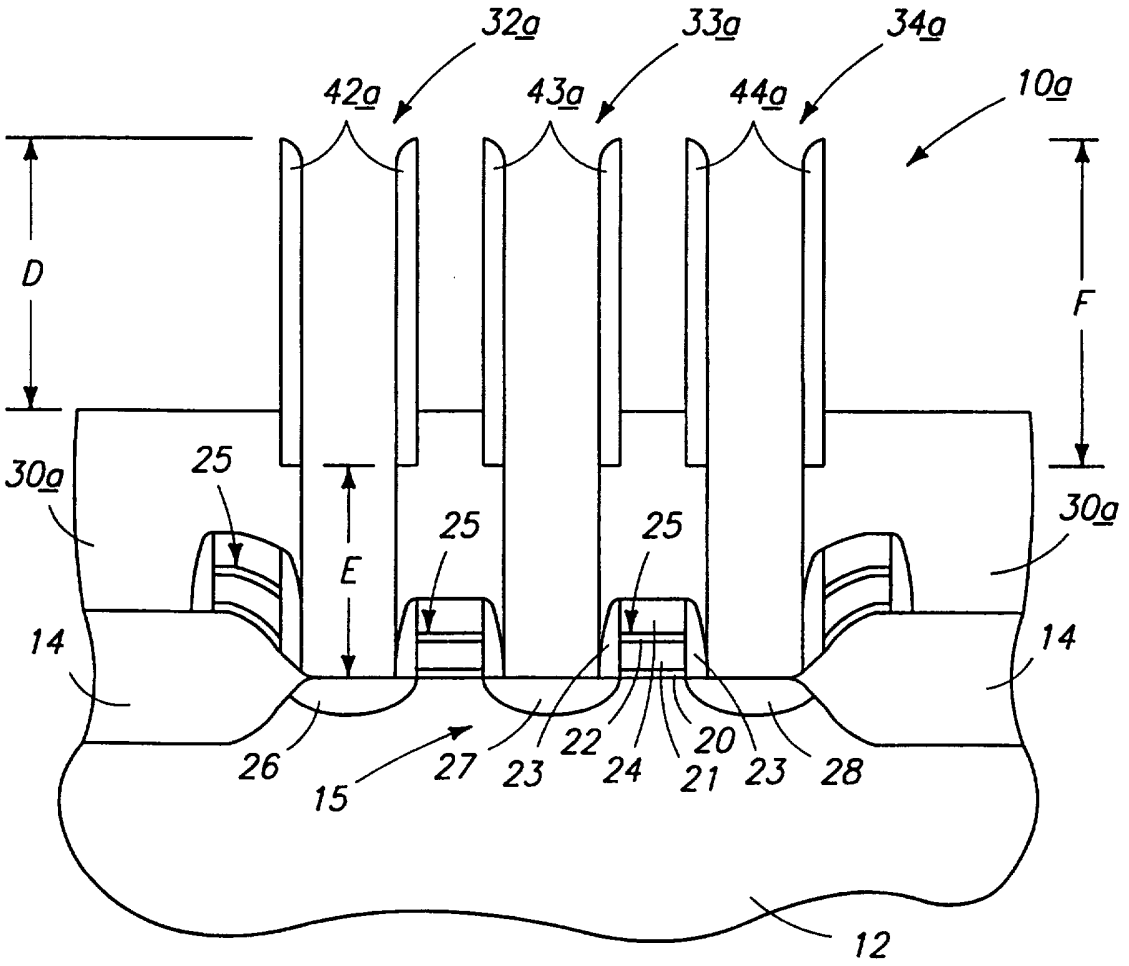
32a
33a
34a
42a
43a
44a
10a
D
F
E
30a
25
25
25
30a
14
14
26
15
27
23
22
24
21
20
23
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Fig 11

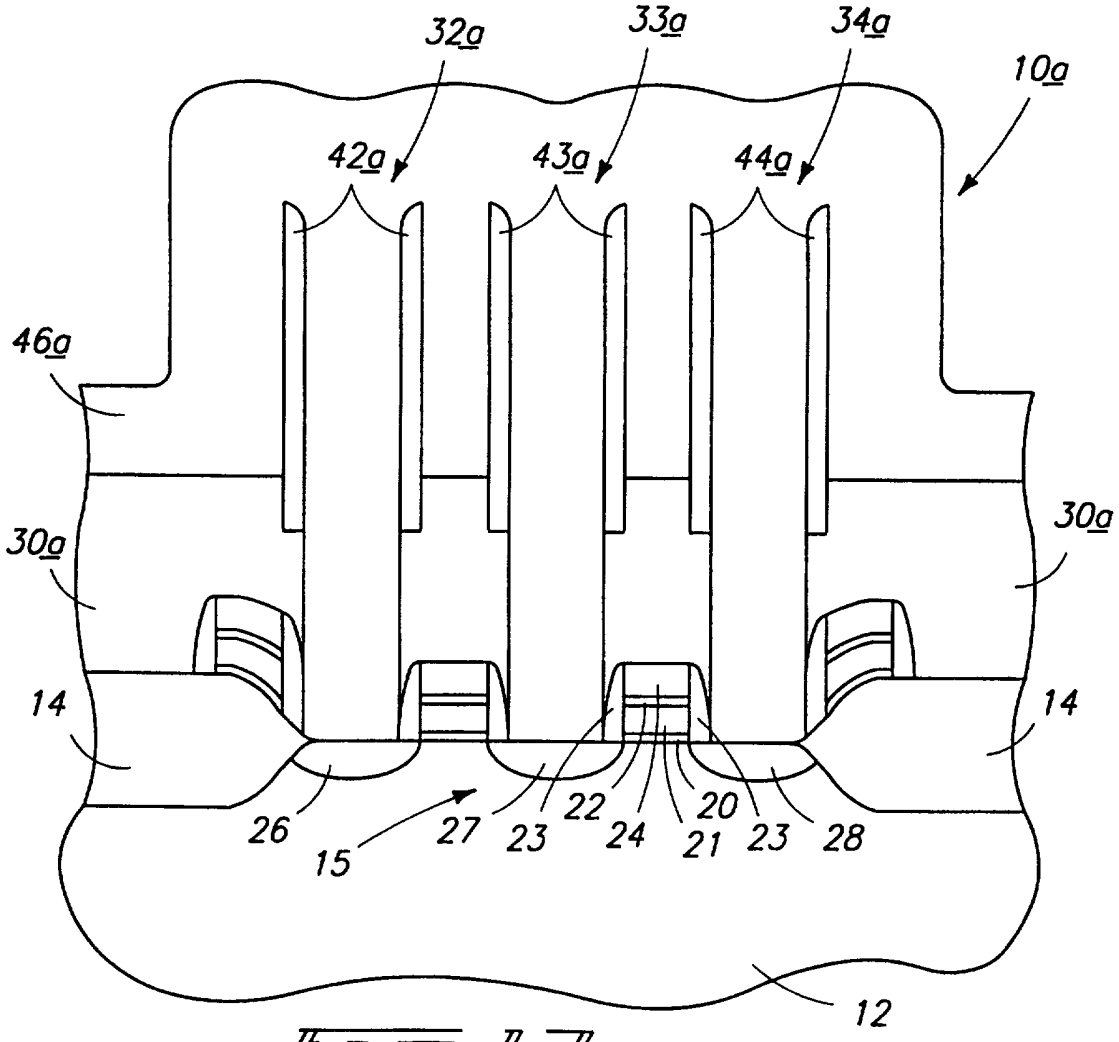
32a
33a
34a
10a
42a
43a
44a
46a
30a
30a
14
14
26
15
27
23
22
24
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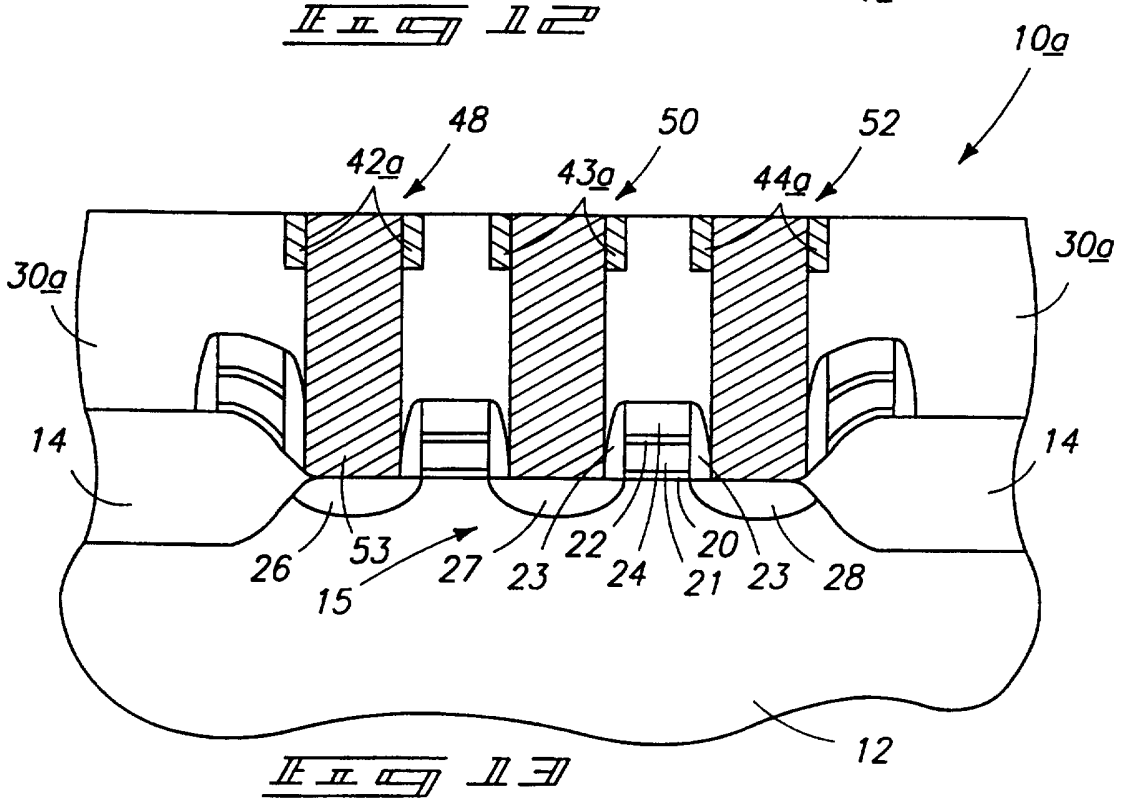
Fig 12


10a
48
50
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42a
43a
44a
30a
30a
14
14
26
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Fig 13

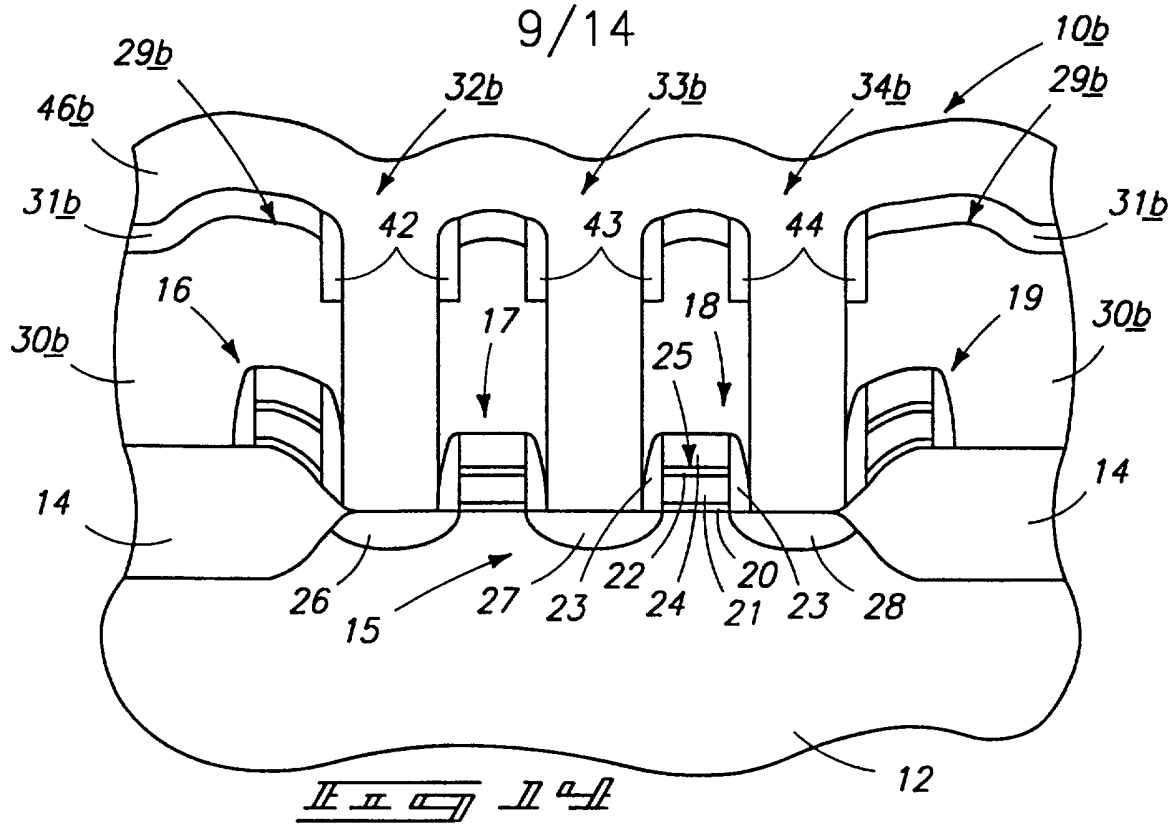
29b
32b
33b
34b
10b
29b
46b
31b
42
43
44
31b
16
17
18
19
30b
25
30b
14
14
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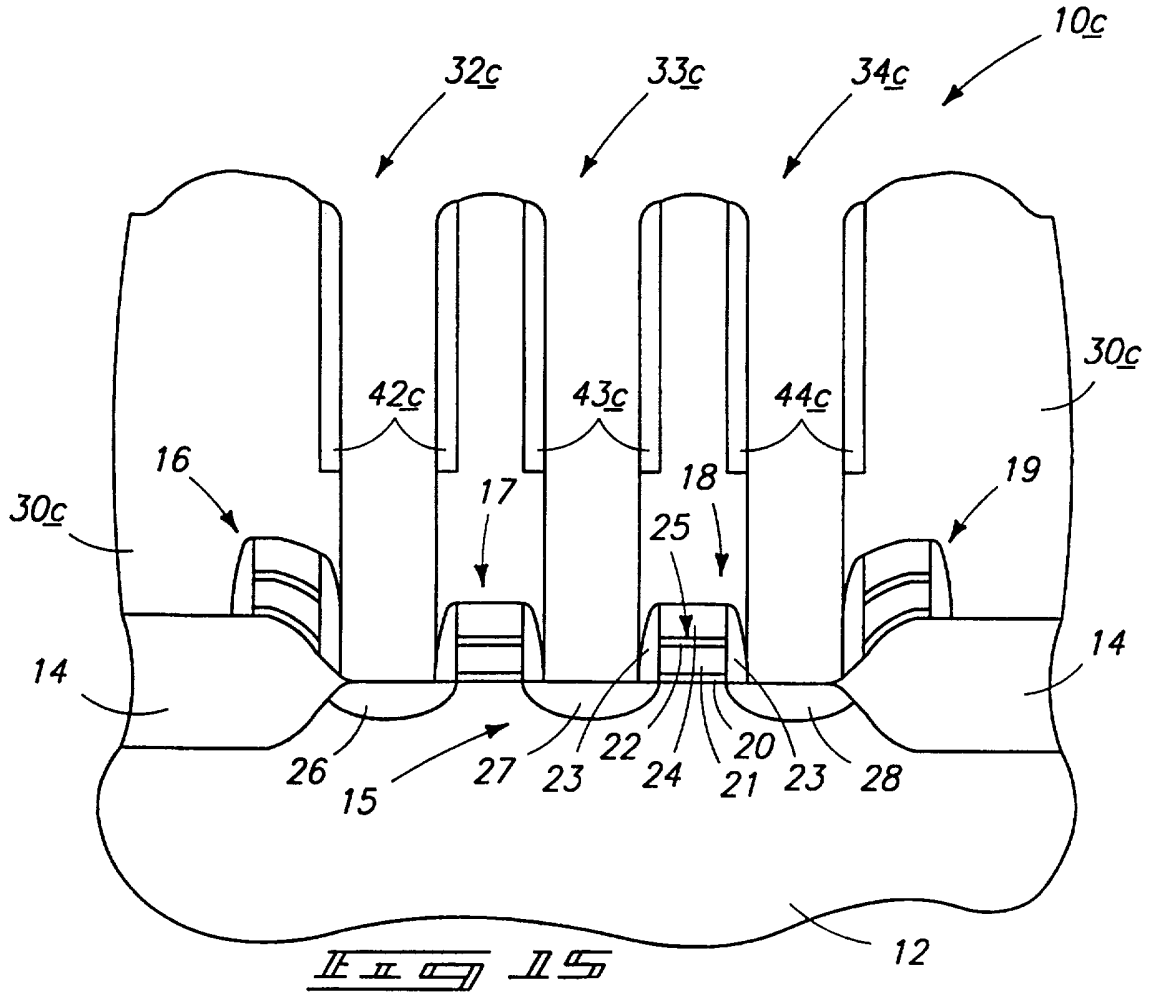
Fig 14


10c
32c
33c
34c
30c
42c
43c
44c
16
17
18
19
30c
25
14
14
26
15
27
23
22
24
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23
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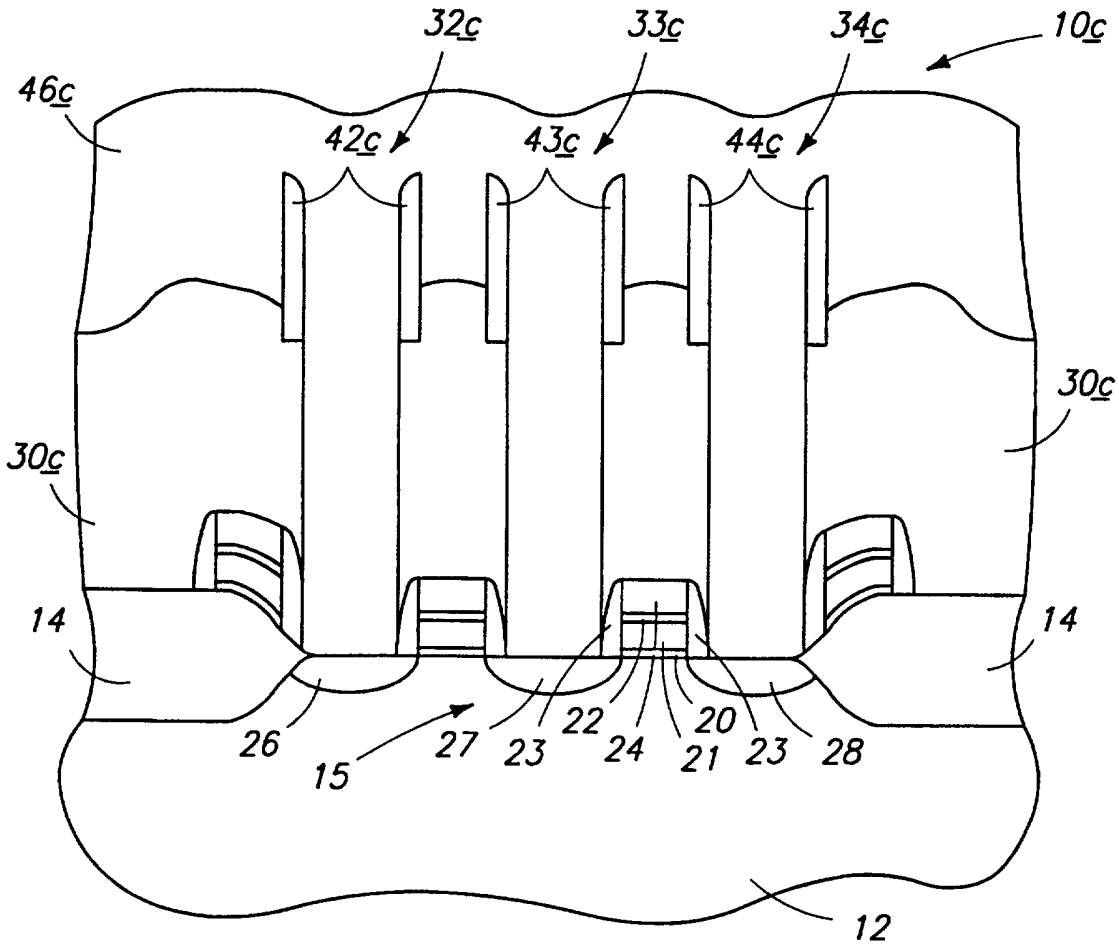
Fig 15


32c
33c
34c
10c
46c
42c
43c
44c
30c
30c
14
14
26
15
27
23
22
24
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23
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Fig 16

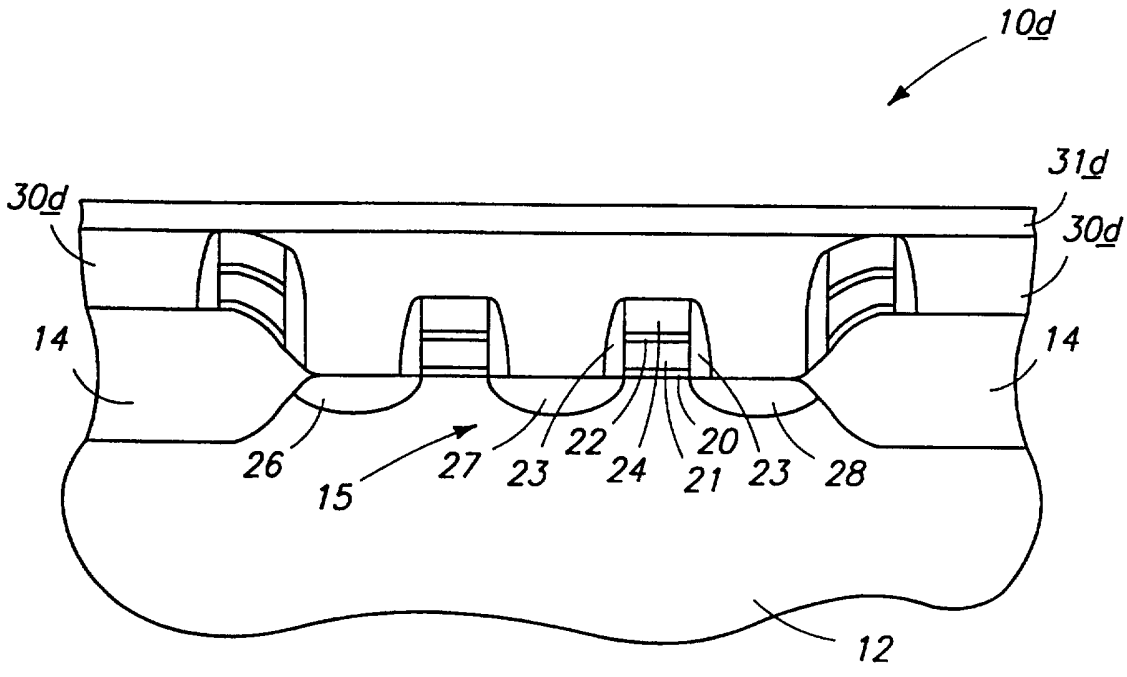

10d
31d
30d
30d
14
14
26
15
27
23
22
24
20
21
23
28
12

Fig 17

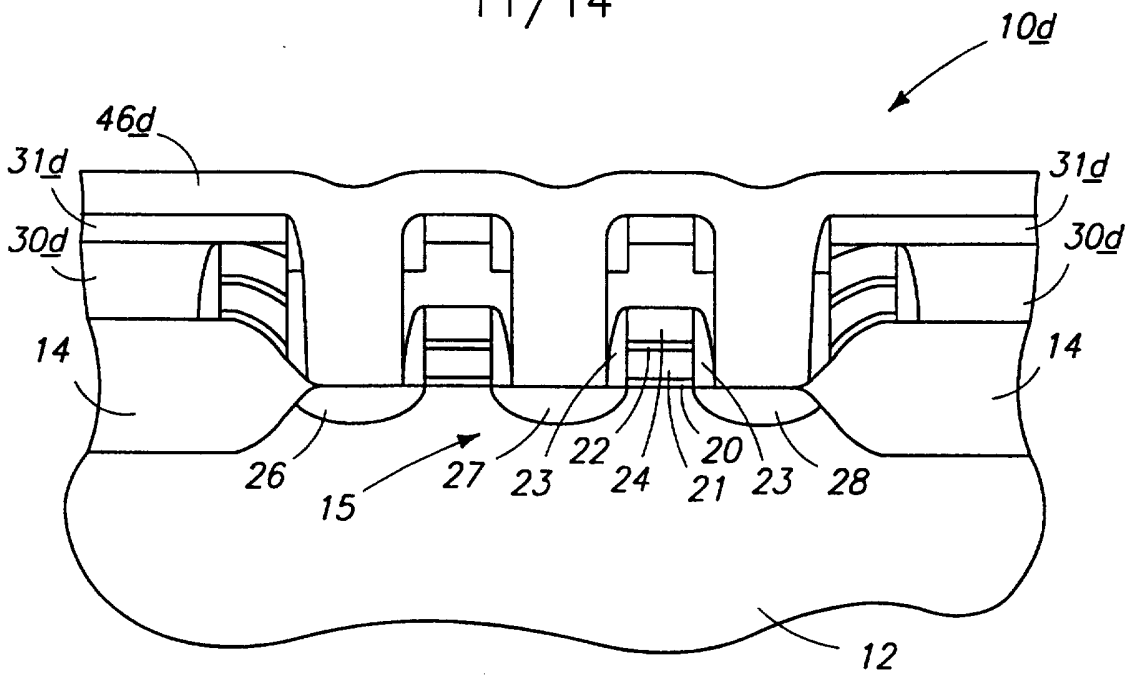


Fig 18B

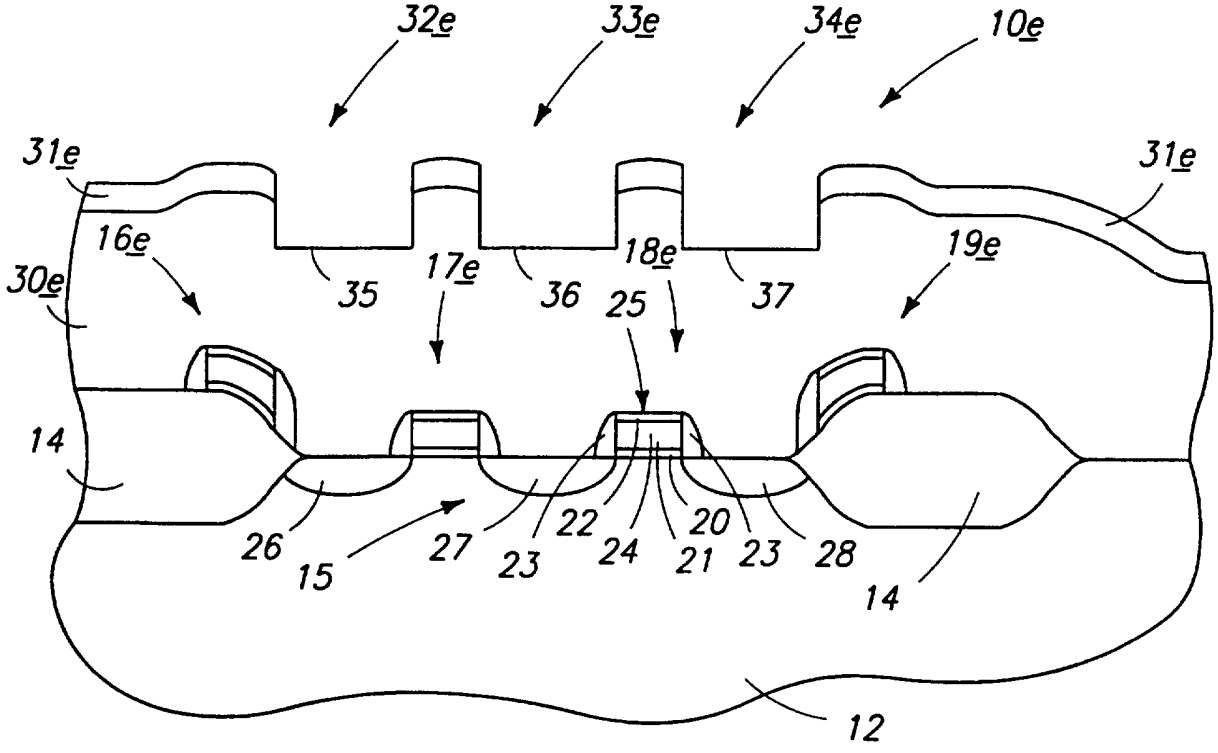
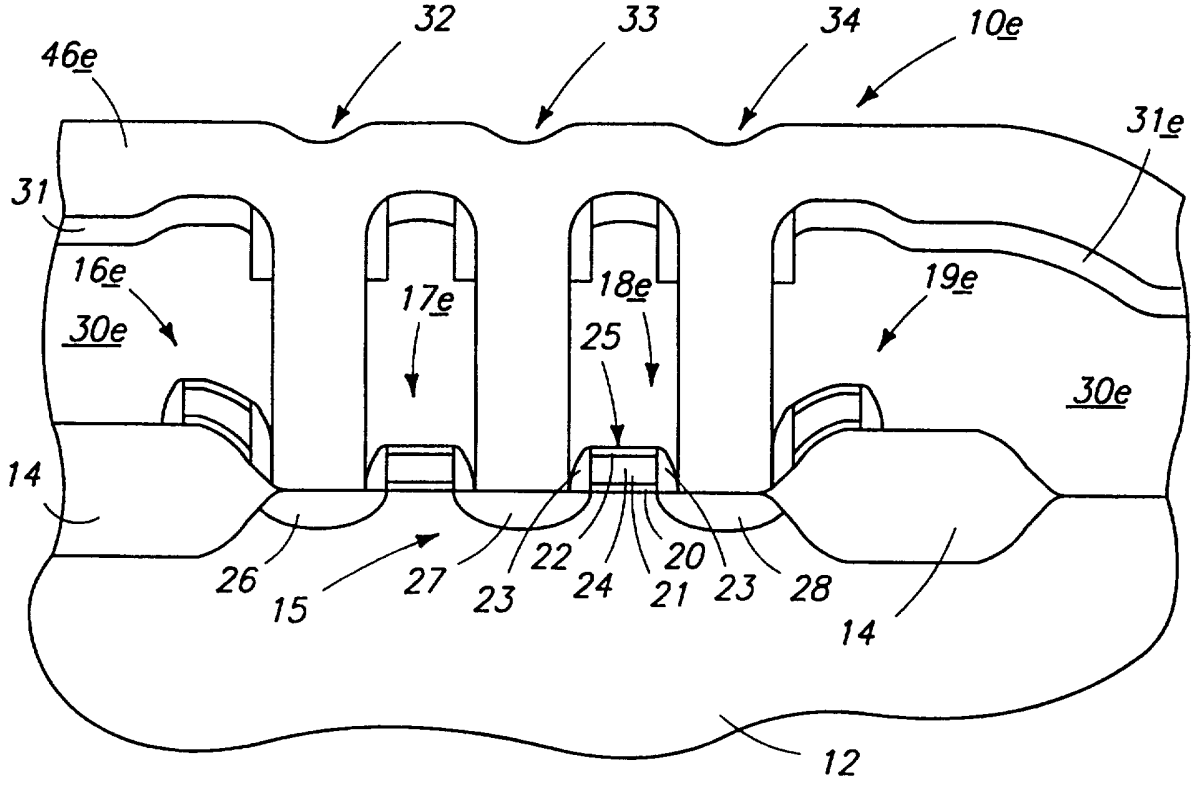


Fig 19


32
33
34
10e
46e
31e
31
16e
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17e
18e
25
19e
30e
14
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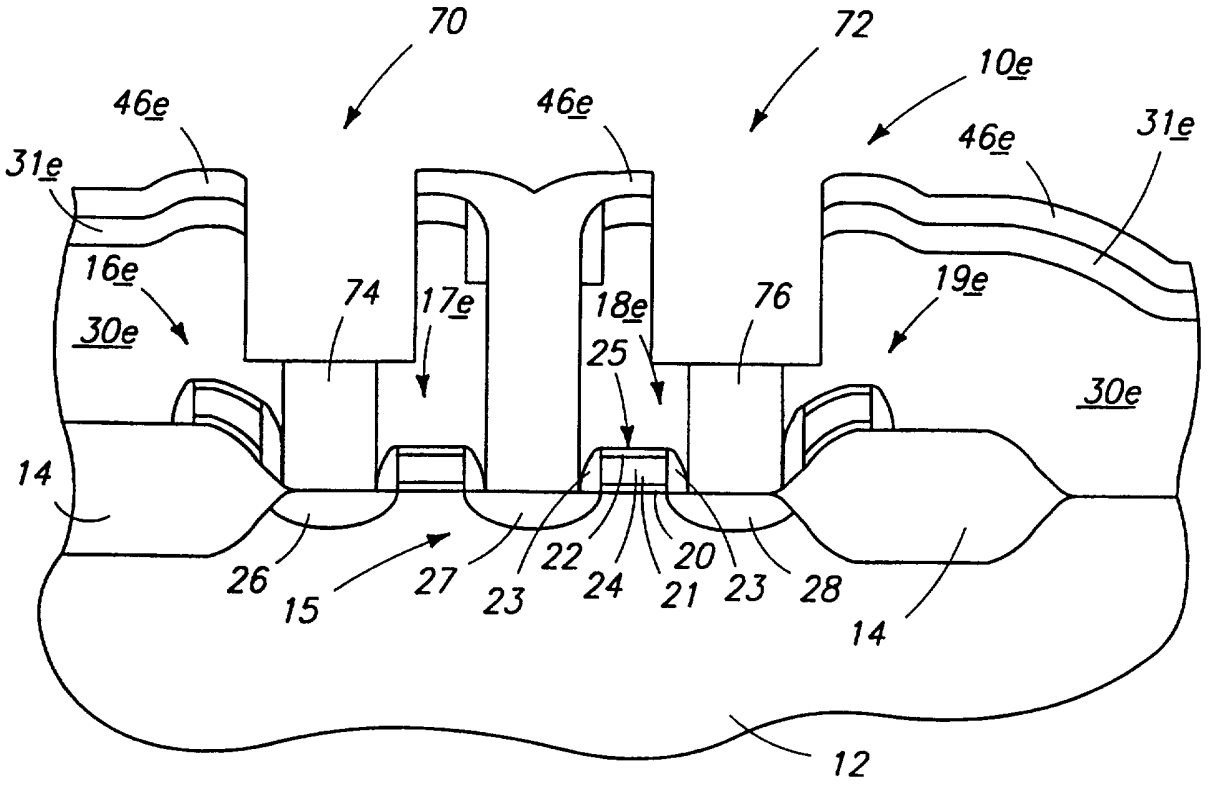
Fig 20


70
72
10e
46e
46e
46e
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31e
16e
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18e
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76
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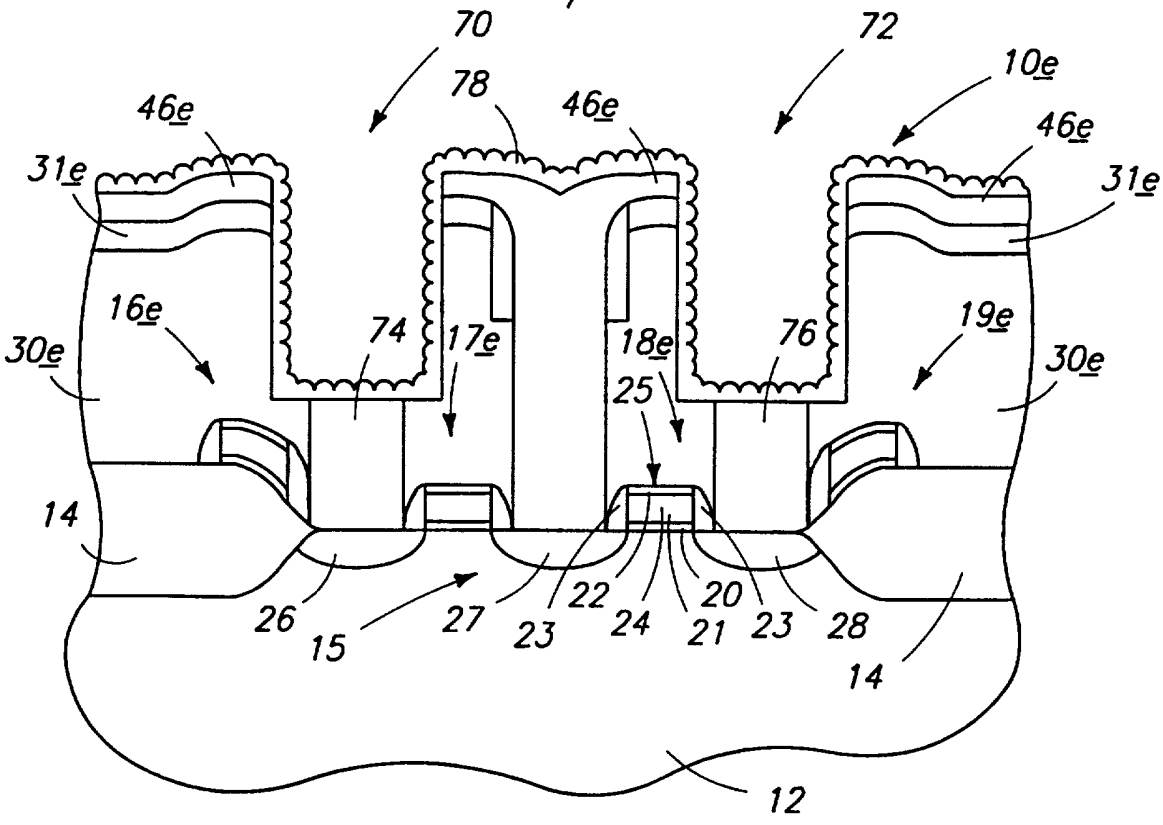
Fig 21


70
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78
10e
46e
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46e
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16e
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19e
30e
30e
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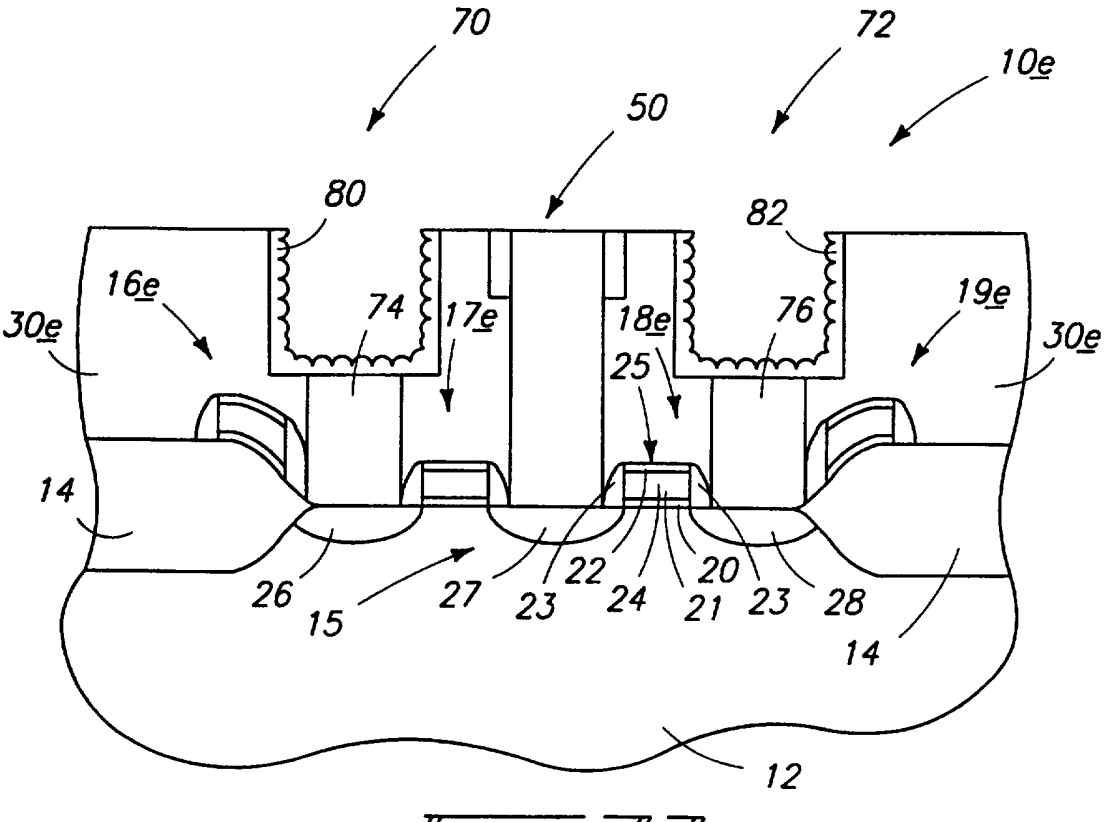
Fig 2


70
72
10e
50
80
82
16e
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17e
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76
19e
30e
30e
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14
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15
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Fig 3

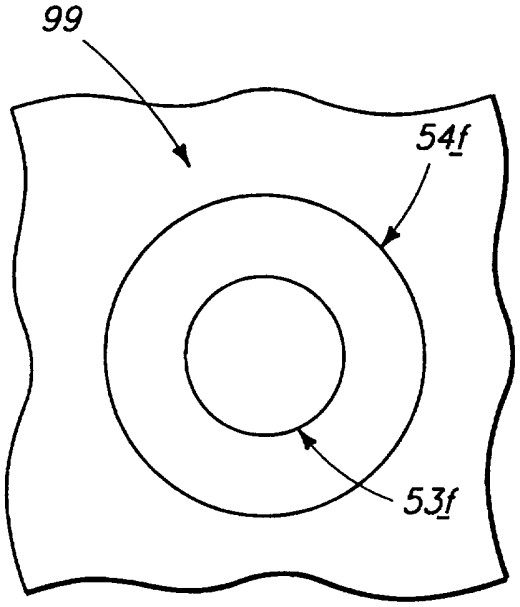

Fig 24

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/04660

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 27/108, 29/94, 31/119
US CL : 257/306, 311, 752; 437/191, 204
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/303, 306, 307, 308, 311, 752; 437/189, 191, 204

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,068,711 A (MilSE) 26 November 1991 (26.11.91), see figs. 4f and 5.	18 and 20
A,E	US 5,629,539 A (AOKI ET AL.) 13 May 1997 (13.05.97), see entire document.	1-20
A,P	US 5,608,247 A (BROWN) 04 March 1997 (04.03.97), see entire document.	1-20
A	US 4,898,841 A (HO) 06 February 1990 (06.02.90), see figs. 3a-3e.	1-6 and 8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 JULY 1997	30 JUL 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DONALD L. MONIN, JR Telephone No. (703) 308-4895

Form PCT/ISA/210 (second sheet)(July 1992)*